DA9180.004
15 September, 2005

MAS9180

AM Receiver IC

- **Single Band Receiver IC**
- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**
- **Fast Startup Feature**

DESCRIPTION

The MAS9180 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiver. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary.

MAS9180 has both differential and asymmetric input options and also options for compensating shunt capacitances of different crystals (See ordering information on page 15).

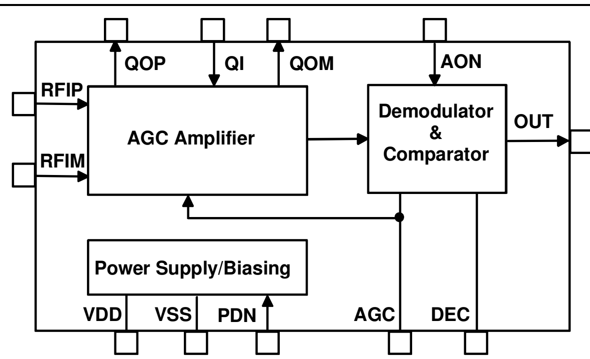
FEATURES

- Single Band Receiver IC
- Highly Sensitive AM Receiver, 0.4 μV_{RMS} typ.
- Wide Supply Voltage Range from 1.1 V to 5.5 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter
- Both Differential and Asymmetric Input Versions
- Crystal Compensation Capacitance Options

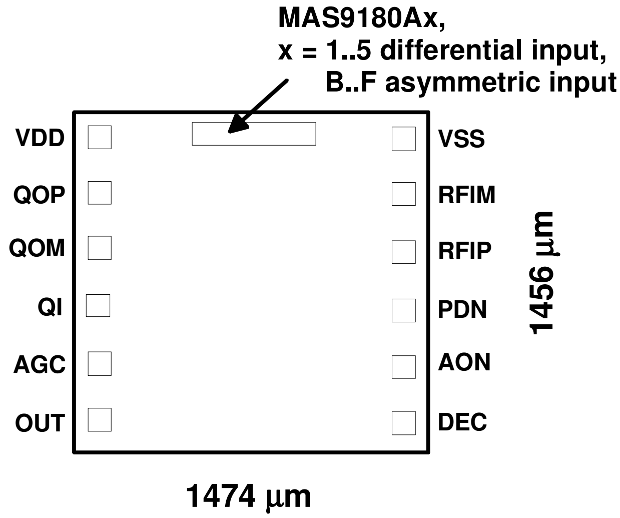
APPLICATIONS

- Single Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK), HGB (Switzerland) and BPC (China)

BLOCK DIAGRAM



MAS9180 PAD LAYOUT



DIE size = 1.47 x 1.46 mm; PAD size = 80 x 80 µm

Note: Because the substrate of the die is internally connected to VDD, the die has to be connected to VDD or left floating. Please make sure that VDD is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	174 µm	1262 µm	
Positive Quartz Filter Output for Crystal	QOP	174 µm	1057 µm	
Negative Quartz Filter Output for Crystal	QOM	174 µm	854 µm	4
Quartz Filter Input for Crystal and External Compensation Capacitor	QI	174 µm	648 µm	
AGC Capacitor	AGC	174 µm	444 µm	
Receiver Output	OUT	175 µm	240 µm	1
Demodulator Capacitor	DEC	1295 µm	225 µm	
AGC On Control	AON	1295 µm	425 µm	2
Power Down	PDN	1295 µm	624 µm	3
Positive Receiver Input	RFIP	1295 µm	825 µm	5
Negative Receiver Input	RFIM	1295 µm	1039 µm	5
Power Supply Ground	VSS	1282 µm	1200 µm	

Notes:

1) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
2) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
3) PDN = VSS means receiver on; PDN = VDD means receiver off
   Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
4) External crystal compensation capacitor pin QOM is connected only in MAS9190A5 and AF versions. It is left unconnected in MAS9180A1 and AB..E versions which have internal compensation capacitor.
5) Differential input versions A1..A5 have 600 kΩ biasing MOSFET-transistors towards ground from both receiver inputs RFIP and RFIM. Asymmetric input versions AB..AF have input pin RFIM unconnected.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}-V_{SS}		-0.3	6	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Power Dissipation	P_{MAX}			100	mW
Operating Temperature	T_{OP}		-40	+85	°C
Storage Temperature	T_{ST}		-55	+150	°C

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 1.4V, Temperature = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10		5.5	V
Current Consumption	I_{DD}	VDD=1.4 V, Vin=0 µVrms VDD=1.4 V, Vin=20 mVrms VDD=3.6 V, Vin=0 µVrms VDD=3.6 V, Vin=20 mVrms	 31 27	64 37 67 40	 91 65	µA
Stand-By Current	I_{DDoff}				0.1	µA
Input Frequency Range	f_{IN}		40		100	kHz
Minimum Input Voltage	$V_{IN\ min}$			0.4	1	µVrms
Maximum Input Voltage	$V_{IN\ max}$		20			mVrms
Receiver Input Resistance Receiver Input Capacitance	R_{RFI} C_{RFI}	Differential Input MAS9180A1..5 f=40 kHz..77.5 kHz		330 4.5		kΩ pF
Receiver Input Resistance Receiver Input Capacitance	R_{RFI} C_{RFI}	Asymmetric Input MAS9180AB..F f=40 kHz..77.5 kHz		670 6.4		kΩ pF
Input Levels $\lvert I_{IN}\rvert$<0.5 µA	V_{IL} V_{IH}		 0.8 V_{DD}		0.2 V_{DD}	V
Output Current V_{OL}<0.2 V_{DD};V_{OH} >0.8 V_{DD}	$\lvert I_{OUT}\rvert$		5			µA
Output Pulse	T_{100ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	50		140	ms
	T_{200ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	150		230	ms
	T_{500ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	400	500	600	ms
	T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	700	800	900	ms
Startup Time	T_{Start}	Fast Start-up, Vin=0.4 µVrms Fast Start-up, Vin=20 mVrms		1.3 3.5		s
Output Delay Time	T_{Delay}			50	100	ms

TYPICAL APPLICATION

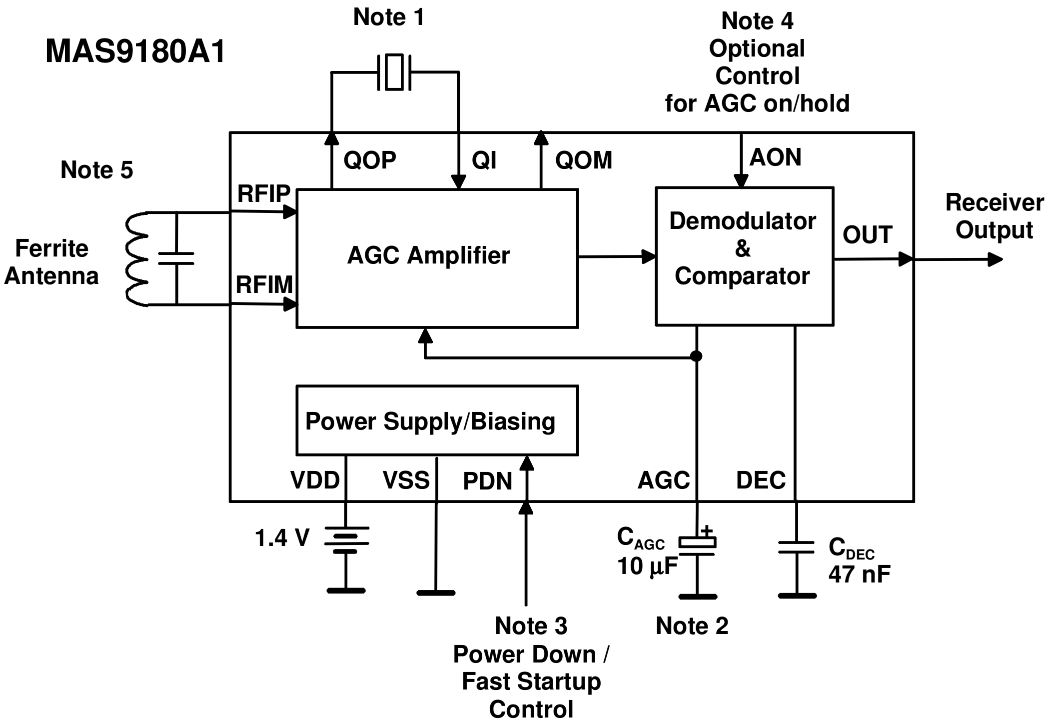


Figure 1 Application circuit of differential input and internal compensation capacitance option version MAS9180A1.

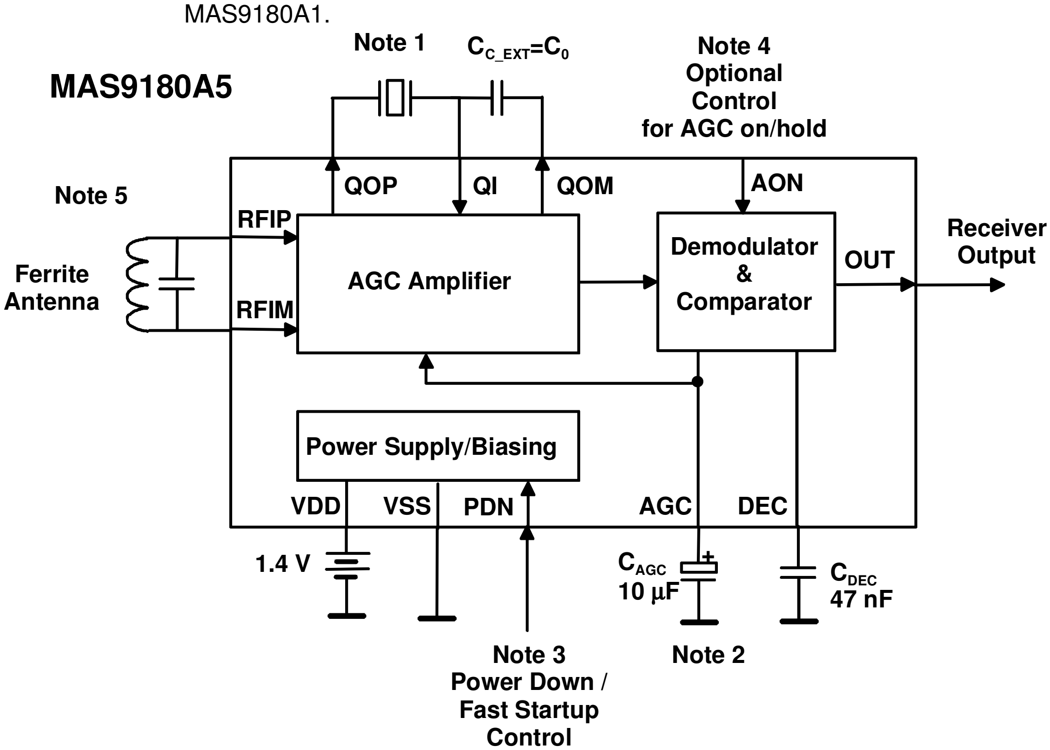


Figure 2 Application circuit of differential input and external compensation capacitance option version MAS9180A5.

TYPICAL APPLICATION (Continued)

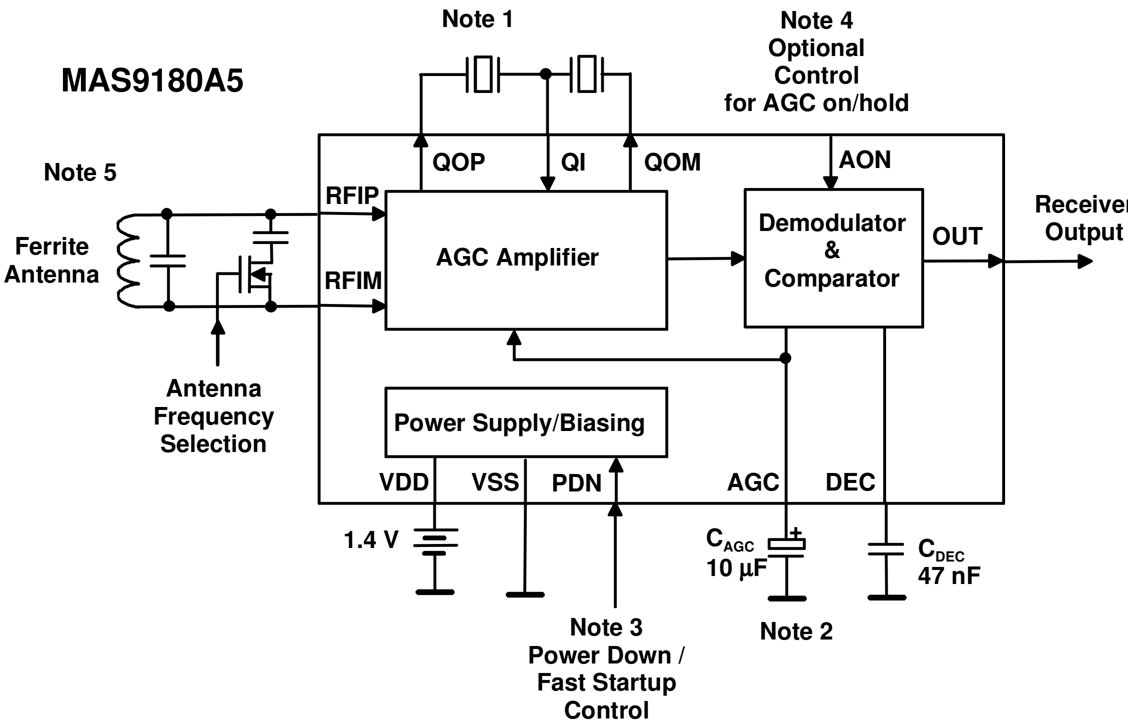


Figure 3 Dual band application circuit of differential input and external compensation capacitance option version MAS9180A5.

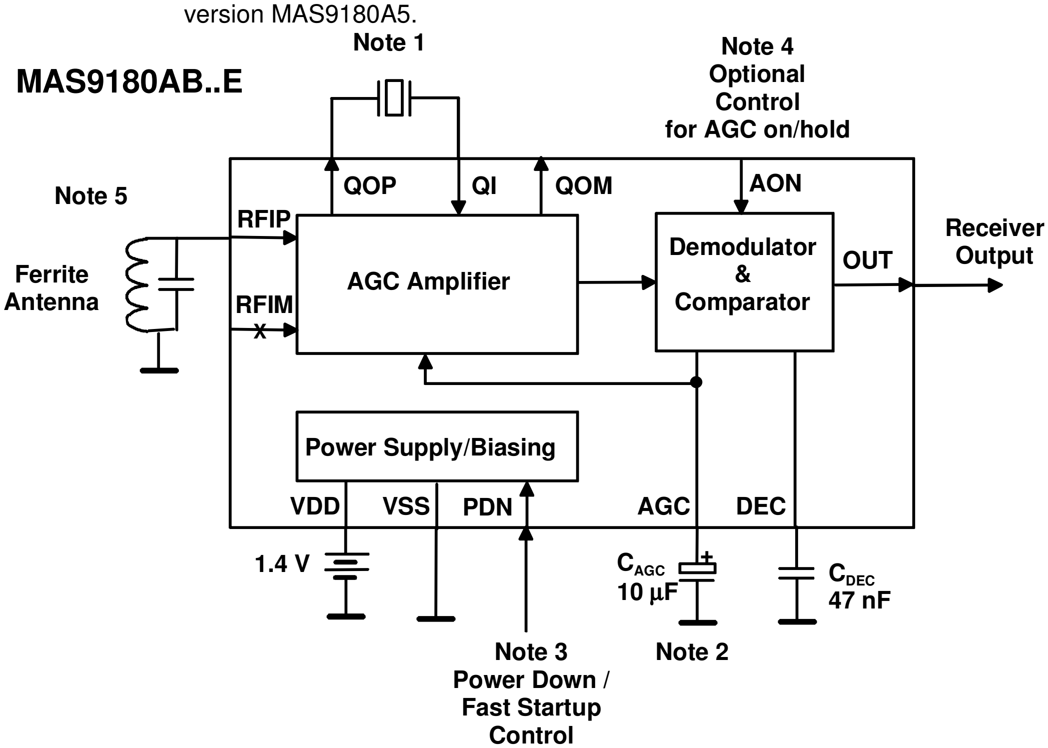


Figure 4 Application circuit of asymmetric input and internal compensation capacitance version option MAS9180AB..E.

TYPICAL APPLICATION (Continued)

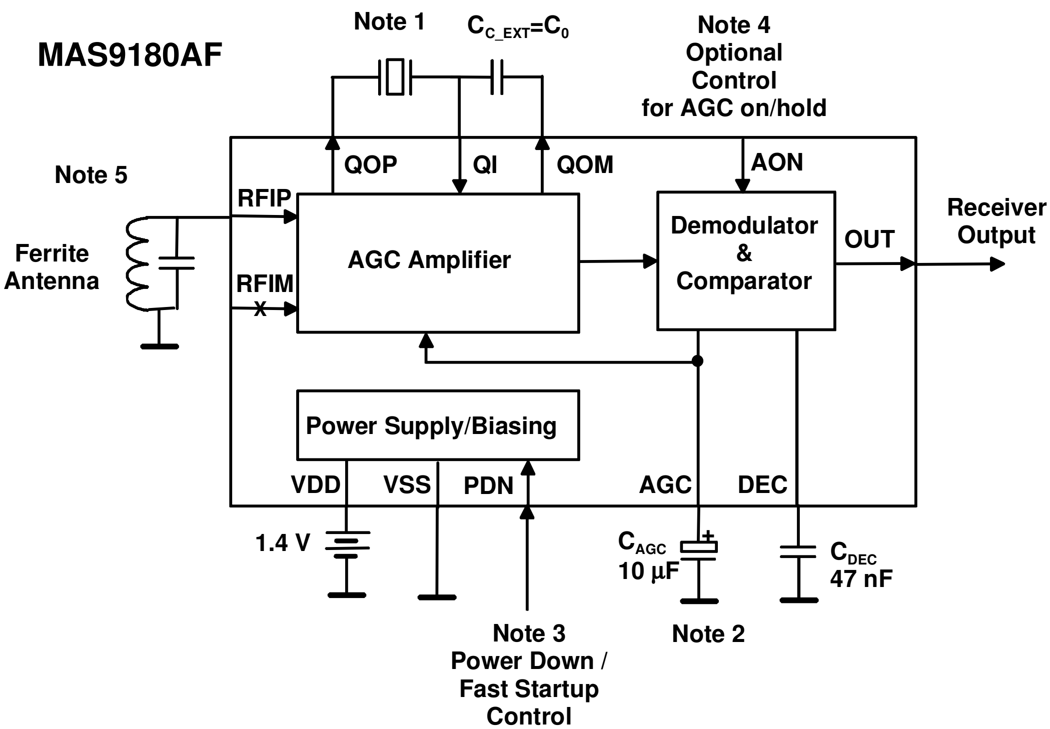


Figure 5 Application circuit of asymmetric input and external compensation capacitance option version MAS9180AF.

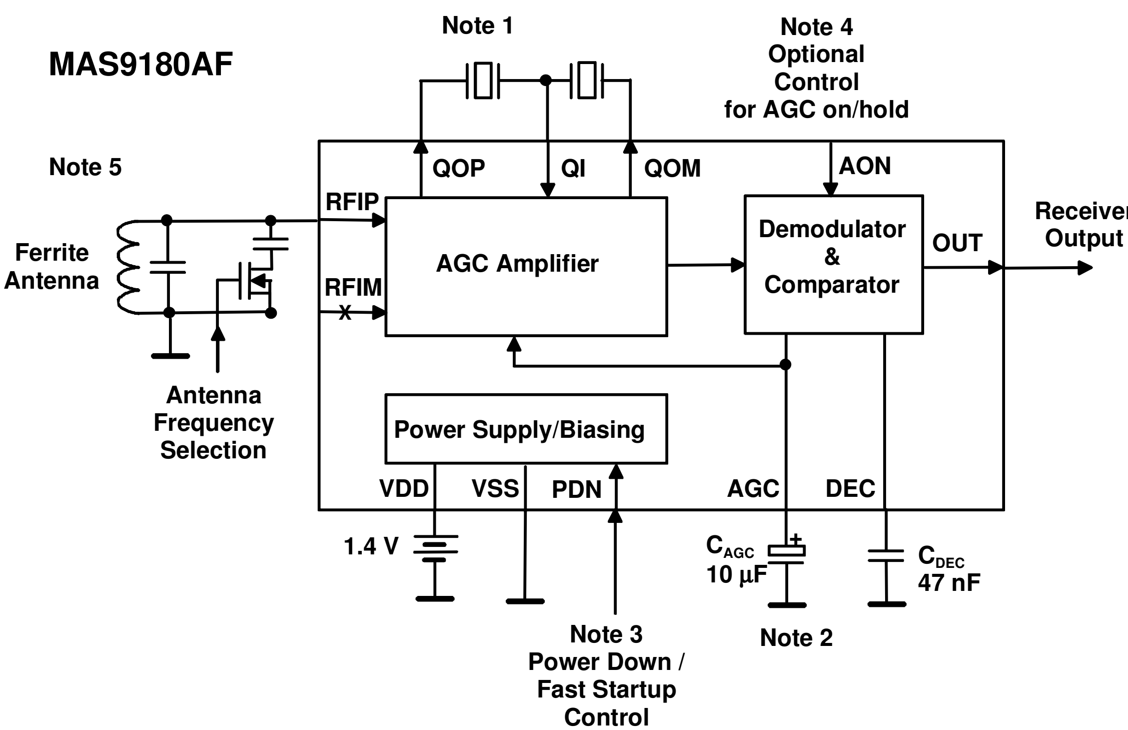


Figure 6 Dual band application circuit of asymmetric input and external compensation capacitance option version MAS9180AF.

TYPICAL APPLICATION (Continued)

Note 1: Crystals
The crystal as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 1). The crystal shunt capacitance C_0 should be matched as well as possible with the internal shunt capacitance compensation capacitor C_C of MAS9180. MAS9180A5 and MAS9180AF are options for external crystal compensation capacitor. The external compensation capacitor should be matched similarly as well as possible with crystals shunt capacitance. See Compensation Capacitance Options on table 2.

Table 1 Time-Signal System Frequencies

Time-Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 kHz
HGB	Switzerland	75 kHz	75.003 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz
BPC	China	68.5 kHz	68.505 kHz

Table 2 Compensation Capacitance Options

Device	C_C	Crystal Description	Input
MAS9180A1	0.75 pF	For low C_0 crystal	Differential
MAS9180A5	C_{C_EXT}	For any crystals, external compensation capacitor	Differential
MAS9180AB	0.75 pF	For low C_0 crystal	Asymmetric
MAS9180AC	1.25 pF	For low C_0 crystal	Asymmetric
MAS9180AD	1.5 pF	For low C_0 crystal	Asymmetric
MAS9180AE	2.5 pF	For low C_0 crystal	Asymmetric
MAS9180AF	C_{C_EXT}	For any crystals, external compensation capacitor	Asymmetric

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example crystal with 1 pF floating package shunt capacitance can have 0.85 pF grounded package shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

In dual band receiver configuration the crystals can be connected in parallel thus external compensation capacitor value C_{C_EXT} must be sum of two crystals' shunt capacitances. Instead of parallel crystal connection it is also possible to connect other crystal from QOP pin and the other crystal from QOM pin to common QI pin (figure 3). In this circuit configuration no external compensation capacitor is required since the crystals compensate each other. The sensitivity of dual band receiver configuration will be lower than that of single band receiver configuration since the noise band width of crystal filter with two parallel crystals is double.

Table 3 below presents some crystal manufacturers having suitable crystals for timesignal receiver application.

Table 3. Crystal Manufacturers and Crystal Types in Alphaphetical Order for Timesignal Receiver Application

Manufacturer	Crystal Type	Dimensions	Web Link
Citizen	CFV-206	ø 2.0 x 6.0	http://www.citizen.co.jp/tokuhan/quartz/
Epson	C-2-Type C-4-Type	ø 1.5 x 5.0 ø 2.0 x 6.0	http://www.epsondevice.com/e/
KDS Daishinku	DT-261	ø 2.0 x 6.0	http://www.kdsj.co.jp/english.html
Microcrystal	MX1V-L2N MX1V-T1K	ø 2.0 x 6.0 ø 2.0 x 8.1	http://www.microcrystal.com/
Seiko Instruments	VTC-120	ø 1.2 x 4.7	http://speed.sii.co.jp/pub/compo/quartz/topE.jsp

TYPICAL APPLICATION (Continued)

Note 2: AGC Capacitor
The AGC and DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum 100 MΩ. Also probes with at least 100 MΩ impedance should be used for voltage probing of AGC and DEC pins. DEC capacitor can be low leakage chip capacitor.

Note 3: Power Down / Fast Startup Control
Both power down and fast startup are controlled using the PDN pin. The device is in power down (turned off) if PDN = VDD and in power up (turned on) if PDN = VSS. Fast startup is triggered automatically by the falling edge of PDN signal, i.e., controlling device from power down to power up. The VDD must be high before falling edge of PDN to guarantee proper operation of fast startup circuitry. The startup time without proper fast startup control can be several minutes but with fast startup it is shortened typically to few seconds.

Note 4: Optional Control for AGC On/Hold
AON control pin has internal pull up which turns AGC circuit on all the time if AON pin is left unconnected. Optionally AON control can be used to hold and release AGC circuit. Stepper motor drive etc. can produce disturbing amount of noise which can shift the input amplifier gain to unoptimal level. This can be avoided by controlling AGC hold (AON=VSS) during stepper motor drive periods and releasing AGC (AON=VDD) when motors are not driven.

Note 5: Ferrite Antenna
The ferrite antenna converts the transmitted radio wave into a voltage signal. It has an important role in determining receiver performance. Recommended antenna impedance at resonance is around 150 kΩ.
Low antenna impedance corresponds to low noise but often also to small signal amplitude. On the other hand high antenna impedance corresponds to high noise but also large signal. The optimum performance where signal-to-noise ratio is at maximum is achieved in between.
The antenna should have also some selectivity for rejecting near signal band disturbances. This is determined by the antenna quality factor which should be approximately 100. Much higher quality factor antennas suffer from extensive tuning accuracy requirements and possible tuning drifts by the temperature.

Antenna impedance can be calculated using equation 1 where f_0, L, Q_{ant} and C are resonance frequency, coil inductance, antenna quality factor and antenna tuning capacitor respectively. Antenna quality factor Q_{ant} is defined by ratio of resonance frequency f_0 and antenna bandwidth B (equation 2).

$$R_{antenna} = 2\pi \cdot f_0 \cdot L \cdot Q_{antenna} = \frac{Q_{antenna}}{2\pi \cdot f_0 \cdot C} = \frac{1}{2\pi \cdot B \cdot C}$$ **Equation 1.**

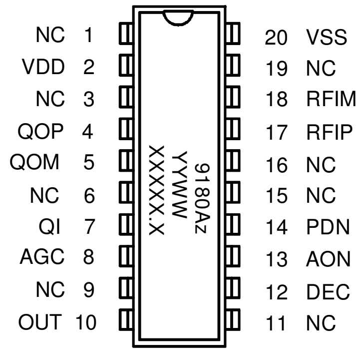
$$Q_{antenna} = \frac{f_0}{B}$$ **Equation 2.**

Table 4 below presents some antenna manufacturers for timesignal application.

Table 4. Antenna Manufacturers and Antenna Types in Alphaphetical Order for Timesignal Application

Manufacturer	Antenna Type	Dimensions	Web Link
HR Electronic GmbH	60716 (60kHz) 60708 (77.5kHz)	ø 10 x 60 mm	http://www.hrelectronic.com/
Sumida	ACL80A (40kHz)	ø 10 x 80 mm	http://www.sumida.com/

MAS9180 SAMPLES IN SBDIL 20 PACKAGE



Top Marking Definitions:
YYWW = Year Week
XXXXX.X = Lot Number
z=Sample Version Number

PIN DESCRIPTION

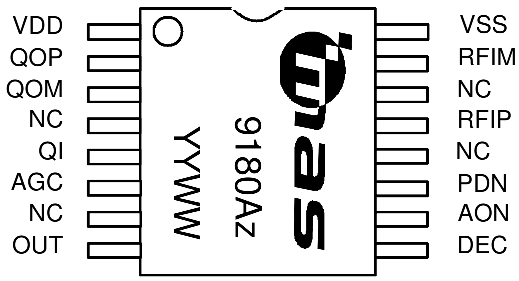
Pin Name	Pin	Type	Function	Note
NC	1			
VDD	2	P	Positive Power Supply	
NC	3			
QOP	4	AO	Positive Quartz Filter Output for Crystal	
QOM	5		Negative Quartz Filter Output for External Compensation Capacitor or Second Crystal	5
NC	6			1
QI	7	AI	Quartz Filter Input for Crystal and External Compensation Capacitor	
AGC	8	AO	AGC Capacitor	
NC	9			
OUT	10	DO	Receiver Output	2
NC	11			
DEC	12	AO	Demodulator Capacitor	
AON	13	DI	AGC On Control	3
PDN	14	DI	Power Down Input	4
NC	15			
NC	16			
RFIP	17	AI	Positive Receiver Input	6
RFIM	18	AI	Negative Receiver Input	6
NC	19			
VSS	20	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:

1) Pin 6 between QOM and QI must be connected to VSS to eliminate DIL package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
4) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
5) External crystal compensation capacitor pin QOM is connected only in MAS9190A5 and AF versions. It is left unconnected in MAS9180A1 and AB..E versions which have internal compensation capacitor.
6) Differential input versions A1..A5 have 600 kΩ biasing MOSFET-transistors towards ground from both receiver inputs RFIP and RFIM. Asymmetric input versions AB..AF have input pin RFIM unconnected.

PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE



Top Marking Definitions:
z = Version Number
YYWW = Year Week

PIN DESCRIPTION

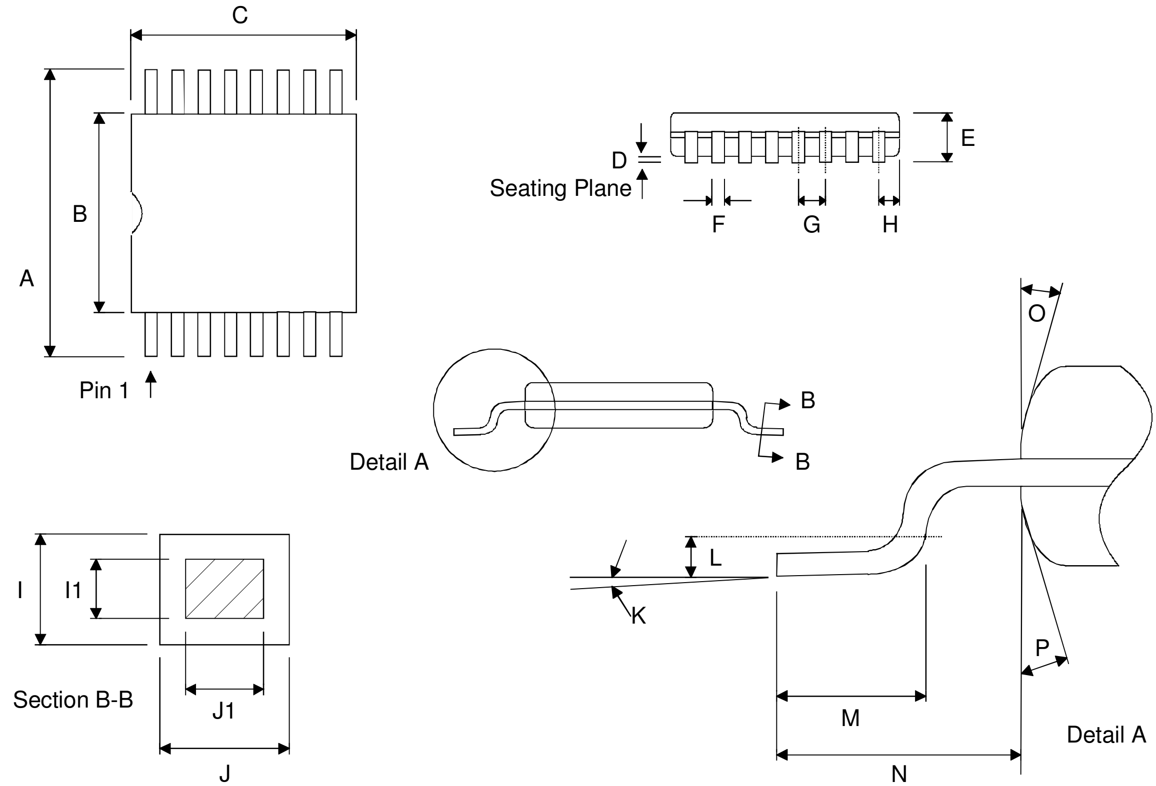
Pin Name	Pin	Type	Function	Note
VDD	1	P	Positive Power Supply	
QOP	2	AO	Positive Quartz Filter Output for Crystal	
QOM	3	AO	Negative Quartz Filter Output for External Compensation Capacitor or Second Crystal	5
NC	4			1
QI	5	AI	Quartz Filter Input for Crystal and External Compensation Capacitor	
AGC	6	AO	AGC Capacitor	
NC	7			
OUT	8	DO	Receiver Output	2
DEC	9	AO	Demodulator Capacitor	
AON	10	DI	AGC On Control	3
PDN	11	DI	Power Down Input	4
NC	12			
RFIP	13	AI	Positive Receiver Input	6
NC	14			
RFIM	15	AI	Negative Receiver Input	6
VSS	16	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:

1) Pin 4 between quartz crystal filter pins must be connected to VSS to eliminate package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up (to AGC on) with current < 1 µA which is switched off at power down
4) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
5) External crystal compensation capacitor pin QOM is connected only in MAS9190A5 and AF versions. It is left unconnected in MAS9180A1 and AB..E versions which have internal compensation capacitor.
6) Differential input versions A1..A5 have 600 kΩ biasing MOSFET-transistors towards ground from both receiver inputs RFIP and RFIM. Asymmetric input versions AB..AF have input pin RFIM unconnected.

PACKAGE (TSSOP16) OUTLINES



Dimension	Min	Max	Unit
A	6.40 BSC		mm
B	4.30	4.50	mm
C	5.00 BSC		mm
D	0.05	0.15	mm
E		1.10	mm
F	0.19	0.30	mm
G	0.65 BSC		mm
H	0.18	0.28	mm
I	0.09	0.20	mm
I1	0.09	0.16	mm
J	0.19	0.30	mm
J1	0.19	0.25	mm
K	0°	8°	
L	0.24	0.26	mm
M (The length of a terminal for soldering to a substrate)	0.50	0.75	mm
N	1.00 REF		mm
O	12°		
P	12°		

Dimensions do not include mold flash, protrusions, or gate burrs.
All dimensions are in accordance with JEDEC standard MO-153.

SOLDERING INFORMATION

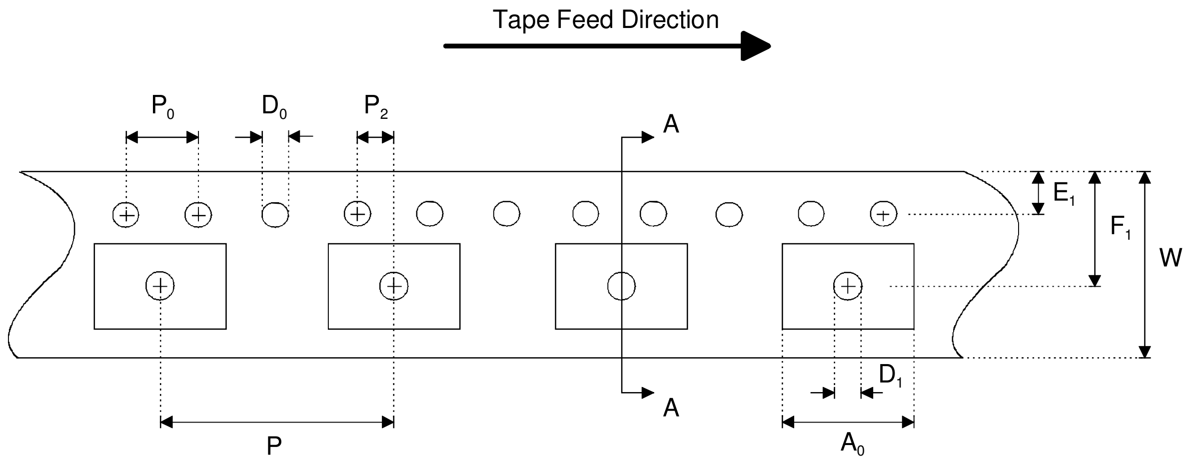
◆ **For Eutectic Sn/Pb TSSOP-16**

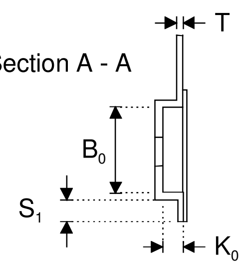
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Temperature	240°C
Maximum Number of Reflow Cycles	2
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Sn 85% Pb 15%

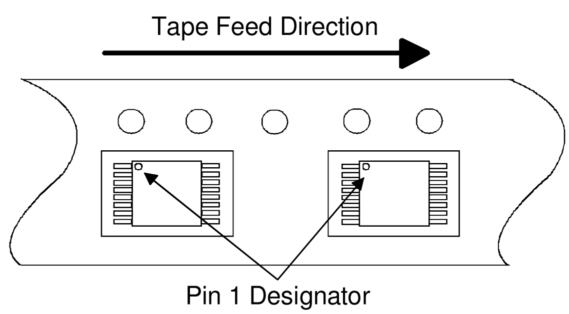
◆ **For Pb-Free, RoHS Compliant TSSOP-16**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS

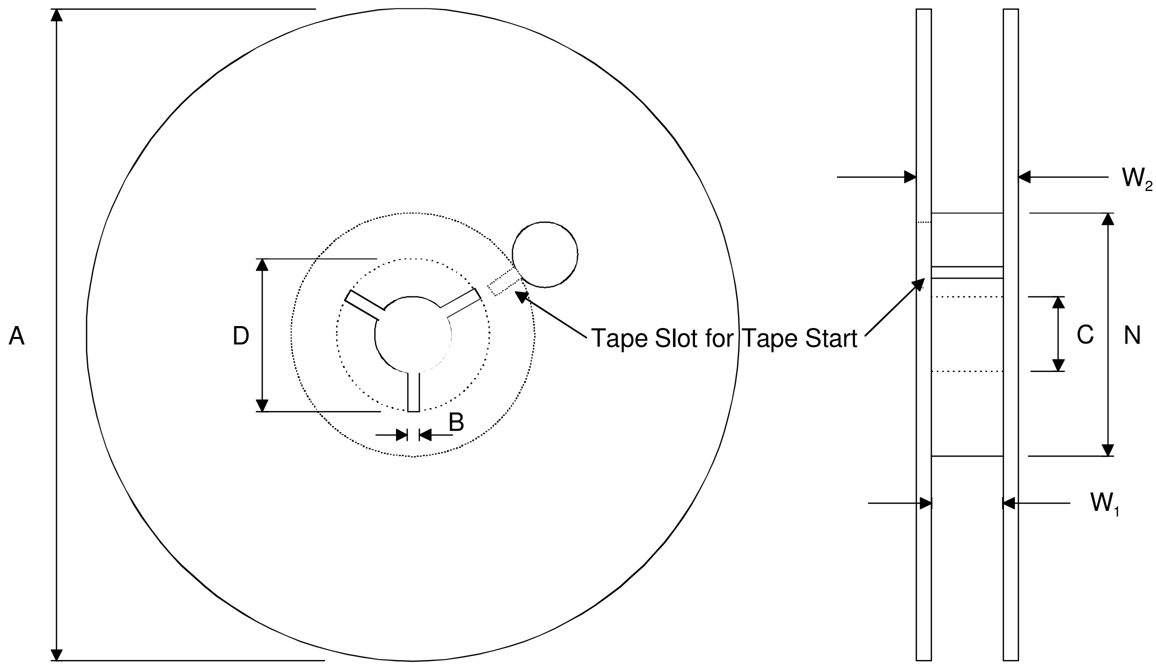






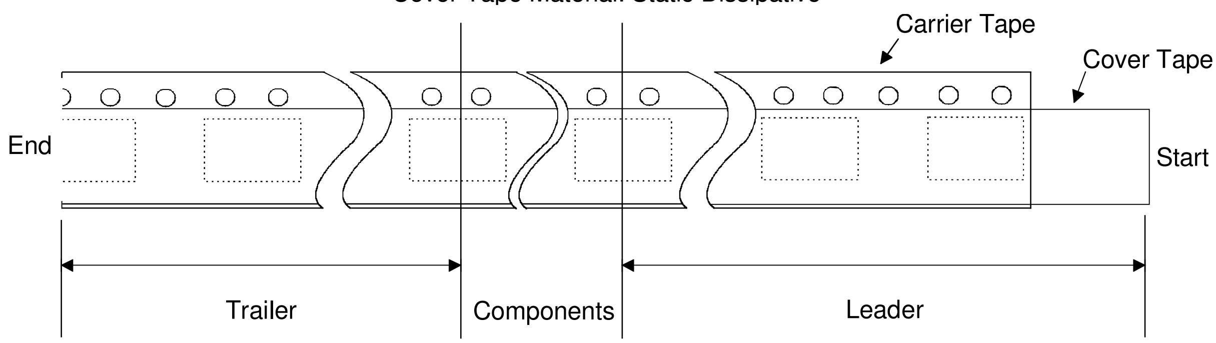
Dimension	Min	Max	Unit
A_0	6.50	6.70	mm
B_0	5.20	5.40	mm
D_0	1.50 +0.10 / -0.00		mm
D_1	1.50		mm
E_1	1.65	1.85	mm
F_1	7.20	7.30	mm
K_0	1.20	1.40	mm
P	11.90	12.10	mm
P_0	4.0		mm
P_2	1.95	2.05	mm
S_1	0.6		mm
T	0.25	0.35	mm
W	11.70	12.30	mm

REEL SPECIFICATIONS



2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Description	Capacitance Option
MAS9180A1TC00	Single Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	C_C = 0.75 pF
MAS9180A5TC00	Single Band AM-Receiver IC with Differential Input	EWS-tested wafer, Thickness 400 µm.	External compensation capacitor
MAS9180A1UA06	Single Band AM-Receiver IC with Differential Input	TSSOP-16, Tape & Reel	C_C = 0.75 pF
MAS9180A1UC06	Single Band AM-Receiver IC with Differential Input	TSSOP-16, Pb-free, RoHS compliant, Tape & Reel	C_C = 0.75 pF
MAS9180ABTC00	Single Band AM-Receiver IC with Asymmetric Input	EWS-tested wafer, Thickness 400 µm.	C_C = 0.75 pF
MAS9180ACTC00	Single Band AM-Receiver IC with Asymmetric Input	EWS-tested wafer, Thickness 400 µm.	C_C = 1.25 pF
MAS9180ADTC00	Single Band AM-Receiver IC with Asymmetric Input	EWS-tested wafer, Thickness 400 µm.	C_C = 1.5 pF
MAS9180AETC00	Single Band AM-Receiver IC with Asymmetric Input	EWS-tested wafer, Thickness 400 µm.	C_C = 2.5 pF
MAS9180AFTC00	Single Band AM-Receiver IC with Asymmetric Input	EWS-tested wafer, Thickness 400 µm.	External compensation capacitor

Contact Micro Analog Systems Oy for other wafer thickness options.

◆ **The formation of product code**

An example for MAS9180A1TC00:

MAS9180	**A**	**1**	**TC**	**00**
Product name	Design version	Input type and capacitance option: Differential input and C_C = 0.75 pF	Package type: TC = 400 µm thick EWS tested wafer UA = TSSOP16 (Pb/Sn) UC = TSSOP16 (Pb-free, RoHS compliant)	Delivery format: 00 = bare wafer 06 = Tape & Reel

LOCAL DISTRIBUTOR

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