MAS9279

IC FOR 10.00 – 52.00 MHz VCTCXO

- **Fourth Order Compensation**
- **Frequency Stability +/- 0.3 ppm**
- **Wide Frequency Range**
- **Very Low Phase Noise**
- **Low Voltage**
- **Minimum Operating Temperature –40 °C**
- **Tri State CMOS Output**

DESCRIPTION

The MAS9279 is an integrated circuit well suited to build high end VCTCXO for telecommunication. The trimming is done through a serial bus and the calibration information is stored in an internal PROM. This means no rework for trimming is needed.

To build a VCTCXO only crystal is required in addition to MAS9279. The compensation method is fully analog, working continuously without generating any steps or other interference.

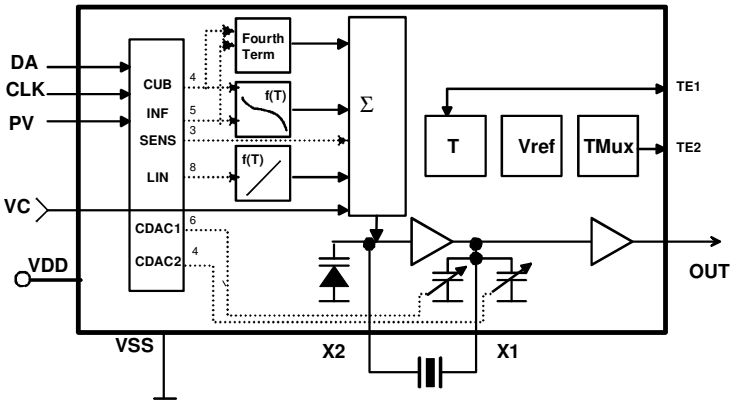
FEATURES

- Very small size
- Minimal current consumption
- Wide operating temperature range
- Very low phase noise
- Programmable VC-sensitivity
- Minimum operating temperature –40 °C
- Oscillator frequency output $f_0/2$ version available

APPLICATIONS

- VCTCXO for high end telecommunications systems
- TCXO for high end telecommunication systems

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Description	Symbol	x-coordinate	y-coordinate	Note
Power Supply Voltage	VDD	149	1340	
Programming Input	PV	561	1340	
Serial Bus Clock Input	CLK	1000	1340	
Serial Bus Data Input	DA	1565	1340	
Temperature Output	TE1	2024	1340	3
Test Multiplexer Output	TE2	2016	140	3
Voltage Control Input	VC	147	140	
Crystal Oscillator Output	X1	1261	140	
Crystal/Varactor Oscillator Input	X2	518	140	
Power Supply Ground	VSS	1549	140	
Buffer Output	OUT	1810	140	

Note: Because the substrate of the die is internally connected to GND, the die has to be connected to GND or left floating. Make sure that GND is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.
Note: Pad coordinates are measured from the left bottom corner of the chip to the center of the pads. The coordinates may vary depending on sawing width and location, however, distances between pads are accurate.
Note 3: Valid for MAS9279A1, A3, A5 and A7. In MAS9279A2, A4, A6 and A8 TE1 and TE2 pins have been swapped.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD} - V_{SS}	-0.3	6.0	V	
Input Pin Voltage		V_{SS} -0.3	V_{DD} + 0.3	V	1)
Power Dissipation	P_{MAX}		100	mW	
Storage Temperature	T_{ST}	-55	150	°C	
ESD Rating; HBM			2	kV	2)

Note 1: Not valid for programming pin PV
Note 2: In X1 and X2 pins maximum ESD rating is 1.5kV

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}		2.7	3.3	5.5	V	
Supply Current	I_{CC}	Vdd = 3.3 Volt		6.0		mA	1
Operating Temperature	T_{OP}		-40		+85	°C	
Crystal Pulling Sensitivity	S		24	28	35	ppm/pF	2
Crystal Pulling Sensitivity	S		28	33	38	ppm/pF	3
Crystal Load Capacitance	C_L	Vc = 1.2V		8		pF	2
Crystal Load Capacitance	C_L	Vc = 1.2V		10		pF	3

Note 1: At 26MHz crystal
Note 2: MAS9279A1, MAS9279A3, MAS9279A5, MAS9279A7
Note 3: MAS9279A2, MAS9279A4, MAS9279A6, MAS9279A8

ELECTRICAL CHARACTERISTICS

(recommended operation conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Frequency Range	f_o	10.00		52.00	MHz	
Voltage Control Range	V_C	0		Vdd	V	1)
Voltage Control Sensitivity	V_{CSENS}	7.3		10.4	ppm/V	2)
Voltage Control Sensitivity	V_{CSENS}	8.8		13.4	ppm/V	3)
Voltage Control Sensitivity	V_{CSENS}	10.1		14.5	ppm/V	4)
Frequency vs. Supply Voltage	df_o			±0.2	ppm	5)
Frequency vs. Load Change	df_o			±0.2	ppm	6)
Output Voltage (10 pF, VDD 2.7 V)	V_{out}		2.3		Vpp	
Output Voltage (10 pF, VDD 5.0 V)	V_{out}		4.5		Vpp	
Rise and Fall Time (10 - 50 pF)			3		ns	
Output Symmetry			45-55		%	
Compensation Range ± 1.0 ppm	T_C	-40		85	°C	
Compensation Range ± 0.75 ppm	T_C	-20		70	°C	
Compensation Range ± 0.3 ppm	T_C	10		50	°C	
Compensation Range Linear Part	a1	-0.4		-0.1	ppm/K	9)
Compensation Inflection Point	INF	23		31	°C	
Compensation Range Cubic Part	a3		95		ppm^2/K^3	
Compensation CDAC1 (4 Bit)	C_{X1}	-1.5		2.4	ppm	2) 7)
Compensation CDAC2 (6 Bit)	C_{X2}	-21		27	ppm	2) 8)
Compensation CDAC1 (4 Bit)	C_{X1}	-2.6		2.1	ppm	3) 7)
Compensation CDAC2 (6 Bit)	C_{X2}	-26		32	ppm	3) 8)
Compensation CDAC1 (4 Bit)	C_{X1}	-3.0		2.6	ppm	4) 7)
Compensation CDAC2 (6 Bit)	C_{X2}	-32		36	ppm	4) 8)
Amplitude Start up Time	T_{START}		2		ms	
Tri State Output Buffer ON State OFF State	DA	 0 1.6		 0.55 VDD	V	

Note 1: In TCXO leave Vc floating
Note 2: With 23 ppm/pF crystal
Note 3: With 28 ppm/pF crystal.
Note 4: With 33 ppm/pF crystal
Note 5: VDD +/- 5%
Note 6: R=10 kohm +/- 10%, C=10 pF +/- 10%
Note 7: CDAC2=6.
Note 8: CDAC1=4.
Note 9: With LIN=255 temperature compensation is in off mode

IC OUTLINES

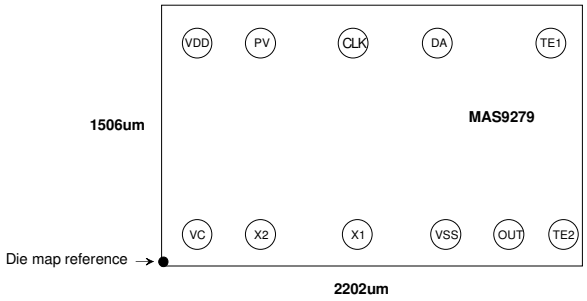


Figure 1. MAS9279A1, A3, A5, A7

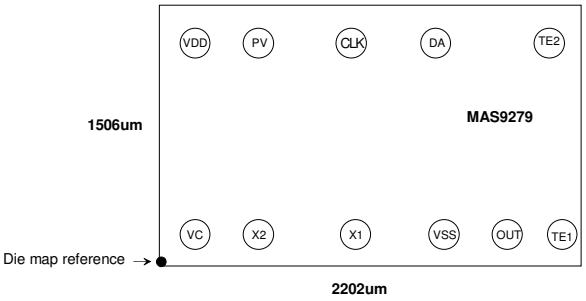
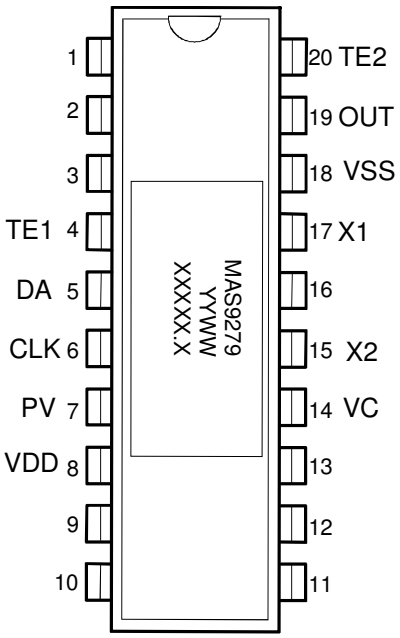


Figure 2. MAS9279A2, A4, A6, A8

Note 1: MAS9279 pads are round with 80 µm diameter at opening.
Note 2: Pin CLK can either be connected to VSS or left floating, pin PV should be connected to Ground or left floating and pin TE1 must be left floating in VCTCXO module end-user application.
Note 3: Die map reference is the actual left bottom corner of the sawn chip.

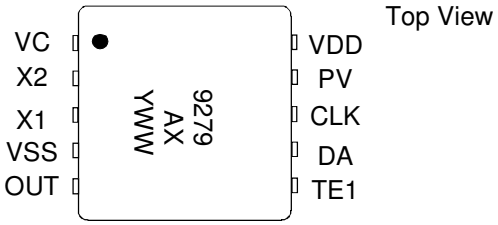
SAMPLES IN SB20 DIL PACKAGE



Top marking:
YYWW = Year, Week
XXXXX.X = Lot number

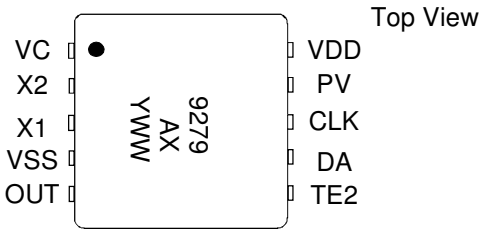
DEVICE OUTLINE CONFIGURATION

QFN10 3x3



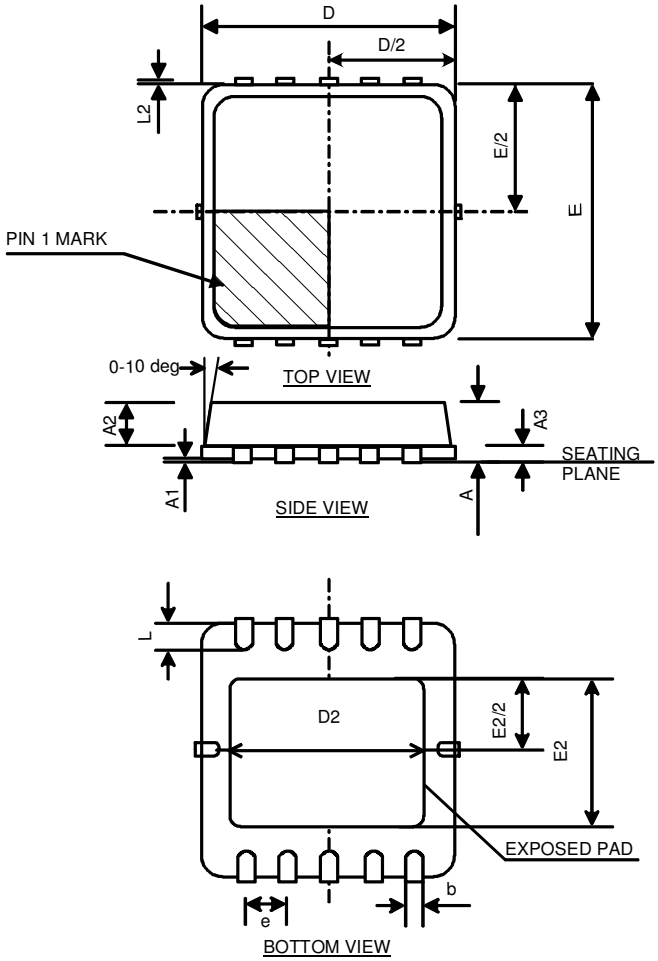
A = product version
X = Load / Output version 1, 3, 5, 7
Y = year
WW = week

QFN10 3x3



A = product version
X = Load / Output version 2, 4, 6, 8
Y = year
WW = week

PACKAGE (QFN10 3X3) OUTLINE



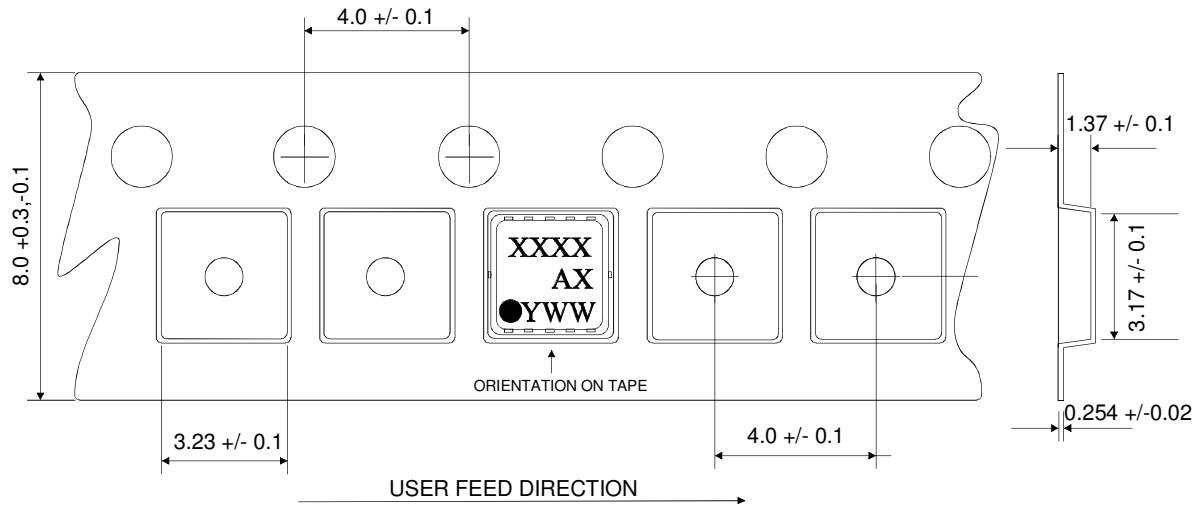
Symbol	Min	Nom	Max	Unit
A	0.8	0.9	1.0	mm
A1	0	0.025	0.05	mm
A2	0.65	0.70	0.75	mm
A3	0.15	0.20	0.25	mm
b	0.200	0.250	0.300	mm
D		3.00 BSC		mm
D2	1.92	2.02	2.12	mm
E		3.00 BSC		mm
E2	1.65	1.70	1.75	mm
e		0.50 BSC		mm
L	0.350	0.400	0.450	mm
L2	-	-	0.125	mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.

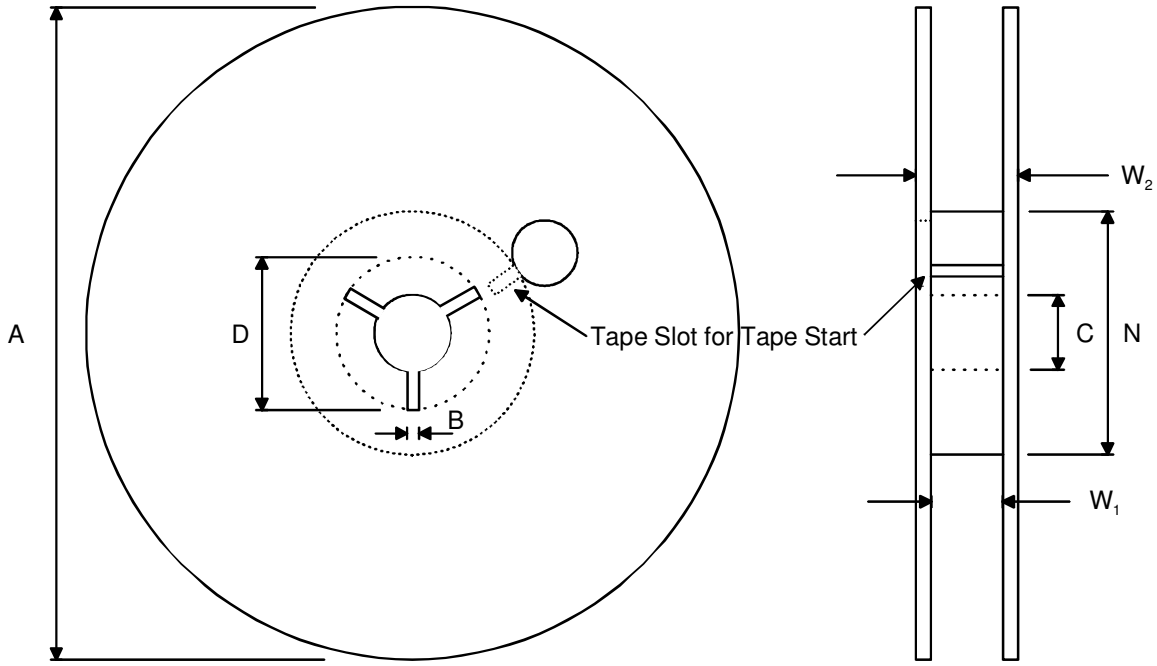
SOLDERING INFORMATION

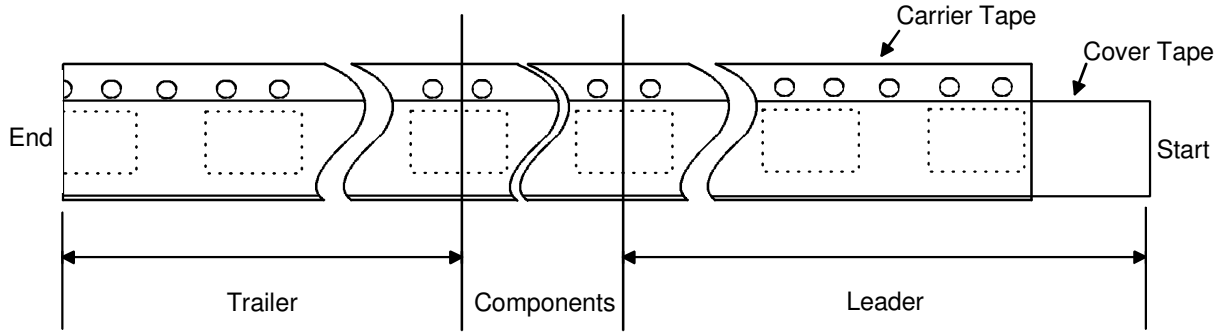
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS



REEL SPECIFICATIONS





Dimension	Min	Max	Unit
A		178	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	8.4	9.9	mm
W_2 (measured at hub)		14.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm

ORDERING INFORMATION

Product Code	Product	TE OUTPUT In QFN10	Package	Comments
MAS9279A1TG00	IC FOR VCTCXO		EWS Tested wafers 215 µm	For 8pF Crystal load
MAS9279A1HH06	IC FOR VCTCXO	TE1	QFN10, T&R, 3.000 pcs/reel; Pb free, RoHS compliant	For 8pF Crystal load
MAS9279A2TG00	IC FOR VCTCXO		EWS Tested wafers 215 µm	For 10pF Crystal load
MAS9279A2HH06	IC FOR VCTCXO	TE2	QFN10, T&R, 3.000 pcs/reel; Pb free, RoHS compliant	For 10pF Crystal load
MAS9279A3TG00	IC FOR VCTCXO Frequency output $f_0/2$		EWS Tested wafers 215 µm	For 8pF Crystal load
MAS9279A3HH06	IC FOR VCTCXO Frequency output $f_0/2$	TE1	QFN10, T&R, 3.000 pcs/reel; Pb free, RoHS compliant	For 8pF Crystal load
MAS9279A4TG00	IC FOR VCTCXO Frequency output $f_0/2$		EWS Tested wafers 215 µm	For 10pF Crystal load
MAS9279A4HH06	IC FOR VCTCXO Frequency output $f_0/2$	TE2	QFN10, T&R, 3.000 pcs/reel; Pb free, RoHS compliant	For 10pF Crystal load
MAS9279A5TG00	IC FOR TCXO		EWS Tested wafers 215 µm	For 8pF Crystal load
MAS9279A5HH06	IC FOR TCXO	TE1	QFN10, T&R, 3.000 pcs/reel; Pb free, RoHS compliant	For 8pF Crystal load
MAS9279A6TG00	IC FOR TCXO		EWS Tested wafers 215 µm	For 10pF Crystal load
MAS9279A6HH06	IC FOR TCXO	TE2	QFN10, T&R, 3.000 pcs/reel; Pb free, RoHS compliant	For 10pF Crystal load
MAS9279A7TG00	IC FOR TCXO Frequency output $f_0/2$		EWS Tested wafers 215 µm	For 8pF Crystal load
MAS9279A7HH06	IC FOR TCXO Frequency output $f_0/2$	TE1	QFN10, T&R, 3.000 pcs/reel; Pb free, RoHS compliant	For 8pF Crystal load
MAS9279A8TG00	IC FOR TCXO Frequency output $f_0/2$		EWS Tested wafers 215 µm	For 10pF Crystal load
MAS9279A8HH06	IC FOR TCXO Frequency output $f_0/2$	TE2	QFN10, T&R, 3.000 pcs/reel; Pb free, RoHS compliant	For 10pF Crystal load

Contact Micro Analog Systems Oy for other wafer thickness and bonding options

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