# Intel® LXT971A

*3.3V Dual-Speed Fast Ethernet PHY Transceiver*

**Datasheet**

The LXT971A is an IEEE compliant Fast Ethernet PHY Transceiver that directly supports both 100BASE-TX and 10BASE-T applications. It provides a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MACs). The LXT971A also provides a Low Voltage PECL (LVPECL) interface for use with 100BASE-FX fiber networks.

This document also supports the LXT971 device.

The LXT971A supports full-duplex operation at 10 Mbps and 100 Mbps. Its operating condition can be set using auto-negotiation, parallel detection, or manual control.

The LXT971A is fabricated with an advanced CMOS process and requires only a single 3.3V power supply.

## Applications

- Combination 10BASE-T/100BASE-TX or 100BASE-FX Network Interface Cards (NICs)
- 10/100 PCMCIA Cards
- Cable Modems and Set-Top Boxes

## Product Features

- 3.3V Operation.
- Low power consumption (300 mW typical).
- Low-power “Sleep” mode.
- 10BASE-T and 100BASE-TX using a single RJ-45 connection.
- Supports auto-negotiation and parallel detection.
- MII interface with extended register capability.
- Robust baseline wander correction performance.
- 100BASE-FX fiber-optic capable.
- Standard CSMA/CD or full-duplex operation.
- Supports JTAG boundary scan.
- Configurable via MDIO serial port or hardware control pins.
- Integrated, programmable LED drivers.
- 64-ball Plastic Ball Grid Array (PBGA).
  - — LXT971ABC - Commercial (0° to 70°C ambient).
  - —LXT971ABE - Extended (-40° to 85°C ambient).
- 64-pin Low-profile Quad Flat Package (LQFP).
  - — LXT971ALC - Commercial (0° to 70°C ambient).
  - — LXT971ALE - Extended (-40° to 85°C ambient).

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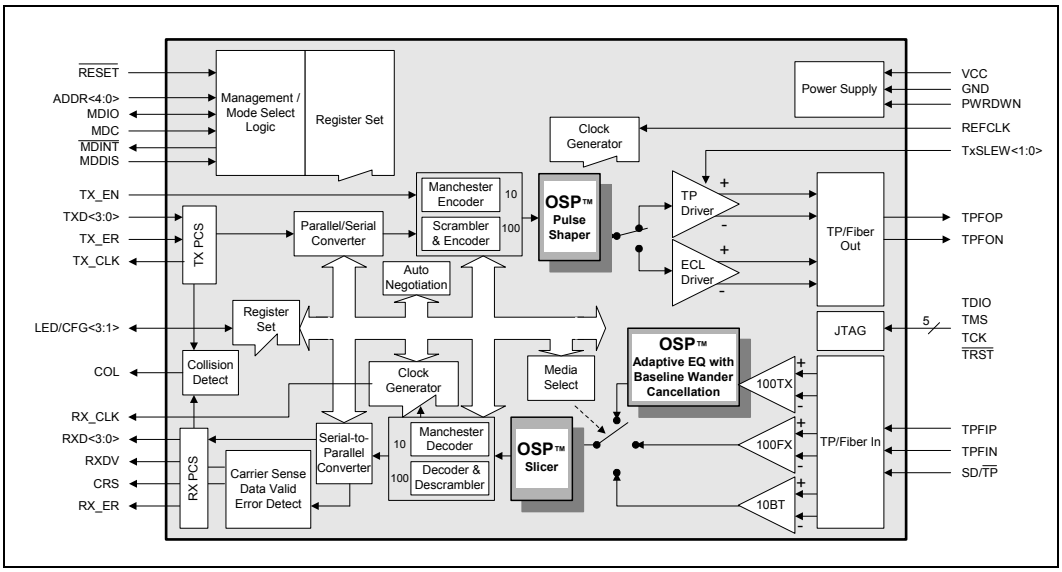
# Revision History

| Revision 002<br>Revision Date: August 6, 2002 | |
|---|---|
| **Page** | **Description** |
| | Globally replaced “pseudo-PECL” with Low-Voltage PECL”, except when identified with 5 V. |
| 1 | Front Page: Changed “pseudo-ECL (PECL)” to “Low Voltage PECL (LVPECL).<br>Added “JTAG Boundary Scan” to Product Features on front page. |
| 12 | Modified Figure 2 “LXT971A 64-Ball PBGA Assignments” (replaced TEST1 and TEST0 with GND). |
| 13 | Modified Figure 3 “LXT971A 64-Pin LQFP Assignments” (replaced TEST1 and TEST0 with GND). |
| 14 | Modified Table 1 “LQFP Numeric Pin List” (replaced TEST1 and TEST0 with GND). |
| 16 | Added note under Section 2.0, “Signal Descriptions”: “Intel recommends that all inputs and multi-function pins be tied to the inactive states and all outputs be left floating, if unused.” |
| 17 | Modified SD/$\overline{TP}$ description in Table 3 “LXT971A Network Interface Signal Descriptions”.<br>Added Table note 2. |
| 18 | Modified Table 4 “LXT971A Miscellaneous Signal Descriptions”. |
| 19 | Modified Table 5 “LXT971A Power Supply Signal Descriptions”. |
| 20 | Added Table 8 “LXT971A Pin Types and Modes”. |
| 22 | Replaced second paragraph under Section 3.2.1.2, “Fiber Interface”. |
| 23 | Added Section 3.2.2.1, “Increased MII Drive Strength”. |
| 23 | Changed “Far-End Fault” title to ‘100BASE-FX Far-End Fault”.<br>Modified first sentence under this heading. |
| 30 | Modified Figure 8 “Hardware Configuration Settings”. |
| 35 | Added paragraph after bullets under Section 3.6.7.2, “Test Loopback”. |
| 43 | Modified text under Section 3.7.3.4, “Fiber PMD Sublayer”. |
| 47 | Modified Table 13 “Supported JTAG Instructions”. |
| 47 | Modified Table 14 “Device ID Register”. |
| 52 | Added a new Section 4.3, “The Fiber Interface”. |
| 53 | Replaced Figure 25 “Typical LXT971A-to-3.3 V Fiber Transceiver Interface Circuitry”. |
| 54 | Added Figure 26 “Typical LXT971A-to-5 V Fiber Transceiver Interface Circuitry”. |
| 55 | Added Figure 27 “ON Semiconductor Triple PECL-to-LVPECL Translator”. |
| 56 | Modified Table 17 “Absolute Maximum Ratings”. |
| 56 | Modified Table 18 “Operating Conditions”: Added Typ values to Vcc current. |
| 57 | Modified Table 20 “Digital I/O Characteristics - MII Pins”. |
| 58 | Modified Table 22 “I/O Characteristics - LED/CFG Pins”. |
| 58 | Added Table 23 “I/O Characteristics – SD/TP Pin”. |
| 60 | Added Table 28 “LXT971A Thermal Characteristics”. |
| 65 | Modified Table 33 “10BASE-T Receive Timing Parameters” |
| 72 | Modified Table 42 “Register Bit Map”. (Added Table 26 information). |
| 86 | Added Table 57 “Digital Config Register (Address 26)”. |
| 87 | Modified Table 58 “Transmit Control Register (Address 30)”. |
| 90 | Added Section 8.0, “Product Ordering Information”. |

| Revision 001<br>Revision Date: January 2001 | |
|---|---|
| **Page** | **Description** |
| N/A | Clock Requirements: Modified language under Clock Requirements heading. |
| | Table 21 I/O Characteristics REFCLK: Changed values for Input Clock Duty Cycle under Min from 40 to 35 and under Max from 60 to 65. |

## Figure 1. LXT971A Block Diagram

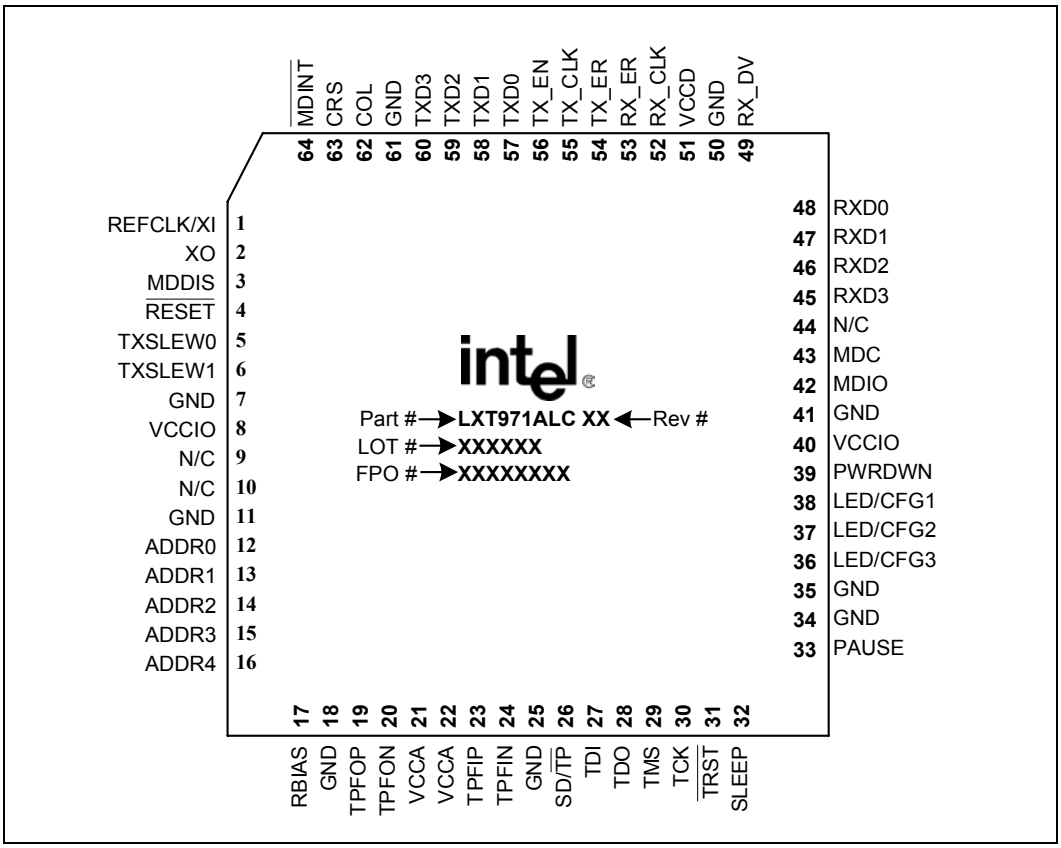


# 1.0 Pin Assignments

**Figure 2. LXT971A 64-Ball PBGA Assignments**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| A | $\overline{\text{MDINT}}$ | CRS | TXD3 | TXD0 | RX_ER | VCCD | RX_DV | RXD0 | A |
| B | REF CLK/XI | COL | TXD2 | TX_EN | TX_ER | RX_ CLK | N/C | RXD1 | B |
| C | XO | $\overline{\text{RESET}}$ | GND | TXD1 | TX_ CLK | GND | N/C | RXD2 | C |
| D | Tx SLEW0 | Tx SLEW1 | MDDIS | GND | VCCIO | RXD3 | N/C | MDIO | D |
| E | ADDR0 | ADDR1 | GND | GND | VCCIO | LED/ CFG1 | MDC | PWR DWN | E |
| F | ADDR3 | ADDR2 | GND | GND | TDI | TMS | LED/ CFG2 | LED/ CFG3 | F |
| G | ADDR4 | SD/$\overline{\text{TP}}$ | VCCA | VCCA | TDO | TCK | GND | GND | G |
| H | RBIAS | TPFOP | TPFON | TPFIP | TPFIN | $\overline{\text{TRST}}$ | SLEEP | PAUSE | H |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | |

**Figure 3. LXT971A 64-Pin LQFP Assignments**



## Table 1. LQFP Numeric Pin List

| Pin | Symbol | Type | Reference for Full Description |
|---|---|---|---|
| 1 | REFCLK/XI | Input | Table 4 on page 18 |
| 2 | XO | Output | Table 4 on page 18 |
| 3 | MDDIS | Input | Table 2 on page 16 |
| 4 | $\overline{\text{RESET}}$ | Input | Table 4 on page 18 |
| 5 | TxSLEW0 | Input | Table 4 on page 18 |
| 6 | TxSLEW1 | Input | Table 4 on page 18 |
| 7 | GND | – | Table 5 on page 19 |
| 8 | VCCIO | – | Table 5 on page 19 |
| 9 | N/C | – | Table 4 on page 18 |
| 10 | N/C | – | Table 4 on page 18 |
| 11 | GND | – | Table 5 on page 19 |
| 12 | ADDR0 | Input | Table 4 on page 18 |
| 13 | ADDR1 | Input | Table 4 on page 18 |
| 14 | ADDR2 | Input | Table 4 on page 18 |
| 15 | ADDR3 | Input | Table 4 on page 18 |
| 16 | ADDR4 | Input | Table 4 on page 18 |
| 17 | RBIAS | Analog Input | Table 4 on page 18 |
| 18 | GND | – | Table 5 on page 19 |
| 19 | TPFOP | Output | Table 3 on page 17 |
| 20 | TPFON | Output | Table 3 on page 17 |
| 21 | VCCA | – | Table 5 on page 19 |
| 22 | VCCA | – | Table 5 on page 19 |
| 23 | TPFIP | Input | Table 3 on page 17 |
| 24 | TPFIN | Input | Table 3 on page 17 |
| 25 | GND | – | Table 5 on page 19 |
| 26 | SD/$\overline{\text{TP}}$ | Input | Table 3 on page 17 |
| 27 | TDI | Input | Table 6 on page 19 |
| 28 | TDO | Output | Table 6 on page 19 |
| 29 | TMS | Input | Table 6 on page 19 |
| 30 | TCK | Input | Table 6 on page 19 |
| 31 | $\overline{\text{TRST}}$ | Input | Table 6 on page 19 |
| 32 | SLEEP | Input | Table 4 on page 18 |
| 33 | PAUSE | Input | Table 4 on page 18 |
| 34 | GND | – | Table 5 on page 19 |
| 35 | GND | – | Table 5 on page 19 |
| 36 | LED/CFG3 | I/O | Table 7 on page 19 |

## Table 1. LQFP Numeric Pin List (Continued)

| Pin | Symbol | Type | Reference for Full Description |
|---|---|---|---|
| 37 | LED/CFG2 | I/O | Table 7 on page 19 |
| 38 | LED/CFG1 | I/O | Table 7 on page 19 |
| 39 | PWRDWN | Input | Table 4 on page 18 |
| 40 | VCCIO | – | Table 5 on page 19 |
| 41 | GND | – | Table 5 on page 19 |
| 42 | MDIO | I/O | Table 2 on page 16 |
| 43 | MDC | Input | Table 2 on page 16 |
| 44 | N/C | – | Table 4 on page 18 |
| 45 | RXD3 | Output | Table 2 on page 16 |
| 46 | RXD2 | Output | Table 2 on page 16 |
| 47 | RXD1 | Output | Table 2 on page 16 |
| 48 | RXD0 | Output | Table 2 on page 16 |
| 49 | RX_DV | Output | Table 2 on page 16 |
| 50 | GND | – | Table 5 on page 19 |
| 51 | VCCD | – | Table 5 on page 19 |
| 52 | RX_CLK | Output | Table 2 on page 16 |
| 53 | RX_ER | Output | Table 2 on page 16 |
| 54 | TX_ER | Input | Table 2 on page 16 |
| 55 | TX_CLK | Output | Table 2 on page 16 |
| 56 | TX_EN | Input | Table 2 on page 16 |
| 57 | TXD0 | Input | Table 2 on page 16 |
| 58 | TXD1 | Input | Table 2 on page 16 |
| 59 | TXD2 | Input | Table 2 on page 16 |
| 60 | TXD3 | Input | Table 2 on page 16 |
| 61 | GND | – | Table 5 on page 19 |
| 62 | COL | Output | Table 2 on page 16 |
| 63 | CRS | Output | Table 2 on page 16 |
| 64 | $\overline{\text{MDINT}}$ | Open Drain | Table 2 on page 16 |

# 2.0 Signal Descriptions

*Note:* Intel recommends that all inputs and multi-function pins be tied to the inactive states and all outputs be left floating, if unused.

## Table 2. LXT971A MII Signal Descriptions

| PBGA Pin# | LQFP Pin# | Symbol | Type[1] | Signal Description |
|---|---|---|---|---|
| **Data Interface Pins** | | | | |
| A3<br>B3<br>C4<br>A4 | 60<br>59<br>58<br>57 | TXD3<br>TXD2<br>TXD1<br>TXD0 | I | **Transmit Data**. TXD is a bundle of parallel data signals that are driven by the MAC. TXD<3:0> transitions synchronously with respect to the TX_CLK. TXD<0> is the least significant bit. |
| B4 | 56 | TX_EN | I | **Transmit Enable**. The MAC asserts this signal when it drives valid data on TXD. This signal must be synchronized to TX_CLK. |
| C5 | 55 | TX_CLK | O | **Transmit Clock**. TX_CLK is sourced by the PHY in both 10 and 100 Mbps operations.<br>2.5 MHz for 10 Mbps operation, 25 MHz for 100 Mbps operation. |
| D6<br>C8<br>B8<br>A8 | 45<br>46<br>47<br>48 | RXD3<br>RXD2<br>RXD1<br>RXD0 | O | **Receive Data**. RXD is a bundle of parallel signals that transition synchronously with respect to the RX_CLK. RXD<0> is the least significant bit. |
| A7 | 49 | RX_DV | O | **Receive Data Valid**. The LXT971A asserts this signal when it drives valid data on RXD. This output is synchronous to RX_CLK. |
| A5 | 53 | RX_ER | O | **Receive Error**. Signals a receive error condition has occurred. This output is synchronous to RX_CLK. |
| B5 | 54 | TX_ER | I | **Transmit Error**. Signals a transmit error condition. This signal must be synchronized to TX_CLK. |
| B6 | 52 | RX_CLK | O | **Receive Clock**. 25 MHz for 100 Mbps operation, 2.5 MHz for 10 Mbps operation. Refer to "Clock Requirements" on page 26 in Section 3.0, "Functional Description". |
| B2 | 62 | COL | O | **Collision Detected**. The LXT971A asserts this output when a collision is detected. This output remains High for the duration of the collision. This signal is asynchronous and is inactive during full-duplex operation. |
| A2 | 63 | CRS | O | **Carrier Sense**. During half-duplex operation (Register bit 0.8 = 0), the LXT971A asserts this output when either transmitting or receiving data packets. During full-duplex operation (Register bit 0.8 = 1), CRS is asserted only during receive. CRS assertion is asynchronous with respect to RX_CLK. CRS is de-asserted on loss of carrier, synchronous to RX_CLK. |
| 1. Type Column Coding: I = Input, O = Output, A = Analog, OD = Open Drain | | | | |

## Table 2. LXT971A MII Signal Descriptions (Continued)

| PBGA Pin# | LQFP Pin# | Symbol | Type[1] | Signal Description |
|---|---|---|---|---|
| **MII Control Interface Pins** | | | | |
| D3 | 3 | MDDIS | I | **Management Disable**. When MDDIS is High, the MDIO is disabled from read and write operations.<br>When MDDIS is Low at power-up or reset, the Hardware Control Interface pins control only the initial or "default" values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel. |
| E7 | 43 | MDC | I | **Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 8 MHz. |
| D8 | 42 | MDIO | I/O | **Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication. |
| A1 | 64 | $\overline{\text{MDINT}}$ | OD | **Management Data Interrupt**. When Register bit 18.1 = 1, an active Low output on this pin indicates status change. Interrupt is cleared by reading Register 19. |
| 1. Type Column Coding: I = Input, O = Output, A = Analog, OD = Open Drain | | | | |

## Table 3. LXT971A Network Interface Signal Descriptions

| PBGA Pin# | LQFP Pin# | Symbol | Type[1] | Signal Description |
|---|---|---|---|---|
| H2<br>H3 | 19<br>20 | TPFOP<br>TPFON | O | Twisted-Pair/Fiber Outputs, Positive & Negative.<br>During 100BASE-TX or 10BASE-T operation, TPFOP/N pins drive 802.3 compliant pulses onto the line.<br>During 100BASE-FX operation, TPFOP/N pins produce differential LVPECL outputs for fiber transceivers. |
| H4<br>H5 | 23<br>24 | TPFIP<br>TPFIN | I | Twisted-Pair/Fiber Inputs, Positive & Negative.<br>During 100BASE-TX or 10BASE-T operation, TPFIP/N pins receive differential 100BASE-TX or 10BASE-T signals from the line.<br>During 100BASE-FX operation, TPFIP/N pins receive differential LVPECL inputs from fiber transceivers. |
| G2 | 26 | SD/$\overline{\text{TP}}$ | I | **Signal Detect**[2]: Dual function input depending on the state of the device.<br>**Reset and Power-Up.** Media mode selection:<br>Tie High for FX mode (Register bit 16.0 = 1)<br>Tie Low for TP mode (Register bit 16.0 = 0)<br>**Normal Operation (FX Mode):** SD input from the fiber transceiver.<br>**Normal Operation (TP Mode):** Tie to GND (uses an internal pull-down). |
| 1. Type Column Coding: I = Input, O = Output, A = Analog, OD = Open Drain<br>2. For standard digital loopback testing (Register bit 0.14) in FX mode, the SD pin should be tied to an LVPECL logic High (2.4 V). | | | | |

## Table 4. LXT971A Miscellaneous Signal Descriptions

| PBGA Pin# | LQFP Pin# | Symbol | Type[1] | Signal Description |
|---|---|---|---|---|
| D1<br>D2 | 5<br>6 | TxSLEW0<br>TxSLEW1 | I | **Tx Output Slew Controls 0 and 1**. These pins select the TX output slew rate (rise and fall time) as follows:<br>TxSLEW1 / TxSLEW0 / Slew Rate (Rise and Fall Time)<br>0 / 0 / 3.0 ns<br>0 / 1 / 3.4 ns<br>1 / 0 / 3.9 ns<br>1 / 1 / 4.4 ns |
| C2 | 4 | $\overline{\text{RESET}}$ | I | **Reset**. This active Low input is OR'ed with the control register Reset bit (Register bit 0.15). The LXT971A reset cycle is extended to 258 µs (nominal) after reset is de-asserted. |
| G1<br>F1<br>F2<br>E2<br>E1 | 16<br>15<br>14<br>13<br>12 | ADDR4<br>ADDR3<br>ADDR2<br>ADDR1<br>ADDR0 | I<br>I<br>I<br>I<br>I | **Address <4:0>**. Sets device address. |
| H1 | 17 | RBIAS | AI | **Bias**. This pin provides bias current for the internal circuitry. Must be tied to ground through a 22.1 kΩ, 1% resistor. |
| H8 | 33 | PAUSE | I | **Pause**. When set High, the LXT971A advertises Pause capabilities during auto-negotiation. |
| H7 | 32 | SLEEP | I | **Sleep**. When set High, this pin enables the LXT971A to go into a low-power sleep mode. The value of this pin can be overridden by Register bit 16.6 when in managed mode. |
| E8 | 39 | PWRDWN | I | **Power Down**. When set High, this pin puts the LXT971A in a power-down mode. |
| B1<br>C1 | 1<br>2 | REFCLK/XI<br>XO | I<br>O | **Crystal Input and Output**. A 25 MHz crystal oscillator circuit can be connected across XI and XO. A clock can also be used at XI. Refer to "Clock Requirements" on page 26 in the Functional Description section. |
| B7, C7<br>D7 | 9, 10<br>44 | N/C | - | **No Connection**. These pins are not used and should not be terminated. |

1. Type Column Coding: I = Input, O = Output, A = Analog, OD = Open Drain.

### Table 5. LXT971A Power Supply Signal Descriptions

| PBGA Pin# | LQFP Pin# | Symbol | Type | Signal Description |
|---|---|---|---|---|
| A6 | 51 | VCCD | – | **Digital Power.** Requires a 3.3V power supply. |
| D4, E3 E4, F3 F4, C6, C3, G7, G8 | 7, 11, 18, 25, 34, 35, 41, 50, 61 | GND | – | **Ground.** |
| E5, D5 | 8, 40 | VCCIO | – | **MII Power.** Requires either a 3.3V or a 2.5V supply. Must be supplied from the same source used to power the MAC on the other side of the MII. |
| G3, G4 | 21, 22 | VCCA | – | **Analog Power.** Requires a 3.3V power supply. |

### Table 6. LXT971A JTAG Test Signal Descriptions

| PBGA Pin# | LQFP Pin# | Symbol | Type[1] | Signal Description |
|---|---|---|---|---|
| F5 | 27 | TDI[2] | I | **Test Data Input**. Test data sampled with respect to the rising edge of TCK. |
| G5 | 28 | TDO[2] | O | **Test Data Output**. Test data driven with respect to the falling edge of TCK. |
| F6 | 29 | TMS[2] | I | **Test Mode Select**. |
| G6 | 30 | TCK[2] | I | **Test Clock**. Test clock input sourced by ATE. |
| H6 | 31 | $\overline{\text{TRST}}$[2] | I | **Test Reset**. Test reset input sourced by ATE. |

1. Type Column Coding: I = Input, O = Output, A = Analog, OD = Open Drain.
2. If JTAG port is not used, these pins do not need to be terminated.

### Table 7. LXT971A LED Signal Descriptions

| PBGA Pin# | LQFP Pin# | Symbol | Type[1] | Signal Description |
|---|---|---|---|---|
| E6<br>F7<br>F8 | 38<br>37<br>36 | LED/CFG1<br>LED/CFG2<br>LED/CFG3 | I/O | **LED Drivers 1-3.** These pins drive LED indicators. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 56 on page 85 for details).<br>**Configuration Inputs 1-3.** These pins also provide initial configuration settings (refer to Table 9 on page 30 for details). |

1. Type Column Coding: I = Input, O = Output, A = Analog, OD = Open Drain.
2. Pull-up/pull-down resistors of 10 k can be implemented if LEDs are used in the design.

### Table 8. LXT971A Pin Types and Modes

| Modes | RXD 0-3 | RXDV | Tx/Rx CLKS Output | RXER Output | COL Output | CRS Output | TXD 0-3 Input | TXEN Input | TXER Input |
|---|---|---|---|---|---|---|---|---|---|
| HWReset | DL | DL | DH | DL | DL | DL | IPLD | IPLD | IPLD |
| SFTPWRDN | DL | DL | Active | DL | DL | DL | IPLD | IPLD | IPLD |
| HWPWRDN | High Z | High Z | High Z | High Z | High Z | High Z | High Z | High Z | High Z |
| ISOLATE | HZ w/ IPLD | HZ w/ IPLD | HZ w/ IPLD | HZ w/ IPLD | HZ w/ IPLD | HZ w/ IPLD | IPLD | IPLD | IPLD |
| SLEEP | DL | DL | DL | DL | DL | DL | IPLD | IPLD | IPLD |

1. A High Z (High impedance) or three-state determines when the device is drawing a current of less than 20 nA. A High Z with PLD (High impedance with pull-down) state determines when the device is drawing a current of less than 20 µA.
2. DL = Driven Low (Logic 0), DH = Driven High (Logic 1), IPLD = Internal Pull-Down (Weak)

# 3.0 Functional Description

## 3.1 Introduction

The LXT971A is a single-port Fast Ethernet 10/100 transceiver that supports 10 Mbps and 100 Mbps networks and complies with all applicable requirements of IEEE 802.3. The LXT971A directly drives either a 100BASE-TX line (up to 140 meters) or a 10BASE-T line (up to 185 meters). The device also supports 100BASE-FX operation via a Low Voltage PECL (LVPECL) interface.

### 3.1.1 Comprehensive Functionality

The LXT971A provides a standard Media Independent Interface (MII) for 10/100 MACs. The LXT971A performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X standard. This device also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

The LXT971A reads its configuration pins on power-up to check for forced operation settings. If not configured for forced operation, the device uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT971A auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT971A automatically detects the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and sets its operating conditions accordingly.

The LXT971A provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

### 3.1.2 OSP™ Architecture

The LXT971A incorporates high-efficiency Optimal Signal Processing™ design techniques, combining the best properties of digital and analog signal processing to produce a truly optimal device.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). This results in improved receiver noise and cross-talk performance.

The OSP signal processing scheme also requires substantially less computational logic than traditional DSP-based designs. This lowers power consumption and also reduces the logic switching noise generated by DSP engines. This logic switching noise can be a considerable source of EMI generated on the device's power supplies.

The OSP-based LXT971A provides improved data recovery, EMI performance and low power consumption.

## 3.2 Network Media / Protocol Support

The LXT971A supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX).

### 3.2.1 10/100 Network Interface

The network interface port consists of five external pins (two differential signal pairs and a signal detect pin). The I/O pins are shared between twisted-pair (TP) and fiber. Refer to Figure 3 on page 13 for specific pin assignments.

The LXT971A output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX output. When not transmitting data, the LXT971A generates 802.3-compliant link pulses or idle code. Input signals are decoded either as a 100BASE-TX, 100BASE-FX, or 10BASE-T input, depending on the mode selected. Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

#### 3.2.1.1 Twisted-Pair Interface

The LXT971A supports either 100BASE-TX or 10BASE-T connections over 100Ω, Category 5, Unshielded Twisted Pair (UTP) cable. When operating at 100 Mbps, the LXT971A continuously transmits and receives MLT3 symbols. When not transmitting data, the LXT971A generates “IDLE” symbols.

During 10 Mbps operation, Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state. Link pulses are transmitted periodically to keep the link up.

Only a transformer, RJ-45 connector, load resistor, and bypass capacitors are required to complete this interface. On the transmit side, the LXT971A has an active internal termination and does not require external termination resistors. Intel's patented waveshaping technology shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings (refer to Table 4 on page 18) allow the designer to match the output waveform to the magnetic characteristics. On the receive side, the internal impedance is high enough that it has no practical effect on the external termination circuit.

#### 3.2.1.2 Fiber Interface

The LXT971A fiber port is designed to interface with common industry-standard fiber modules. It incorporates a Low Voltage PECL interface that complies with the ANSI X3.166 standard for seamless integration.

Fiber mode is selected through Register bit 16.0 by the following two methods:

1. Drive the SD input to a value greater than 600 mV during power-up and reset states (all LVPECL signaling levels from a fiber transceiver are acceptable).
2. Configure Register bit 16.0 = 1 through the MDIO interface.

#### 3.2.1.3 Fault Detection and Reporting

The LXT971A supports two fault detection and reporting mechanisms. “Remote Fault” refers to a MAC-to-MAC communication function that is essentially transparent to PHY layer devices. It is used only during auto-negotiation, and is applicable only to twisted-pair links. “Far-End Fault” is an optional PMA-layer function that may be embedded within PHY devices. The LXT971A supports both functions (see Section 3.2.1.3.1 and Section 3.2.1.3.2).

##### 3.2.1.3.1 Remote Fault

Register bit 4.13 in the Auto-Negotiation Advertisement Register is reserved for Remote Fault indications. It is typically used when re-starting the auto-negotiation sequence to indicate to the link partner that the link is down because the advertising device detected a fault.

When the LXT971A receives a Remote Fault indication from its partner during auto-negotiation it does the following:

- Sets Register bit 5.13 in the Link Partner Base Page Ability Register, and
- Sets the Remote Fault Register bit 1.4 in the MII Status Register to pass this information to the local controller.

##### 3.2.1.3.2 100BASE-FX Far-End Fault

The SD/$\overline{\text{TP}}$ pin monitors signal quality during normal operation in fiber mode. If the signal quality degrades beyond the fault threshold, the fiber transceiver reports a signal quality fault condition via the SD/$\overline{\text{TP}}$ pin. Loss of signal quality blocks any fiber data from being received and causes a link loss.

If the LXT971A detects a signal fault condition, it can transmit the Far-End Fault Indication (FEFI) over the fiber link. The FEFI consists of 84 consecutive ones followed by a single zero. This pattern must be repeated at least three times. The LXT971A transmits the far-end fault code a minimum of three times if all the following conditions are true:

- Fiber mode is selected.
- Fault Code transmission is enabled (Register bit 16.2 = 1).
- Either Signal Detect indicates no signal or the receive PLL cannot lock.
- Loopback is not enabled.

### 3.2.2 MII Data Interface

The LXT971A supports a standard Media Independent Interface (MII). The MII consists of a data interface and a management interface. The MII Data Interface passes data between the LXT971A and a Media Access Controller (MAC). Separate parallel buses are provided for transmit and receive. This interface operates at either 10 Mbps or 100 Mbps. The speed is set automatically, once the operating conditions of the network link have been determined. Refer to “MII Operation” on page 32 for additional details.

#### 3.2.2.1 Increased MII Drive Strength

A higher Media Independent Interface (MII) drive strength may be desired in some designs to drive signals over longer PCB trace lengths, or over high-capacitive loads, through multiple vias, or through a connector. The MII drive strength in the LXT971A can be increased by setting Register

bit 26.11 through software control. Setting Register bit 26.11 = 1 through the MDC/MDIO interface sets the MII pins (RXD[0:3], RX_DV, RX_CLK, RX_ER, COL, CRS, and TX_CLK) to a higher drive strength.

## 3.2.3 Configuration Management Interface

The LXT971A provides both an MDIO interface and a Hardware Control Interface for device configuration and management.

### 3.2.3.1 MDIO Management Interface

The LXT971A supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT971A. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers.

Some registers are required and their functions are defined by the IEEE 802.3 standard. The LXT971A also supports additional registers for expanded functionality. The LXT971A supports multiple internal registers, each of which is 16 bits wide. Specific register bits are referenced using an “X.Y” notation, where X is the register number (0-31) and Y is the bit number (0-15).

The physical interface consists of a data line (MDIO) and clock line (MDC). Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, the MDIO read and write operations are disabled and the Hardware Control Interface provides primary configuration control. When MDDIS is Low, the MDIO port is enabled for both read and write operations and the Hardware Control Interface is not used.

#### 3.2.3.1.1 MDIO Addressing

The protocol allows one controller to communicate with multiple LXT971A chips. Pins ADDR<4:0> determine the chip address.

#### 3.2.3.1.2 MDIO Frame Structure

The physical interface consists of a data line (MDIO) and clock line (MDC). The frame structure is shown in Figures 4 and 5 (read and write). MDIO Interface timing is shown in Table 38 on page 69.

**Figure 4. Management Interface Read Frame Structure**

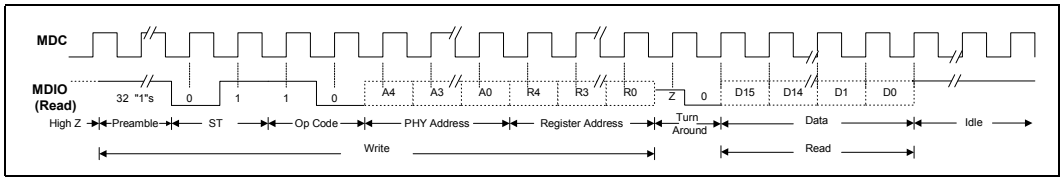
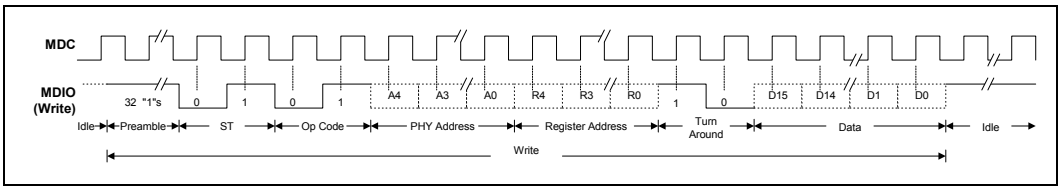


**Figure 5. Management Interface Write Frame Structure**




#### 3.2.3.1.3 MII Interrupts

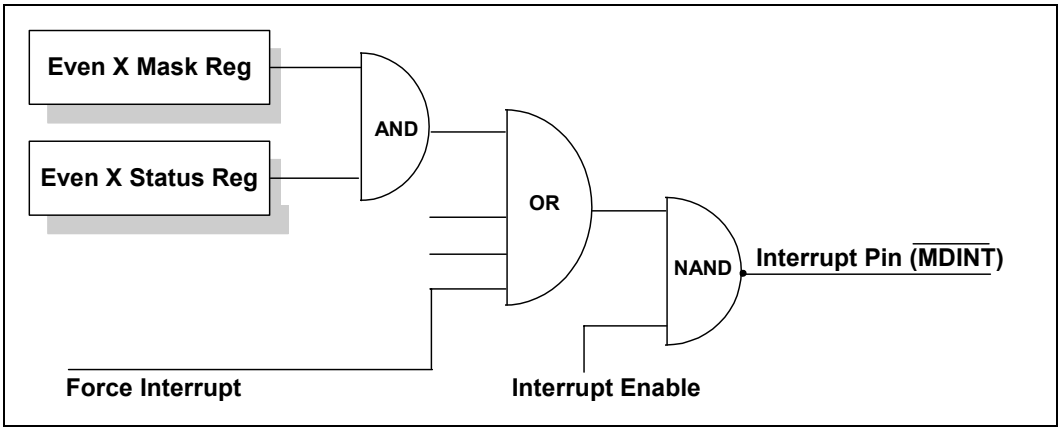
The LXT971A provides a single interrupt pin ($\overline{\text{MDINT}}$). Interrupt logic is shown in Figure 6. The LXT971A also provides two dedicated interrupt registers. Register 18 provides interrupt enable and mask functions and Register 19 provides interrupt status. Setting Register bit 18.1 = 1, enables the device to request interrupt via the $\overline{\text{MDINT}}$ pin. An active Low on this pin indicates a status change on the LXT971A. Interrupts may be caused by four conditions:

- Auto-negotiation complete
- Speed status change
- Duplex status change
- Link status change

### 3.2.3.2 Hardware Control Interface

The LXT971A provides a Hardware Control Interface for applications where the MDIO is not desired. The Hardware Control Interface uses the three LED driver pins to set device configuration. Refer to the Hardware Configuration Settings section on page 30 for additional details.

**Figure 6. Interrupt Logic**



# 3.3 Operating Requirements

## 3.3.1 Power Requirements

The LXT971A requires three power supply inputs (VCCD, VCCA, and VCCIO). The digital and analog circuits require 3.3V supplies (VCCD and VCCA). These inputs may be supplied from a single source. Each supply input must be de-coupled to ground.

An additional supply may be used for the MII (VCCIO). The supply may be either +2.5V or +3.3V. Also, the inputs on the MII interface are tolerant to 5V signals from the controller on the other side of the MII interface. Refer to Table 20 on page 57 for MII I/O characteristics.

As a matter of good practice, these supplies should be as clean as possible.

## 3.3.2 Clock Requirements

### 3.3.2.1 External Crystal/Oscillator

The LXT971A requires a reference clock input that is used to generate transmit signals and recover receive signals. It may be provided by either of two methods: by connecting a crystal across the oscillator pins (XI and XO), or by connecting an external clock source to pin XI. The connection of a clock source to the XI pin requires the XO pin to be left open. A crystal-based clock is recommended over a derived clock (i.e., PLL-based) to minimize transmit jitter. Refer to the LXT971A/972A Design and Layout Guide for a list of recommended clock sources.

A crystal is typically used in NIC applications. An external 25 MHz clock source, rather than a crystal, is frequently used in switch applications. Refer to Table 21 on page 57 for clock timing requirements.

### 3.3.2.2 MDIO Clock

The MII management channel (MDIO) also requires an external clock. The managed data clock (MDC) speed is a maximum of 8 MHz. Refer to Table 38 on page 69 for details.

# 3.4 Initialization

When the LXT971A is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link. The configuration bits may be set by the Hardware Control or MDIO interface as shown in Figure 7.

## 3.4.1 MDIO Control Mode

In the MDIO Control mode, the LXT971A reads the Hardware Control Interface pins to set the initial (default) values of the MDIO registers. Once the initial values are set, bit control reverts to the MDIO interface.

### 3.4.2 Hardware Control Mode

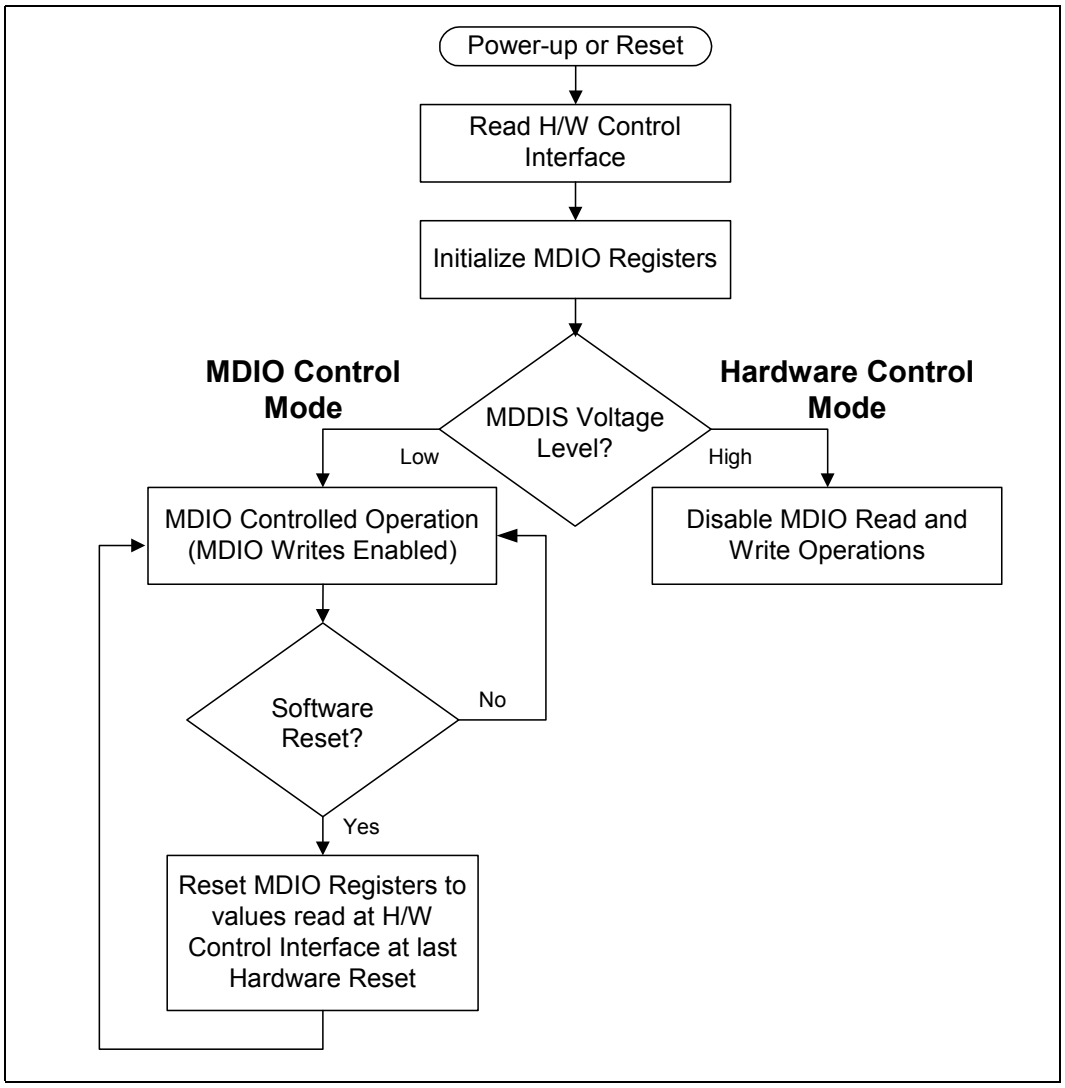
In the Hardware Control Mode, LXT971A disables direct write operations to the MDIO registers via the MDIO Interface. On power-up or hardware reset the LXT971A reads the Hardware Control Interface pins and sets the MDIO registers accordingly.

The following modes are available using either Hardware Control or MDIO Control:

- Force network link to 100FX (Fiber).
- Force network link operation to:
  - 100BASE-TX, Full-Duplex.
  - 100BASE-TX, Half-Duplex.
  - 10BASE-T, Full-Duplex.
  - 10BASE-T, Half-Duplex.
- Allow auto-negotiation/parallel-detection.

When the network link is forced to a specific configuration, the LXT971A immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT971A begins the auto-negotiation/parallel-detection operation.

**Figure 7. Initialization Sequence**




## 3.4.3 Reduced Power Modes

The LXT971A offers two power-down modes and a sleep mode.

### 3.4.3.1 Hardware Power Down

The hardware power-down mode is controlled by the PWRDWN pin. When PWRDWN is High, the following conditions are true:

- The LXT971A network port and clock are shut down.
- All outputs are three-stated.
- All weak pad pull-up and pull-down resistors are disabled.
- The MDIO registers are not accessible.

#### 3.4.3.2 Software Power Down

Software power-down control is provided by Register bit 0.11 in the Control Register (refer to Table 43 on page 74). During soft power-down, the following conditions are true:

- The network port is shut down.
- The MDIO registers remain accessible.

#### 3.4.3.3 Sleep Mode

The LXT971A supports a power-saving sleep mode. Sleep mode is enabled when SLEEP is asserted via pin 32(LQFP)/H7(PBGA). The value of pin 32/H7 can be overridden by Register bit 16.6 when in managed mode as shown in Table 4 on page 18. The LXT971A enters into sleep mode when SLEEP is enabled and no energy is detected on the twisted-pair input for 1-3 seconds (the time is controlled by Register bits 16.4:3 in the Configuration Register, with a default of 3.04 seconds).

During this mode, the LXT971A still responds to management transactions (MDC/MDIO). In this mode the power consumption is minimized, and the supply current is reduced below the maximum value given in Table 18 on page 56. If the LXT971A detects activity on the twisted-pair inputs, it comes out of the sleep state and check for link. If no link is detected in 1-3 seconds (programmable) it reverts back to the low power sleep state.

***Note:*** Sleep Mode is not functional in fiber network applications.

### 3.4.4 Reset

The LXT971A provides both hardware and software resets. Configuration control of auto-negotiation, speed, and duplex mode selection is handled differently for each. During a hardware reset, auto-negotiation and speed configuration settings are read in from pins (refer to Table 9 on page 30 for pin settings and to Table 43 on page 74 for register bit definitions).

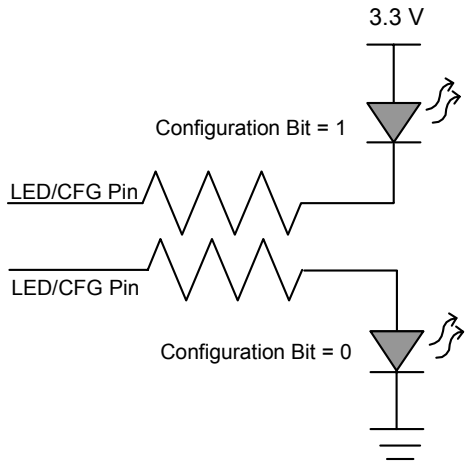
During a software reset (0.15 = 1), these bit settings are not re-read from the pins. They revert back to the values that were read in during the last hardware reset. Therefore, any changes to pin values made since the last hardware reset is not detected during a software reset.

During a hardware reset, register information is unavailable for 1 ms after de-assertion of the reset. During a software reset (0.15 = 1) the registers are available for reading. The reset bit should be polled to see when the part has completed reset (0.15 = 0).

## 3.4.5 Hardware Configuration Settings

The LXT971A provides a hardware option to set the initial device configuration. The hardware option uses the three LED driver pins. This provides three control bits, as listed in Table 9. The LED drivers can operate as either open-drain or open-source circuits as shown in Figure 8.

**Figure 8. Hardware Configuration Settings**




1. The LED/CFG pins automatically adjust their polarity upon power-up or reset.
2. Unused LEDs may be implemented with pull-up/ pull-down resistors of 10 K.

**Table 9. Hardware Configuration Settings**

| Desired Mode | | | LED/CFG*n* Pin Settings[1] | | | Resulting Register Bit Values | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Control Register | | | AN Advertisement Registers | | | |
| Auto-Neg | Speed (Mbps) | Duplex | 1 | 2 | 3 | Auto-Neg 0.12 | Speed 0.13 | FD 0.8 | 100FD 4.8 | 100TX 4.7 | 10FD 4.6 | 10T 4.5 |
| Disabled | 10 | Half | Low | Low | Low | 0 | 0 | 0 | N/A Auto-Negotiation Advertisement | | | |
| | | Full | Low | Low | High | | | 1 | | | | |
| | 100 | Half | Low | High | Low | | 1 | 0 | | | | |
| | | Full | Low | High | High | | | 1 | | | | |
| Enabled | 100 Only | Half | High | Low | Low | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| | | Full | High | Low | High | | | 1 | 1 | 1 | 0 | 0 |
| | 10/100 | Half Only | High | High | Low | | | 0 | 0 | 1 | 0 | 1 |
| | | Full or Half | High | High | High | | | 1 | 1 | 1 | 1 | 1 |

1. Refer to Table 7 on page 19 for LED/CFG pin assignments.

## 3.5 Establishing Link

See Figure 9 for an overview of link establishment.

### 3.5.1 Auto-Negotiation

If not configured for forced operation, the LXT971A attempts to auto-negotiate with its link partner by sending Fast Link Pulse (FLP) bursts. Each burst consists of up to 33 link pulses spaced 62.5 µs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may be present or absent to indicate a "1" or a "0". Each FLP burst exchanges 16 bits of data, which are referred to as a "link code word". All devices that support auto-negotiation must implement the "Base Page" defined by IEEE 802.3 (registers 4 and 5). LXT971A also supports the optional "Next Page" function as described in Tables 50 and 51 on page 80 (registers 7 and 8).

#### 3.5.1.1 Base Page Exchange

By exchanging Base Pages, the LXT971A and its link partner communicate their capabilities to each other. Both sides must receive at least three identical base pages for negotiation to continue. Each side identifies the highest common capabilities that both sides support and configures itself accordingly.

#### 3.5.1.2 Next Page Exchange

Additional information, above that required by base page exchange is also sent via "Next Pages". The LXT971A fully supports the IEEE 802.3ab method of negotiation via Next Page exchange.

#### 3.5.1.3 Controlling Auto-Negotiation

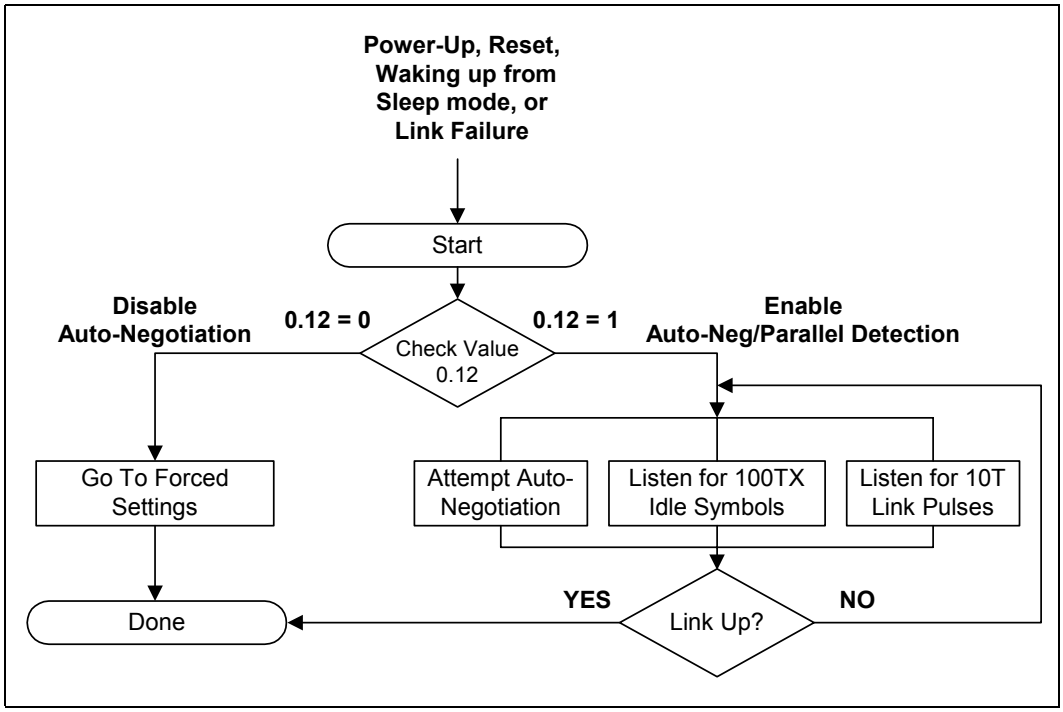
When auto-negotiation is controlled by software, the following steps are recommended:

- After power-up, power-down, or reset, the power-down recovery time, as specified in Table 40 on page 70, must be exhausted before proceeding.
- Set the Auto-Negotiation Advertisement Register bits.
- Enable auto-negotiation (set MDIO Register bit 0.12 = 1).

### 3.5.2 Parallel Detection

For the parallel detection feature of auto-negotiation, the LXT971A also monitors for 10BASE-T Normal Link Pulses (NLP) and 100BASE-TX Idle symbols. If either is detected, the device automatically reverts to the corresponding operating mode. Parallel detection allows the LXT971A to communicate with devices that do not support auto-negotiation.

**Figure 9. Link Establishment Overview**




## 3.6 MII Operation

The LXT971A device implements the Media Independent Interface (MII) as defined in the IEEE 802.3 standard. Separate channels are provided for transmitting data from the MAC to the LXT971A (TXD), and for passing data received from the line (RXD) to the MAC. Each channel has its own clock, data bus, and control signals. Nine signals are used to pass received data to the MAC: RXD<3:0>, RX_CLK, RX_DV, RX_ER, COL, and CRS. Seven signals are used to transmit data from the MAC: TXD<3:0>, TX_CLK, TX_EN, and TX_ER.

The LXT971A supplies both clock signals as well as separate outputs for carrier sense and collision. Data transmission across the MII is normally implemented in 4-bit-wide nibbles.

### 3.6.1 MII Clocks

The LXT971A is the master clock source for data transmission and supplies both MII clocks (RX_CLK and TX_CLK). It automatically sets the clock speeds to match link conditions. When the link is operating at 100 Mbps, the clocks are set to 25 MHz. When the link is operating at 10 Mbps, the clocks are set to 2.5 MHz. Figures 10 through 12 show the clock cycles for each mode. The transmit data and control signals must always be synchronized to TX_CLK by the MAC. The LXT971A samples these signals on the rising edge of TX_CLK.

### 3.6.2 Transmit Enable

The MAC must assert TX_EN the same time as the first nibble of preamble, and de-assert TX_EN after the last bit of the packet.

### 3.6.3 Receive Data Valid

The LXT971A asserts RX_DV when it receives a valid packet. Timing changes depend on line operating speed:

- For 100BASE-TX links, RX_DV is asserted from the first nibble of preamble to the last nibble of the data packet.
- For 10BT links, the entire preamble is truncated. RX_DV is asserted with the first nibble of the Start of Frame Delimiter (SFD) “5D” and remains asserted until the end of the packet.

### 3.6.4 Carrier Sense

Carrier Sense (CRS) is an asynchronous output. It is always generated when a packet is received from the line and in half-duplex mode when a packet is transmitted. Table 10 summarizes the conditions for assertion of carrier sense, collision, and data loopback signals.

Carrier sense is not generated when a packet is transmitted and in full-duplex mode.

### 3.6.5 Error Signals

When LXT971A is in 100 Mbps mode and receives an invalid symbol from the network, it asserts RX_ER and drives “1110” on the RXD pins.

When the MAC asserts TX_ER, the LXT971A drives “H” symbols out on the TPFOP/N pins.

### 3.6.6 Collision

The LXT971A asserts its collision signal, asynchronously to any clock, whenever the line state is half-duplex and the transmitter and receiver are active at the same time. Table 10 summarizes the conditions for assertion of carrier sense, collision, and data loopback signals.

**Figure 10. 10BASE-T Clocking**

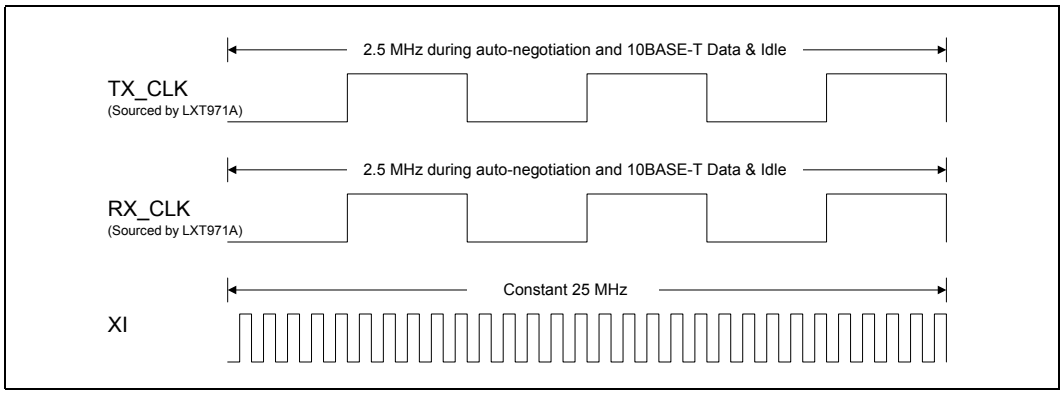



**Figure 11. 100BASE-X Clocking**

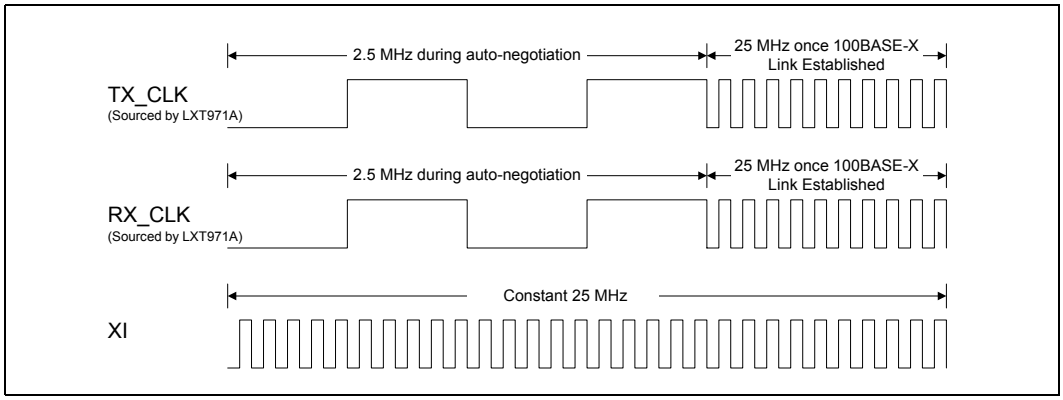
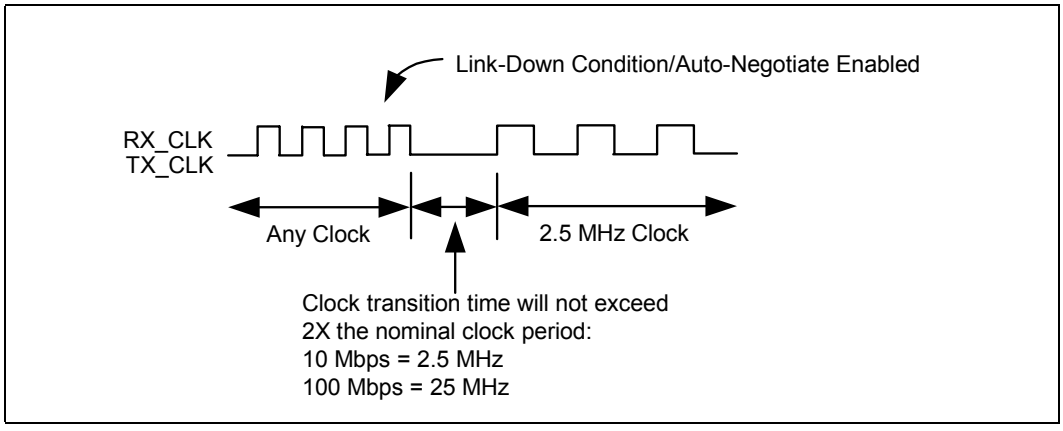



**Figure 12. Link Down Clock Transition**




## 3.6.7 Loopback

The LXT971A provides two loopback functions, operational and test (see Table 10). Loopback paths are shown in Figure 13.

### 3.6.7.1 Operational Loopback

Operational loopback is provided for 10 Mbps half-duplex links when Register bit 16.8 = 0. Data transmitted by the MAC (TXData) is looped back on the receive side of the MII (RXData). Operational loopback is not provided for 100 Mbps links, full-duplex links, or when 16.8 = 1.

### 3.6.7.2 Test Loopback

A test loopback function is provided for diagnostic testing of the LXT971A. During test loopback, twisted-pair and fiber interfaces are disabled. Data transmitted by the MAC is internally looped back by the LXT971A and returned to the MAC.

Test loopback is available for both 100BASE-TX and 10BASE-T operation, and is enabled by setting the following register bits:

- Register bit 0.14 = 1
- Register bit 0.8 = 1 (full-duplex)
- Register bit 0.12 = 0 (disable auto-negotiation).

Test loopback is also available for 100BASE-FX operation. Test loopback in this mode is enabled by setting Register bit 0.14 = 1 and tying the SD input to an LVPECL logic High value (2.4 V).

**Figure 13. Loopback Paths**

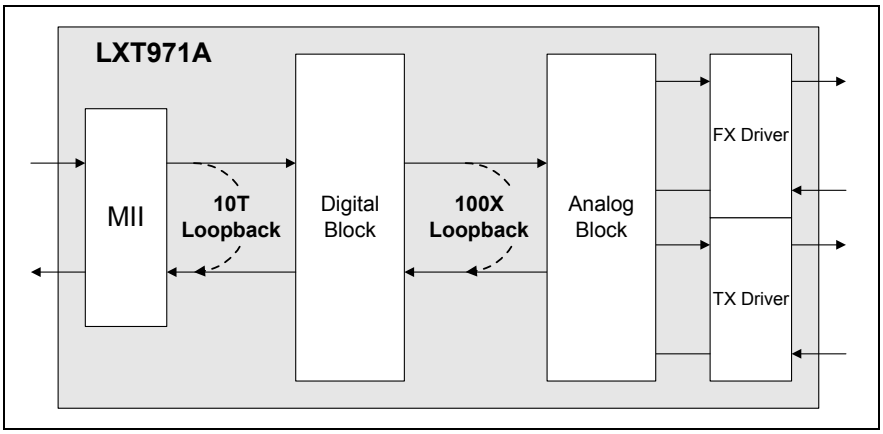


**Table 10. Carrier Sense, Loopback, and Collision Conditions**

| Speed | Duplex Condition | Carrier Sense | Test[1] Loopback | Operational Loopback | Collision |
|---|---|---|---|---|---|
| 100 Mbps | Full-Duplex | Receive Only | Yes | No | None |
| | Half-Duplex | Transmit or Receive | No | No | Transmit and Receive |
| 10 Mbps | Full-Duplex | Receive Only | Yes | No | None |
| | Half-Duplex, Register bit 16.8 = 0 | Transmit or Receive | Yes | Yes | Transmit and Receive |
| | Half-Duplex, Register bit 16.8 = 1 | Transmit or Receive | No | No | Transmit and Receive |

1. Test Loopback is enabled when 0.14 = 1

# 3.7 100 Mbps Operation

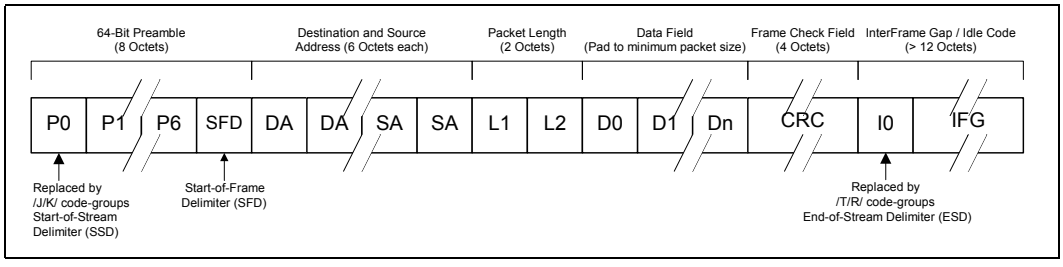
## 3.7.1 100BASE-X Network Operations

During 100BASE-X operation, the LXT971A transmits and receives 5-bit symbols across the network link. Figure 14 shows the structure of a standard frame packet. When the MAC is not actively transmitting data, the LXT971A sends out Idle symbols on the line.

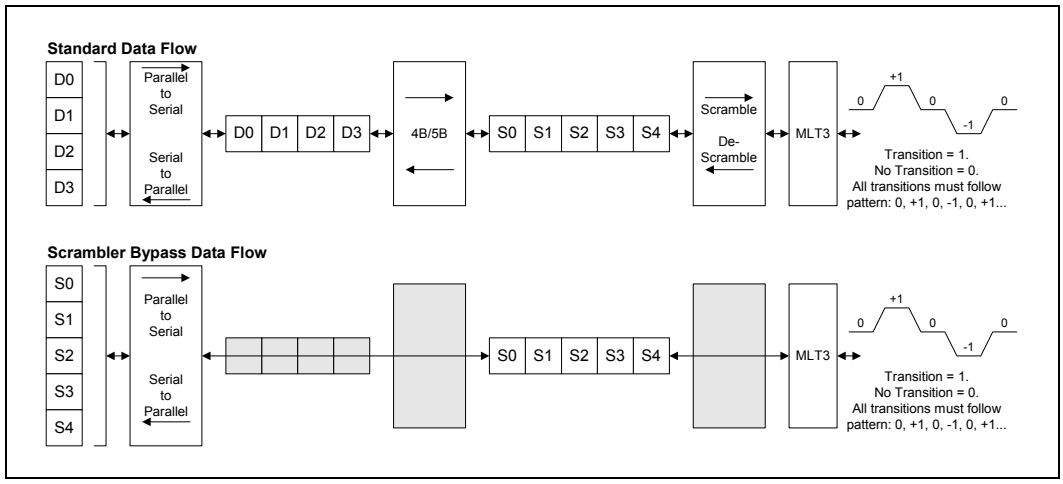
In 100BASE-TX mode, the LXT971A scrambles and transmits the data to the network using MLT-3 line code (Figure 15 on page 37). MLT-3 signals received from the network are de-scrambled, decoded, and sent across the MII to the MAC.

In 100BASE-FX mode, the LXT971A transmits and receives NRZI signals across the LVPECL interface. An external 100FX transceiver module is required to complete the fiber connection. To enable 100BASE-FX operation, auto-negotiation must be disabled and FX selected.

**Figure 14. 100BASE-X Frame Format**



### Figure 15. 100BASE-TX Data Path

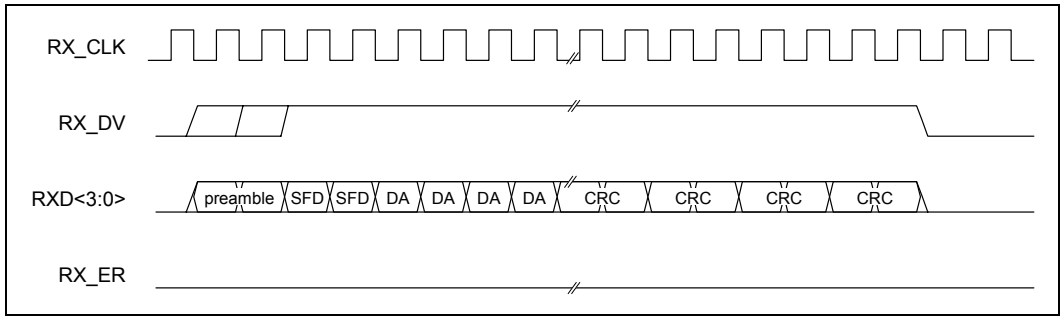



As shown in Figure 14 on page 36, the MAC starts each transmission with a preamble pattern. As soon as the LXT971A detects the start of preamble, it transmits a Start-of-Stream Delimiter (SSD, symbols J and K) to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the SFD, packet data, and CRC.

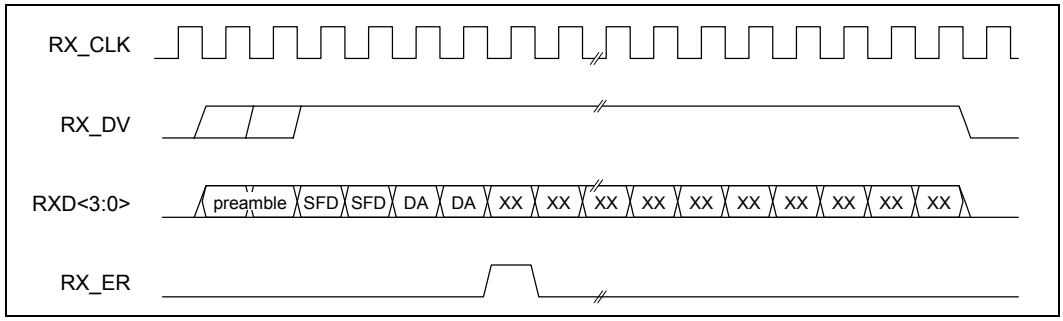
Once the packet ends, the LXT971A transmits the End-of- Stream Delimiter (ESD, symbols T and R) and then returns to transmitting Idle symbols. 4B/5B coding is shown in Table 11 on page 40.

Figure 16 shows normal reception with no errors. When the LXT971A receives invalid symbols from the line, it asserts RX_ER as shown in Figure 17.

### Figure 16. 100BASE-TX Reception with No Errors




### Figure 17. 100BASE-TX Reception with Invalid Symbol



### 3.7.2 Collision Indication

Figure 18 shows normal transmission. Upon detection of a collision, the COL output is asserted and remains asserted for the duration of the collision as shown in Figure 19.

**Figure 18. 100BASE-TX Transmission with No Errors**

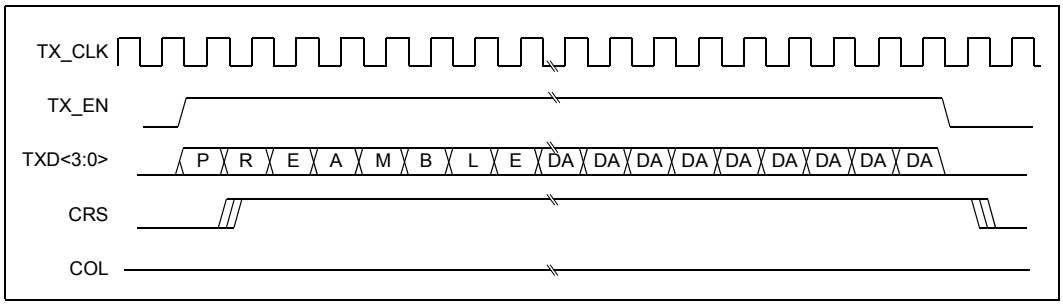
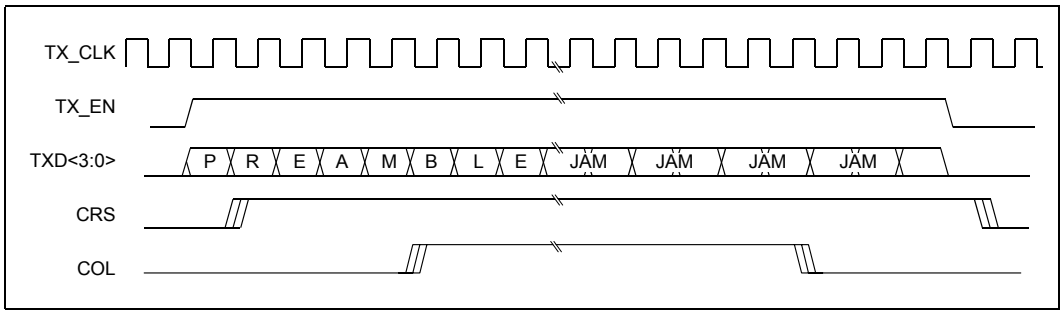



**Figure 19. 100BASE-TX Transmission with Collision**




### 3.7.3 100BASE-X Protocol Sublayer Operations

With respect to the 7-layer communications model, the LXT971A is a Physical Layer 1 (PHY) device. The LXT971A implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) sublayers of the reference model defined by the IEEE 802.3u standard. The following paragraphs discuss LXT971A operation from the reference model point of view.

#### 3.7.3.1 PCS Sublayer

The Physical Coding Sublayer (PCS) provides the MII interface, as well as the 4B/5B encoding/decoding function.

For 100BASE-TX and 100FX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TX_EN is de-asserted.

##### 3.7.3.1.1 Preamble Handling

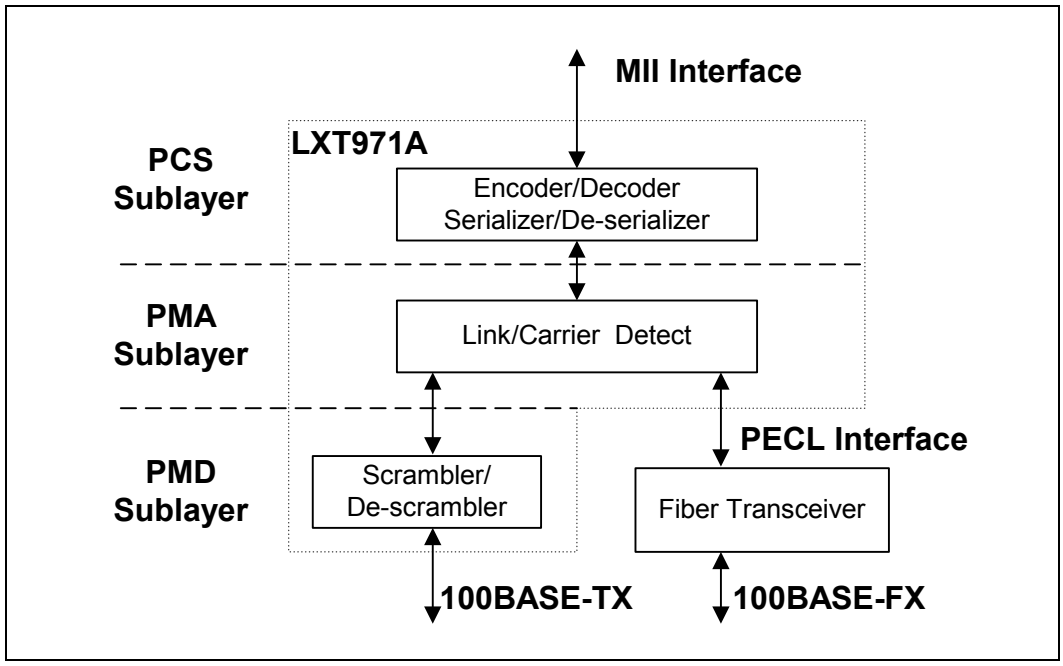
When the MAC asserts TX_EN, the PCS substitutes a /J/K symbol pair, also known as the Start-of-Stream Delimiter (SSD), for the first two nibbles received across the MII. The PCS layer continues to encode the remaining MII data, following the coding in Table 11, until TX_EN is de-asserted. It then returns to supplying IDLE symbols to the line driver.

In the receive direction, the PCS layer performs the opposite function, substituting two preamble nibbles for the SSD.

#### 3.7.3.1.2 Dribble Bits

The LXT971A handles dribbles bits in all modes. If one to four dribble bits are received, the nibble is passed across the MII, and padded with ones if necessary. If five to seven dribble bits are received, the second nibble is not sent to the MII bus.

**Figure 20. Protocol Sublayers**



## Table 11. 4B/5B Coding

| Code Type | 4B Code 3 2 1 0 | Name | 5B Code 4 3 2 1 0 | Interpretation |
|---|---|---|---|---|
| DATA | 0 0 0 0 | 0 | 1 1 1 1 0 | Data 0 |
| | 0 0 0 1 | 1 | 0 1 0 0 1 | Data 1 |
| | 0 0 1 0 | 2 | 1 0 1 0 0 | Data 2 |
| | 0 0 1 1 | 3 | 1 0 1 0 1 | Data 3 |
| | 0 1 0 0 | 4 | 0 1 0 1 0 | Data 4 |
| | 0 1 0 1 | 5 | 0 1 0 1 1 | Data 5 |
| | 0 1 1 0 | 6 | 0 1 1 1 0 | Data 6 |
| | 0 1 1 1 | 7 | 0 1 1 1 1 | Data 7 |
| | 1 0 0 0 | 8 | 1 0 0 1 0 | Data 8 |
| | 1 0 0 1 | 9 | 1 0 0 1 1 | Data 9 |
| | 1 0 1 0 | A | 1 0 1 1 0 | Data A |
| | 1 0 1 1 | B | 1 0 1 1 1 | Data B |
| | 1 1 0 0 | C | 1 1 0 1 0 | Data C |
| | 1 1 0 1 | D | 1 1 0 1 1 | Data D |
| | 1 1 1 0 | E | 1 1 1 0 0 | Data E |
| | 1 1 1 1 | F | 1 1 1 0 1 | Data F |
| IDLE | undefined | I [1] | 1 1 1 11 | Used as inter-stream fill code |
| CONTROL | 0 1 0 1 | J [2] | 1 1 0 0 0 | Start-of-Stream Delimiter (SSD), part 1 of 2 |
| | 0 1 0 1 | K [2] | 1 0 0 0 1 | Start-of-Stream Delimiter (SSD), part 2 of 2 |
| | undefined | T [3] | 0 1 1 0 1 | End-of-Stream Delimiter (ESD), part 1 of 2 |
| | undefined | R [3] | 0 0 1 1 1 | End-of-Stream Delimiter (ESD), part 2 of 2 |

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

**Table 11. 4B/5B Coding (Continued)**

| Code Type | 4B Code 3 2 1 0 | Name | 5B Code 4 3 2 1 0 | Interpretation |
|---|---|---|---|---|
| INVALID | undefined | H [4] | 0 0 1 0 0 | Transmit Error. Used to force signaling errors |
| | undefined | Invalid | 0 0 0 0 0 | Invalid |
| | undefined | Invalid | 0 0 0 0 1 | Invalid |
| | undefined | Invalid | 0 0 0 1 0 | Invalid |
| | undefined | Invalid | 0 0 0 1 1 | Invalid |
| | undefined | Invalid | 0 0 1 0 1 | Invalid |
| | undefined | Invalid | 0 0 1 1 0 | Invalid |
| | undefined | Invalid | 0 1 0 0 0 | Invalid |
| | undefined | Invalid | 0 1 1 0 0 | Invalid |
| | undefined | Invalid | 1 0 0 0 0 | Invalid |
| | undefined | Invalid | 1 1 0 0 1 | Invalid |

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

## 3.7.3.2 PMA Sublayer

### 3.7.3.2.1 Link

In 100 Mbps mode, the LXT971A establishes a link whenever the scrambler becomes locked and remains locked for approximately 50 ms. Whenever the scrambler loses lock (receiving less than 12 consecutive idle symbols during a 2 ms window), the link is taken down. This provides a very robust link, essentially filtering out any small noise hits that may otherwise disrupt the link. Furthermore, 100 Mbps idle patterns will not bring up a 10 Mbps link.

The LXT971A reports link failure via the MII status bits (Register bits 1.2 and 17.10) and interrupt functions. Link failure causes the LXT971A to re-negotiate if auto-negotiation is enabled.

### 3.7.3.2.2 Link Failure Override

The LXT971A normally transmits data packets only if it detects the link is up. Setting Register bit 16.14 = 1 overrides this function, allowing the LXT971A to transmit data packets even when the link is down. This feature is provided as a diagnostic tool. Note that auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT971A automatically transmits FLP bursts if the link is down.

### 3.7.3.2.3 Carrier Sense

For 100BASE-TX and 100FX links, a start-of-stream delimiter (SSD) or /J/K symbol pair causes assertion of carrier sense (CRS). An end-of-stream delimiter (ESD) or /T/R symbol pair causes de-assertion of CRS. The PMA layer also de-asserts CRS if IDLE symbols are received without /T/R; however, in this case RX_ER is asserted for one clock cycle when CRS is de-asserted.

Usage of CRS for Interframe Gap (IFG) timing is *not* recommended for the following reasons:

- De-assertion time for CRS is slightly longer than assertion time. This causes IFG intervals to appear somewhat shorter to the MAC than it actually is on the wire.
- CRS de-assertion is not aligned with TX_EN de-assertion on transmit loopbacks in half-duplex mode.

#### 3.7.3.2.4 Receive Data Valid

The LXT971A asserts RX_DV to indicate that the received data maps to valid symbols. However, RXD outputs zeros until the received data is decoded and available for transfer to the controller.

### 3.7.3.3 Twisted-Pair PMD Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides the signal scrambling and de-scrambling, line coding and decoding (MLT-3 for 100BASE-TX, Manchester for 10BASE-T), as well as receiving, polarity correction, and baseline wander correction functions.

**Scrambler/De-scrambler**

The purpose of the scrambler is to spread the signal power spectrum and further reduce EMI using an 11-bit, data-independent polynomial. The receiver automatically decodes the polynomial whenever IDLE symbols are received.

**Scrambler Seeding**

Once the transmit data (or Idle symbols) are properly encoded, they are scrambled to further reduce EMI and to spread the power spectrum using an 11-bit scrambler seed. Five seed bits are determined by the PHY address, and the remaining bits are hard coded in the design.

**Scrambler Bypass**

The scrambler/de-scrambler can be bypassed by setting Register bit 16.12 = 1. The scrambler is automatically bypassed when the fiber port is enabled. Scrambler bypass is provided for diagnostic and test support.

#### 3.7.3.3.1 Baseline Wander Correction

The LXT971A provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition “unbalanced”. This means that the average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander can cause receiver errors at long-line lengths (100 meters) in less robust designs. Exact characteristics of the wander are completely data dependent.

The LXT971A baseline wander correction characteristics allow the device to recover error-free data while receiving worst-case “killer” packets over all cable lengths.

#### 3.7.3.3.2 Polarity Correction

The 100BASE-TX de-scrambler automatically detects and corrects for the condition where the receive signal at TPFIP and TPFIN is inverted.

#### 3.7.3.3.3 Programmable Slew Rate Control

The LXT971A device supports a slew rate mechanism whereby one of four pre-selected slew rates can be used. This allows the designer to optimize the output waveform to match the characteristics of the magnetics. The slew rate is determined by the TxSLEW pins as shown in Table 4 on page 18.

### 3.7.3.4 Fiber PMD Sublayer

The LXT971A provides a Low Voltage PECL interface for connection to an external 3.3 V or 5.0 V fiber-optic transceiver. (The external transceiver provides the PMD function for fiber media.) The LXT971A uses an NRZI format for the fiber interface. The fiber interface operates at 100 Mbps and does not support 10FL applications.

## 3.8 10 Mbps Operation

The LXT971A operates as a standard 10BASE-T transceiver. The LXT971A supports all the standard 10 Mbps functions. During 10BASE-T operation, the LXT971A transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the LXT971A drives link pulses onto the line.

In 10BASE-T mode, the polynomial scrambler/de-scrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT971A and sent across the MII to the MAC.

The LXT971A does not support fiber connections at 10 Mbps.

### 3.8.1 10BASE-T Preamble Handling

The LXT971A offers two options for preamble handling, selected by Register bit 16.5. In 10BASE-T Mode when 16.5 = 0, the LXT971A strips the entire preamble off of received packets. CRS is asserted coincident with SFD. RX_DV is held Low for the duration of the preamble. When RX_DV is asserted, the very first two nibbles driven by the LXT971A are the SFD “5D” hex followed by the body of the packet.

In 10BASE-T mode with 16.5 = 1, the LXT971A passes the preamble through the MII and asserts RX_DV and CRS simultaneously. In 10BASE-T loopback, the LXT971A loops back whatever the MAC transmits to it, including the preamble.

### 3.8.2 10BASE-T Carrier Sense

For 10BASE-T links, CRS assertion is based on reception of valid preamble, and de-assertion on reception of an end-of-frame (EOF) marker. Register bit 16.7 allows CRS de-assertion to be synchronized with RX_DV de-assertion. Refer to Table 52 on page 81.

### 3.8.3 10BASE-T Dribble Bits

The LXT971A device handles dribbles bits in all modes. If one to four dribble bits are received, the nibble is passed across the MII, padded with ones if necessary. If five to seven dribble bits are received, the second nibble is not sent to the MII bus.

### 3.8.4 10BASE-T Link Integrity Test

In 10BASE-T mode, the LXT971A always transmits link pulses. When the Link Integrity Test function is enabled (the normal configuration), it monitors the connection for link pulses. Once link pulses are detected, data transmission is enabled and remains enabled as long as either the link pulses or data transmission continue. If the link pulses stop, the data transmission is disabled.

If the Link Integrity Test function is disabled, the LXT971A transmits to the connection regardless of detected link pulses. The Link Integrity Test function can be disabled by setting Register bit 16.14 = 1.

#### 3.8.4.1 Link Failure

Link failure occurs if the Link Integrity Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT971A returns to the auto-negotiation phase if auto-negotiation is enabled. If the Link Integrity Test function is disabled by setting Register bit 16.14 = 1 in the Configuration Register, the LXT971A transmits packets, regardless of link status.

### 3.8.5 10BASE-T SQE (Heartbeat)

By default, the Signal Quality Error (SQE) or heartbeat function is disabled on the LXT971A. To enable this function, set Register bit 16.9 = 1. When this function is enabled, the LXT971A asserts its COL output for 5-15 BT after each packet. See Figure 35 on page 67 for SQE timing parameters.

### 3.8.6 10BASE-T Jabber

If a transmission exceeds the jabber timer, the LXT971A disables the transmit and loopback functions. See Figure 34 on page 67 for jabber timing parameters.

The LXT971A automatically exits jabber mode after the unjabber time has expired. This function can be disabled by setting Register bit 16.10 = 1.

### 3.8.7 10BASE-T Polarity Correction

The LXT971A automatically detects and corrects for the condition where the receive signal (TPFIP/N) is inverted. Reversed polarity is detected if eight inverted link pulses, or four inverted end-of-frame (EOF) markers, are received consecutively. If link pulses or data are not received by the maximum receive time-out period (96-128 ms), the polarity state is reset to a non-inverted state.

## 3.9 Monitoring Operations

### 3.9.1 Monitoring Auto-Negotiation

Auto-negotiation can be monitored as follows:

- Register bit 17.7 is set to 1 once the auto-negotiation process is completed.
- Register bits 1.2 and 17.10 are set to 1 once the link is established.

- Register bits 17.14 and 17.9 can be used to determine the link operating conditions (speed and duplex).

#### 3.9.1.1 Monitoring Next Page Exchange

The LXT971A offers an Alternate Next Page mode to simplify the next page exchange process. Normally, Register bit 6.1 (Page Received) remains set until read. When Alternate Next Page mode is enabled Register bit 6.1 is automatically cleared whenever a new negotiation process takes place. This prevents the user from reading an old value in 6.1 and assuming that Registers 5 and 8 (Partner Ability) contain valid information. Additionally, the LXT971A uses Register bit 6.5 to indicate when the current received page is the base page. This information is useful for recognizing when next pages must be resent due to a new negotiation process starting. Register bits 6.1 and 6.5 are cleared when read.

### 3.9.2 LED Functions

The LXT971A incorporates three direct LED drivers. On power up all the drivers are asserted for approximately 1 second after reset de-asserts. Each LED driver can be programmed using the LED Configuration Register (refer to Table 56 on page 85) to indicate one of the following conditions:

- Operating Speed
- Transmit Activity
- Receive Activity
- Collision Condition
- Link Status
- Duplex Mode

The LED drivers can also be programmed to display various combined status conditions. For example, setting Register bits 20.15:12 = 1101 produces the following combination of Link and Activity indications:

- If Link is down LED is off.
- If Link is up LED is on.
- If Link is up and activity is detected, the LED blinks at the stretch interval selected by Register bits 20.3:2 and continues to blink as long as activity is present.

The LED driver pins also provide initial configuration settings. The LED pins are sensitive to polarity and automatically pull up or pull down to configure for either open drain or open collector circuits (10 mA Max current rating) as required by the hardware configuration. Refer to the discussion of "Hardware Configuration Settings" on page 30 for details.

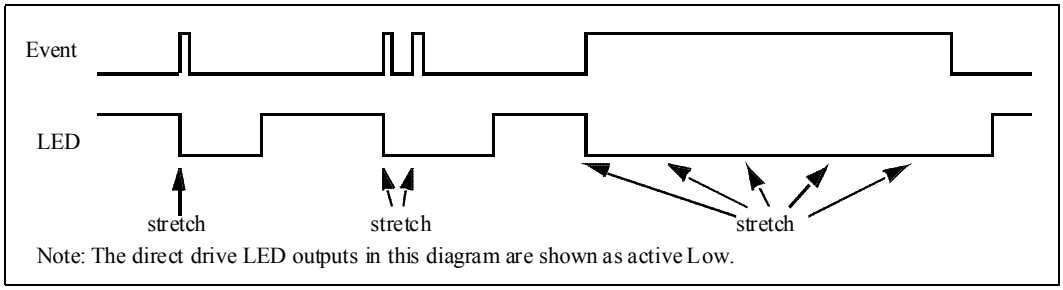
#### 3.9.2.1 LED Pulse Stretching

The LED Configuration Register also provides optional LED pulse stretching to 30, 60, or 100 ms. The pulse stretch time is further extended if the event occurs again during this pulse stretch period.

When an event such as receiving a packet occurs it is edge detected and it starts the stretch timer. The LED driver remains asserted until the stretch timer expires. If another event occurs before the stretch timer expires then the stretch timer is reset and the stretch time is extended.

When a long event (such as duplex status) occurs it is edge detected and it starts the stretch timer. When the stretch timer expires the edge detector is reset so that a long event causes another pulse to be generated from the edge detector which resets the stretch timer and causes the LED driver to remain asserted. Figure 21 shows how the stretch operation functions.

**Figure 21. LED Pulse Stretching**




## 3.10 Boundary Scan (JTAG1149.1) Functions

LXT971A includes a IEEE 1149.1 boundary scan test port for board level testing. All digital input, output, and input/output pins are accessible. The BSDL file is available by contacting your local sales office or by accessing the Intel website (www.intel.com).

### 3.10.1 Boundary Scan Interface

This interface consists of five pins (TMS, TDI, TDO, $\overline{\text{TRST}}$, and TCK). It includes a state machine, data register array, and instruction register. The TMS and TDI pins are internally pulled up. TCK is internally pulled down. TDO does not have an internal pull-up or pull-down.

### 3.10.2 State Machine

The TAP controller is a 16 state machine driven by the TCK and TMS pins. Upon reset the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS and TDI are high for five TCK periods.

### 3.10.3 Instruction Register

After the state machine resets, the IDCODE instruction is always invoked. The decode logic ensures the correct data flow to the Data registers according to the current instruction. Valid instructions are listed in Table 13.

### 3.10.4 Boundary Scan Register (BSR)

Each Boundary Scan Register (BSR) cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. There are four modes of operation as listed in Table 12.

### Table 12. BSR Mode of Operation

| Mode | Description |
|---|---|
| 1 | Capture |
| 2 | Shift |
| 3 | Update |
| 4 | System Function |

### Table 13. Supported JTAG Instructions

| Name | Code | Description | Mode | Data Register |
|---|---|---|---|---|
| EXTEST | 1111 1111 1110 1000 | External Test | Test | BSR |
| IDCODE | 1111 1111 1111 1110 | ID Code Inspection | Normal | ID REG |
| SAMPLE | 1111 1111 1111 1000 | Sample Boundary | Normal | BSR |
| HIGHZ | 1111 1111 1100 1111 | Force Float | Normal | Bypass |
| CLAMP | 1111 1111 1110 1111 | Control Boundary to 1/0 | Test | Bypass |
| BYPASS | 1111 1111 1111 1111 | Bypass Scan | Normal | Bypass |

### Table 14. Device ID Register

| 31:28 | 27:12 | 11:8 | 7:1 | 0 |
|---|---|---|---|---|
| Version[2] | Part ID (hex) | Jedec Continuation Characters | JEDEC ID[1] | Reserved |
| XXXX | 03CB | 0000 | 111 1110 | 1 |

1. The JEDEC IS is an 8-bit identifier. The MSB is for parity and is ignored. Intel's JEDEC ID is FE (1111 1110), which becomes 111 1110.
2. See the LXT971A/972A Specification Update (document number 249354) for the current version of the Jedec continuation characters.

# 4.0 Application Information

## 4.1 Magnetics Information

The LXT971A requires a 1:1 ratio for both the receive and transmit transformers. The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 15 for transformer requirements.

A cross-reference list of magnetic manufacturers and part numbers is available in Magnetic Manufacturers for Networking Product Applications (document number 248991) and is found on the Intel web site (www.Intel.com). Before committing to a specific component, contact the manufacturer for current product specifications and validate the magnetics for the specific application.

**Table 15. Magnetics Requirements**

| Parameter | Min | Nom | Max | Units | Test Condition |
|---|---|---|---|---|---|
| Rx turns ratio | – | 1 : 1 | – | – | – |
| Tx turns ratio | – | 1 : 1 | – | – | – |
| Insertion loss | 0.0 | 0.6 | 1.1 | dB | – |
| Primary inductance | 350 | – | – | µH | – |
| Transformer isolation | – | 1.5 | – | kV | – |
| Differential to common mode rejection | 40 | – | – | dB | .1 to 60 MHz |
| | 35 | – | – | dB | 60 to 100 MHz |
| Return Loss | -16 | – | – | dB | 30 MHz |
| | -10 | – | – | dB | 80 MHz |

## 4.2 Typical Twisted-Pair Interface

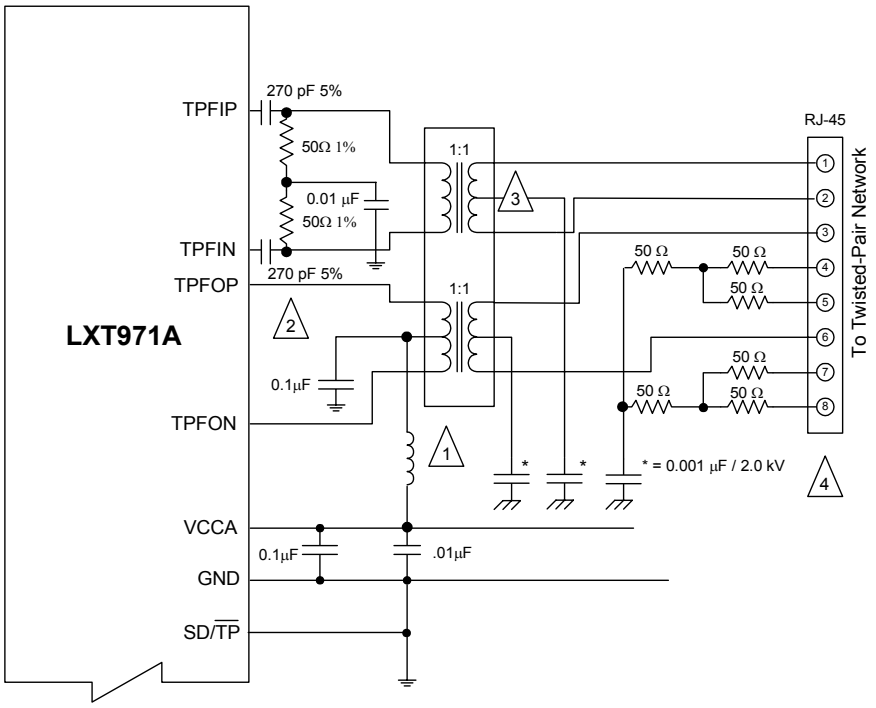
Table 16 provides a comparison of the RJ-45 connections for NIC and Switch applications in a typical twisted-pair interface setting.

**Table 16. I/O Pin Comparison of NIC and Switch RJ-45 Setups**

| Symbol | RJ-45 | |
|---|---|---|
| | Switch | NIC |
| TPIP | 1 | 3 |
| TPIN | 2 | 6 |
| TPOP | 3 | 1 |
| TPON | 6 | 2 |

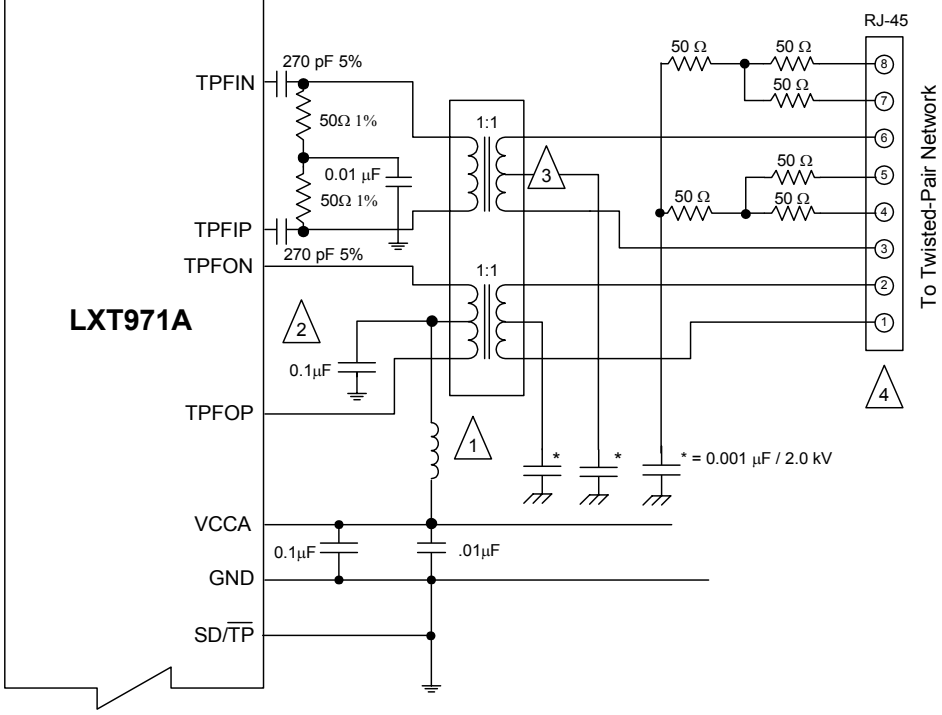
Figure 22 on page 49 shows a typical twisted-pair interface with the RJ-45 connections crossed over for a Switch configuration. Figure 23 on page 50 provides a typical twisted-pair interface with the RJ-45 connections configured for a NIC application.

## Figure 22. Typical Twisted-Pair Interface - Switch



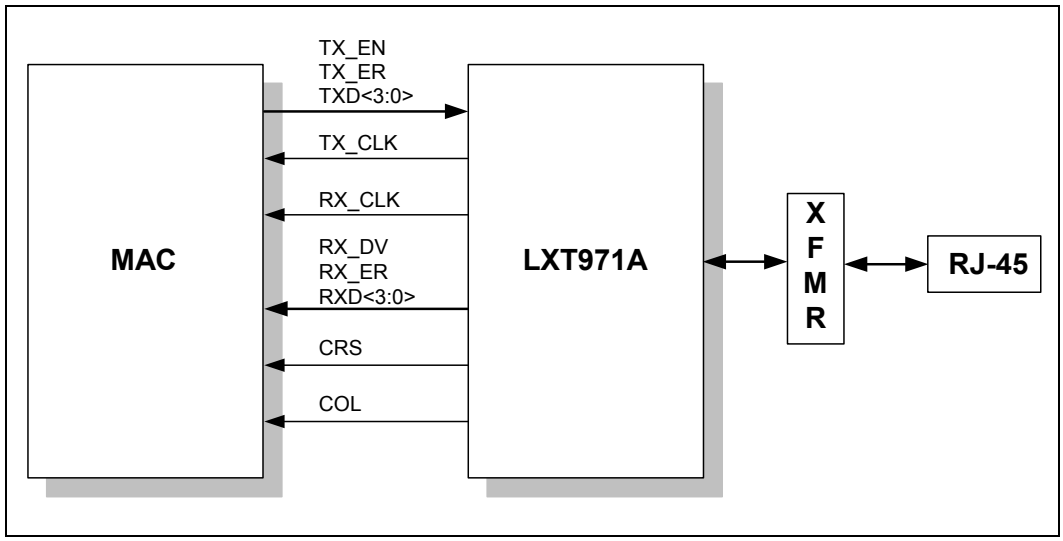

1. Center-tap current may be supplied from 3.3 V VCCA as shown. Additional power savings may be realized by supplying the center-tap from a 2.5 V current source. A separate ferrite bead (rated at 50 mA) should be used to supply center-tap current.
2. The 100 Ω transmit load termination resistor typically required is integrated in the LXT971A.
3. Magnetics without a receive pair center-tap do not require a 2 kV termination.
4. RJ-45 connections shown are for a standard switch application. For a standard NIC RJ-45 setup, see Figure 23 on page 50.

## Figure 23. Typical Twisted-Pair Interface - NIC




1. Center-tap current may be supplied from 3.3 V VCCA as shown. Additional power savings may be realized by supplying the center-tap from a 2.5 V current source. A separate ferrite bead (rated at 50 mA) should be used to supply center-tap current.
2. The 100 Ω transmit load termination resistor typically required is integrated in the LXT971A.
3. Magnetics without a receive pair center-tap do not require a 2 kV termination.
4. RJ-45 connections shown for standard NIC. TX/RX crossover may be required for repeater and switch applications.

**Figure 24. Typical MII Interface**



## 4.3 The Fiber Interface

The fiber interface consists of an LVPECL transmit and receive pair to an external fiber-optic transceiver. Both 3.3 V fiber-optic transceivers and 5 V fiber-optic transceivers can be used with the LXT971A.

The following should occur in 3.3 V fiber transceiver applications as shown in Figure 25:

- The transmit pair should be DC-coupled with the 50 Ω/16 Ω pull-up combination
- The receive pair should be DC-coupled with an emitter current path for the fiber transceiver
- The signal detect pin should be DC-coupled with an emitter current path for the fiber transceiver

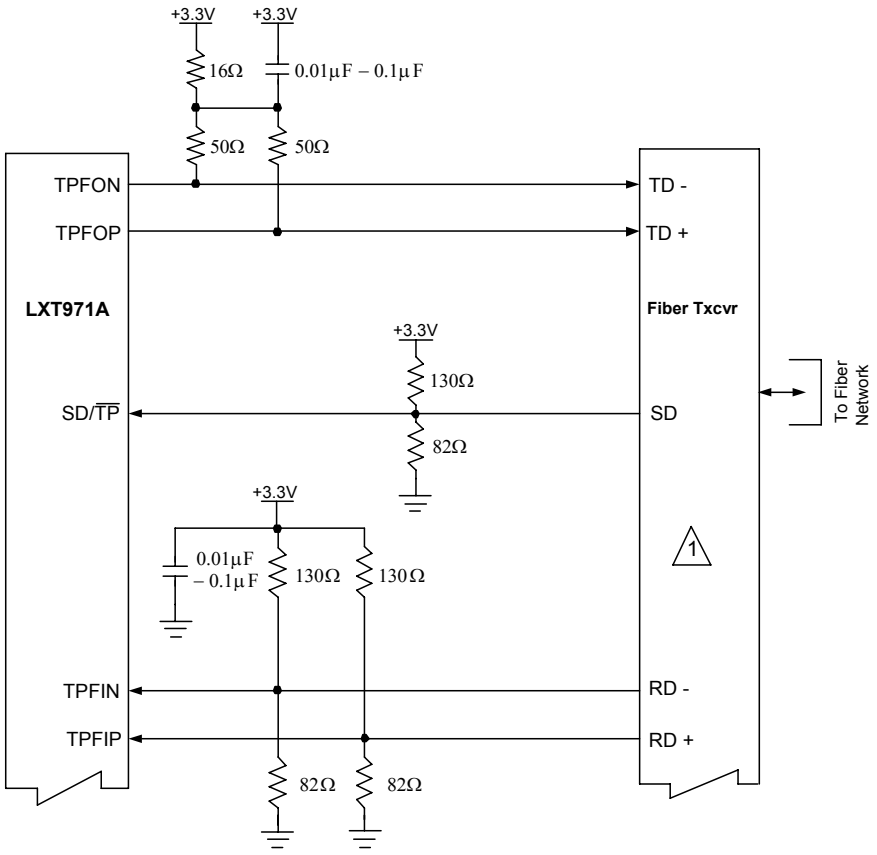
Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 25 shows a typical example of an LXT971A-to-3.3 V fiber transceiver interface.

The following occurs in 5 V fiber transceiver applications as shown in Figure 26:

- The transmit pair should be AC-coupled and re-biased to 5 V PECL input levels
- The receive pair should be AC-coupled with an emitter current path for the fiber transceiver and re-biased to 3.3 V LVPECL input levels.

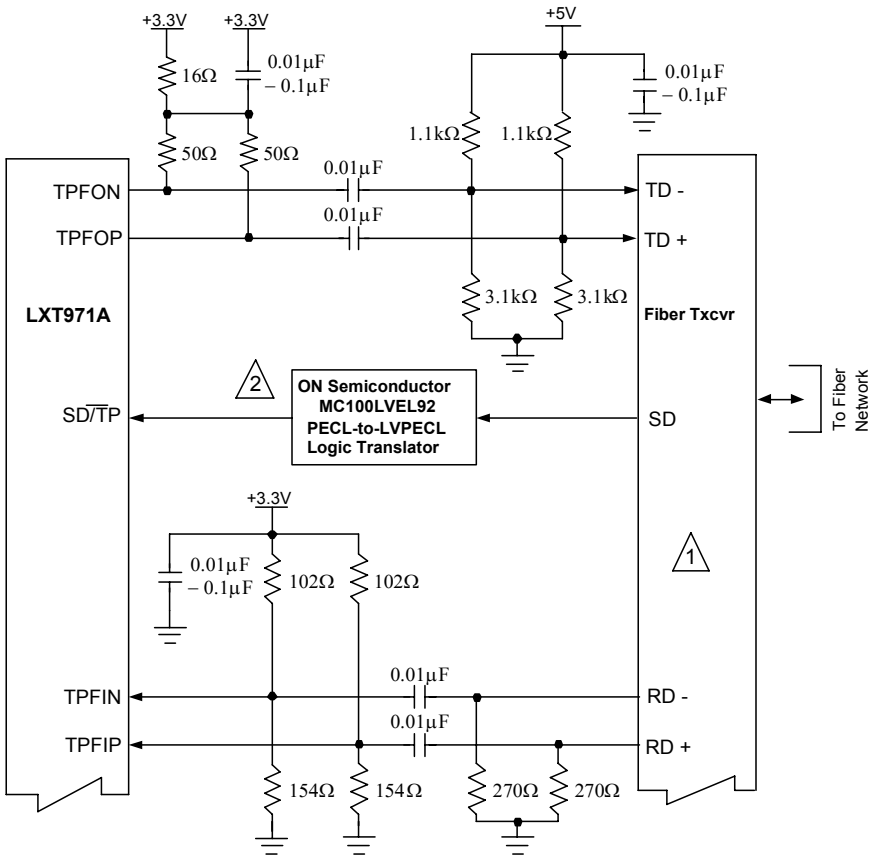
The signal detect pin on a 5 V fiber transceiver interface should use the logic translator circuitry as shown in Figure 27. Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 26 shows a typical example of an LXT971A-to-5 V fiber transceiver interface, while Figure 27 shows the interface circuitry for the logic translator.

## Figure 25. Typical LXT971A-to-3.3 V Fiber Transceiver Interface Circuitry



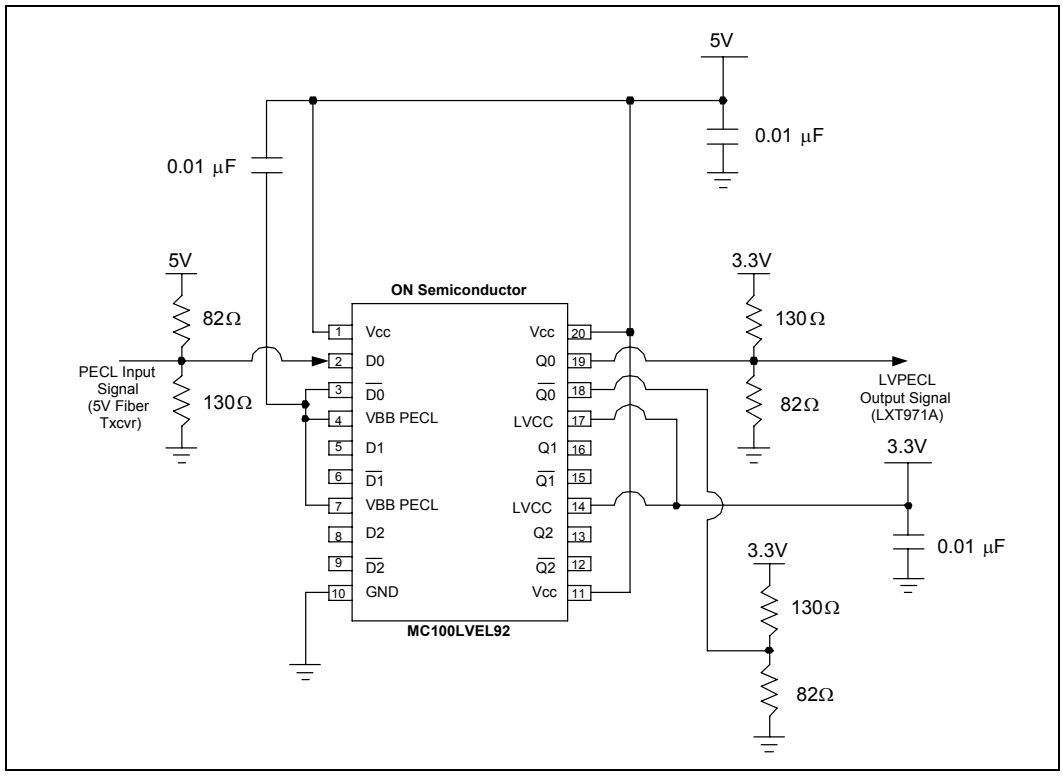

1. Refer to the transceiver manufacturer's recommendations for termination circuitry.

## Figure 26. Typical LXT971A-to-5 V Fiber Transceiver Interface Circuitry




1. Refer to the transceiver manufacturer's recommendations for termination circuitry.
2. See Figure 27 for recommended logic translator interface circuitry.

## Figure 27. ON Semiconductor Triple PECL-to-LVPECL Translator



# 5.0 Test Specifications

*Note:* Table 17 through Table 40 and Figure 28 through Figure 41 represent the performance specifications of the LXT971A. These specifications are guaranteed by test except where noted "by design." Minimum and maximum values listed in Table 19 through Table 40 apply over the recommended operating conditions specified in Table 18.

## 5.1 Electrical Parameters

### Table 17. Absolute Maximum Ratings

| Parameter | | Sym | Min | Max | Units |
|---|---|---|---|---|---|
| Supply voltage | | VCC | -0.3 | 4.0 | V |
| Operating temperature | LXT971A_C (Commercial) | TOPA | -15 | +85 | ºC |
| | LXT971A_E (Extended) | TOPA | -55 | +100 | ºC |
| Storage temperature | | TST | -65 | +150 | ºC |

***Caution:*** Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

### Table 18. Operating Conditions

| Parameter | | Sym | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| Recommended operating temperature | LXT971A_C (Commercial) | TOPA | 0 | – | 70 | ºC |
| | LXT971A_E (Extended) | TOPA | -40 | – | 85 | ºC |
| Recommended supply voltage[2] | Analog & Digital | Vcca, Vccd | 3.14 | 3.3 | 3.45 | V |
| | I/O | Vccio | 2.35 | – | 3.45 | V |
| VCC current | 100BASE-TX | ICC | – | 92 | 110 | mA |
| | 10BASE-T | ICC | – | 66 | 82 | mA |
| | 100BASE-FX | ICC | – | 72 | 95 | mA |
| | Sleep Mode | ICC | – | 40 | 45 | mA |
| | Hard Power Down | ICC | – | – | 1 | mA |
| | Soft Power Down | Icc | – | 51 | – | mA |
| | Auto-Negotiation | ICC | – | 90 | 110 | mA |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.

## Table 19. Digital I/O Characteristics[2]

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input Low voltage | $V_{IL}$ | – | – | 0.8 | V | – |
| Input High voltage | $V_{IH}$ | 2.0 | – | – | V | – |
| Input current | $I_I$ | -10 | – | 10 | µA | 0.0 < $V_I$ < $V_{CC}$ |
| Output Low voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = 4 mA |
| Output High voltage | $V_{OH}$ | 2.4 | – | – | V | $I_{OH}$ = -4 mA |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Applies to all pins except MII, LED, XI/XO, and SD/$\overline{TP}$ pins. Refer to Table 20 for MII I/O Characteristics, Table 21 for XI/XO and Table 22 for LED Characteristics.

## Table 20. Digital I/O Characteristics - MII Pins

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input Low voltage | $V_{IL}$ | – | – | 0.8 | V | – |
| Input High voltage | $V_{IH}$ | 2.0 | – | – | V | – |
| Input current | $I_I$ | -10 | – | 10 | µA | 0.0 < $V_I$ < VCCIO |
| Output Low voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = 4 mA |
| Output High voltage | $V_{OH}$ | 2.2 | – | – | V | $I_{OH}$ = -4 mA, VCCIO = 3.3V |
| | $V_{OH}$ | 2.0 | – | – | V | $I_{OH}$ = -4 mA, VCCIO = 2.5V |
| Driver output resistance (Line driver output enabled) | $R_O$[2] | – | 100 | – | W | VCCIO = 2.5V |
| | $R_O$[2] | – | 100 | – | W | VCCIO = 3.3V |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

## Table 21. I/O Characteristics - REFCLK/XI and XO Pins

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | – | – | 0.8 | V | – |
| Input High Voltage | $V_{IH}$ | 2.0 | – | – | V | – |
| Input Clock Frequency Tolerance[2] | $\Delta f$ | – | – | ±100 | ppm | – |
| Input Clock Duty Cycle[2] | Tdc | 35 | – | 65 | % | – |
| Input Capacitance | $C_{IN}$ | – | 3.0 | – | pF | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.

### Table 22. I/O Characteristics - LED/CFG Pins

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | VIL | – | – | 0.8 | V | – |
| Input High Voltage | VIH | 2.0 | – | – | V | – |
| Input Current | II | -10 | – | 10 | µA | 0 < VI < VCCIO |
| Output Low Voltage | VOL | – | – | 0.4 | V | IOL = 10 mA |
| Output High Voltage | VOH | 2.0 | – | – | V | IOH = -10 mA |

### Table 23. I/O Characteristics – SD/$\overline{TP}$ Pin

| Parameter | Sym | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| **Reset and Power-Up States – FX/TP Mode Configuration** | | | | | | |
| Fiber Mode (Register bit 16.0 = 1) | $V_{FX}$ | 600 | 1600-2400 | – | mV | – |
| Twisted-Pair Mode (Register bit 16.0 = 0) | $V_{TP}$ | – | GND | 500 | mV | – |
| **100BASE-FX Mode Normal Operation – SD Input from Fiber Transceiver** | | | | | | |
| Input Low Voltage | $V_{IL}$ | 1.49 | 1.6 | 1.83 | V | VCCD = 3.3 V |
| Input High Voltage | $V_{IH}$ | 2.14 | 2.4 | 2.42 | V | VCCD = 3.3 V |

1. Typical values are for design aid only; not guaranteed and not subject to production testing.

### Table 24. 100BASE-TX Transceiver Characteristics

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Peak differential output voltage | VP | 0.95 | – | 1.05 | V | Note 2 |
| Signal amplitude symmetry | Vss | 98 | – | 102 | % | Note 2 |
| Signal rise/fall time | TRF | 3.0 | – | 5.0 | ns | Note 2 |
| Rise/fall time symmetry | TRFS | – | – | 0.5 | ns | Note 2 |
| Duty cycle distortion | DCD | 35 | 50 | 65 | % | Offset from 16 ns pulse width at 50% of pulse peak |
| Overshoot/Undershoot | VOS | – | – | 5 | % | – |
| Jitter (measured differentially) | – | – | – | 1.4 | ns | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω(+/-1%) resistor.

## Table 25. 100BASE-FX Transceiver Characteristics

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Peak differential output voltage (single ended) | VOP | 0.6 | – | 1.5 | V | – |
| Signal rise/fall time | TRF | – | – | 1.9 | ns | 10 <–> 90%<br>2.0 pF load |
| Jitter (measured differentially) | – | – | – | 1.3 | ns | – |
| **Receiver** | | | | | | |
| Peak differential input voltage | VIP | 0.55 | – | 1.5 | V | – |
| Common mode input range | VCMIR | – | – | VCC - 0.7 | V | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

## Table 26. 10BASE-T Transceiver Characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Peak differential output voltage | VOP | 2.2 | 2.5 | 2.8 | V | With transformer, line replaced by 100 Ω resistor |
| Transition timing jitter added by the MAU and PLS sections | – | 0 | 2 | 11 | ns | After line model specified by IEEE 802.3 for 10BASE-T MAU |
| **Receiver** | | | | | | |
| Receive Input Impedance | ZIN | – | – | 22 | kΩ | – |
| Differential Squelch Threshold | VDS | 300 | 420 | 585 | mV | – |

## Table 27. 10BASE-T Link Integrity Timing Characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Time Link Loss Receive | TLL | 50 | – | 150 | ms | – |
| Link Pulse | TLP | 2 | – | 7 | Link Pulses | – |
| Link Min Receive Timer | TLR MIN | 2 | – | 7 | ms | – |
| Link Max Receive Timer | TLR MAX | 50 | – | 150 | ms | – |
| Link Transmit Period | TIt | 8 | – | 24 | ms | – |
| Link Pulse Width | Tlpw | 60 | – | 150 | ns | – |

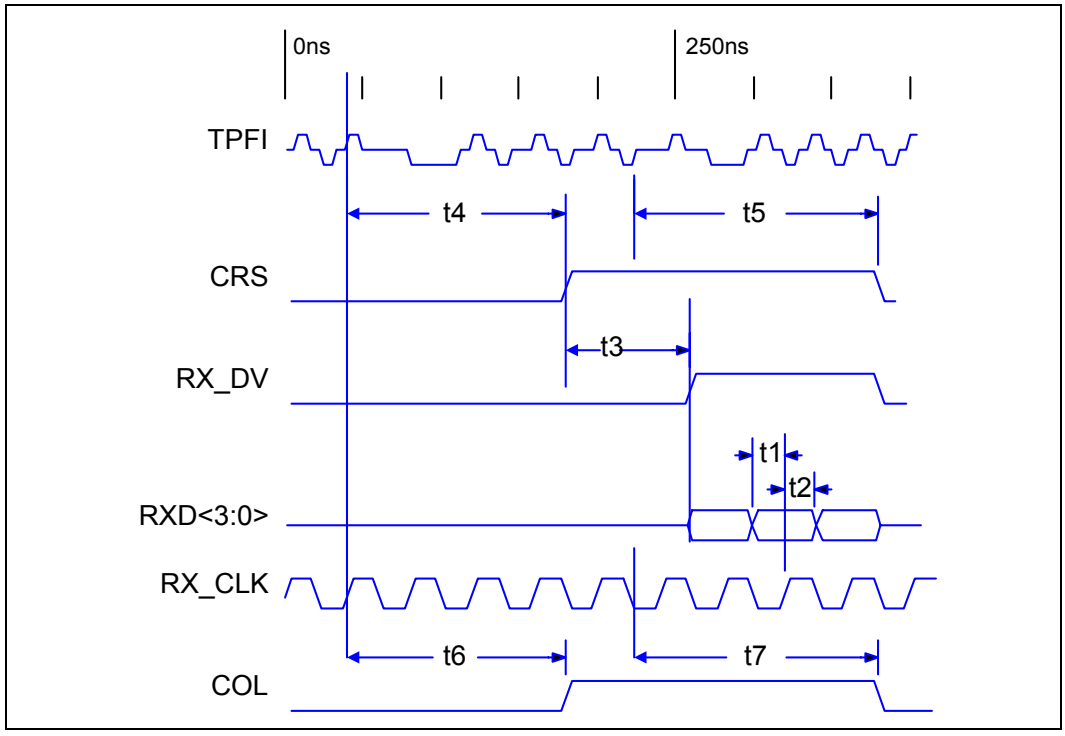
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

### Table 28. LXT971A Thermal Characteristics

| Parameter | LXT971ALC | LXT971ALE | LXT971ABE |
|---|---|---|---|
| Package | 1 0x 10 x1.4 64 LD LQFP | 10 x 10 x 1.4 64 LQFP | 7 x 7 x .96 64 BGA-CSP |
| Theta-JA | 58 C/W | 56 C/W | 42 C/W |
| Theta-JC | 27 C/W | 25 C/W | 20 C/W |
| Psi - JT | 3.4 C/W | 3.0 C/W | – |

## 5.2 Timing Diagrams

### Figure 28. 100BASE-TX Receive Timing - 4B Mode

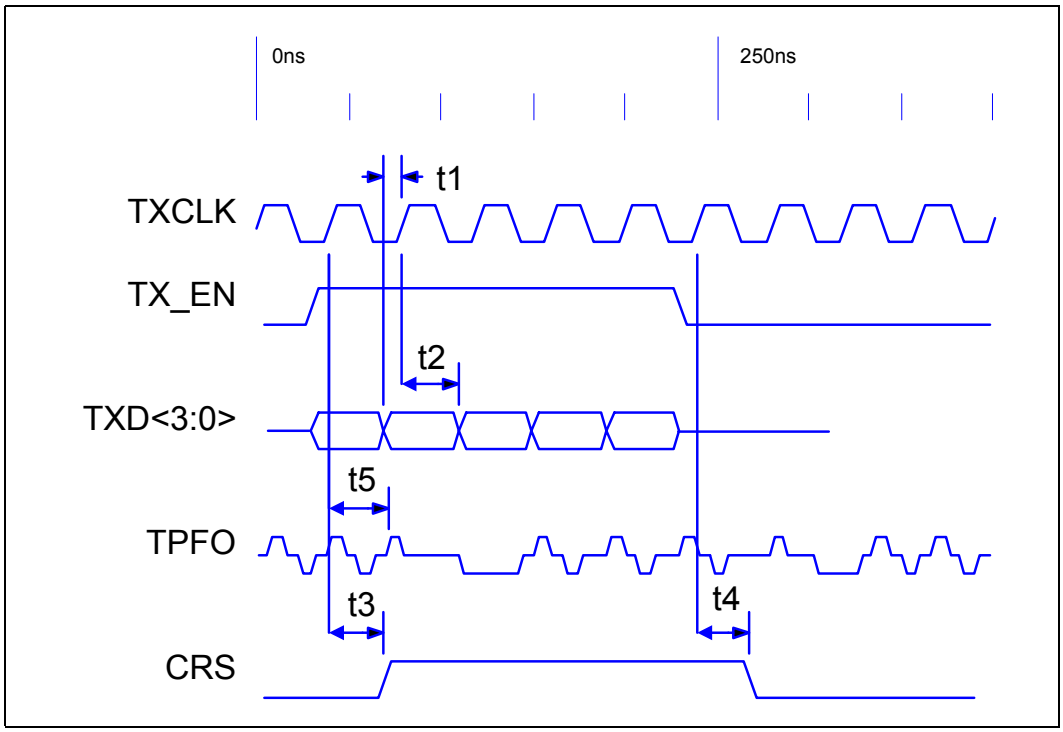



### Table 29. 100BASE-TX Receive Timing Parameters - 4B Mode

| Parameter | Sym | Min | Typ[1] | Max | Units[2] | Test Conditions |
|---|---|---|---|---|---|---|
| RXD<3:0>, RX_DV, RX_ER setup to RX_CLK High | t1 | 10 | – | – | ns | – |
| RXD<3:0>, RX_DV, RX_ER hold from RX_CLK High | t2 | 10 | – | – | ns | – |
| CRS asserted to RXD<3:0>, RX_DV | t3 | 3 | – | 5 | BT | – |
| Receive start of “J” to CRS asserted | t4 | 12 | – | 16 | BT | – |
| Receive start of “T” to CRS de-asserted | t5 | 10 | – | 17 | BT | – |
| Receive start of “J” to COL asserted | t6 | 16 | – | 22 | BT | – |
| Receive start of “T” to COL de-asserted | t7 | 17 | – | 20 | BT | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. BT is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = $10^{-8}$ s or 10 ns.

### Figure 29. 100BASE-TX Transmit Timing - 4B Mode

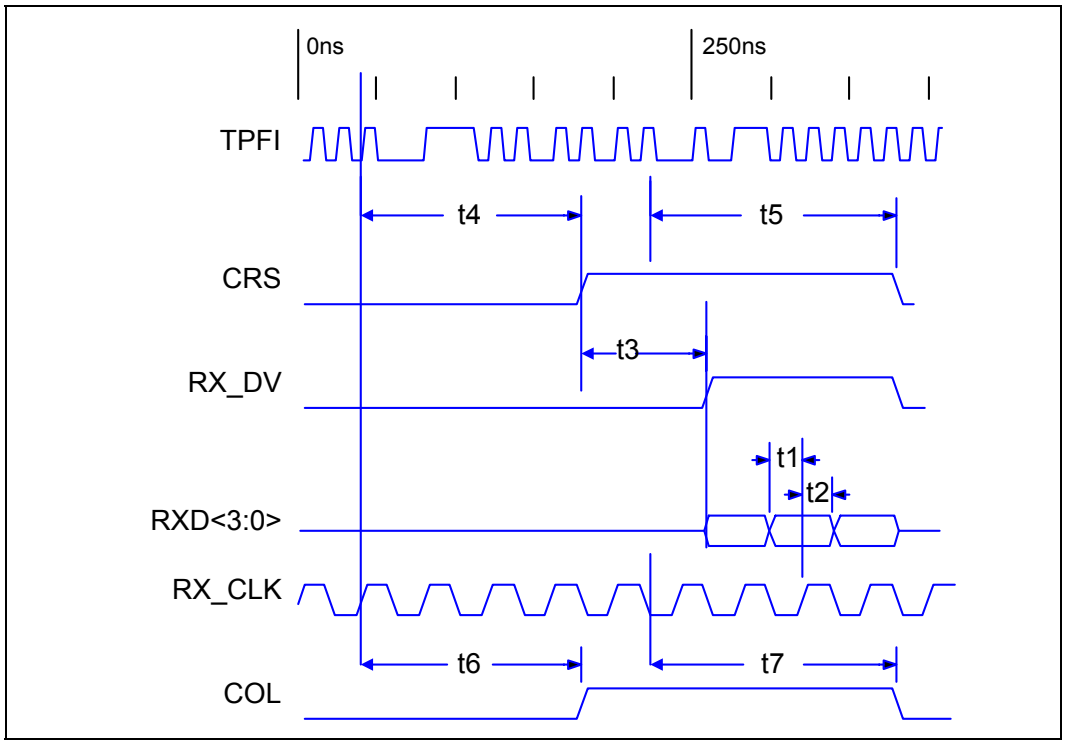



### Table 30. 100BASE-TX Transmit Timing Parameters - 4B Mode

| Parameter | Symbol | Min | Typ[1] | Max | Units[2] | Test Conditions |
|---|---|---|---|---|---|---|
| TXD<3:0>, TX_EN, TX_ER setup to TX_CLK High | t1 | 12 | – | – | ns | – |
| TXD<3:0>, TX_EN, TX_ER hold from TX_CLK High | t2 | 0 | – | – | ns | – |
| TX_EN sampled to CRS asserted | t3 | 20 | – | 24 | BT | – |
| TX_EN sampled to CRS de-asserted | t4 | 24 | – | 28 | BT | – |
| TX_EN sampled to TPFO out (Tx latency) | t5 | 5.3 | – | 5.7 | BT | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. BT is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = $10^{-8}$ s or 10 ns.

### Figure 30. 100BASE-FX Receive Timing

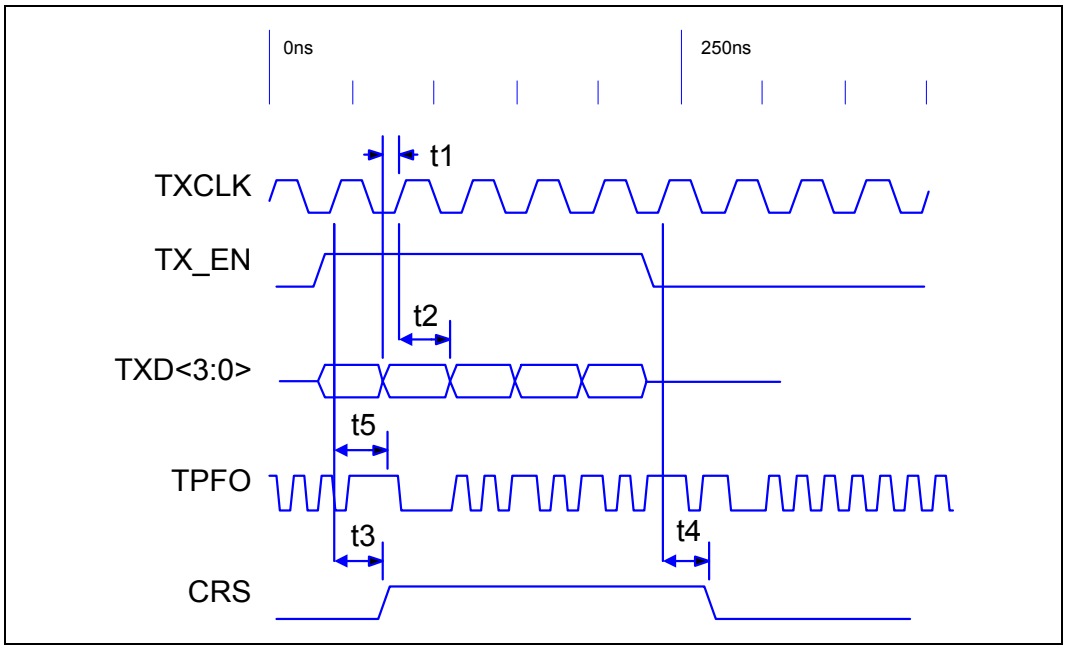



### Table 31. 100BASE-FX Receive Timing Parameters

| Parameter | Sym | Min | Typ[1] | Max | Units[2] | Test Conditions |
|---|---|---|---|---|---|---|
| RXD<3:0>, RX_DV, RX_ER setup to RX_CLK High | t1 | 10 | – | – | ns | – |
| RXD<3:0>, RX_DV, RX_ER hold from RX_CLK High | t2 | 10 | – | – | ns | – |
| CRS asserted to RXD<3:0>, RX_DV | t3 | 3 | – | 5 | BT | – |
| Receive start of “J” to CRS asserted | t4 | 12 | – | 16 | BT | – |
| Receive start of “T” to CRS de-asserted | t5 | 16 | – | 22 | BT | – |
| Receive start of “J” to COL asserted | t6 | 10 | – | 15 | BT | – |
| Receive start of “T” to COL de-asserted | t7 | 14 | – | 18 | BT | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. BT is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = $10^{-8}$ s or 10 ns.

### Figure 31. 100BASE-FX Transmit Timing

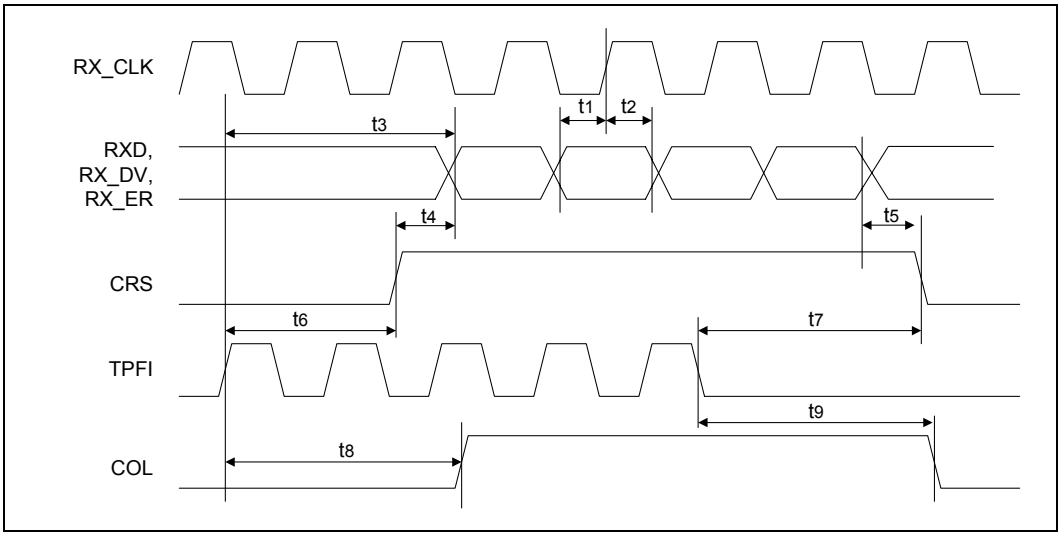



### Table 32. 100BASE-FX Transmit Timing Parameters

| Parameter | Symbol | Min | Typ[1] | Max | Units[2] | Test Conditions |
|---|---|---|---|---|---|---|
| TXD<3:0>, TX_EN, TX_ER setup to TX_CLK High | t1 | 12 | – | – | ns | – |
| TXD<3:0>, TX_EN, TX_ER hold from TX_CLK High | t2 | 0 | – | – | ns | – |
| TX_EN sampled to CRS asserted | t3 | 17 | – | 20 | BT | – |
| TX_EN sampled to CRS de-asserted | t4 | 22 | – | 24 | BT | – |
| TX_EN sampled to TPFO out (Tx latency) | t5 | 5 | – | 5.3 | BT | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. BT is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 100BASE-T bit time = $10^{-8}$ s or 10 ns.

## Figure 32. 10BASE-T Receive Timing

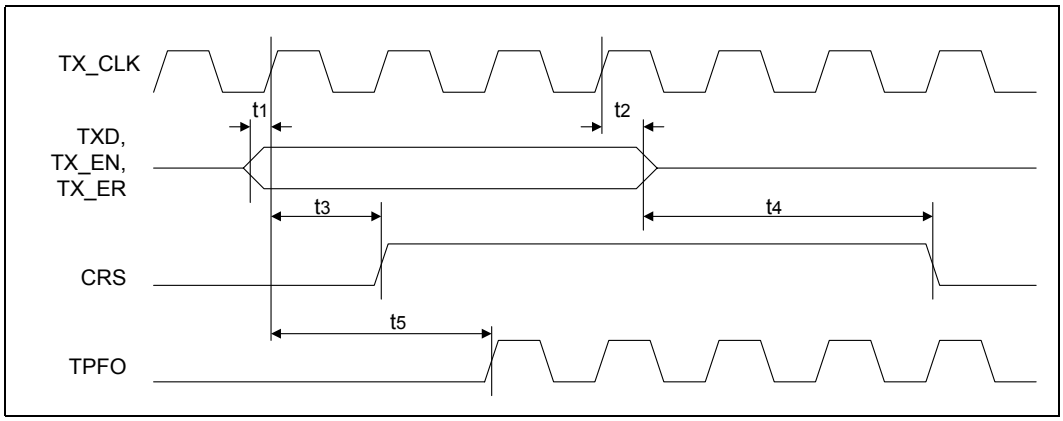



## Table 33. 10BASE-T Receive Timing Parameters

| Parameter | Sym | Min | Typ[1] | Max | Units[2] | Test Conditions |
|---|---|---|---|---|---|---|
| RXD, RX_DV, RX_ER Setup to RX_CLK High | t1 | 10 | – | – | ns | – |
| RXD, RX_DV, RX_ER Hold from RX_CLK High | t2 | 10 | – | – | ns | – |
| TPFIP/N in to RXD out (Rx latency) | t3 | 4.2 | – | 6.6 | BT | – |
| CRS asserted to RXD, RX_DV, RX_ER asserted | t4 | 5 | – | 32 | BT | – |
| RXD, RX_DV, RX_ER de-asserted to CRS de-asserted | t5 | 0.3 | – | 0.5 | BT | – |
| TPFI in to CRS asserted | t6 | 2 | – | 28 | BT | – |
| TPFI quiet to CRS de-asserted | t7 | 6 | – | 10 | BT | – |
| TPFI in to COL asserted | t8 | 1 | – | 31 | BT | – |
| TPFI quiet to COL de-asserted | t9 | 5 | – | 10 | BT | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. BT is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 10BASE-T bit time = $10^{-7}$ s or 100 ns.

### Figure 33. 10BASE-T Transmit Timing

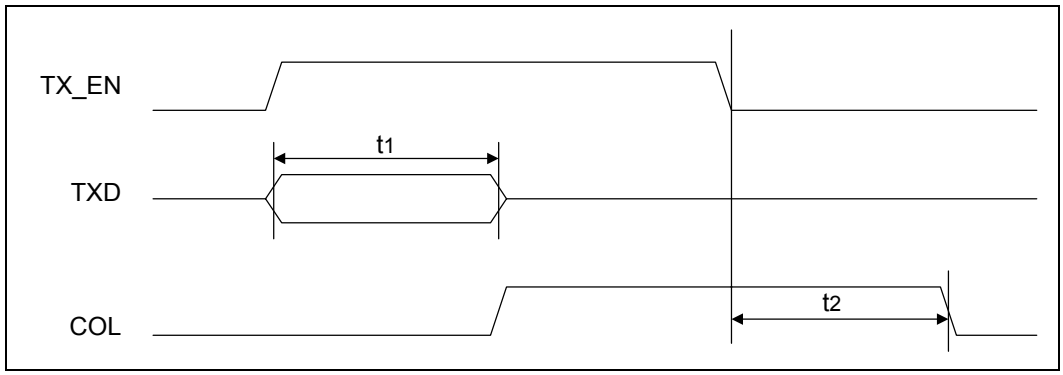



### Table 34. 10BASE-T Transmit Timing Parameters

| Parameter | Symbol | Min | Typ[1] | Max | Units[2] | Test Conditions |
|---|---|---|---|---|---|---|
| TXD, TX_EN, TX_ER setup to TX_CLK High | t1 | 10 | – | – | ns | – |
| TXD, TX_EN, TX_ER hold from TX_CLK High | t2 | 0 | – | – | ns | – |
| TX_EN sampled to CRS asserted | t3 | – | 2 | – | BT | – |
| TX_EN sampled to CRS de-asserted | t4 | – | 1 | – | BT | – |
| TX_EN sampled to TPFO out (Tx latency) | t5 | – | 72.5 | – | BT | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. BT is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate. 10BASE-T bit time = $10^{-7}$ s or 100 ns.

### Figure 34. 10BASE-T Jabber and Unjabber Timing

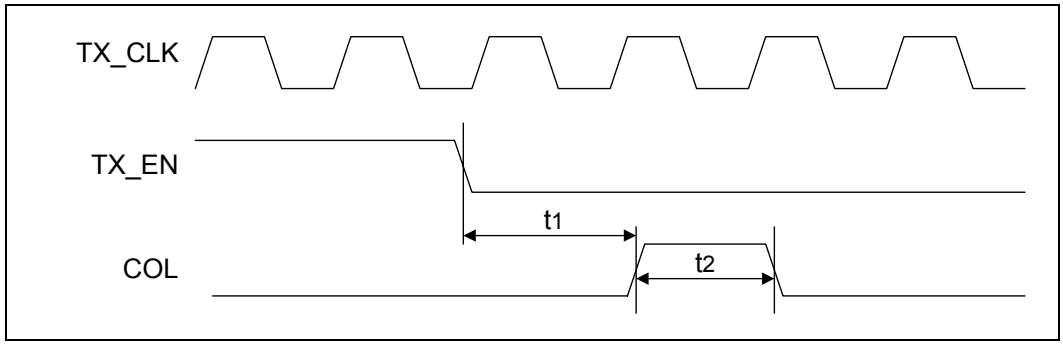



### Table 35. 10BASE-T Jabber and Unjabber Timing Parameters

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Maximum transmit time | t1 | 20 | – | 150 | ms | – |
| Unjab time | t2 | 250 | – | 750 | ms | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

### Figure 35. 10BASE-T SQE (Heartbeat) Timing

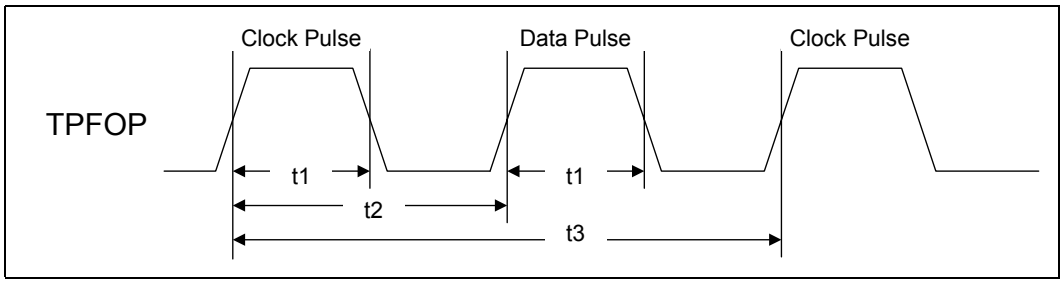



### Table 36. 10BASE-T SQE Timing Parameters

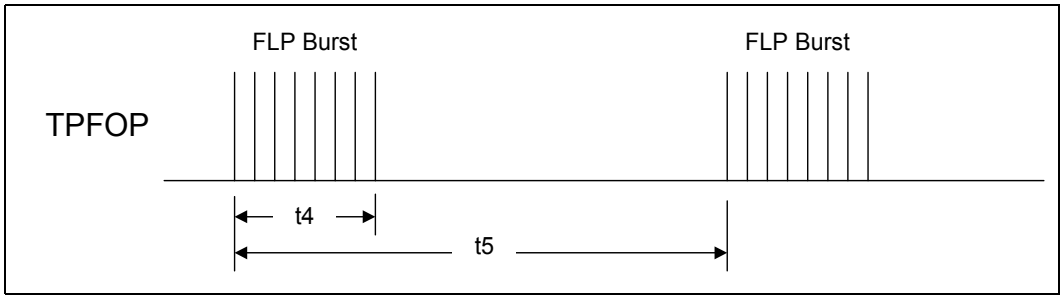
| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| COL (SQE) Delay after TX_EN off | t1 | 0.65 | – | 1.6 | us | – |
| COL (SQE) Pulse duration | t2 | 0.5 | – | 1.5 | us | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

### Figure 36. Auto-Negotiation and Fast Link Pulse Timing




### Figure 37. Fast Link Pulse Timing

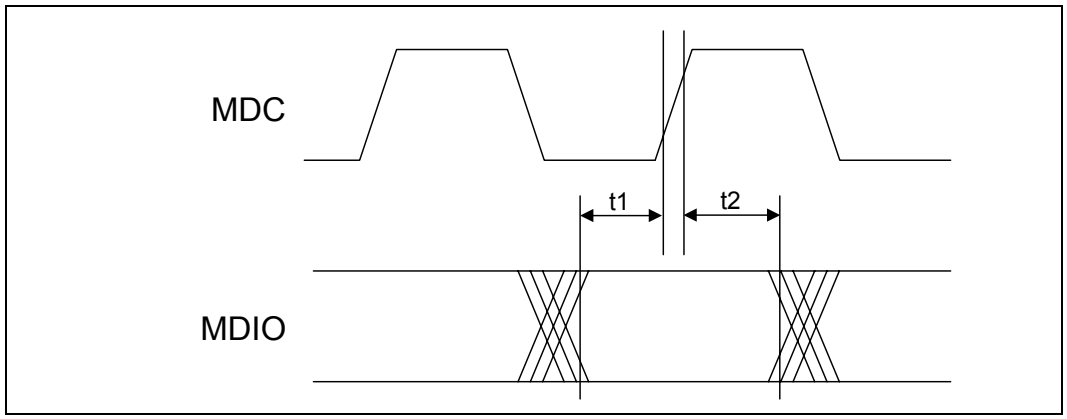



### Table 37. Auto-Negotiation and Fast Link Pulse Timing Parameters

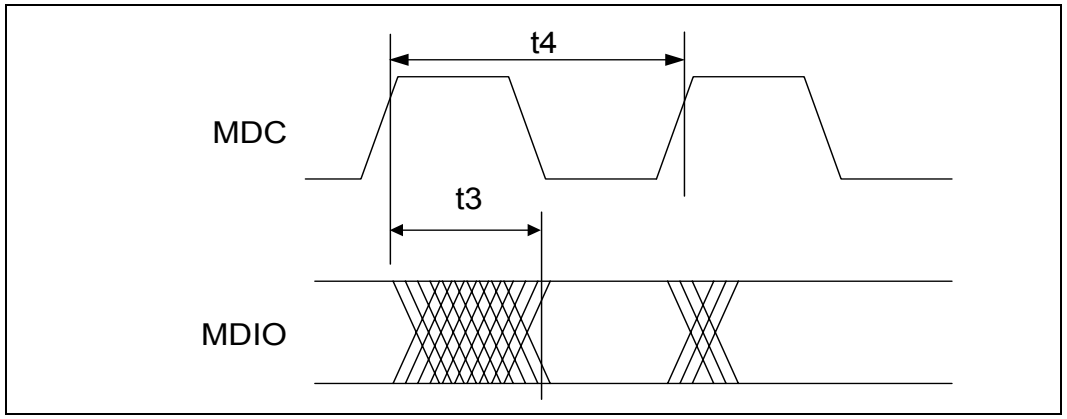
| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Clock/Data pulse width | t1 | – | 100 | – | ns | – |
| Clock pulse to Data pulse | t2 | 55.5 | – | 63.8 | µs | – |
| Clock pulse to Clock pulse | t3 | 123 | – | 127 | µs | – |
| FLP burst width | t4 | – | 2 | – | ms | – |
| FLP burst to FLP burst | t5 | 8 | 12 | 24 | ms | – |
| Clock/Data pulses per burst | – | 17 | – | 33 | ea | – |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

### Figure 38. MDIO Input Timing




### Figure 39. MDIO Output Timing

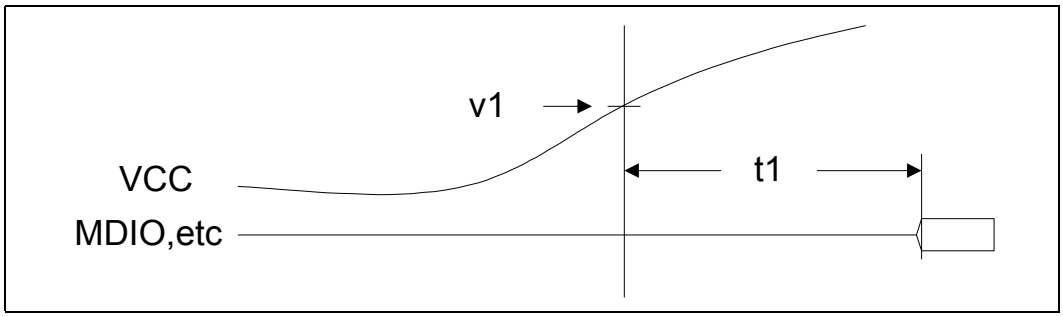



### Table 38. MDIO Timing Parameters

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| MDIO setup before MDC, sourced by STA | t1 | 10 | – | – | ns | – |
| MDIO hold after MDC, sourced by STA | t2 | 5 | – | – | ns | – |
| MDC to MDIO output delay, source by PHY | t3 | – | – | 150 | ns | – |
| MDC period | t4 | 125 | – | – | ns | MDC = 8 MHz |

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

### Figure 40. Power-Up Timing

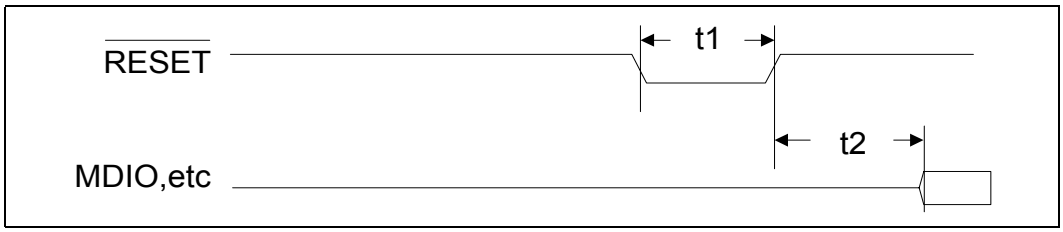



### Table 39. Power-Up Timing Parameters

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Voltage threshold | v1 | – | 2.9 | – | V | – |
| Power Up delay[2] | t1 | – | – | 300 | µs | – |

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Power-up delay is specified as a maximum value because it refers to the PHY guaranteed performance - the PHY comes out of reset after a delay of No MORE Than 300 µs. System designers should consider this as a minimum value - After threshold v1 is reached, the MAC should delay No LESS Than 300 µs before accessing the MDIO port.

### Figure 41. $\overline{\text{RESET}}$ Pulse Width and Recovery Timing




### Table 40. $\overline{\text{RESET}}$ Pulse Width and Recovery Timing Parameters

| Parameter | Symbol | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $\overline{\text{RESET}}$ pulse width | t1 | 10 | – | – | ns | – |
| $\overline{\text{RESET}}$ recovery delay[2] | t2 | – | | 300 | µs | – |

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Reset Recovery Delay is specified as a maximum value because it refers to the PHY guaranteed performance - the PHY comes out of reset after a delay of No MORE Than 300 µs. System designers should consider this as a minimum value - After de-asserting RESET*, the MAC should delay No LESS Than 300 µs before accessing the MDIO port.

# 6.0 Register Definitions

The LXT971A register set includes multiple 16-bit registers. Table 41 presents a complete register listing. Table 42 is a complete memory map of all registers and Tables 43 through 58 provide individual register definitions.

Base registers (0 through 8) are defined in accordance with the "Reconciliation Sublayer and Media Independent Interface" and "Physical Layer Link Signaling for 10/100 Mbps Auto-Negotiation" sections of the IEEE 802.3 standard.

Additional registers are defined in accordance with the IEEE 802.3 standard for adding unique chip functions.

**Table 41. Register Set**

| Address | Register Name | Bit Assignments |
|---|---|---|
| 0 | Control Register | Refer to Table 43 on page 74 |
| 1 | Status Register #1 | Refer to Table 44 on page 75 |
| 2 | PHY Identification Register 1 | Refer to Table 45 on page 76 |
| 3 | PHY Identification Register 2 | Refer to Table 46 on page 76 |
| 4 | Auto-Negotiation Advertisement Register | Refer to Table 47 on page 77 |
| 5 | Auto-Negotiation Link Partner Base Page Ability Register | Refer to Table 48 on page 78 |
| 6 | Auto-Negotiation Expansion Register | Refer to Table 49 on page 79 |
| 7 | Auto-Negotiation Next Page Transmit Register | Refer to Table 50 on page 79 |
| 8 | Auto-Negotiation Link Partner Received Next Page Register | Refer to Table 51 on page 80 |
| 9 | 1000BASE-T/100BASE-T2 Control Register | Not Implemented |
| 10 | 1000BASE-T/100BASE-T2 Status Register | Not Implemented |
| 15 | Extended Status Register | Not Implemented |
| 16 | Port Configuration Register | Refer to Table 52 on page 81 |
| 17 | Status Register #2 | Refer to Table 53 on page 82 |
| 18 | Interrupt Enable Register | Refer to Table 54 on page 83 |
| 19 | Interrupt Status Register | Refer to Table 55 on page 84 |
| 20 | LED Configuration Register | Refer to Table 56 on page 85 |
| 21-25 | Reserved | – |
| 26 | Digital Config Register | Refer to Table 57 on page 86 |
| 27-29 | Reserved | – |
| 30 | Transmit Control Register | Refer to Table 58 on page 87 |

## Table 42. Register Bit Map

| Reg Title | Bit Fields | | | | | | | | | | | | | | | | Addr |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| **Control Register** | | | | | | | | | | | | | | | | | |
| Control | Reset | Loopback | Speed Select | A/N Enable | Power Down | Isolate | Re-start A/N | Duplex Mode | COL Test | Speed Select | Reserved | | | | | | 0 |
| **Status Register** | | | | | | | | | | | | | | | | | |
| Status | 100Base-T4 | 100Base-X Full Duplex | 100Base-X Half Duplex | 10Mbps Full Duplex | 10Mbps Half Duplex | 100Base-T2 Full Duplex | 100Base-T2 Half Duplex | Extended Status | Reserved | MF Preamble Suppress | A/N Complete | Remote Fault | A/N Ability | Link Status | Jabber Detect | Extended Capability | 1 |
| **PHY ID Registers** | | | | | | | | | | | | | | | | | |
| PHY ID 1 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 2 |
| PHY ID2 | PHY ID No | | | | | | MFR Model No | | | | | | MFR Rev No | | | | 3 |
| **Auto-Negotiation Advertisement Register** | | | | | | | | | | | | | | | | | |
| A/N Advertise | Next Page | Reserved | Remote Fault | Reserved | Asymm Pause | Pause | 100Base-T4 | 100Base-TX Full Duplex | 100Base-TX | 10Base-T Full Duplex | 10Base-T | IEEE Selector Field | | | | | 4 |
| **Auto-Negotiation Link Partner Base Page Ability Register** | | | | | | | | | | | | | | | | | |
| A/N Link Ability | Next Page | Ack | Remote Fault | Reserved | Asymm Pause | Pause | 100Base-T4 | 100Base-TX Full Duplex | 100Base-TX | 10Base-T Full Duplex | 10Base-T | IEEE Selector Field | | | | | 5 |
| **Auto-Negotiation Expansion Register** | | | | | | | | | | | | | | | | | |
| A/N Expansion | Reserved | | | | | | | | | | Base Page | Parallel Detect Fault | Link Partner Next Page Able | Next Page Able | Page Received | Link Partner A/N Able | 6 |
| **Auto-Negotiation Next Page Transmit Register** | | | | | | | | | | | | | | | | | |
| A/N Next Page Txmit | Next Page | Reserved | Message Page | Ack 2 | Toggle | Message / Unformatted Code Field | | | | | | | | | | | 7 |
| **Auto-Negotiation Link Partner Next Page Receive Register** | | | | | | | | | | | | | | | | | |

## Table 42. Register Bit Map (Continued)

| Reg Title | Bit Fields | | | | | | | | | | | | | | | | Addr |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| **A/N Link Next Page** | Next Page | Ack | Message Page | Ack 2 | Toggle | Message / Unformatted Code Field | | | | | | | | | | | 8 |
| **Configuration Register** | | | | | | | | | | | | | | | | | |
| **Port Config** | Reserved | Force Link Pass | Txmit Disable | Bypass Scrambler (100TX) | Reserved | Jabber (10T) | SQE (10T) | TP Loopback (10T) | CRS Select (10T) | Sleep Mode | PRE_EN | Sleep Timer | | Fault Code Enable | Alternate Next Page | Fiber Select | 16 |
| **Status Register #2** | | | | | | | | | | | | | | | | | |
| **Status Register #2** | Reserved | 10/100 Mode | Transmit Status | Receive Status | Collision Status | Link | Duplex Mode | Auto-Neg | Auto-Neg Complete | Reserved | Polarity | Pause | Error | Reserved | Reserved | | 17 |
| **Interrupt Enable Register** | | | | | | | | | | | | | | | | | |
| **Interrupt Enable** | Reserved | | | | | | | Reserved | Auto-Neg Mask | Speed Mask | Duplex Mask | Link Mask | Reserved | Reserved | Interrupt Enable | Test Interrupt | 18 |
| **Interrupt Status Register** | | | | | | | | | | | | | | | | | |
| **Interrupt Status** | Reserved | | | | | | | Reserved | Auto-Neg Done | Speed Change | Duplex Change | Link Change | Reserved | MD Interrupt | Reserved | Reserved | 19 |
| **LED Configuration Register** | | | | | | | | | | | | | | | | | |
| **LED Config** | LED1 | | | | LED2 | | | | LED3 | | | | LED Freq | | Pulse Stretch | Reserved | 20 |
| **Digital Config Register (Address 26)** | | | | | | | | | | | | | | | | | |
| **Digital Config** | Reserved | | | | Increased MII Drive Strength | Reserved | Show Symbol Error | Reserved | | | | | | | | | 26 |
| **Transmit Control Register** | | | | | | | | | | | | | | | | | |
| **Trans. Control** | Reserved | | | Transmit Low Pwr | Port Rise Time Control | | | Reserved | | | | | | | | | 30 |

## Table 43. Control Register (Address 0)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 0.15 | Reset | 1 = PHY reset<br>0 = Normal operation | R/W<br>SC | 0 |
| 0.14 | Loopback | 1 = Enable loopback mode<br>0 = Disable loopback mode | R/W | 0 |
| 0.13 | Speed Selection | 0.6 / 0.13 / Speed Selected<br>1 / 1 / Reserved<br>1 / 0 / 1000 Mbps (not supported)<br>0 / 1 / 100 Mbps<br>0 / 0 / 10 Mbps | R/W | Note 2 |
| 0.12 | Auto-Negotiation Enable | 1 = Enable auto-negotiation process<br>0 = Disable auto-negotiation process | R/W | Note 2 |
| 0.11 | Power-Down | 1 = Power-down<br>0 = Normal operation | R/W | 0 |
| 0.10 | Isolate | 1 = Electrically isolate PHY from MII<br>0 = Normal operation | R/W | 0 |
| 0.9 | Restart Auto-Negotiation | 1 = Restart auto-negotiation process<br>0 = Normal operation | R/W<br>SC | 0 |
| 0.8 | Duplex Mode | 1 = Full-duplex<br>0 = Half-duplex | R/W | Note 2 |
| 0.7 | Collision Test | 1 = Enable COL signal test<br>0 = Disable COL signal test | R/W | 0 |
| 0.6 | Speed Selection | 0.6 / 0.13 / Speed Selected<br>1 / 1 / Reserved<br>1 / 0 / 1000 Mbps (not supported)<br>0 / 1 / 100 Mbps<br>0 / 0 / 10 Mbps | R/W | 0 |
| 0.5:0 | Reserved | Write as 0, ignore on Read | R/W | 00000 |

1. R/W = Read/Write
   RO = Read Only
   SC = Self Clearing
2. Default value of Register bits 0.12, 0.13 and 0.8 are determined by the LED/CFG*n* pins (refer to Table 9 on page 30).

### Table 44. MII Status Register #1 (Address 1)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 1.15 | 100BASE-T4<br>Not Supported | 1 = PHY able to perform 100BASE-T4<br>0 = PHY not able to perform 100BASE-T4 | RO | 0 |
| 1.14 | 100BASE-X Full-Duplex | 1 = PHY able to perform full-duplex 100BASE-X<br>0 = PHY not able to perform full-duplex 100BASE-X | RO | 1 |
| 1.13 | 100BASE-X Half-Duplex | 1 = PHY able to perform half-duplex 100BASE-X<br>0 = PHY not able to perform half-duplex 100BASE-X | RO | 1 |
| 1.12 | 10 Mbps Full-Duplex | 1 = PHY able to operate at 10 Mbps in full-duplex mode<br>0 = PHY not able to operate at 10 Mbps full-duplex mode | RO | 1 |
| 1.11 | 10 Mbps Half-Duplex | 1 = PHY able to operate at 10 Mbps in half-duplex mode<br>0 = PHY not able to operate at 10 Mbps in half-duplex | RO | 1 |
| 1.10 | 100BASE-T2 Full-Duplex<br>Not Supported | 1 = PHY able to perform full-duplex 100BASE-T2<br>0 = PHY not able to perform full-duplex 100BASE-T2 | RO | 0 |
| 1.9 | 100BASE-T2 Half-Duplex<br>Not Supported | 1 = PHY able to perform half-duplex 100BASE-T2<br>0 = PHY not able to perform half-duplex 100BASE-T2 | RO | 0 |
| 1.8 | Extended Status | 1 = Extended status information in register 15<br>0 = No extended status information in register 15 | RO | 0 |
| 1.7 | Reserved | 1 = ignore when read | RO | 0 |
| 1.6 | MF Preamble Suppression | 1 = PHY accepts management frames with preamble suppressed<br>0 = PHY will not accept management frames with preamble suppressed | RO | 0 |
| 1.5 | Auto-Negotiation complete | 1 = Auto-negotiation complete<br>0 = Auto-negotiation not complete | RO | 0 |
| 1.4 | Remote Fault | 1 = Remote fault condition detected<br>0 = No remote fault condition detected | RO/LH | 0 |
| 1.3 | Auto-Negotiation Ability | 1 = PHY is able to perform auto-negotiation<br>0 = PHY is not able to perform auto-negotiation | RO | 1 |
| 1.2 | Link Status | 1 = Link is up<br>0 = Link is down | RO/LL | 0 |
| 1.1 | Jabber Detect | 1 = Jabber condition detected<br>0 = Jabber condition not detected | RO/LH | 0 |
| 1.0 | Extended Capability | 1 = Extended register capabilities<br>0 = Basic register capabilities | RO | 1 |

1. RO = Read Only
   LL = Latching Low
   LH = Latching High

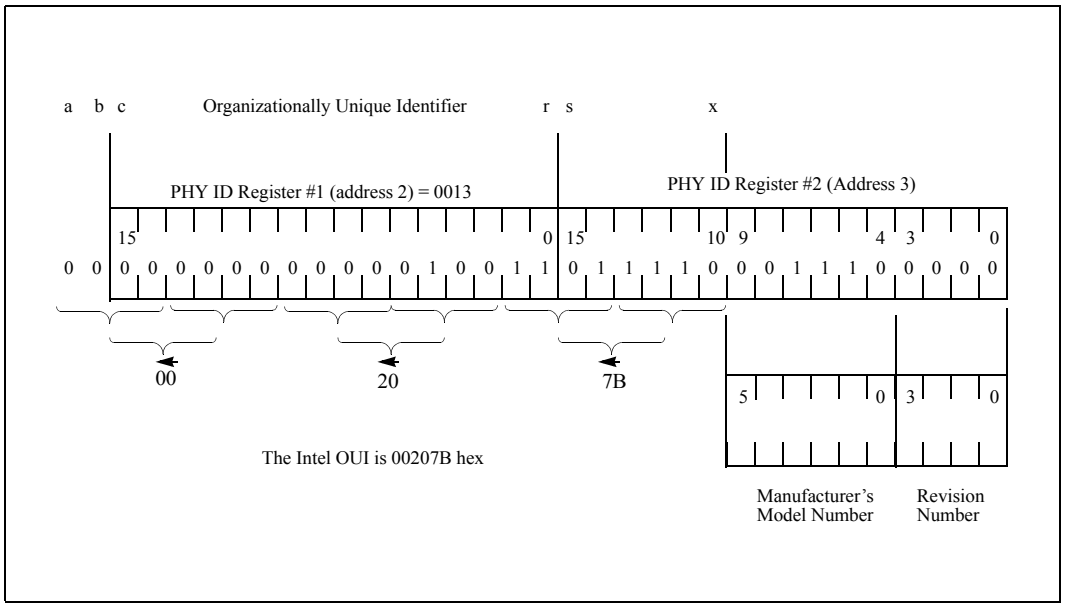
### Table 45. PHY Identification Register 1 (Address 2)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 2.15:0 | PHY ID Number | The PHY identifier composed of bits 3 through 18 of the OUI. | RO | 0013 hex |
| 1. RO = Read Only | | | | |

### Table 46. PHY Identification Register 2 (Address 3)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 3.15:10 | PHY ID number | The PHY identifier composed of bits 19 through 24 of the OUI. | RO | 011110 |
| 3.9:4 | Manufacturer's model number | 6 bits containing manufacturer's part number. | RO | 001110 |
| 3.3:0 | Manufacturer's revision number | 4 bits containing manufacturer's revision number. | RO | xxxx (See the LXT971A/972A Specification Update) |
| 1. RO = Read Only | | | | |

### Figure 42. PHY Identifier Bit Mapping



## Table 47. Auto-Negotiation Advertisement Register (Address 4)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 4.15 | Next Page | 1 = Port has ability to send multiple pages.<br>0 = Port has no ability to send multiple pages. | R/W | 0 |
| 4.14 | Reserved | Ignore. | RO | 0 |
| 4.13 | Remote Fault | 1 = Remote fault.<br>0 = No remote fault. | R/W | 0 |
| 4.12 | Reserved | Ignore. | R/W | 0 |
| 4.11 | Asymmetric Pause | Pause operation defined in Clause 40 and 27. | R/W | 0 |
| 4.10 | Pause | 1 = Pause operation enabled for full-duplex links.<br>0 = Pause operation disabled. | R/W | Note 2 |
| 4.9 | 100BASE-T4 | 1 = 100BASE-T4 capability is available.<br>0 = 100BASE-T4 capability is not available.<br>(The LXT971A does not support 100BASE-T4 but allows this bit to be set to advertise in the auto-negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.) | R/W | 0 |
| 4.8 | 100BASE-TX full-duplex | 1 = Port is 100BASE-TX full-duplex capable.<br>0 = Port is not 100BASE-TX full-duplex capable. | R/W | Note 3 |
| 4.7 | 100BASE-TX | 1 = Port is 100BASE-TX capable.<br>0 = Port is not 100BASE-TX capable. | R/W | Note 3 |
| 4.6 | 10BASE-T full-duplex | 1 = Port is 10BASE-T full-duplex capable.<br>0 = Port is not 10BASE-T full-duplex capable. | R/W | Note 3 |
| 4.5 | 10BASE-T | 1 = Port is 10BASE-T capable.<br>0 = Port is not 10BASE-T capable. | R/W | Note 3 |
| 4.4:0 | Selector Field, S<4:0> | <00001> = IEEE 802.3.<br><00010> = IEEE 802.9 ISLAN-16T.<br><00000> = Reserved for future auto-negotiation development.<br><11111> = Reserved for future auto-negotiation development.<br>Unspecified or reserved combinations should not be transmitted. | R/W | 00001 |

1. R/W = Read/Write
   RO = Read Only
2. The default setting of Register bit 4.10 (PAUSE) is determined by pin 33/H8 at reset.
3. Default values of Register bits 4.5, 4.6, 4.7, and 4.8 are determined by LED/CFG*n* pins at reset. Refer to Table 9 for details.

## Table 48. Auto-Negotiation Link Partner Base Page Ability Register (Address 5)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 5.15 | Next Page | 1 = Link Partner has ability to send multiple pages.<br>0 = Link Partner has no ability to send multiple pages. | RO | N/A |
| 5.14 | Acknowledge | 1 = Link Partner has received Link Code Word from LXT971A.<br>0 = Link Partner has not received Link Code Word from the LXT971A. | RO | N/A |
| 5.13 | Remote Fault | 1 = Remote fault.<br>0 = No remote fault. | RO | N/A |
| 5.12 | Reserved | Ignore. | RO | N/A |
| 5.11 | Asymmetric Pause | Pause operation defined in Clause 40 and 27.<br>1 = Link Partner is Pause capable.<br>0 = Link Partner is not Pause capable. | RO | N/A |
| 5.10 | Pause | 1 = Link Partner is Pause capable.<br>0 = Link Partner is not Pause capable. | RO | N/A |
| 5.9 | 100BASE-T4 | 1 = Link Partner is 100BASE-T4 capable.<br>0 = Link Partner is not 100BASE-T4 capable. | RO | N/A |
| 5.8 | 100BASE-TX full-duplex | 1 = Link Partner is 100BASE-TX full-duplex capable.<br>0 = Link Partner is not 100BASE-TX full-duplex capable. | RO | N/A |
| 5.7 | 100BASE-TX | 1 = Link Partner is 100BASE-TX capable.<br>0 = Link Partner is not 100BASE-TX capable. | RO | N/A |
| 5.6 | 10BASE-T full-duplex | 1 = Link Partner is 10BASE-T full-duplex capable.<br>0 = Link Partner is not 10BASE-T full-duplex capable. | RO | N/A |
| 5.5 | 10BASE-T | 1 = Link Partner is 10BASE-T capable.<br>0 = Link Partner is not 10BASE-T capable. | RO | N/A |
| 5.4:0 | Selector Field S<4:0> | <00001> = IEEE 802.3.<br><00010> = IEEE 802.9 ISLAN-16T.<br><00000> = Reserved for future auto-negotiation development.<br><11111> = Reserved for future auto-negotiation development.<br>Unspecified or reserved combinations shall not be transmitted. | RO | N/A |

1. RO = Read Only

### Table 49. Auto-Negotiation Expansion (Address 6)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 6.15:6 | Reserved | Ignore on read. | RO | 0 |
| 6.5 | Base Page | This bit indicates the status of the auto-negotiation variable base page. It flags synchronization with the auto-negotiation state diagram, allowing detection of interrupted links. This bit is only used if Register bit 16.1 (Alternate NP feature) is set.<br>1 = Base page = true<br>0 = Base page = false | RO/ LH | 0 |
| 6.4 | Parallel Detection Fault | 1 = Parallel detection fault has occurred.<br>0 = Parallel detection fault has not occurred. | RO/ LH | 0 |
| 6.3 | Link Partner Next Page Able | 1 = Link partner is next page able.<br>0 = Link partner is not next page able. | RO | 0 |
| 6.2 | Next Page Able | 1 = Local device is next page able.<br>0 = Local device is not next page able. | RO | 1 |
| 6.1 | Page Received | 1 = Indicates that a new page has been received and the received code word has been loaded into Register 5 (Base Pages) or Register 8 (Next Pages) as specified in Clause 28 of IEEE 802.3. This bit is cleared on Read. If Register bit 16.1 is set, the Page Received bit is also cleared when mr_page_rx = false or transmit_disable = true. | RO LH | 0 |
| 6.0 | Link Partner A/N Able | 1 = Link partner is auto-negotiation able.<br>0 = Link partner is not auto-negotiation able. | RO | 0 |
| 1. RO = Read Only LH = Latching High | | | | |

### Table 50. Auto-Negotiation Next Page Transmit Register (Address 7)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 7.15 | Next Page (NP) | 1 = Additional next pages follow<br>0 = Last page | R/W | 0 |
| 7.14 | Reserved | Write as 0, ignore on read | RO | 0 |
| 7.13 | Message Page (MP) | 1 = Message page<br>0 = Unformatted page | R/W | 1 |
| 7.12 | Acknowledge 2 (ACK2) | 1 = Complies with message<br>0 = Cannot comply with message | R/W | 0 |
| 7.11 | Toggle (T) | 1 = Previous value of the transmitted Link Code Word equalled logic zero<br>0 = Previous value of the transmitted Link Code Word equalled logic one | R/W | 0 |
| 7.10:0 | Message/Unformatted Code Field | | R/W | 00000000 001 |
| 1. RO = Read Only. R/W = Read/Write | | | | |

### Table 51. Auto-Negotiation Link Partner Next Page Receive Register (Address 8)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 8.15 | Next Page (NP) | 1 = Link Partner has additional next pages to send<br>0 = Link Partner has no additional next pages to send | RO | 0 |
| 8.14 | Acknowledge (ACK) | 1 = Link Partner has received Link Code Word from LXT971A<br>0 = Link Partner has not received Link Code Word from LXT971A | RO | 0 |
| 8.13 | Message Page (MP) | 1 = Page sent by the Link Partner is a Message Page<br>0 = Page sent by the Link Partner is an Unformatted Page | RO | 0 |
| 8.12 | Acknowledge 2 (ACK2) | 1 = Link Partner complies with the message<br>0 = Link Partner cannot comply with the message | RO | 0 |
| 8.11 | Toggle (T) | 1 = Previous value of the transmitted Link Code Word equalled logic zero<br>0 = Previous value of the transmitted Link Code Word equalled logic one | RO | 0 |
| 8.10:0 | Message/Unformatted Code Field | User definable | RO | 0 |

1. RO = Read Only.

## Table 52. Configuration Register (Address 16, Hex 10)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 16.15 | Reserved | Write as zero, ignore on read. | R/W | 0 |
| 16.14 | Force Link Pass | 1 = Force Link pass<br>0 = Normal operation | R/W | 0 |
| 16.13 | Transmit Disable | 1 = Disable Twisted Pair transmitter<br>0 = Normal Operation | R/W | 0 |
| 16.12 | Bypass Scrambler (100BASE-TX) | 1 = Bypass Scrambler and Descrambler<br>0 = Normal Operation | R/W | 0 |
| 16.11 | Reserved | Ignore | R/W | 0 |
| 16.10 | Jabber (10BASE-T) | 1 = Disable Jabber Correction<br>0 = Normal operation | R/W | 0 |
| 16.9 | SQE (10BASE-T) | 1 = Enable Heart Beat<br>0 = Disable Heart Beat | R/W | 0 |
| 16.8 | TP Loopback (10BASE-T) | 1 = Disable TP loopback during half-duplex operation<br>0 = Normal Operation | R/W | 0 |
| 16.7 | CRS Select (10BASE-T) | 1 = CRS deassert extends to RX_DV deassert<br>0 = Normal Operation | R/W | 1 |
| 16.6 | Sleep Mode | 1 = Enable Sleep Mode<br>0 = Disable Sleep Mode | R/W | Note 2 |
| 16.5 | PRE_EN | Preamble Enable.<br>0 = Set RX_DV high coincident with SFD.<br>1 = Set RX_DV high and RXD = preamble when CRS is asserted. | R/W | 0 |
| 16.4:3 | Sleep Timer | 00 = 3.04 seconds<br>01 = 2.00 seconds<br>10 = 1.04 seconds | R/W | 00 |
| 16.2 | Fault Code Enable | 1 = Enable FEFI transmission<br>0 = Disable FEFI transmission | R/W | 1 |
| 16.1 | Alternate NP feature | 1 = Enable alternate auto negotiate next page feature.<br>0 = Disable alternate auto negotiate next page feature | R/W | 0 |
| 16.0 | Fiber Select | 1 = Select fiber mode.<br>0 = Select TP mode. | R/W | Note 3 |

1. R/W = Read /Write
   LHR = Latches High on Reset
2. The default value of Register bit 16.6 is determined by the state of the SLEEP pin 32/H7.
3. The default value of Register bit 16.0 is determined by pin 26/G2 (SD/TP).

### Table 53. Status Register #2 (Address 17)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 17.15 | Reserved | Always 0. | RO | 0 |
| 17.14 | 10/100 Mode | 1 = LXT971A is operating in 100BASE-TX mode.<br>0 = LXT971A is not operating 100BASE-TX mode. | RO | 0 |
| 17.13 | Transmit Status | 1 = LXT971A is transmitting a packet.<br>0 = LXT971A is not transmitting a packet. | RO | 0 |
| 17.12 | Receive Status | 1 = LXT971A is receiving a packet.<br>0 = LXT971A is not receiving a packet. | RO | 0 |
| 17.11 | Collision Status | 1 = Collision is occurring.<br>0 = No collision. | RO | 0 |
| 17.10 | Link | 1 = Link is up.<br>0 = Link is down. | RO | 0 |
| 17.9 | Duplex Mode | 1 = Full-duplex.<br>0 = Half-duplex. | RO | 0 |
| 17.8 | Auto-Negotiation | 1 = LXT971A is in auto-negotiation mode.<br>0 = LXT971A is in manual mode. | RO | 0 |
| 17.7 | Auto-Negotiation Complete | 1 = Auto-negotiation process completed.<br>0 = Auto-negotiation process not completed.<br>This bit is only valid when auto negotiate is enabled, and is equivalent to Register bit 1.5. | RO | 0 |
| 17.6 | Reserved | Always 0. | RO | 0 |
| 17.5 | Polarity | 1 = Polarity is reversed.<br>0 = Polarity is not reversed. | RO | 0 |
| 17.4 | Pause | 1 = Device Pause capable.<br>0 = Device Not Pause capable. | RO | 0 |
| 17:3 | Error | 1 = Error Occurred (Remote Fault, X,Y, Z).<br>0 = No error occurred. | RO | 0 |
| 17:2 | Reserved | Always 0. | RO | 0 |
| 17:1 | Reserved | Always 0. | RO | 0 |
| 17.0 | Reserved | Always 0. | RO | 0 |

1. RO = Read Only. R/W = Read/Write

### Table 54. Interrupt Enable Register (Address 18)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 18.15:9 | Reserved | Write as 0; ignore on read. | R/W | N/A |
| 18.8 | Reserved | Write as 0; ignore on read. | R/W | 0 |
| 18.7 | ANMSK | Mask for Auto Negotiate Complete<br>1 = Enable event to cause interrupt.<br>0 = Do not allow event to cause interrupt. | R/W | 0 |
| 18.6 | SPEEDMSK | Mask for Speed Interrupt<br>1 = Enable event to cause interrupt.<br>0 = Do not allow event to cause interrupt. | R/W | 0 |
| 18.5 | DUPLEXMSK | Mask for Duplex Interrupt<br>1 = Enable event to cause interrupt.<br>0 = Do not allow event to cause interrupt. | R/W | 0 |
| 18.4 | LINKMSK | Mask for Link Status Interrupt<br>1 = Enable event to cause interrupt.<br>0 = Do not allow event to cause interrupt. | R/W | 0 |
| 18.3 | Reserved | Write as 0, ignore on read. | R/W | 0 |
| 18.2 | Reserved | Write as 0, ignore on read. | R/W | 0 |
| 18.1 | INTEN | 1 = Enable interrupts.<br>0 = Disable interrupts. | R/W | 0 |
| 18.0 | TINT | 1 = Force interrupt on $\overline{\text{MDINT}}$.<br>0 = Normal operation. | R/W | 0 |

1. R/W = Read /Write

### Table 55. Interrupt Status Register (Address 19, Hex 13)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 19.15:9 | Reserved | Ignore | RO | N/A |
| 19.8 | Reserved | Ignore | RO | 0 |
| 19.7 | ANDONE | Auto-negotiation Status<br>1= Auto-negotiation has completed.<br>0= Auto-negotiation has not completed. | RO/SC | N/A |
| 19.6 | SPEEDCHG | Speed Change Status<br>1 = A Speed Change has occurred since last reading this register.<br>0 = A Speed Change has not occurred since last reading this register. | RO/SC | 0 |
| 19.5 | DUPLEXCHG | Duplex Change Status<br>1 = A Duplex Change has occurred since last reading this register.<br>0 = A Duplex Change has not occurred since last reading this register. | RO/SC | 0 |
| 19.4 | LINKCHG | Link Status Change Status<br>1 = A Link Change has occurred since last reading this register.<br>0 = A Link Change has not occurred since last reading this register. | RO/SC | 0 |
| 19.3 | Reserved | Ignore. | RO | 0 |
| 19.2 | $\overline{\text{MDINT}}$ | 1 = MII interrupt pending.<br>0 = No MII interrupt pending. | RO | |
| 19.1 | Reserved | Ignore. | RO | N/A |
| 19.0 | Reserved | Ignore | RO | 0 |

1. R/W = Read/Write, RO = Read Only, SC = Self Clearing.

## Table 56. LED Configuration Register (Address 20, Hex 14)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 20.15:12 | LED1<br>Programming bits | 0000 = Display Speed Status (Continuous, Default)<br>0001 = Display Transmit Status (Stretched)<br>0010 = Display Receive Status (Stretched)<br>0011 = Display Collision Status (Stretched)<br>0100 = Display Link Status (Continuous)<br>0101 = Display Duplex Status (Continuous)<br>0110 = Unused<br>0111 = Display Receive or Transmit Activity (Stretched)<br>1000 = Test mode- turn LED on (Continuous)<br>1001 = Test mode- turn LED off (Continuous)<br>1010 = Test mode- blink LED fast (Continuous)<br>1011 = Test mode- blink LED slow (Continuous)<br>1100 = Display Link and Receive Status combined [2] (Stretched)[3]<br>1101 = Display Link and Activity Status combined [2] (Stretched)[3]<br>1110 = Display Duplex and Collision Status combined [4] (Stretched)[3]<br>1111 = Unused | R/W | 0000 |
| 20.11:8 | LED2<br>Programming bits | 0000 = Display Speed Status<br>0001 = Display Transmit Status<br>0010 = Display Receive Status<br>0011 = Display Collision Status<br>0100 = Display Link Status (Default)<br>0101 = Display Duplex Status<br>0110 = Unused<br>0111 = Display Receive or Transmit Activity<br>1000 = Test mode- turn LED on<br>1001 = Test mode- turn LED off<br>1010 = Test mode- blink LED fast<br>1011 = Test mode- blink LED slow<br>1100 = Display Link and Receive Status combined [2] (Stretched)[3]<br>1101 = Display Link and Activity Status combined [2] (Stretched)[3]<br>1110 = Display Duplex and Collision Status combined [4] (Stretched)[3]<br>1111 = Unused | R/W | 0100 |

1. R/W = Read /Write
   RO = Read Only
   LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (Receive or Activity) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Values are relative approximations. Not guaranteed or production tested.

## Table 56. LED Configuration Register (Address 20, Hex 14) (Continued)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 20.7:4 | LED3 Programming bits | 0000 = Display Speed Status<br>0001 = Display Transmit Status<br>0010 = Display Receive Status (Default)<br>0011 = Display Collision Status<br>0100 = Display Link Status<br>0101 = Display Duplex Status<br>0110 = Unused<br>0111 = Display Receive or Transmit Activity<br>1000 = Test mode- turn LED on<br>1001 = Test mode- turn LED off<br>1010 = Test mode- blink LED fast<br>1011 = Test mode- blink LED slow<br>1100 = Display Link and Receive Status combined [2] (Stretched)[3]<br>1101 = Display Link and Activity Status combined [2] (Stretched)[3]<br>1110 = Display Duplex and Collision Status combined [4] (Stretched)[3]<br>1111 = Unused | R/W | 0010 |
| 20.3:2 | LEDFREQ[5] | 00 = Stretch LED events to 30 ms.<br>01 = Stretch LED events to 60 ms.<br>10 = Stretch LED events to 100 ms.<br>11 = Reserved. | R/W | 00 |
| 20.1 | PULSE-STRETCH | 0 = Disable pulse stretching of all LEDs.<br>1 = Enable pulse stretching of all LEDs. | R/W | 1 |
| 20.0 | Reserved | Ignore. | R/W | N/A |

1. R/W = Read /Write
   RO = Read Only
   LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up. The secondary LED driver (Receive or Activity) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch Register bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full-duplex. Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Values are relative approximations. Not guaranteed or production tested.

## Table 57. Digital Config Register (Address 26)

| Bit | Name | Description | Type [1] | Default |
|---|---|---|---|---|
| 26.15:12 | Reserved | Reserved | RO | 0 |
| 26.11 | MII Drive Strength | 1 = Increased MII drive strength<br>0 = Normal MII drive strength | R/W | 0 |
| 26.10 | Reserved | Reserved | RO | 0 |
| 26.9 | Show Symbol Error | 1 = Map Symbol Error Signal To RXER<br>0 = Normal RXER | R/W | 0 |
| 26.8:0 | Reserved | Reserved | RO | 0 |

1. R/W = Read /Write, RO = Read Only, LH = Latching High

### Table 58. Transmit Control Register (Address 30)

| Bit | Name | Description | Type[2] | Default |
|---|---|---|---|---|
| 30.15:11 | Reserved | Ignore | R/W | 0 |
| 30.12 | Transmit Low Power | 1 = Forces the transmitter into low power mode. Also forces a zero-differential transmission.<br>0 = Normal transmission. | R/W | 0 |
| 30.11:10 | Port Rise Time Control[1] | 00 = 3.0 ns (default = TXSLEW<1:0> pins)<br>01 = 3.4 ns<br>10 = 3.9 ns<br>11 = 4.4 ns | R/W | 00 |
| 30.9:0 | Reserved | Ignore | R/W | 0 |

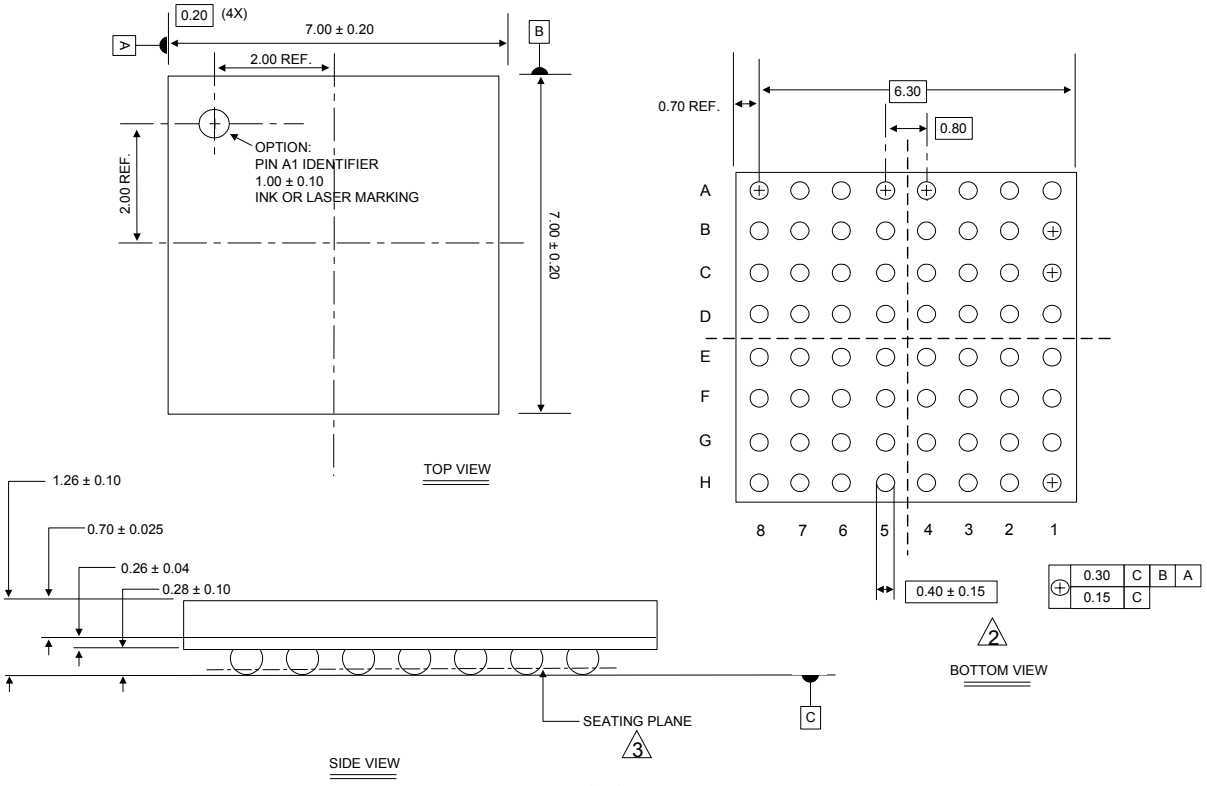
1. Values are relative approximations. Not guaranteed or production tested.
2. R/W = Read/Write

# 7.0 Package Specifications

**Figure 43. PBGA Package Specification**

## 64-Ball Plastic Ball Grid Array Package

- Part Number - LXT971ABC Commercial Temperature Range (0ºC to +70ºC)
- Part Number - LXT971ABE Extended Temperature Range (-40ºC to +85ºC)




NOTES:
1. All dimensions and tolerances conform to ASME Y 14.5 M - 1994.
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
4. Maximum mold to substrate offset shall be 0.127.
5. The surface finish of the package shall be EDM Charmille #18 - #21.
6. Unless otherwise specified tolerance: Decimal ± 0.05 Angular ±2°.

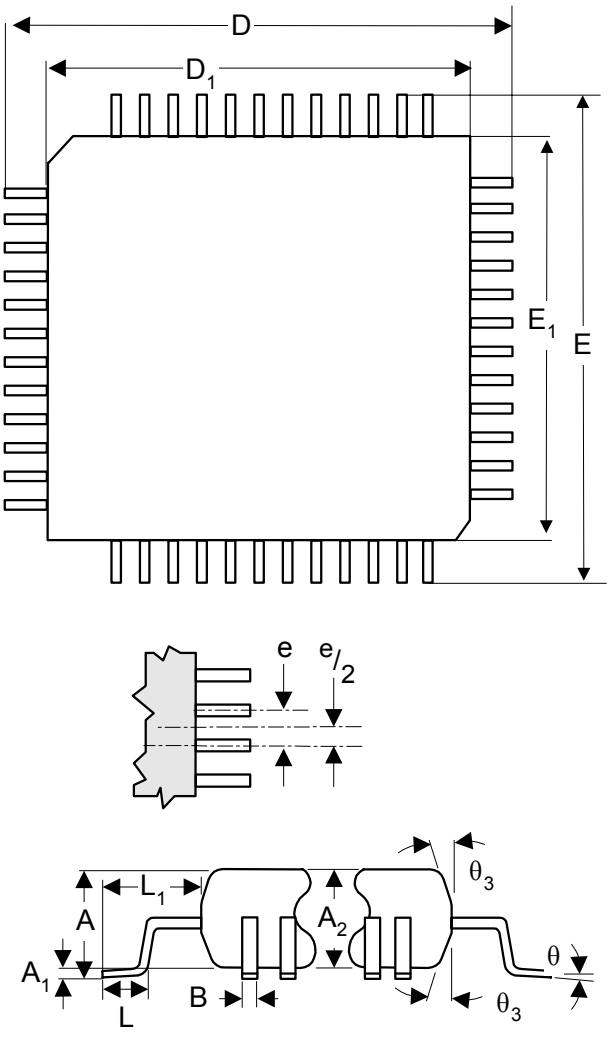
**Figure 44. LXT971A LQFP Package Specifications**

## 64-Pin Low Profile Quad Flat Pack

- Part Number - LXT971ALC Commercial Temperature Range (0ºC to +70ºC)
- Part Number - LXT971ALE Extended Temperature Range (-40ºC to +85ºC)

| Dim | Millimeters | |
|---|---|---|
| | Min | Max |
| A | – | 1.60 |
| $A_1$ | 0.05 | 0.15 |
| $A_2$ | 1.35 | 1.45 |
| B | 0.17 | 0.27 |
| D | 11.85 | 12.15 |
| $D_1$ | 9.9 | 10.1 |
| E | 11.85 | 12.15 |
| $E_1$ | 9.9 | 10.1 |
| e | 0.50 BSC[1] | |
| L | 0.45 | 0.75 |
| $L_1$ | 1.00 REF | |
| $\theta_3$ | 11º | 13º |
| $\theta$ | 0º | 7º |

1. Basic Spacing between Centers



# 8.0 Product Ordering Information

### Table 59. Product Information

| Number | Revision | Qualification | Tray MM | Tape & Reel MM |
|---|---|---|---|---|
| DJLXT971ALC.A4 | A4 | S | 834105 | 834916 |
| DJLXT971ALE.A4 | A4 | S | 835676 | 835791 |
| FLLXT971ABC.A4 | A4 | S | 834103 | 834926 |
| FLLXT971ABE.A4 | A4 | S | 834104 | 835080 |

### Figure 45. Ordering Information - Sample