LXT9761/9781

Fast Ethernet 10/100 Multi-Port Transceiver with RMII

Datasheet

The LXT9781 is an eight-port PHY Fast Ethernet Transceiver that supports IEEE 802.3 physical layer applications at both 10 Mbps and 100 Mbps. It provides a Reduced Media Independent Interface (RMII) for switching and other independent port applications. The LXT9761 offers the same features and functionality in a six-port device. This data sheet uses the singular designation "LXT97x1" to refer to both devices.

All network ports provide a combination twisted-pair (TP) or pseudo-ECL (PECL) interface for a 10/100BASE-TX or 100BASE-FX connection.

The LXT97x1 provides three discrete LED driver outputs for each port, as well as eight global serial LED outputs. The device supports both half- and full-duplex operation at 10 Mbps and 100 Mbps, and requires only a single 3.3V power supply.

Applications

- 100BASE-T, 10/100-TX, or 100BASE-FX Switches and multi-port NICs.

Product Features

- Six or eight IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters
- 3.3V operation
- Optimized for dual-high stacked R45 applications
- Proprietary Optimal Signal Processing™ architecture improves SNR by 3 dB over ideal analog filters
- Robust baseline wander correction 100BASE-FX fiber-optic capability on all ports
- Supports both auto-negotiation and legacy systems without auto-negotiation capability
- JTAG boundary scan
- Multiple Reduced MII (RMII) ports for independent PHY port operation
- Configurable via MDIO port or external control pins.
- Maskable interrupts
- Low power consumption (390 mW per port, typical)
- 208-pin PQFP (LXT9761 and LXT9781)
- 272-pin PBGA (LXT9781 only)

As of January 15, 2001, this document replaces the Level One document *LXT9761/9781 — Fast Ethernet 10/100 Multi-Port Transceiver with RMII.*

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Datasheet

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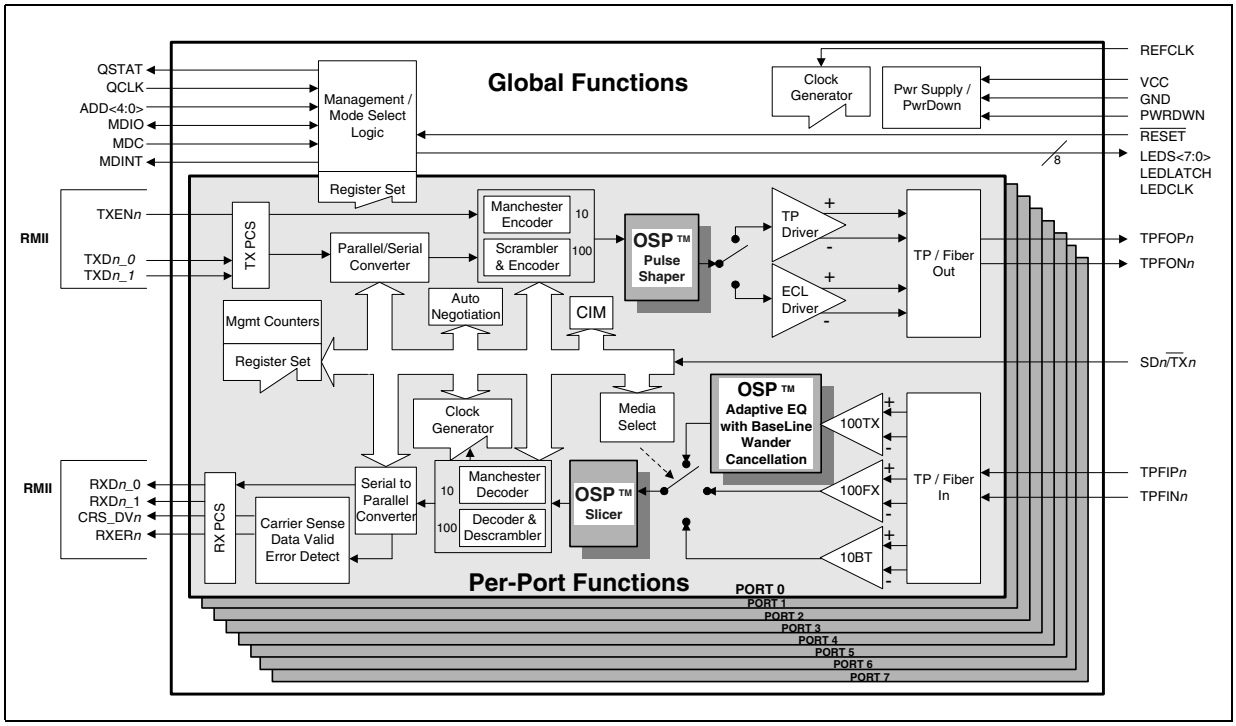
Revision History

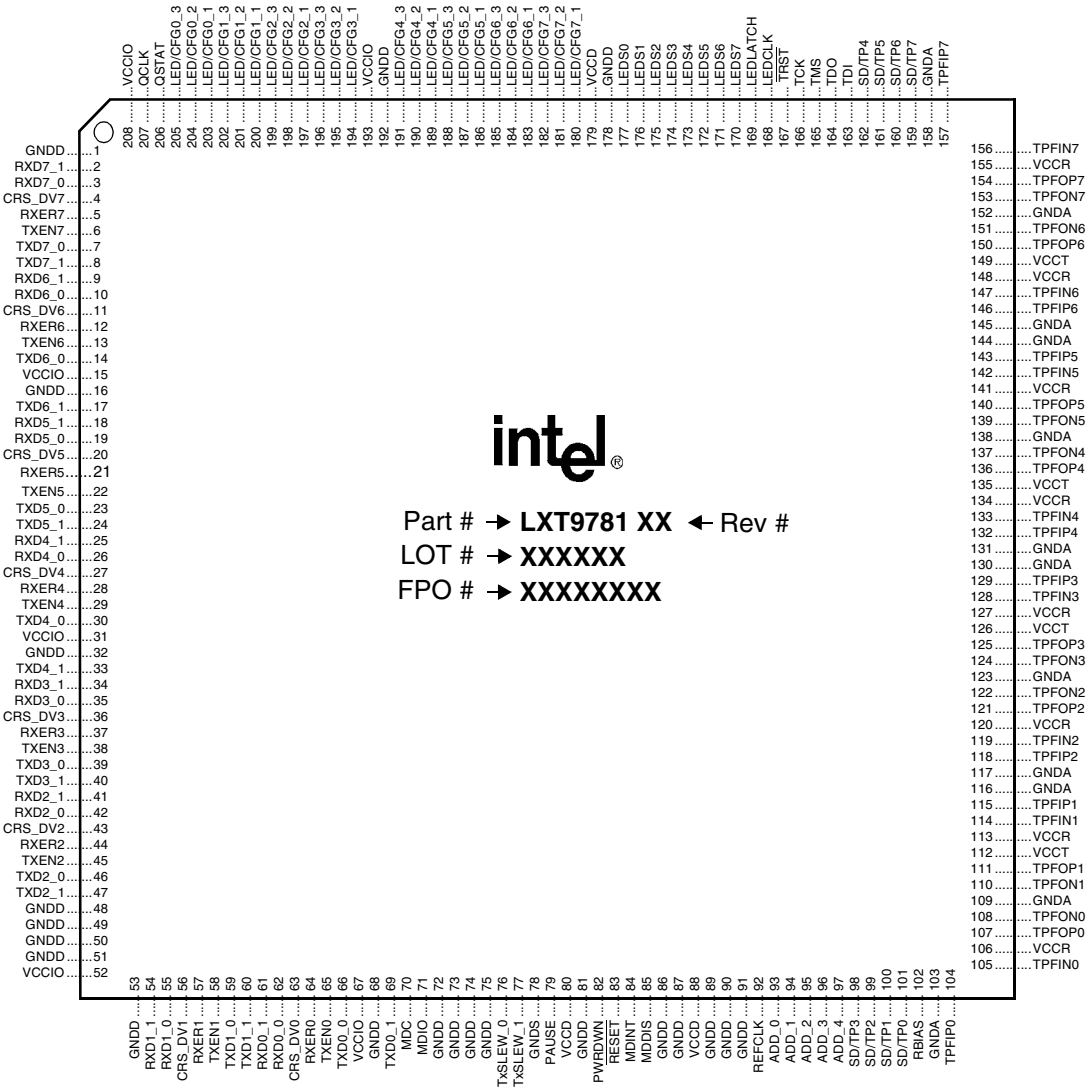
Revision	Date	Description

Figure 1. LXT9781 Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT9781 PQFP Pin Assignments

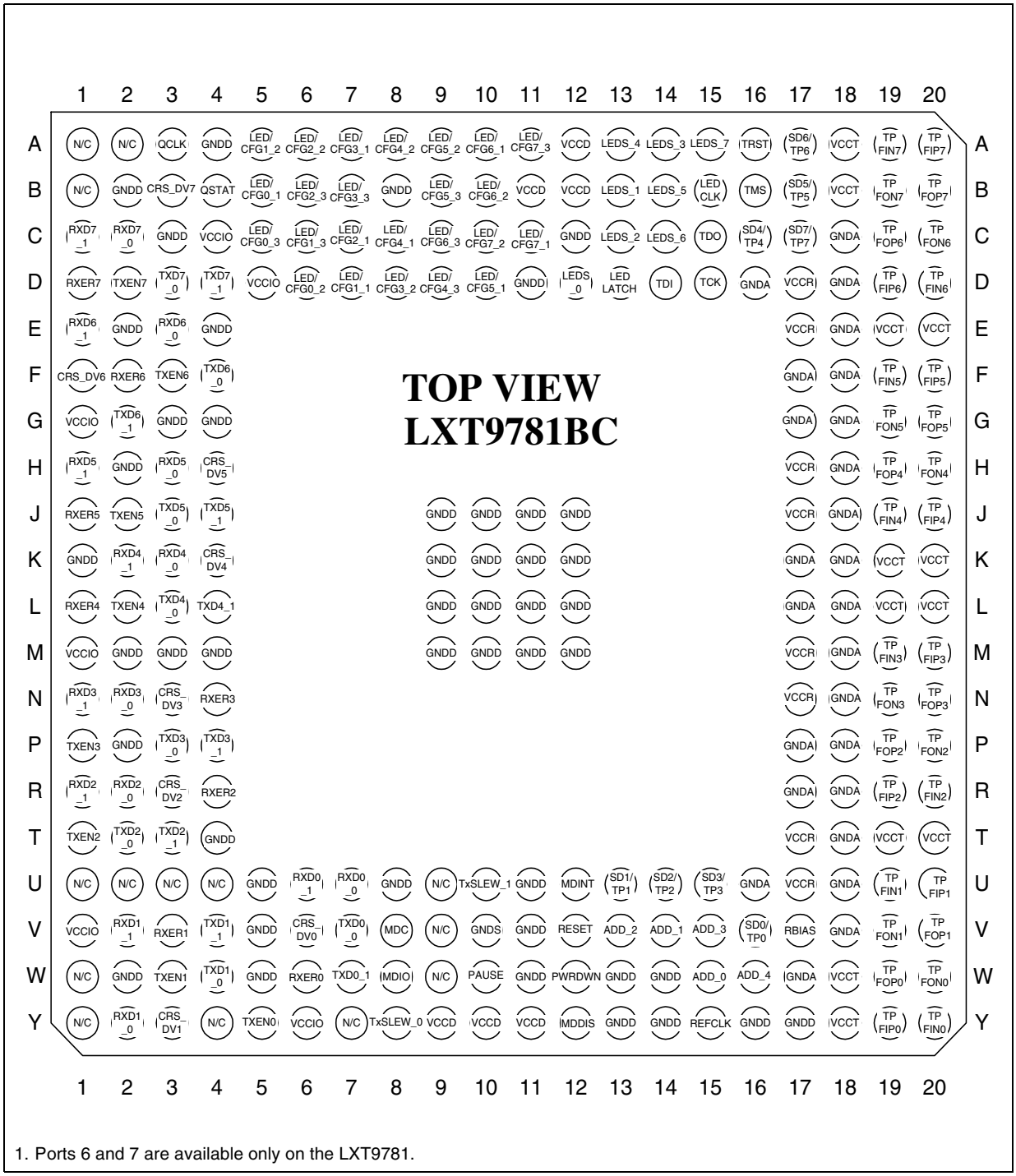


1. Ports 6 and 7 are available only on the LXT9781. These ports are not bonded out on the LXT9761.

Package Topside Markings

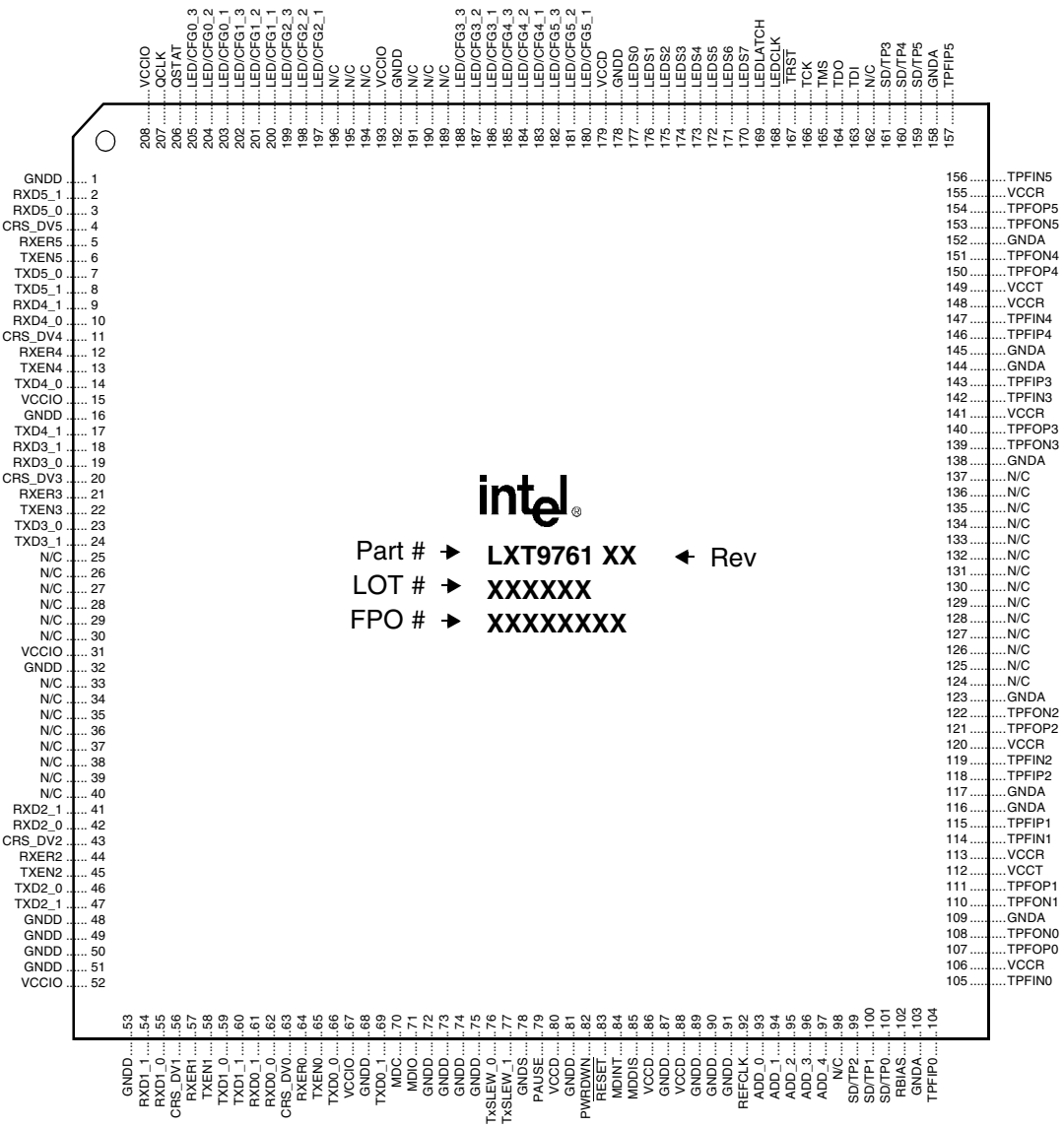
Marking	Definition
Part #	LXT9781 is the unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” (Refer to Specification Update for additional stepping information.)
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Figure 3. LXT9781 PBGA Pin Assignments



1. Ports 6 and 7 are available only on the LXT9781.

Figure 4. LXT9761 PQFP Pin Assignments



1. Ports 6 and 7 are available only on the LXT9781.

Package Topside Markings

Marking	Definition
Part #	LXT9761 is the unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” (Refer to Specification Update for additional stepping information.)
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1. LXT97x1 RMII Signal Descriptions

9761 Pin#	9781 Pin#		Symbol	Type[1]	Signal Description[2, 3]
PQFP	PQFP	PBGA			
RMII Data Interface Pins					
92	92	Y15	REFCLK	I	**Reference Clock**. 50 MHz RMII reference clock is required at this pin. The LXT97x1 samples RMII inputs on the rising edge of REFCLK, and drives RMII outputs on the falling edge.
66 69	66 69	V7 W7	TXD0_0 TXD0_1	I	**Transmit Data - Port 0**. Inputs containing 2-bit parallel di-bits to be transmitted from port 0 are clocked in synchronously to REFCLK.
59 60	59 60	W4 V4	TXD1_0 TXD1_1	I	**Transmit Data - Port 1**. Inputs containing 2-bit parallel di-bits to be transmitted from port 1 are clocked in synchronously to REFCLK.
46 47	46 47	T2 T3	TXD2_0 TXD2_1	I	**Transmit Data - Port 2**. Inputs containing 2-bit parallel di-bits to be transmitted from port 2 are clocked in synchronously to REFCLK.
23 24	39 40	P3 P4	TXD3_0 TXD3_1	I	**Transmit Data - Port 3**. Inputs containing 2-bit parallel di-bits to be transmitted from port 3 are clocked in synchronously to REFCLK.
14 17	30 33	L3 L4	TXD4_0 TXD4_1	I	**Transmit Data - Port 4**. Inputs containing 2-bit parallel di-bits to be transmitted from port 4 are clocked in synchronously to REFCLK.
7 8	23 24	J3 J4	TXD5_0 TXD5_1	I	**Transmit Data - Port 5**. Inputs containing 2-bit parallel di-bits to be transmitted from port 5 are clocked in synchronously to REFCLK.
–	14 17	F4 G2	TXD6_0 TXD6_1	I	**Transmit Data - Port 6**. Inputs containing 2-bit parallel di-bits to be transmitted from port 6 are clocked in synchronously to REFCLK.
–	7 8	D3 D4	TXD7_0 TXD7_1	I	**Transmit Data - Port 7**. Inputs containing 2-bit parallel di-bits to be transmitted from port 7 are clocked in synchronously to REFCLK.
65 58 45 22 13 6 – –	65 58 45 38 29 22 13 6	Y5 W3 T1 P1 L2 J2 F3 D2	TXEN0 TXEN1 TXEN2 TXEN3 TXEN4 TXEN5 TXEN6 TXEN7	I	**Transmit Enable - Ports 0 - 7**. Active High input enables respective port transmitter. This signal must be synchronous to the REFCLK.
62 61	62 61	U7 U6	RXD0_0 RXD0_1	O	**Receive Data - Port 0**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
55 54	55 54	Y2 V2	RXD1_0 RXD1_1	O	**Receive Data - Port 1**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT97x1 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).
3. Ports 6 and 7 are available only on the LXT9781. These pins are not bonded out on the LXT9761.

Table 1. LXT97x1 RMII Signal Descriptions (Continued)

9761 Pin#	9781 Pin#		Symbol	Type[1]	Signal Description[2, 3]
PQFP	PQFP	PBGA			
42 41	42 41	R2 R1	RXD2_0 RXD2_1	O	**Receive Data - Port 2**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
19 18	35 34	N2 N1	RXD3_0 RXD3_1	O	**Receive Data - Port 3**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
10 9	26 25	K3 K2	RXD4_0 RXD4_1	O	**Receive Data - Port 4**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
3 2	19 18	H3 H1	RXD5_0 RXD5_1	O	**Receive Data - Port 5**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
– –	10 9	E3 E1	RXD6_0 RXD6_1	O	**Receive Data - Port 6**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
– –	3 2	C2 C1	RXD7_0 RXD7_1	O	**Receive Data - Port 7**. Receive data signals (2-bit parallel di-bits) are driven synchronously to REFCLK.
63 56 43 20 11 4 – –	63 56 43 36 27 20 11 4	V6 Y3 R3 N3 K4 H4 F1 B3	CRS_DV0 CRS_DV1 CRS_DV2 CRS_DV3 CRS_DV4 CRS_DV5 CRS_DV6 CRS_DV7	O	**Carrier Sense/Receive Data Valid - Ports 0 - 7**. On detection of valid carrier, these signals are asserted asynchronously with respect to REFCLK. CRS_DV*n* is deasserted on loss of carrier, synchronous to REFCLK.
64 57 44 21 12 5 – –	64 57 44 37 28 21 12 5	W6 V3 R4 N4 L1 J1 F2 D1	RXER0 RXER1 RXER2 RXER3 RXER4 RXER5 RXER6 RXER7	O	**Receive Error - Ports 0 - 7**. These signals are synchronous to the respective REFCLK. Active High indicates that received code group is invalid, or that PLL is not locked.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT97x1 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).
3. Ports 6 and 7 are available only on the LXT9781. These pins are not bonded out on the LXT9761.

Table 1. LXT97x1 RMII Signal Descriptions (Continued)

9761 Pin#	9781 Pin#		Symbol	Type[1]	Signal Description[2, 3]
PQFP	PQFP	PBGA			
RMII Control Interface Pins					
70	70	V8	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 8 MHz.
71	71	W8	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication.
84	84	U12	MDINT	OD	**Management Data Interrupt**. When bit 18.1 = 1, an active Low output on this pin indicates status change. Interrupt is cleared when Register 19 is read.
85	85	Y12	MDDIS	I	**Management Disable**. When MDDIS is High, the MDIO is disabled from read and write operations. When MDDIS is Low at power up or reset, the Hardware Control Interface pins control only the initial or “default” values of their respective register bits. After the power-up/ reset cycle is complete, bit control reverts to the MDIO serial channel.

1. Type Column Coding: I = Input, O = Output, OD = Open Drain
2. The LXT97x1 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an “X.Y” notation, where X is the register number (0-32) and Y is the bit number (0-15).
3. Ports 6 and 7 are available only on the LXT9781. These pins are not bonded out on the LXT9761.

Table 2. LXT97x1 Signal Detect/TP Select Signal Descriptions

9761 Pin#	9781 Pin#		Symbol	Type[1]	Signal Description[2]
PQFP	PQFP	PBGA			
101	101	V16	SD0/$\overline{\text{TP0}}$	I	**Signal Detect - Ports 0 - 7**. Tying the SD/TP*n* pins High or to a PECL input sets bit 16.0 = 1 and the respective port is forced to FX mode. In the absence of an active link, the pin must be pulled High to enable loopback in FX mode. Do not enable Auto-Negotiation if FX mode is selected. The SD/TP*n* pins have internal pull-downs. When not using FX mode, SD/TP*n* pins should be tied to GNDA. **TP Select - Ports 0 - 7**. Tying the SD/TP*n* pins Low sets bit 16.0 = 0 and forces the respective port to TP mode.
100	100	U13	SD1/$\overline{\text{TP1}}$		
99	99	U14	SD2/$\overline{\text{TP2}}$		
161	98	U15	SD3/$\overline{\text{TP3}}$		
160	162	C16	SD4/$\overline{\text{TP4}}$		
159	161	B17	SD5/$\overline{\text{TP5}}$		
–	160	A17	SD6/$\overline{\text{TP6}}$		
–	159	C17	SD7/$\overline{\text{TP7}}$		

1. Type Column Coding: I = Input, O = Output.
2. Ports 6 and 7 are available only on the LXT9781. These pins are not bonded out on the LXT9761.

Table 3. LXT97x1 Network Interface Signal Descriptions

9761 Pin#	9781 Pin#		Symbol	Type[1]	Signal Description[2]
PQFP	PQFP	PBGA			
107, 108 111, 110 121, 122 140, 139 150, 151 154, 153 – , – – , –	107, 108 111, 110 121, 122 125, 124 136, 137 140, 139 150, 151 154, 153	W19, W20 V20, V19 P19, P20 N20, N19 H19, H20 G20, G19 C19, C20 B20, B19	TPFOP0, TPFON0 TPFOP1, TPFON1 TPFOP2, TPFON2 TPFOP3, TPFON3 TPFOP4, TPFON4 TPFOP5, TPFON5 TPFOP6, TPFON6 TPFOP7, TPFON7	AO	Twisted-Pair/Fiber Outputs, Positive & Negative - Ports 0-7. During 100BASE-TX or 10BASE-T operation, TPFO pins drive 802.3 compliant pulses onto the line. During 100BASE-FX operation, TPFO pins produce differential PECL outputs for fiber transceivers.
104, 105 115, 114 118, 119 143, 142 146, 147 157, 156 – , – – , –	104, 105 115, 114 118, 119 129, 128 132, 133 143, 142 146, 147 157, 156	Y19, Y20 U20, U19 R19, R20 M20, M19 J20, J19 F20, F19 D19, D20 A20, A19	TPFIP0, TPFIN0 TPFIP1, TPFIN1 TPFIP2, TPFIN2 TPFIP3, TPFIN3 TPFIP4, TPFIN4 TPFIP5, TPFIN5 TPFIP6, TPFIN6 TPFIP7, TPFIN7	AI	Twisted-Pair/Fiber Inputs, Positive & Negative - Ports 0-7. During 100BASE-TX or 10BASE-T operation, TPFI pins receive differential 100BASE-TX or 10BASE-T signals from the line. During 100BASE-FX operation, TPFI pins receive differential PECL inputs from fiber transceivers.

1. Type Column Coding: I = Input, O = Output.
2. Ports 6 and 7 are available only on the LXT9781. These pins are not bonded out on the LXT9761.

Table 4. LXT97x1 JTAG Test Signal Descriptions

PQFP Pin#[1]	9781 PBGA Pin#	Symbol	Type[2]	Signal Description
163	D14	TDI	I, IP	**Test Data Input**. Test data sampled with respect to the rising edge of TCK.
164	C15	TDO	O	**Test Data Output**. Test data driven with respect to the falling edge of TCK.
165	B16	TMS	I, IP	**Test Mode Select**.
166	D15	TCK	I, ID	**Test Clock**. Clock input for JTAG test (REFCLK).
167	A16	$\overline{\text{TRST}}$	I, IP	**Test Reset**. Reset input for JTAG test.

1. Pin numbers apply to both the LXT9761 and the LXT9781.
2. Type Column Coding: I = Input, O = Output, IP = weak Internal Pull-up, ID = weak Internal pull-Down.

Table 5. LXT97x1 Miscellaneous Signal Descriptions

PQFP Pin#[1]	9781 PBGA Pin#	Symbol	Type[2]	Signal Description[3]
76 77	Y8 U10	TxSLEW_0 TxSLEW_1	I	**Tx Output Slew Controls 0 and 1**. These pins select the TX output slew rate (rise and fall time) as follows: **TxSLEW_1** / **TxSLEW_0** / **Slew Rate (Rise and Fall Time)** 0 / 0 / 2.5 ns 0 / 1 / 3.1 ns 1 / 0 / 3.7 ns 1 / 1 / 4.3 ns
79	W10	PAUSE	I	**Pause**. Sets the default value of bit 4.10 (PAUSE). When High, the LXT97x1 advertises Pause capabilities on all ports during auto-negotiation.
82	W12	PWRDWN	I	**Power-Down**. When High, forces the LXT97x1 into global power-down mode. Refer to "Power-Down Mode" on page 27 for more information.
83	V12	$\overline{\text{RESET}}$	I	**Reset**. This active Low input is OR'ed with the control register Reset bit (0.15). When held Low, all outputs are forced to inactive state.
97 96 95 94 93	W16 V15 V13 V14 W15	ADD_4 ADD_3 ADD_2 ADD_1 ADD_0	I I I I I	**Address <4:0>**. Sets base address. Each port adds its port number (starting with 0) to this address to determine its PHY address. Port 0 Address = Base + 0. Port 1 Address = Base + 1. Port 2 Address = Base + 2. Port 3 Address = Base + 3. Port 4 Address = Base + 4. Port 5 Address = Base + 5. Port 6 Address = Base + 6 (LXT9781 Only). Port 7 Address = Base + 7 (LXT9781 Only).
102	V17	RBIAS	AI	**Bias**. This pin provides bias current for the internal circuitry. Must be tied to ground through a 22.1 kΩ 1% resistor.
206	B4	QSTAT	O	**Quick Status**. Provides continuous PHY status updates, without the need for constant polling.
207	A3	QCLK	I	**Quick Clock**. Clock used for sending out QSTAT information. Maximum frequency is 25 MHz.

1. Pin numbers apply to both the LXT9761 and the LXT9781.
2. Type Column Coding: I = Input, O = Output, A = Analog, IP = weak Internal Pull-up, ID = weak Internal pull-Down.
3. The LXT97x1 supports the 802.3 MDIO register set. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-32) and Y is the bit number (0-15).

Table 6. LXT97x1 Power Supply Signal Descriptions

PQFP Pin#[1]	9781 PBGA Pin#	Symbol	Type	Signal Description
LXT9761/81: 80, 88, 179 **LXT9761 Only:** 86	A12, B11, B12, Y9, Y10, Y11	VCCD	-	**Digital Power Supply - Core.** +3.3V supply for core digital circuits.
15, 31, 52, 67, 193, 208	C4, D5, G1, M1, V1, Y6	VCCIO	-	**Digital Power Supply - I/O Ring.** +3.3V supply for digital I/O circuits. Regardless of the IO supply, digital I/O pins remain tolerant of 5V signal levels.
LXT9761/81: 106, 113, 120, 141, 148, 155	D17, E17, H17, J17, M17, N17, T17, U17	VCCR	-	**Analog Power Supply.** +3.3V supply for all analog receive circuits.
LXT9781 Only: 127, 134				
LXT9761/81: 112, 149 **LXT9781 Only:** 126, 135	A18, B18, E19, E20, K19, K20, L19, L20, T19, T20, W18, Y18	VCCT	-	**Analog Power Supply.** +3.3V supply for all analog transmit circuits.
LXT9761/81: 1, 16, 32, 48-51, 53, 68, 72-75, 81, 87, 89, 90, 91, 178, 192 **LXT9781 Only:** 86	A4, B2, B8, C3, C12, D11, E2, E4, G3, G4, H2, J9 - J12, K1, K9 - K12, L9 - L12, M2, M3, M4, M9 - M12, P2, T4, U5, U8, U11, V5, V11, W2, W5, W11,W13, W14, Y13, Y14, Y16, Y17	GNDD	-	**Digital Ground**. Ground return for both core and I/O digital supplies (VCCD and VCCIO). All ground pins can be tied together using a single ground plane.
103, 109, 116, 117, 123, 138, 144, 145, 152, 158 (LXT9761 and LXT9781) 130, 131 (LXT9781 Only)	C18, D16, D18, E18, F17, F18, G17, G18, H18, J18, K17, K18, L17, L18, M18, N18, P17, P18, R17, R18, T18, U16, U18, V18, W17	GNDA	-	**Analog Ground**. Ground return for analog supply. All ground pins can be tied together using a single ground plane.
78	V10	GNDS	-	**Substrate Ground**. Ground for chip substrate. All ground pins can be tied together using a single ground plane.

1. Unless otherwise noted, pin numbers apply to both the LXT9761 and the LXT9781.

Table 7. LXT97x1 LED Signal Descriptions

9761 Pin#	9781 Pin#		Symbol	Type[1]	Signal Description[2]
PQFP	PQFP	PBGA			
177 176 175 174 173 172 171 170	177 176 175 174 173 172 171 170	D12 B13 C13 A14 A13 B14 C14 A15	LEDS_0 LEDS_1 LEDS_2 LEDS_3 LEDS_4 LEDS_5 LEDS_6 LEDS_7	O	**Serial LEDs 0 - 7**. Each serial LED output indicates a particular status condition for every port. Bit 0 is assigned to Port 0, bit 1 to Port 1, etc. There are 8 possible LEDs per port, for a total of 48 display LEDs. However, typical equipment designs use no more than 3 LEDs per port, selected by the designer. Using per-event, rather than per-port outputs reduces the number of serial shift registers required. Instead of requiring an external serial-to-parallel shift register for each port, this method requires only one per LED type, reducing board space and component costs. Refer to "Serial LED Functions" on page 38 for details.
168	168	B15	LEDCLK	O	**LED Clock.** 1 MHz clock for LED serial data output.
169	169	D13	LEDLATCH	O	**LED Framing.** Framing signal for serial LED outputs.
203 204 205	203 204 205	B5 D6 C5	LED/CFG0_1 LED/CFG0_2 LED/CFG0_3	I/OD/OS	**Port 0 LED Drivers 1 -3.** These pins drive LED indicators for Port 0. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 48 on page 74 for details). **Port 0 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 29 for details).
200 201 202	200 201 202	D7 A5 C6	LED/CFG1_1 LED/CFG1_2 LED/CFG1_3	I/OD/OS	**Port 1 LED Drivers 1 -3.** These pins drive LED indicators for Port 1. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 48 on page 74 for details). **Port 1 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 29 for details).
197 198 199	197 198 199	C7 A6 B6	LED/CFG2_1 LED/CFG2_2 LED/CFG2_3	I/OD/OS	**Port 2 LED Drivers 1 -3.** These pins drive LED indicators for Port 2. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 48 on page 74 for details). **Port 2 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 29 for details).
186 187 188	194 195 196	A7 D8 B7	LED/CFG3_1 LED/CFG3_2 LED/CFG3_3	I/OD/OS	**Port 3 LED Drivers 1 -3.** These pins drive LED indicators for Port 3. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 48 on page 74 for details). **Port 3 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 29 for details).

1. Type Column Coding: I = Input, O = Output, A = Analog, OD = Open Drain, OS = Open Source.
2. Ports 6 and 7 are available only on the LXT9781. These pins are not bonded out on the LXT9761.

Table 7. LXT97x1 LED Signal Descriptions (Continued)

9761 Pin#	9781 Pin#		Symbol	Type[1]	Signal Description[2]
PQFP	PQFP	PBGA			
183 184 185	189 190 191	C8 A8 D9	LED/CFG4_1 LED/CFG4_2 LED/CFG4_3	I/OD/OS	**Port 4 LED Drivers 1 -3.** These pins drive LED indicators for Port 4. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 48 on page 74 for details). **Port 4 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 29 for details).
180 181 182	186 187 188	D10 A9 B9	LED/CFG5_1 LED/CFG5_2 LED/CFG5_3	I/OD/OS	**Port 5 LED Drivers 1 -3.** These pins drive LED indicators for Port 5. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 48 on page 74 for details). **Port 5 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 29 for details).
– – –	183 184 185	A10 B10 C9	LED/CFG6_1 LED/CFG6_2 LED/CFG6_3	I/OD/OS	**Port 6 LED Drivers 1 -3.** These pins drive LED indicators for Port 6. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 48 on page 74 for details). **Port 6 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 29 for details).
– – –	180 181 182	C11 C10 A11	LED/CFG7_1 LED/CFG7_2 LED/CFG7_3	I/OD/OS	**Port 7 LED Drivers 1 -3.** These pins drive LED indicators for Port 7. Each LED can display one of several available status conditions as selected by the LED Configuration Register (refer to Table 48 on page 74 for details). **Port 7 Configuration Inputs 1-3.** When operating in Hardware Control Mode, these pins also provide configuration control options (refer to Table 9 on page 29 for details).

1. Type Column Coding: I = Input, O = Output, A = Analog, OD = Open Drain, OS = Open Source.
2. Ports 6 and 7 are available only on the LXT9781. These pins are not bonded out on the LXT9761.

Table 8. Unused Pins

LXT9761 PQFP Pin#[1]	LXT9781 PBGA Pin#	Symbol	Type	Signal Description
25-30, 33-40, 98, 124-137, 162, 189-191, 194-196	A1,A2,B1,U1,U2,U3,U4, U9,V9,W1,W9, Y1,Y4,Y7	N/C	–	**No Connection.** These pins should be left unconnected.

1. These pins are used for the two additional ports available on the LXT9781. They are not bonded out on the LXT9761.

2.0 Functional Description

2.1 Introduction

The LXT9781 is an eight-port Fast Ethernet 10/100 Transceiver that supports 10 Mbps and 100 Mbps networks. It complies with all applicable requirements of IEEE 802.3. The LXT9781 provides a Reduced MII (RMII) for each individual network port to interface with multiple 10/100 MACs. Each port can directly drive either a 100BASE-TX line (up to 100 meters) or a 10BASE-T line (up to 185 meters). The LXT9781 also supports 100BASE-FX operation via a Pseudo-ECL (PECL) interface. The LXT9761 offers the same features and functionality in a six-port device. This data sheet uses the singular designation “LXT97x1” to refer to both devices.

2.1.1 OSP™ Architecture

Intel's LXT97x1 incorporates high-efficiency Optimal Signal Processing™ design techniques, combining the best properties of digital and analog signal processing to produce a truly optimal device.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). The result is improved receiver noise and cross-talk performance.

The OSP architecture also requires substantially less computational logic than traditional DSP-based designs. This lowers power consumption and also reduces the logic switching noise generated by DSP engines clocked at speeds up to 125 MHz. The logic switching noise can be a considerable source of EMI generated on the device’s power supplies.

The OSP-based LXT97x1 provides improved data recovery, EMI performance and power consumption.

2.1.2 Comprehensive Functionality

The LXT97x1 performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. This device also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

On power-up, the LXT97x1 reads its configuration pins to check for forced operation settings. If not configured for forced operation, each port uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT97x1 will auto-negotiate with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT97x1 will automatically detect the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and set its operating conditions accordingly.

The LXT97x1 provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

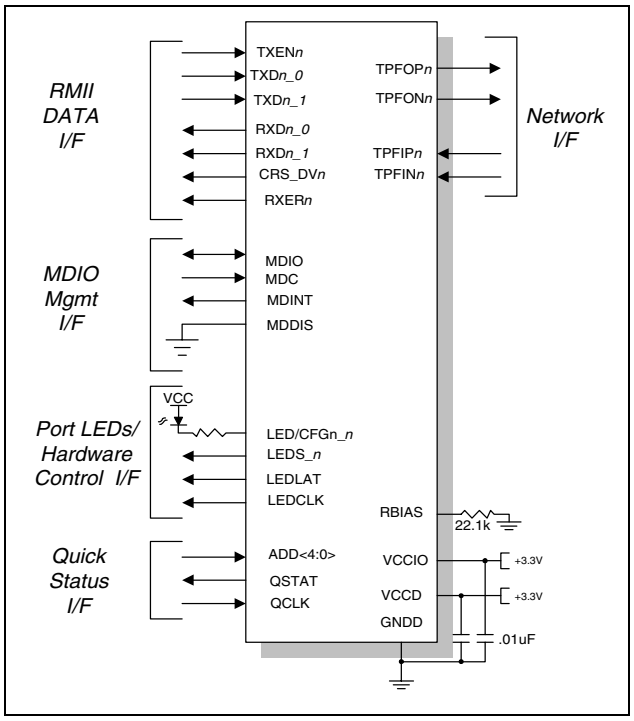
2.2 Interface Descriptions

2.2.1 10/100 Network Interface

The LXT97x1 supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX). Each network interface port consists of four external pins (two differential signal pairs). The pins are shared between twisted-pair (TP) and fiber. The LXT97x1 pinout is designed to interface seamlessly with dual-high stacked RJ45 connectors. Refer to Table 3 for specific pin assignments.

The LXT97x1 output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX output. When not transmitting data, the LXT97x1 generates 802.3-compliant link pulses or idle code. Input signals are decoded either as a 100BASE-TX, 100-BASE-FX, or 10BASE-T input, depending on the mode selected. Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

Figure 5. LXT97x1 Interfaces



2.2.1.1 Twisted-Pair Interface

When operating at 100 Mbps, MLT3 symbols are continuously transmitted and received. When not transmitting data, the LXT97x1 generates “IDLE” symbols.

During 10 Mbps operation, Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state.

The LXT97x1 supports either 100BASE-TX or 10BASE-T connections over 100Ω, Category 5, Unshielded Twisted Pair (UTP). Only a transformer, series capacitors, load resistors, RJ45 and bypass capacitors are required to complete this interface. On the receive side, the internal

impedance is high enough that it has no practical effect on the external termination circuit. On the transmit side, Intel's patented waveshaping technology shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings (refer to Table 5 on page 17) allow the designer to match the output waveform to the magnetic characteristics.

2.2.1.2 Fiber Interface

The LXT97x1 provides a PECL interface that complies with the ANSI X3.166 specification. This interface is suitable for driving a fiber-optic coupler.

Fiber ports cannot be enabled via auto-negotiation; they must be enabled via the Hardware Control Interface or MDIO registers.

2.2.2 RMII Interface

The LXT97x1 provides a separate RMII for each network port, each complying with the RMII standard. The RMII includes both a data interface and an MDIO management interface.

2.2.3 Configuration Management Interface

The LXT97x1 provides both an MDIO Management interface and a Hardware Control interface (via the LED/CFG pins) for device configuration and management. Mode control selection is provided via the MDDIS pin as shown in Table 1.

2.2.3.1 MDIO Management Interface

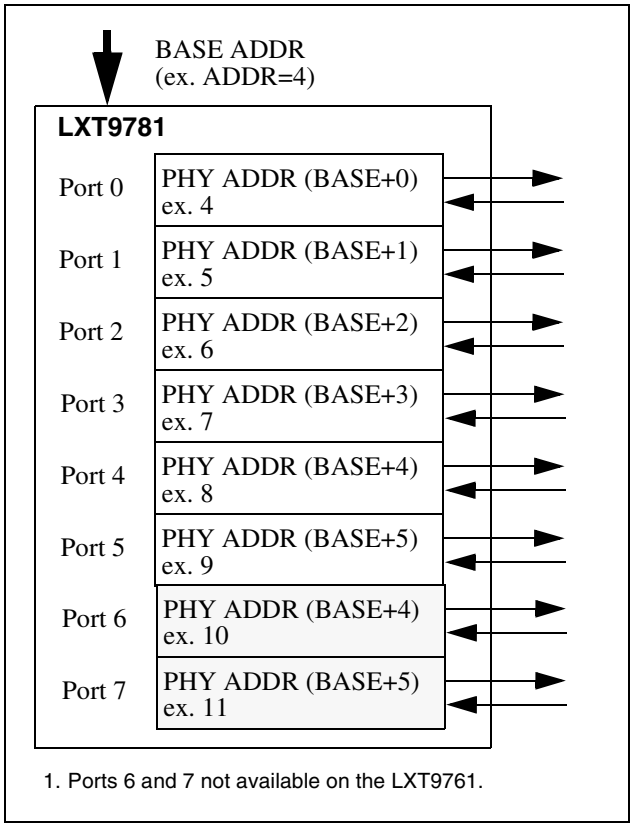
The LXT97x1 supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT97x1. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers. Some registers are required and their functions are defined by the IEEE 802.3 specification. Additional registers allow for expanded functionality. Specific bits in the registers are referenced using an "X.Y" notation, where X is the register number (0-32) and Y is the bit number (0-15).

The physical interface consists of a data line (MDIO) and clock line (MDC). Operation of this interface is controlled by the MDDIS input pin. When MDDIS is High, the MDIO read and write operations are disabled and the Hardware Control Interface provides primary configuration control. When MDDIS is Low, the MDIO port is enabled for both read and write operations and the Hardware Control Interface is not used. The timing for the MDIO Interface is shown in Table 30 on page 60. MDIO read and write cycles are shown in Figure 7 (read) and Figure 8 (write).

MII Addressing

The protocol allows one controller to communicate with multiple LXT97x1 chips. Pins ADD_<4:0> determine the base address. Each port adds its port number (0 through 5 for the LXT9761, or 0 through 7 for the LXT9781) to the base address to obtain its port address as shown in Figure 6.

Figure 6. Port Address Scheme



1. Ports 6 and 7 not available on the LXT9761.

Figure 7. Management Interface Read Frame Structure

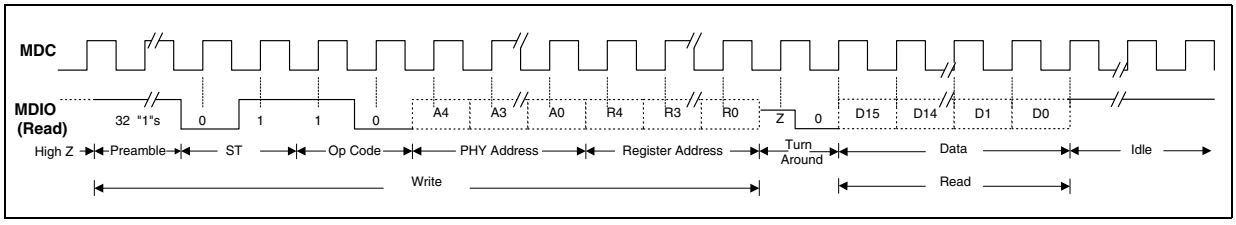
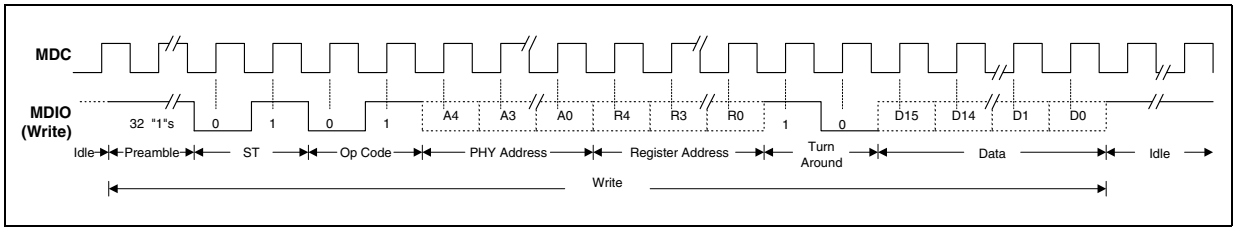


Figure 8. Management Interface Write Frame Structure



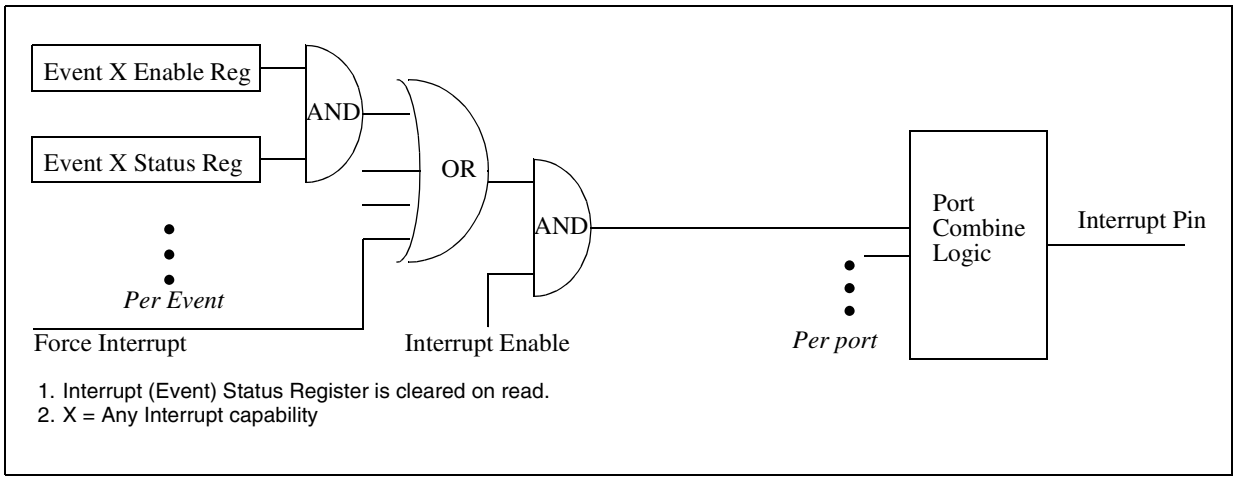
MII Interrupts

The LXT97x1 provides a single interrupt pin available to all ports. Interrupt logic is shown in Figure 9. The LXT97x1 also provides two dedicated interrupt registers for each port. Register 18 provides interrupt enable and mask functions and Register 19 provides interrupt status. Setting bit 18.1 = 1, enables a port to request interrupt via the MDINT pin. An active Low on this pin indicates a status change on the LXT97x1. However, because it is a shared interrupt, it does not indicate which port is requesting service.

Interrupts may be caused by any one of the following conditions:

- Auto-negotiation complete.
- Speed status change.
- Duplex status change.
- Link status change.

Figure 9. Interrupt Logic



2.2.3.2 Hardware Control Interface

The LXT97x1 provides a Hardware Control Interface for applications where the MDIO is not desired. The Hardware Control Interface uses the three LED driver pins for each port.

2.3 Operating Requirements

2.3.1 Power Requirements

The LXT97x1 requires four power supply inputs: VCCD, VCCT, VCCR, and VCCIO. The digital and analog circuits require 3.3 V supplies (VCCD, VCCT and VCCR). These inputs may be supplied from a single source although decoupling is required to each respective ground.

An additional supply may be used for the RMII (VCCIO). VCCIO should be supplied from the same power source used to supply the controller on the other side of the RMII interface. Refer to Table 18 on page 53 for RMII I/O characteristics.

As a matter of good practice, these supplies should be as clean as possible. Typical filtering and decoupling are shown in Figure 21 on page 47.

2.3.2 Clock Requirements

2.3.2.1 Reference Clock

The LXT97x1 requires a constant 50 MHz reference clock (REFCLK). The reference clock is used to generate transmit signals and recover receive signals. A crystal-based clock is recommended over a derived clock (i.e, PLL-based) to minmize transmit jitter. Refer to Table 19 on page 53 for clock timing requirements.

2.4 Initialization

When the LXT97x1 is first powered on, reset, or encounters a link failure state, it checks the MDIO register configuration bits to determine the line speed and operating conditions to use for the network link. The configuration bits may be set by the Hardware Control or MDIO interface as shown in Figure 10.

2.4.1 MDIO Control Mode

In the MDIO Control mode, the LXT97x1 reads the Hardware Control Interface pins to set the initial (default) values of the MDIO registers. Once the initial values are set, bit control reverts to the MDIO interface.

2.4.2 Hardware Control Mode

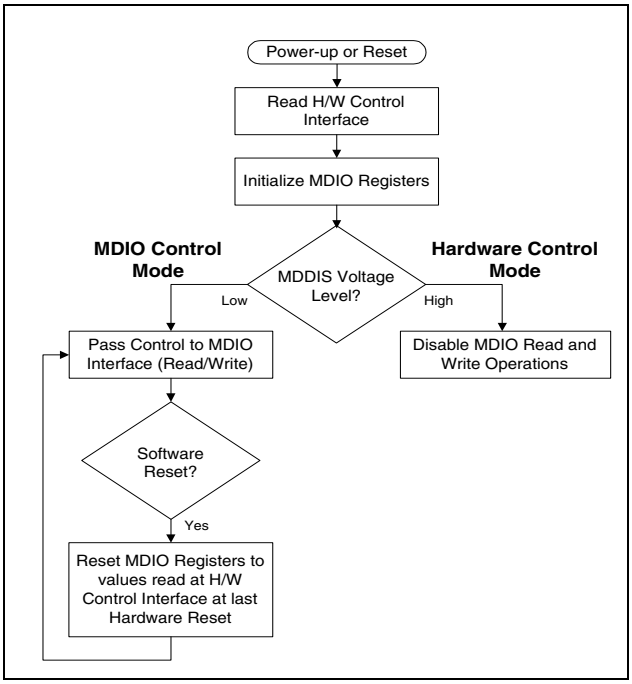
In the Hardware Control Mode, LXT97x1 disables direct write operations to the MDIO registers via the MDIO Interface. On power-up or hardware reset the LXT97x1 reads the Hardware Control Interface pins and sets the MDIO registers accordingly.

The following modes are available using either Hardware Control or MDIO Control:

- Force network link to 100FX (Fiber).
- Force network link operation to:
  100TX, Full-Duplex.
  100TX, Half-Duplex.
  10BASE-T, Full-Duplex.
  10BASE-T, Half-Duplex.
- Allow auto-negotiation / parallel-detection.

When the network link is forced to a specific configuration, the LXT97x1 immediately begins operating the network interface as commanded. When auto-negotiation is enabled, the LXT97x1 begins the auto-negotiation / parallel-detection operation.

Figure 10. Initialization Sequence



2.4.3 Power-Down Mode

The LXT97x1 offers both global and per-port power-down modes.

2.4.3.1 Global (Hardware) Power Down

The global power-down mode is controlled by PWRDWN pin 82 (PQFP) or W12 (PBGA). When PWRDWN is High, the following conditions are true:

- All LXT97x1 ports and clock are shut down.
- All outputs are tri-stated.
- All weak pad pull-up and pull-down resistors are disabled.
- The MDIO registers are not accessible.
- The MDIO registers are reset after power down.

2.4.3.2 Port (Software) Power Down

Individual port power-down control is provided by bit 0.11 in the respective port Control Registers (refer to Table 35 on page 65). During individual port power-down, the following conditions are true:

- The individual port is shut down.
- The MDIO registers remain accessible.
- The MDIO registers are unaffected.

2.4.4 Reset

The LXT97x1 provides both hardware and software resets. Configuration control of Auto-Negotiation, speed and duplex mode selection is handled differently for each. During a hardware reset, settings for bits 0.13, 0.12 and 0.8 are read in from the pins (refer to Table 9 on page 29 for pin settings and to Table 35 on page 65 for register bit definitions).

During a software reset (0.15 = 1), these bit settings are not re-read from the pins. They revert back to the values that were read in during the last hardware reset. Therefore, any changes to pin values made since the last hardware reset will not be detected during a software reset.

During a hardware reset, register information is unavailable for 1 ms after de-assertion of the reset. During a software reset (0.15 = 1) the registers are available for reading. The reset bit should be polled to see when the part has completed reset (0.15 = 0).

2.4.5 Hardware Configuration Settings

The LXT97x1 provides a hardware option to set the initial device configuration. The hardware option uses the three LED/CFG driver pins for each port. This provides three control bits per port, as listed in Table 9. The LED drivers can operate as either open drain or open source circuits as shown in Figure 11. The LED/CFG pins are sensitive to polarity and will automatically pull up or pull down to configure for either open drain or open source circuits (10 mA max current rating) as required by the hardware configuration. In applications where all ports are configured the same, several pins may be tied together with a single resistor.

Note: Auto-Negotiation must be disabled before selecting fiber operation.

Figure 11. Hardware Control Settings

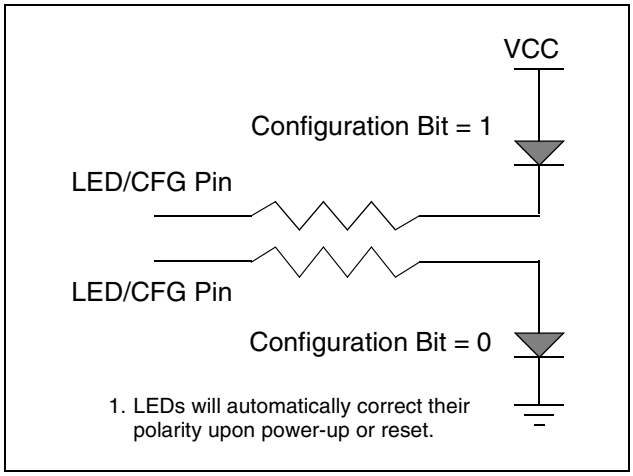


Table 9. Hardware Configuration Settings

Desired Configuration			Pin Settings			Resulting Register Bit Values						
			LED/CFG*n*_[1]			Control Register			AN Advertisement Register			
AutoNeg Mode	Speed Mode	Duplex Mode	1	2	3	AutoNeg 0.12	Speed 0.13	FD 0.8	100FD 4.8	100TX 4.7	10 FD 4.6	10T 4.5
Disabled	10	Half	0	0	0	0	0	0	X X X X [2] Auto-Negotiation Advertisement			
		Full	0	0	1			1				
	100	Half	0	1	0		1	0				
		Full	0	1	1			1				
Enabled[3]	100	Half	1	0	0	1	1	0	0	1	0	0
		Full	1	0	1			1	1			
	10/100	Half	1	1	0			0	0		0	1
		Full	1	1	1			1	1		1	

1. These pins set the default values for registers 0 and 4 accordingly.
2. X = Don't Care.
3. Do not select Fiber mode with Auto-Negotiation enabled.

2.5 Link Establishment

2.5.1 Auto-Negotiation

The LXT97x1 attempts to auto-negotiate with its counter-part across the link by sending Fast Link Pulse (FLP) bursts. Each burst consists of 33 link pulses spaced 62.5 µs apart. Odd link pulses (clock pulses) are always present. Even link pulses (data pulses) may be present or absent to indicate a "1" or a "0". Each FLP burst exchanges 16 bits of data, which are referred to as a "page". All devices that support auto-negotiation must implement the "Base Page" defined by IEEE 802.3 (registers 4 and 5). The LXT97x1 also supports the optional 'Next Page' function (registers 7 and 8).

2.5.1.1 Base Page Exchange

By exchanging Base Pages, the LXT97x1 and its link partner communicate their capabilities to each other. Both sides must receive at least three identical base pages for negotiation to proceed. Each side finds the highest common capabilities that both sides support. Both sides then exchange more pages, and finally agree on the operating state of the line.

2.5.1.2 Next Page Exchange

Additional information, above that required by base page exchange is also sent via "Next Pages'. The LXT97x1 fully supports the 802.3 method of negotiation via Next Page exchange.

2.5.1.3 Controlling Auto-Negotiation

When auto-negotiation is controlled by software, the following steps are recommended:

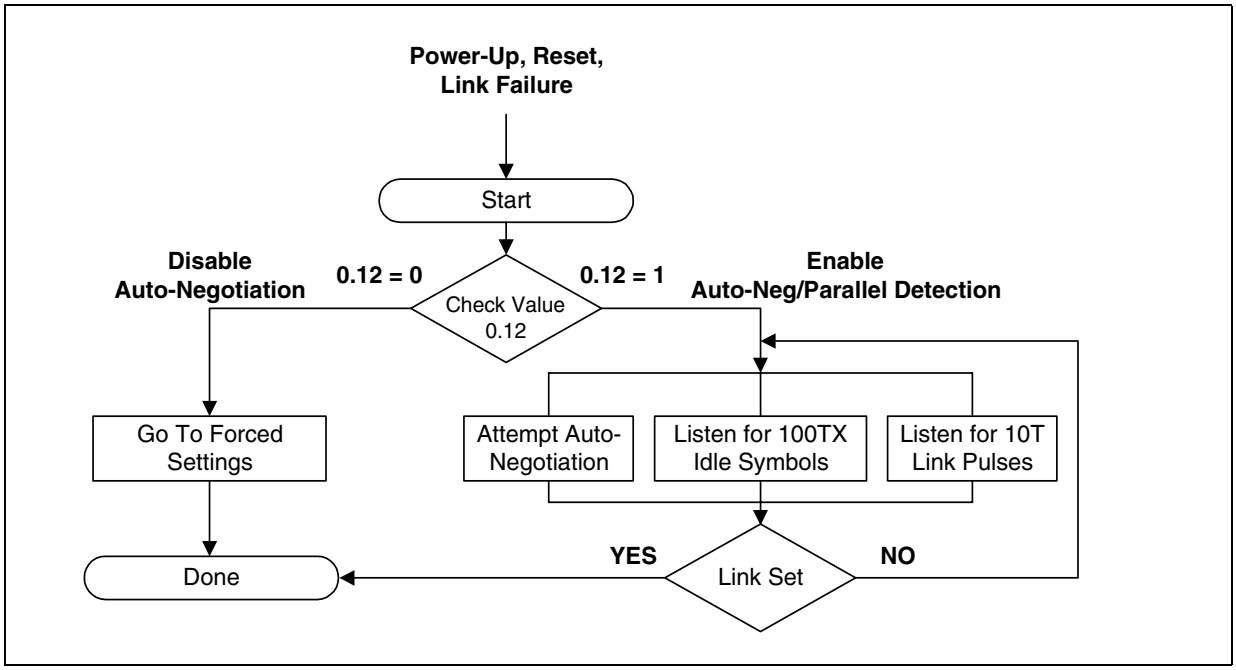
- After power-up, power-down, or reset, the power-down recovery time, (see Table 31 on page 61), must be exhausted before proceeding.
- Set the auto-negotiation advertisement bits.
- Enable auto-negotiation (set MDIO bit 0.12 = 1).

Note: Do not enable Auto-Negotiation if fiber mode is selected.

2.5.2 Parallel Detection

In parallel with auto-negotiation, the LXT97x1 also monitors for 10 Mbps Normal Link Pulses (NLP) or 100 Mbps Idle symbols. If either is detected, the device automatically reverts to the corresponding operating mode. Parallel detection allows the LXT97x1 to communicate with devices that do not support auto-negotiation.

Figure 12. Auto-Negotiation Operation



2.6 RMII Operation

The LXT97x1 provides an independent Reduced MII port for each network port. Each RMII uses four signals to pass received data to the MAC: RXD*n*<1:0>, RXER*n*, and CRS_DV*n* (where *n* reflects the port number). Three signals are used to transmit data from the MAC: TXD*n*_<1:0>, and TXEN*n*. Both Receive and transmit signals are clocked by REFCLK. Data transmission across the RMII is implemented in di-bit pairs which equal a 4-bit-wide nibble.

2.6.1 Reference Clock

The LXT97x1 requires a 50 MHz reference clock (REFCLK). The LXT97x1 samples the RMII input signals on the rising edge of REFCLK and drives RMII output signals on the falling edge.

2.6.2 Transmit Enable

TXEN*n* must be asserted and de-asserted synchronously with REFCLK. The MAC must assert TXEN*n* the same time as the first nibble of preamble. TXEN*n* must be de-asserted after the last bit of the packet.

2.6.3 Carrier Sense & Data Valid

The LXT97x1 asserts CRS_DV*n* when it detects activity on the line. However, RXD*n* outputs zeros until the received data is decoded and available for transfer to the controller.

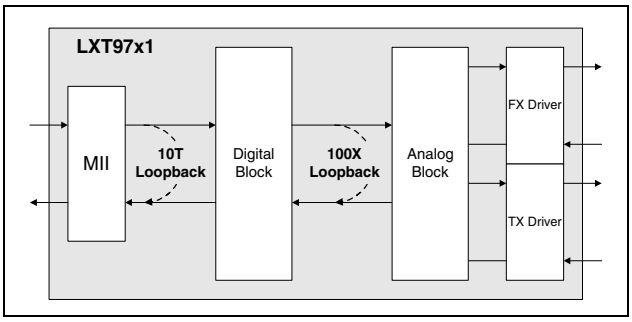
2.6.4 Receive Error

Whenever the LXT97x1 receives an errored symbol from the network, it asserts RXER*n*. When it detects a bad Start-of-Stream Delimiter (SSD) it drives a "10" jam pattern on the RXD pins to indicate a false carrier event.

2.6.5 Loopback

A test loopback function is available for 100 Mbps RMII testing. Bits 0.8, 0.13 and 0.14 must be set High for correct operation. When data is looped back, whatever the MAC transmits is looped back in its entirety, including the preamble. In FX mode, the respective SIGDET pin must be pulled High to enable loopback.

Figure 13. Loopback Paths



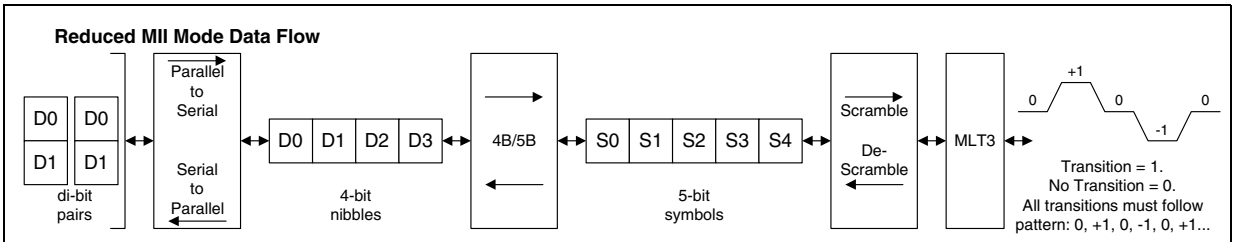
2.6.6 Out of Band Signalling

The LXT97x1 has the capability of encoding status information in the RXData stream during IPG. Refer to the section on Monitoring Operations (page 42) for details.

2.6.7 4B/5B Coding Operations

The 100BASE-X protocol specifies the use of a 5-bit symbol code on the network media. However, data is normally transmitted across the RMII interface in 2-bit nibblets or “di-bits”. The LXT97x1 incorporates a parallel/serial converter that translates between di-bit pairs and 4-bit nibbles, and a 4B/5B encoder/decoder circuit that translates between 4-bit nibbles and 5-bit symbols for the 100BASE-X connection. Figure 14 shows the data conversion flow from nibbles to symbols. Table 10 on page 34 shows 4B/5B symbol coding (not all symbols are valid).

Figure 14. RMII Data Flow



1. An independent RMII port serves each independent Network port. Network port configurations are independently selectable.
2. The Scrambler can be bypassed by setting 16.12 = 0.

2.7 100 Mbps Operation

2.7.1 100BASE-X Network Operations

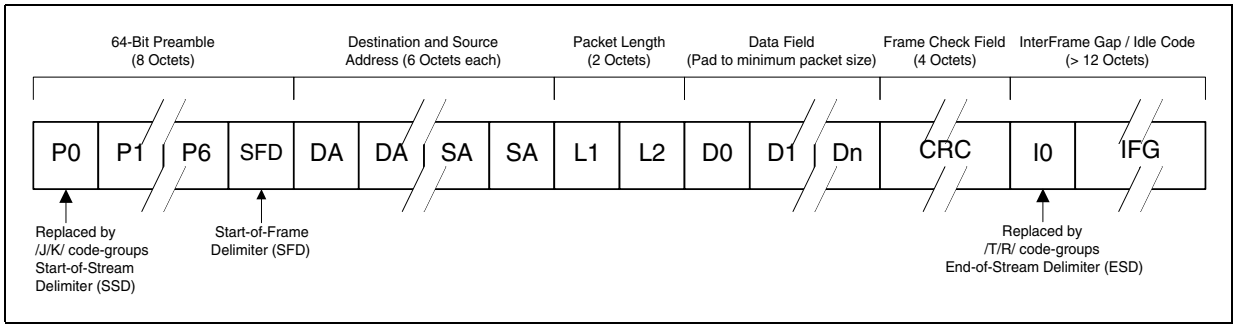
During 100BASE-X operation, the LXT97x1 transmits and receives 5-bit symbols across the network link. Figure 15 shows the structure of a standard frame packet. When the MAC is not actively transmitting data, the LXT97x1 sends out Idle symbols on the line.

In 100TX mode, the LXT97x1 scrambles the data and transmits it to the network using MLT-3 line code. The MLT-3 signals received from the network are descrambled and decoded and sent across the RMII to the MAC.

In 100FX mode, the LXT97x1 transmits and receives NRZI signals across the PECL interface. An external 100FX transceiver module is required to complete the fiber connection.

As shown in Figure 15, the MAC starts each transmission with a preamble pattern. As soon as the LXT97x1 detects the start of preamble, it transmits a J/K Start of Stream Delimiter (SSD) symbol to the network. It then encodes and transmits the rest of the packet, including the balance of the preamble, the Start of Frame Delimiter (SFD), packet data, and CRC. Once the packet ends, the LXT97x1 transmits the T/R End of Stream Delimiter (ESD) symbol and then returns to transmitting Idle symbols.

Figure 15. 100BASE-X Frame Format



2.7.2 100BASE-X Protocol Sublayer Operations

With respect to the 7-layer communications model, the LXT97x1 is a Physical Layer 1 (PHY) device. The LXT97x1 implements the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) sublayers of the reference model defined by the IEEE 802.3u specification. The following paragraphs discuss LXT97x1 operation from the reference model point of view.

2.7.2.1 PCS Sublayer

The Physical Coding Sublayer (PCS) provides the RMII interface, as well as the 4B/5B encoding/ decoding function.

For 100TX and 100FX operation, the PCS layer provides IDLE symbols to the PMD-layer line driver as long as TXEN is de-asserted.

For 10T operation, the PCS layer merely provides a bus interface and serialization/de-serialization function. 10T operation does not use the 4B/5B encoder.

Preamble Handling

When the MAC asserts TXEN, the PCS substitutes a /J/K symbol pair, also known as the Start of Stream Delimiter (SSD), for the first two nibbles received across the RMII. The PCS layer continues to encode the remaining RMII data, following Table 10 on page 34, until TXEN is de-asserted. It then returns to supplying IDLE symbols to the line driver.

In the receive direction, the PCS layer performs the opposite function, substituting two preamble nibbles for the SSD.

Dribble Bits

The LXT97x1 handles dribbles bits in all modes. If between 1-4 dribble bits are received, the nibble will be passed across the RMII. If between 5-7 dribble bits are received, the second nibble will not be sent onto the RMII bus.

Figure 16. Protocol Sublayers

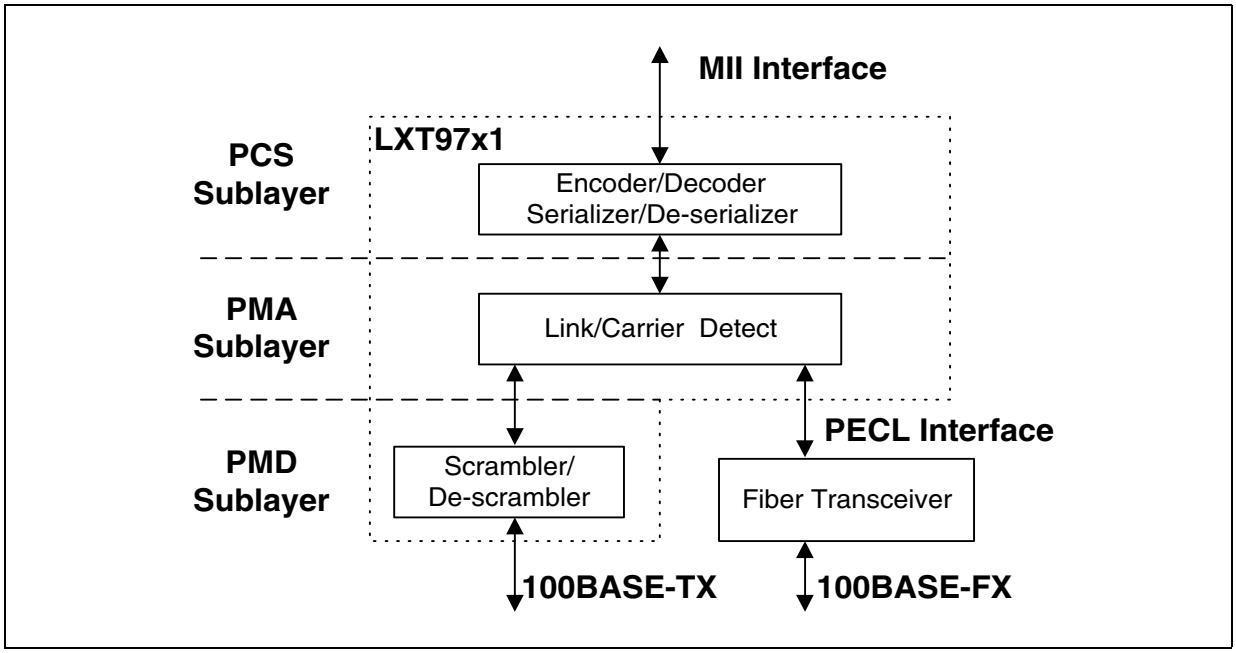


Table 10. 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
DATA	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

Table 10. 4B/5B Coding (Continued)

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
IDLE	undefined	I [1]	1 1 1 11	Idle. Used as inter-stream fill code
	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
CONTROL	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (ESD), part 1 of 2
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (ESD), part 2 of 2
	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	undefined	Invalid	0 0 0 0 0	Invalid
	undefined	Invalid	0 0 0 0 1	Invalid
	undefined	Invalid	0 0 0 1 0	Invalid
INVALID	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 0 1 1 0	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

2.7.2.2 PMA Sublayer

Link

In 100Mbps mode, the LXT97x1 establishes a link whenever the scrambler becomes locked and remains locked for approximately 50 ms. Whenever the scrambler loses lock (<12 consecutive idle symbols during a 2 ms window), the link will be taken down. This provides a very robust link, essentially filtering out any small noise hits that may otherwise disrupt the link. Furthermore 100M idle patterns will not bring up a 10M link.

The LXT97x1 reports link failure via the RMII status bits (1.2, 17.10, and 19.4) and interrupt functions. If auto-negotiate is enabled, link failure causes the LXT97x1 to re-negotiate.

Link Failure Override

The LXT97x1 will normally transmit 100 Mbps data packets or Idle symbols only if it detects the link is up, and transmits only FLP bursts if the link is not up. Setting bit 16.14 = 1 overrides this function, allowing the LXT97x1 to transmit data packets even when the link is down. This feature is provided as a diagnostic tool. Note that auto-negotiation must be disabled to transmit data packets in the absence of link. If auto-negotiation is enabled, the LXT97x1 will automatically begin transmitting FLP bursts if the link goes down.

Carrier Sense/Data Valid

The LXT97x1 asserts CRS_DV whenever the respective port receiver is non-idle (as defined by the RMII Specification Revision 1.2), including false carrier events. Assertion of CRS_DV is asynchronous with respect to REFCLK. In the event that signal decoding is not complete when CRS_DV is asserted, the LXT97x1 outputs 00 on the RXD1:0 lines until the decoded data is available.

When the line returns to an idle state CRS_DV is de-asserted, asynchronously with respect to REFCLK. In the event that the FIFO still contains data to be passed to the MAC via the RMII when CRS is de-asserted, CRS_DV will toggle on nibble boundaries until the FIFO is empty. For 100BASE-X signals, CRS_DV toggles at 25 MHz. For 10BASE-T signals, CRS_DV toggles at 2.5 MHz.

2.7.2.3 Twisted-Pair PMD Sublayer

The twisted-pair Physical Medium Dependent (PMD) layer provides the signal scrambling and descrambling, line coding and decoding (MLT-3 for 100TX, Manchester for 10T), as well as receiving, polarity correction, and baseline wander correction functions.

Scrambler/Descrambler (100TX Only)

The purpose of the scrambler is to spread the signal power spectrum and further reduce EMI using an 11-bit, non-data-dependent polynomial. The receiver automatically decodes the polynomial whenever IDLE symbols are received.

The scrambler/descrambler can be bypassed by setting bit 16.12 = 1. The scrambler is automatically bypassed when the fiber port is enabled. Scramber bypass is provided for diagnostic and test support.

Baseline Wander Correction (100TX Only)

The LXT97x1 provides a baseline wander correction function which makes the device robust under all network operating conditions. The MLT3 coding scheme used in 100BASE-TX is by definition “unbalanced”. This means that the DC average value of the signal voltage can “wander” significantly over short time intervals (tenths of seconds). This wander can cause receiver errors, particularly in less robust designs, at long line lengths (100 meters). The exact characteristics of the wander are completely data dependent.

The LXT97x1 baseline wander correction characteristics allow the device to recover error-free data while receiving worst-case “killer” packets over all cable lengths.

Polarity Correction

The LXT97x1 automatically detects and corrects for the condition where the receive signal (TPFIP/N) is inverted. Reversed polarity is detected if eight inverted link pulses, or four inverted End-of-Frame (EOF) markers, are received consecutively. If link pulses or data are not received by the maximum receive time-out period, the polarity state is reset to a non-inverted state.

2.7.2.4 Fiber PMD Sublayer

The LXT97x1 provides a PECL interface for connection to an external fiber-optic transceiver. (The external transceiver provides the PMD function for fiber media.) The LXT97x1 uses an NRZI format and operates at 100 Mbps. The LXT97x1 does not support 10FL applications.

Signal Fault Indications

The LXT97x1 Signal Detect pins receive signal fault indications from local fiber transceivers via the SD pins. The device can also detect far end fault code in the received data stream. The LXT97x1 "ORs" both fault conditions to set bit 1.4. Bit 1.4 is set once and clears when read.

Either fault condition causes the LXT97x1 to drop the link unless Forced Link Pass is selected (16.14 = 1). Link down condition is then reported via interrupts and status bits.

In response to locally detected signal faults (SD activated by the local fiber transceiver), the affected port can transmit the far end fault code if fault code transmission is enabled by bit 16.2.

- When bit 16.2 = 1, transmission of the far end fault code is enabled. The LXT97x1 transmits far end fault code if fault conditions are detected by the Signal Detect pins.
- When bit 16.2 = 0, the LXT97x1 does not transmit far end fault code. It continues to transmit idle code and may or may not drop link depending on the setting for bit 16.14.

2.8 10 Mbps Operation

The LXT97x1 will operate as a standard 10BASE-T transceiver and supports all the standard 10 Mbps functions.

During 10BASE-T (10T) operation, the LXT97x1 transmits and receives Manchester-encoded data across the network link. When the MAC is not actively transmitting data, the LXT97x1 sends out link pulses on the line.

In 10T mode, the polynomial scrambler/descrambler is inactive. Manchester-encoded signals received from the network are decoded by the LXT97x1 and sent across the RMII to the MAC. The 10M reversed polarity correction function is the same as the 100M function described on page 36.

The LXT97x1 does not support fiber connections at 10 Mbps.

2.8.1 Preamble Handling

The LXT97x1 offers two options for preamble handling, selected by bit 16.5. In 10T Mode when 16.5 = 0, the LXT97x1 strips the entire preamble off of received packets. CRS_DV is asserted coincident with SFD. CRS_DV is held Low for the duration of the preamble. When CRS_DV is asserted, the very first two nibbles driven by the LXT97x1 are the SFD "5D" hex followed by the body of the packet.

In 10T mode with 16.5 = 1, the LXT97x1 passes the preamble through the RMII and asserts CRS_DV simultaneously.

2.8.2 Dribble Bits

The LXT97x1 device handles dribbles bits in all modes. If between 1-4 dribble bits are received, the nibble will be passed across the RMII, padded with 1s if necessary. If between 5-7 dribble bits are received, the second nibble will not be sent onto the RMII bus.

2.8.3 Link Test

In 10T mode, the LXT97x1 always transmit link pulses. If the link test function is enabled, it monitors the connection for link pulses. Once link pulses are detected, data transmission will be enabled and will remain enabled as long as either the link pulses or data transmission continue. If the link pulses stop, the data transmission will be disabled.

If the link test function is disabled, the LXT97x1 will transmit to the connection regardless of detected link pulses. The link test function can be disabled by setting bit 16.14 = 1.

2.8.3.1 Link Failure

Link failure occurs if Link Test is enabled and link pulses or packets stop being received. If this condition occurs, the LXT97x1 returns to the auto-negotiation phase if auto-negotiation is enabled.

2.8.4 Jabber

If a transmission exceeds the jabber timer, the LXT97x1 will disable the transmit and loopback functions. The RMII does not include a Jabber pin, however the MAC may read Register 1 to determine Jabber status.

The LXT97x1 automatically exits jabber mode after the unjab time has expired. This function can be disabled by setting bit 16.10 = 1.

2.9 Monitoring Operations

2.9.1 Monitoring Auto-Negotiation

Auto-negotiation can be monitored as follows:

- Bits 1.2 and 17.10 = 1 once the link is established.
- Additional bits in Register 1 (refer to Table 36 on page 65) and Register 17 (refer to Table 45 on page 71) can be used to determine the link operating conditions and status.

2.9.2 Serial LED Functions

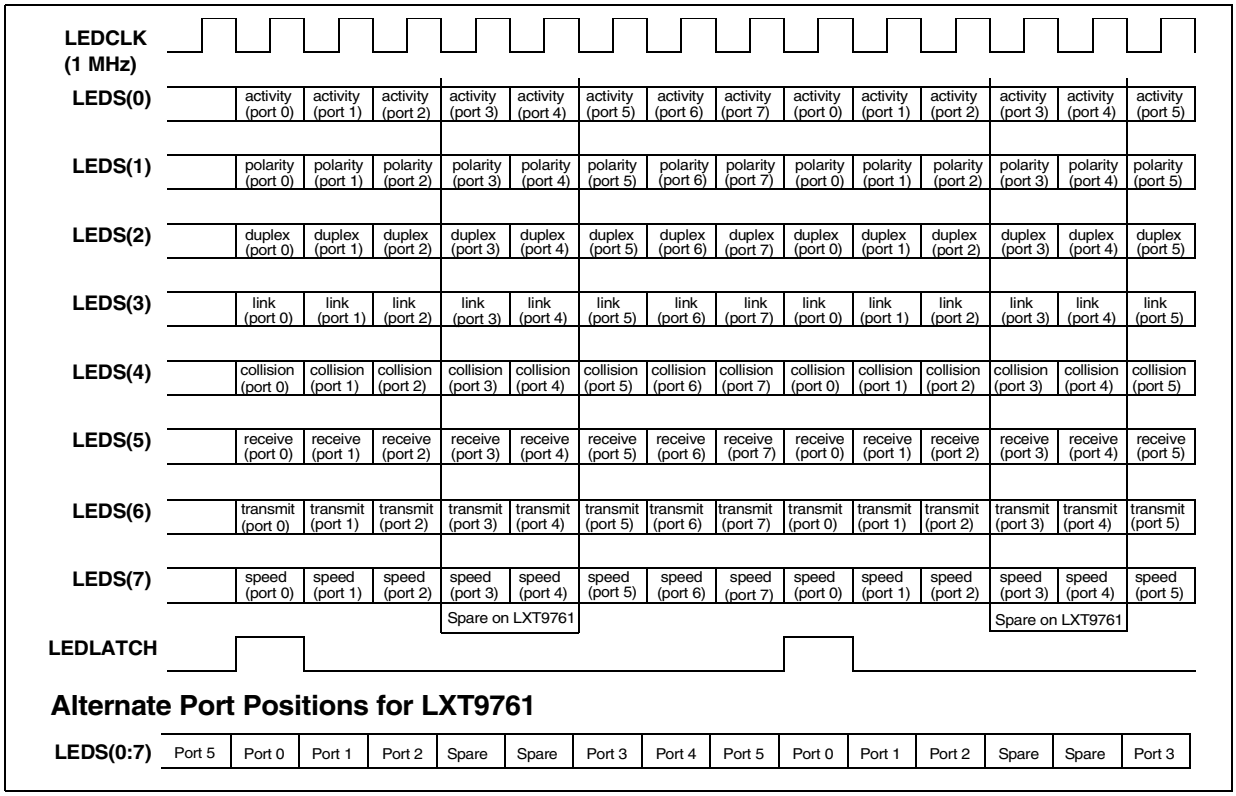
The LXT97x1 provide eight serial LED outputs (LEDS7:0) which may be attached to external HC595-type shift registers (refer to Figure 25 on page 51). The LEDCLK signal is used to shift data into the 595's internal shift register. The LEDLATCH signal is used to load data from the 595's internal shift register to the 595's internal storage register. The LXT97x1 drives the LEDS*n* and LEDLATCH outputs on the falling edge of LEDCLK. All serial LEDs will be stretched in accordance with 20.1 & 20.3:2.

Each serial output reports a specific status condition for all ports. Ports 0 through 7 are assigned bits 0:7 in each stream (bits 3 and 4 are not used on the LXT9761).

Serial outputs report the following conditions for each port:

- LEDS0 Serial Output indicates Activity.
  0 = Active1 = Inactive
- LEDS1 Serial Output indicates Polarity
  0 = Switched Polarity1 = Normal Polarity
- LEDS2 Serial Output indicates Duplex (D).
  0 = Full Duplex1 = Half Duplex
- LEDS3 Serial Output indicates Link.
  0 = Link active1 = Link inactive
- LEDS4 Serial Output indicates Collision.
  0 = Collision active1 = Collision inactive
- LEDS5 Serial Output indicates Receive.
  0 = Receive active1 = Receive inactive
- LEDS6 Serial Output indicates Transmit.
  0 = Transmit active1 = Transmit inactive
- LEDS7 Serial Output indicates Speed.
  0 = 100 Mbps1 = 10 Mbps

Figure 17. Serial LED Streams



2.9.3 Per-Port LED Driver Functions

The LXT97x1 incorporates three direct drive LEDs per port. On power up all the LEDs will light for approximately 1 second after reset de-asserts. Each LED can be programmed to one of several different display modes using the LED Configuration Register. Each per-port LED can be programmed (refer to Table 48 on page 74) to indicate one the following conditions:

- Operating Speed.
- Transmit Activity.
- Receive Activity.
- Collision Condition.
- Link Status.
- Duplex Mode.

The LEDs can also be programmed to display various combined status conditions. For example, setting bits 20.15:12 = 1101 produces the following combination of Link and Activity indications:

- If Link is down LED is off.
- If Link is up LED is on.
- If Link is up AND activity is detected, the LED will blink at the stretch interval selected by bits 20.3:2 and will continue to blink as long as activity is present.

The LED/CFG driver pins are also used to provide initial configuration settings. The LED pins are sensitive to polarity and will automatically pull up or pull down to configure for either open drain or open source circuits (10mA max current rating) as required by the hardware configuration. Refer to the discussion of "Hardware Control Interface" on page 25 for details.

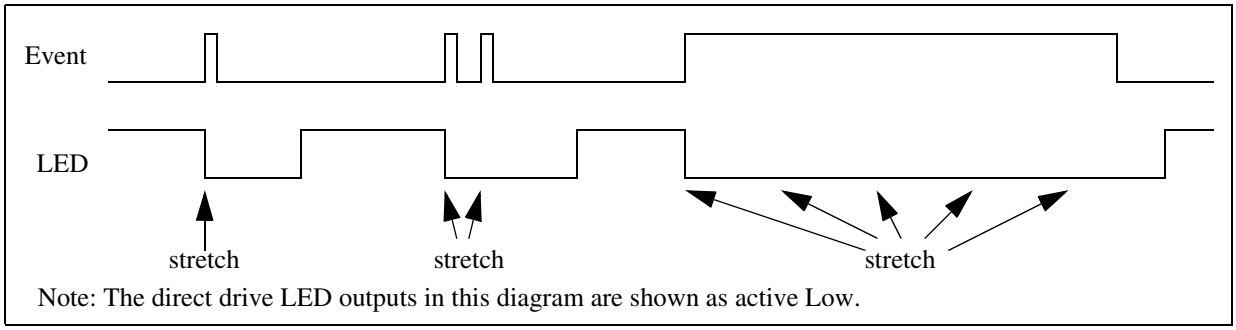
2.9.3.1 LED Pulse Stretching

The LED Configuration Register also provides optional LED pulse stretching to 30, 60, or 100 ms. If during this pulse stretch period, the event occurs again, the pulse stretch time will be further extended.

When an event such as receiving a packet occurs it will be edge detected and it will start the stretch timer. The LED driver will remain asserted until the stretch timer expires. If another event occurs before the stretch timer expires then the stretch timer will be reset and the stretch time will be extended.

When a long event (such as duplex status) occurs it will be edge detected and it will start the stretch timer. When the stretch timer expires the edge detector will be reset so that a long event will cause another pulse to be generated from the edge detector which will reset the stretch timer and cause the LED driver to remain asserted. Figure 18 shows how the stretch operation functions.

Figure 18. LED Pulse Stretching



2.9.4 Using the Quick Status Register

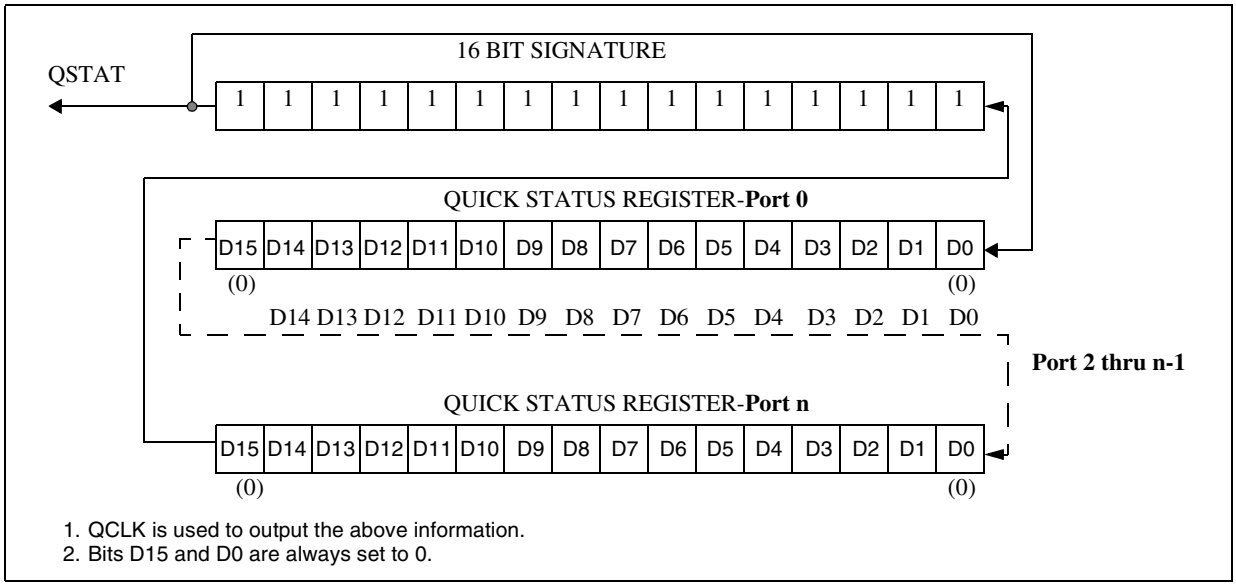
The LXT97x1 continuously sends out the Quick Status Register (Address 17) contents on the QSTAT pin.

This output provides a continuous, real-time status update of several different LXT97x1 attributes and modes. The information can be used to sense RX, TX, COL and to monitor the status and speed of the auto-negotiation process.

A simple signature is used to delineate the start of the QSTAT register information allowing a very simple interface to be designed. The 16 bits of the Quick Status Register are separated by a 16-bit signature frame (1111111111111111).

The LXT97x1 sources this status information separated by the signature with respect to the falling edge of the QCLK input. This allows an ASIC to provide only 1 clock output for multiple PHY devices. The ASIC can also select a frequency up to 25 MHz to operate this interface. Refer to Table 45 on page 71 for Quick Status bits descriptions.

Figure 19. Quick Status Register



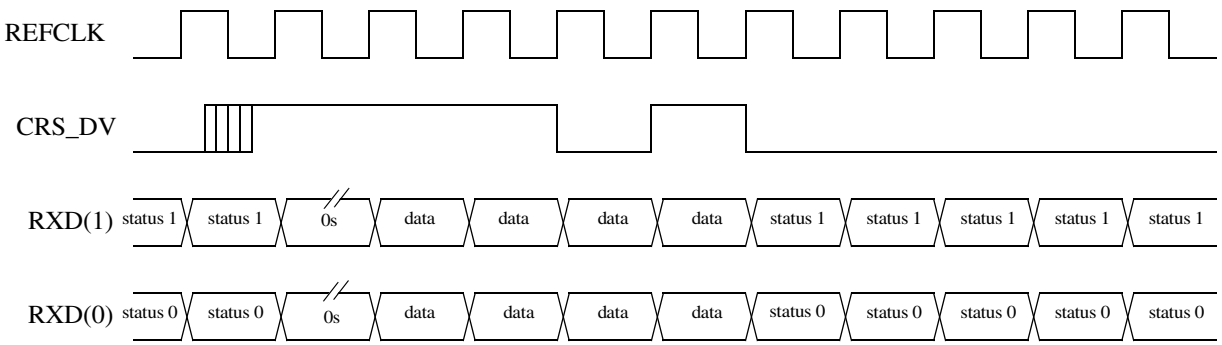
2.9.5 Out-of-Band Signalling

The LXT97x1 provides an out-of-band signalling option to transfer status information across the RMII receive interface. Enabled when 25.0=1, this feature uses the RXD(1:0) data bus during the IPG time as shown in Figure 20.

The two status bits that are transferred across the RXD bus are software selectable via Register 25 (refer to Table 49 on page 75).

In normal operation the LXT97x1 stuffs the RXD bus with zeros during the Inter-Packet Gap (IPG). A software-selectable bit enables the RMII out of band signalling feature. Once this bit is set the LXT97x1 replaces those zeros with the selected status bits during the IPG.

Figure 20. RMII Programmable Out of Band Signalling



1. When network activity is detected, the LXT97x1 asserts CRS_DV asynchronously with respect to REFCLK.
2. After CRS_DV is asserted, the LXT97x1 will zero-stuff the RXData bits until the received data has been processed through the FIFO.
3. When network activity ceases, the LXT97x1 de-asserts CRS_DV synchronously with respect to REFCLK. CRS_DV will toggle until all data in the FIFO has been processed through the RMII. Once the FIFO is empty, the LXT97x1 will drive the status bits selected by the Out-of-Band Signalling Register (refer to Table 49 on page 75) on the RXD outputs.

2.10 Boundary Scan (JTAG1149.1) Functions

The LXT97x1 includes a IEEE 1149.1 boundary scan test port for board level testing. All digital input, output, and input/output pins are accessible.

2.10.1 Boundary Scan Interface

This interface consists of five pins (TMS,TDI,TDO, TCK and TRST). It includes a state machine, data register array, and instruction register. The TMS and TDI pins are internally pulled up. TCK is internally pulled down. TDO does not have an internal pull-up or pull-down.

2.10.2 State Machine

The TAP controller is a 16 Bit state machine driven by the TCK and TMS pins. Upon reset the TEST_LOGIC_RESET state is entered. The state machine is also reset when TMS is high for five TCK periods.

2.10.3 Instruction Register

After the state machine resets, the IDCODE instruction is always invoked. The decode logic ensures the correct data flow to the Data registers according to the current instruction. Valid instructions are listed in Table 12.

2.10.4 Boundary Scan Register

Each BSR cell has two stages. A flip-flop and a latch are used for the serial shift stage and the parallel output stage. There are four modes of operation as listed in Table 11.

Table 11. BSR Mode of Operation

Mode	Description
1	Capture
2	Shift
3	Update
4	System Function

Table 12. Supported JTAG Instructions

Name	Code	Description	Data Register
EXTEST	0000000000000000	External Test	BSR
IDCODE	1111111111111110	ID Code Inspection	ID REG
SAMPLE	1111111111111110	Sample Boundary	BSR
High Z	1111111111001111	Force Float	Bypass
Clamp	1111111111101111	Clamp	BSR
BYPASS	1111111111111111	Bypass Scan	Bypass

Table 13. Device ID Register

31:28	27:12	11:8	7:1	0
Version	**Part ID (hex)**	**Jedec Continuation Characters**	**JEDEC ID[1]**	**Reserved**
0000	2621 (LXT9761) 2635 (LXT9781)	0000	111 1110	1

1. The JEDEC ID is an 8-bit identifier. The MSB is for parity and is ignored. Intel's JEDEC ID is FE (1111 1110) which becomes 111 1110.

3.0 Application Information

3.1 Design Recommendations

The LXT97x1 is designed to comply with IEEE requirements and to provide outstanding receive Bit Error Rate (BER) and long-line-length performance. To achieve maximum performance from the LXT97x1, attention to detail and good design practices are required. Refer to the LXT97x1 Design and Layout Guide for detailed design and layout information.

3.1.1 General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to 50 mV of noise is considered acceptable. 50 to 80 mV of noise is considered marginal. High-frequency switching noise can be reduced, and its effects can be eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of .01 µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT97x1 and the RJ45 connectors at the edge of the board.
- Do not extend any circuit power and ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

3.1.2 Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane can cause EMI problems and degrade line performance. The best approach is to minimize ground noise as much as possible using good general techniques and by filtering the VCC plane. It is generally difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having problems:

- Poorly-regulated or over-burdened power supplies
- Wide data busses (32-bits+) running at a high clock rate
- DC-to-DC converters

Intel recommends filtering the power supply to the analog VCC pins of the LXT97x1. This has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT97x1, which helps line performance. Second, if the VCC planes are laid out correctly, it keeps digital switching noise away from external connectors, reducing EMI problems.

The recommended implementation is to break the VCC plane into two sections. The digital section supplies power to the VCCD and VCCIO pins of the LXT97x1. The analog section supplies power to the VCCA pins. The break between the two planes should run underneath the device. In designs with more than one LXT97x1, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. Beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. A bulk cap (2.2 -10 uF) should be place on each side of each bead.

In addition, a high-frequency bypass cap (.01uf) should be placed near each analog VCC pin.

3.1.3 Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes.

- Follow the guidelines in the *LXT97x1 Design and Layout Guide* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPFOP/N and TPFIP/N signals, away from the magnetics, and away from the RJ45 connectors.
- Place the layers so that the TPFOP/N and TFPIP/N signals can be routed near or next to the ground plane. For EMI reasons, it is more important to shield TPFOP/N than TPFIP/N.

3.1.3.1 Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ-45 connectors to the magnetics, and can be used to terminate unused signal pairs (‘Bob Smith’ termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2kV isolation to the Bob Smith termination.

3.1.4 RMII Terminations

Series termination resistors are not typically required on the RMII signals driven by the LXT97x1.

3.1.5 The RBIAS Pin

The LXT97x1 requires a 22.1 kΩ, 1% resistor directly connected between the RBIAS pin and ground. Place the RBIAS resistor as close to the RBIAS pin as possible. Run an etch directly from the pin to the resistor, and sink the other side of the resistor to a filtered ground. Surround the RBIAS trace with a filtered ground; do not run high-speed signals next to RBIAS.

3.1.6 The Twisted-Pair Interface

Follow standard guidelines for a twisted-pair interface:

- Place the magnetics as close as possible to the LXT97x1.
- Keep transmit pair traces as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- Route the transmit pair adjacent to a ground plane. The optimum arrangement is to place the transmit traces two to three layers from the ground plane, with no intervening signals.
- Improve EMI performance by filtering the TPO center tap. A single ferrite bead may be used to supply center tap current to all ports. All ports draw a combined total of 505 mA so the bead should be rated at 760 mA.

3.1.6.1 Magnetics Information

The LXT97x1 requires a 1:1 ratio for the receive transformers and a 1:1 ratio for the transmit transformers. The transformer isolation voltage should be rated at 1.5 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 14 for transformer requirements. Before committing to a specific component, designers should contact the manufacturer for current product specifications, and validate the magnetics for the specific application.

3.1.7 The Fiber Interface

The fiber interface consists of a PECL transmit and receive pair to an external fiber-optic transceiver. The transmit and receive pair should be DC-coupled to the transceiver, and biased appropriately. Refer to the fiber transceiver manufacturer's recommendations for termination circuitry. Figure 23 on page 49 shows a typical example.

Table 14. Magnetics Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	
Tx turns ratio	–	1 : 1	–	–	
Insertion loss	0.0	0.6	1.1	dB	
Primary inductance	350	–	–	µH	
Transformer isolation	–	1.5	–	kV	
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz

3.2 Typical Application Circuits

Figure 21 through Figure 25 show typical application circuits.

Figure 21. Power and Ground Supply Connections

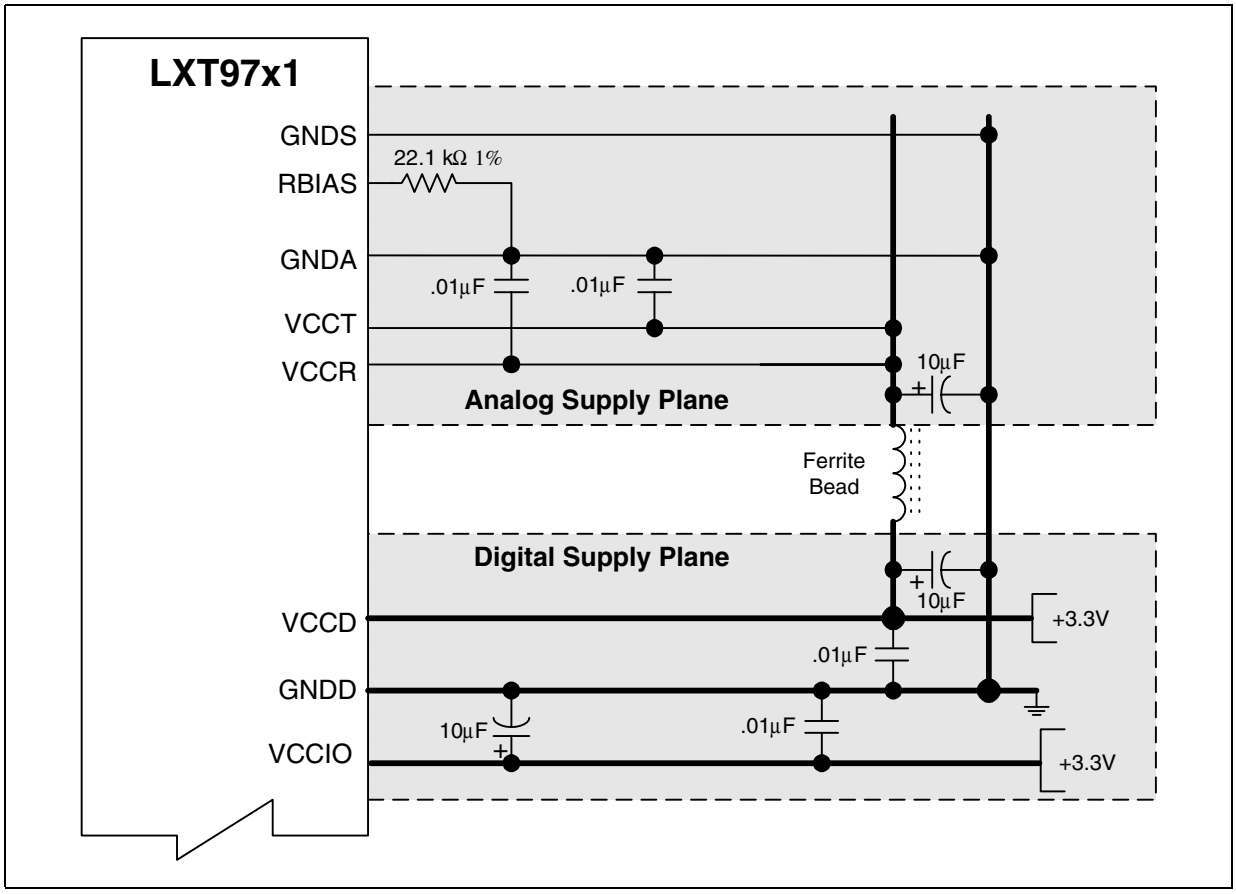
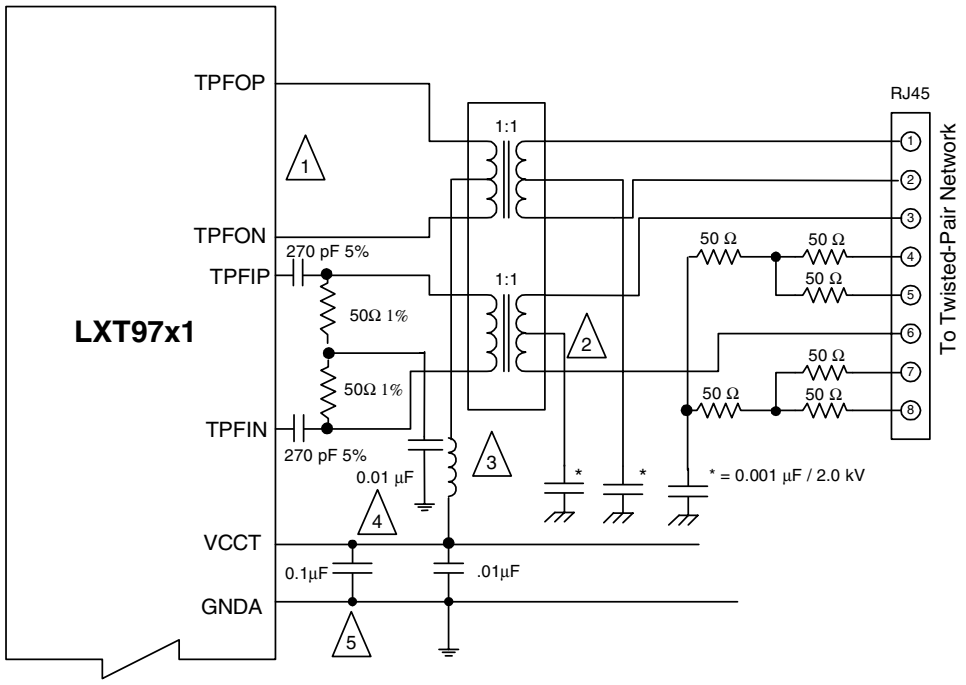
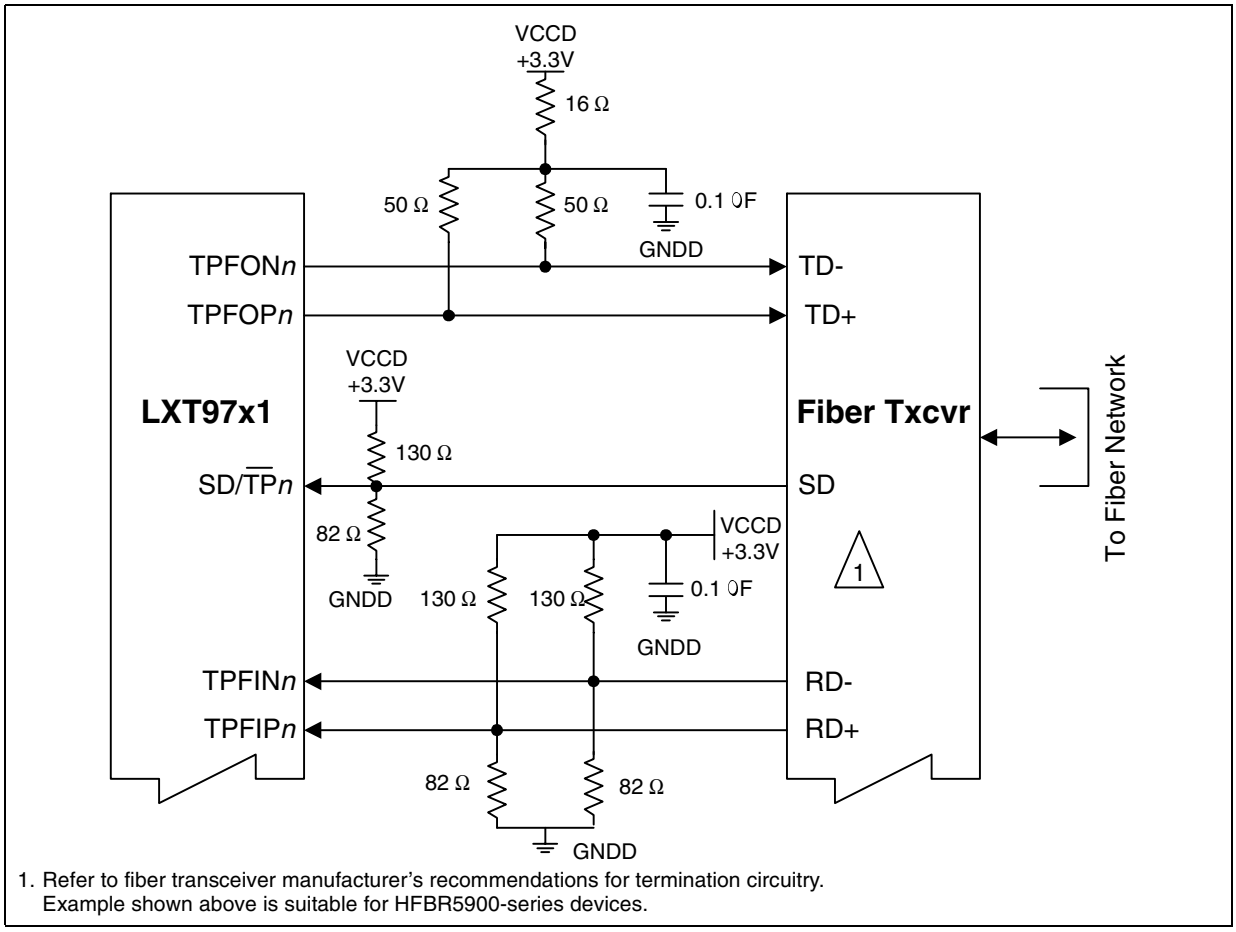


Figure 22. Typical Twisted-Pair Interface



1. The 100Ω transmit load termination resistor typically required is integrated in the LXT97xx.
2. Magnetics without a receive pair center-tap do not require a 2 kV termination.
3. Center tap current may be supplied from 3.3V VCCA as shown. However, additional power savings may be realized by supplying the center-tap from from a 2.5V current source. In either case a single ferrite bead (rated at 800 mA) may be used to supply center tap current to all ports.
4. Receive common mode bypass cap may improve BER performance in systems with noisy power supplies.
5. Recommended 0.1µF capacitor to improve the EMI performance.

Figure 23. Typical Fiber Interface



1. Refer to fiber transceiver manufacturer's recommendations for termination circuitry. Example shown above is suitable for HFBR5900-series devices.

Figure 24. Typical RMII Interface

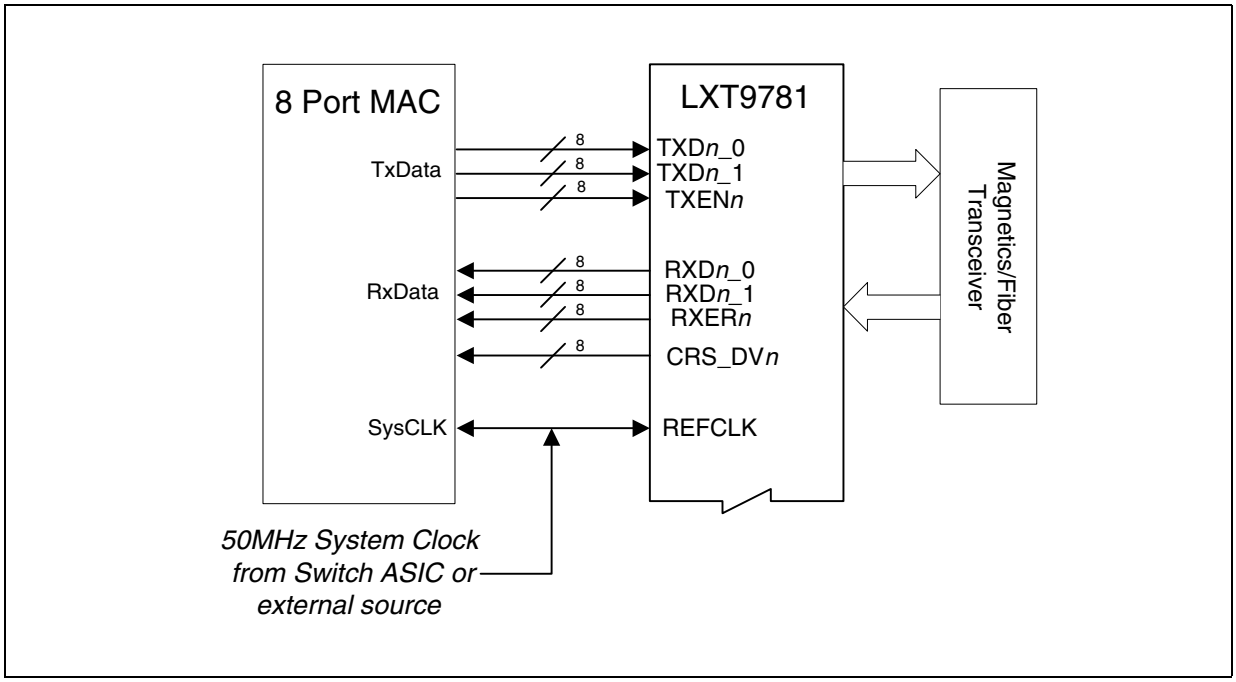
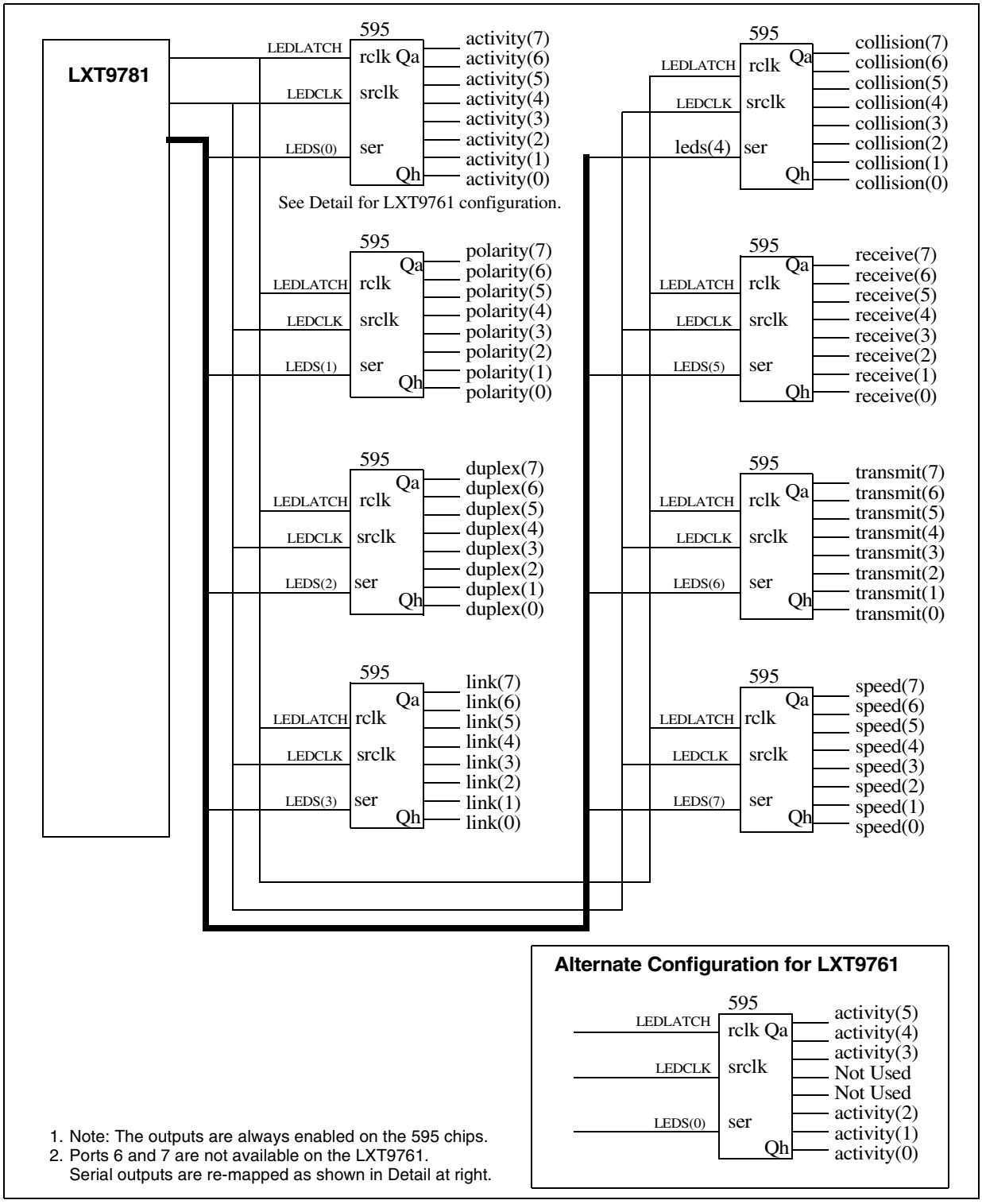


Figure 25. Typical Serial LED Interface



4.0 Test Specifications

Note: Table 15 through Table 31 and Figure 26 through Figure 36 represent the performance specifications of the LXT97x1.
These specifications are guaranteed by test, except where noted "by design." Minimum and maximum values listed in Table 17 through Table 31 apply over the recommended operating conditions specified in Table 16.

Table 15. Absolute Maximum Ratings

Parameter		Sym	Min	Max	Units
Supply voltage		VCC	-0.3	TBD	V
Operating temperature	Ambient	TOPA	-15	+85	ºC
	Case	TOPC	–	+120	ºC
Storage temperature		TST	-65	+150	ºC

Caution: Exceeding these values may cause permanent damage.
Functional operation under these conditions is not implied.
Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 16. Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units
Recommended operating temperature	Ambient	TOPA	0	–	70	ºC
	Case	TOPC	0	–	110	ºC
Recommended supply voltage[2]	Analog & Digital	Vcca, Vccd	3.15	–	3.45	V
	I/O	Vccio	3.15	–	3.45	V
VCC current	100BASE-TX	ICC	–	118[3]	138[3]	mA
	100BASE-FX	ICC	–	–	–	mA
	10BASE-T	ICC	–	118[3]	138[3]	mA
	Power-Down Mode	ICC	–	25	–	mA
	Auto-Negotiation[3]	ICC	–	114.5[3]	138[3]	mA

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Voltages with respect to ground unless otherwise specified.
3. Per-port @ 3.3V.

Table 17. Digital I/O Characteristics [1]

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage[3]	VIL	–	–	0.8	V	–
Input High voltage[3]	VIH	2.0	–	–	V	–

1. Applies to all pins except RMII pins. Refer to Table 18 for RMII I/O Characteristics.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. Does not apply to REFCLK. Refer to Table 19 for clock input levels.

Table 17. Digital I/O Characteristics [1] (Continued)

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input current	I_I	-100	–	100	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

1. Applies to all pins except RMII pins. Refer to Table 18 for RMII I/O Characteristics.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. Does not apply to REFCLK. Refer to Table 19 for clock input levels.

Table 18. Digital I/O Characteristics - RMII Pins

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input current	I_I	-100	–	100	µA	$0.0 < V_I < V_{CC}$
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 4 mA
Output High voltage	V_{OH}	2.2	–	–	V	I_{OH} = -4 mA, V_{CC} = 3.3V
Driver output resistance (Line driver output enabled)	R_O[1]	–	100	–	Ω	V_{CC} = 2.5V
	R_O[1]	–	100	–	Ω	V_{CC} = 3.3V

1. Parameter is guaranteed by design; not subject to production testing.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 19. Required Clock Characteristics

Parameter	Sym	Min	Typ[2]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	–
Input High voltage	V_{IH}	2.0	–	–	V	–
Input frequency	F	–	50	–	MHz	–
Input clock frequency tolerance[1]	Δf	–	–	± 50	ppm	–
Input clock duty cycle[1]	Tdc	35	50	65	%	–

1. Parameter is guaranteed by design; not subject to production testing.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 20. 100BASE-TX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage	V_P	0.95	–	1.05	V	Note 2
Signal amplitude symmetry	Vss	98	–	102	%	Note 2
Signal rise/fall time	T_{RF}	3.0	–	5.0	ns	Note 2

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω(+/-1%) resistor.

Table 20. 100BASE-TX Transceiver Characteristics (Continued)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/fall time symmetry	TRFS	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	± 0.5	ns	Offset from 16ns pulse width at 50% of pulse peak
Overshoot	VO	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω(+/-1%) resistor.

Table 21. 100BASE-FX Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single ended)	VOP	0.6	–	1.5	V	–
Signal rise/fall time	TRF	–	–	1.9	ns	10 <–> 90% 2.0 pF load
Jitter (measured differentially)	–	–	–	1.4	ns	–
Receiver						
Peak differential input voltage	VIP	0.55	–	1.5	V	–
Common mode input range	VCMIR	–	–	VCC - 0.7	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 22. 10BASE-T Transceiver Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	VOP	2.2	2.5	2.8	V	Note 2
Link transmit period	–	8	–	24	ms	–
Transmit timing jitter added by the MAU and PLS sections [3, 4]	–	0	–	11	ns	Note 5
Receiver						
Link min receive timer	TLRmin	2	4	7	ms	–
Link max receive timer	TLRmax	50	64	150	ms	–
Time link loss receive	TLL	50	64	150	ms	–
Differential squelch threshold	VDS	–	390	–	mV Peak	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at the line side of the transformer, line replaced by 100Ω(+/-1%) resistor.
3. Parameter is guaranteed by design; not subject to production testing.
4. IEEE 802.3 specifies maximum jitter addition at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.
5. After line model specified by IEEE 802.3 for 10BASE-T MAU

Figure 26. 100BASE-TX Receive Timing

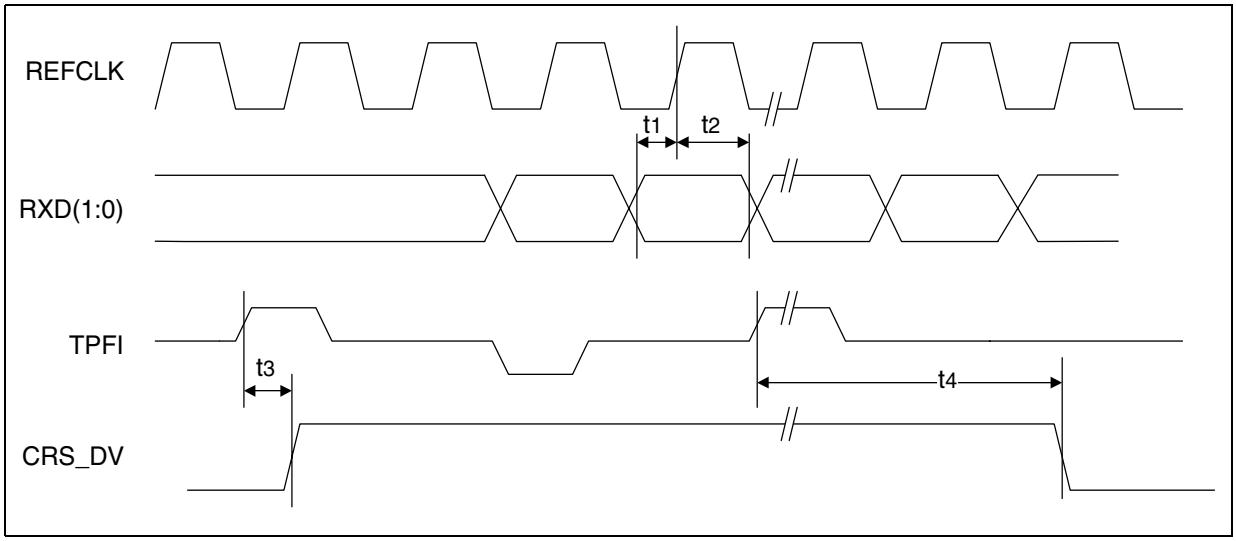


Table 23. 100BASE-TX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD<1:0>, CRS_DV, RXER setup to REFCLK rising edge	t1	4	–	–	ns	–
RXD<1:0>, CRS_DV, RXER hold from REFCLK rising edge	t2	2	–	–	ns	–
Receive start of “J” to CRS_DV asserted	t3	–	14	–	BT	–
Receive start of “T” to CRS_DV de-asserted	t4	–	22	–	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 27. 100BASE-TX Transmit Timing

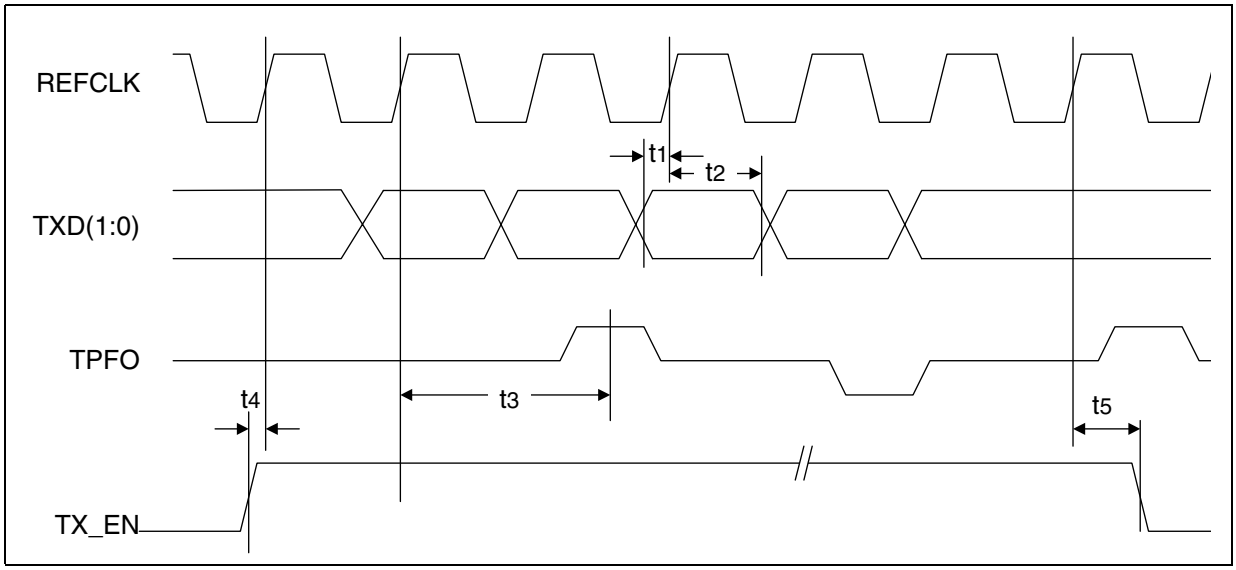


Table 24. 100BASE-TX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD<1:0> setup to REFCLK rising edge	t1	4	–	–	ns	–
TXD<1:0> hold from REFCLK rising edge	t2	2	–	–	ns	–
TX_EN sampled to TPFO out (Tx latency)	t3	–	13	–	BT	–
TX_EN setup to REFCLK rising edge	t4	4	–	–	ns	–
TX_EN hold from REFCLK rising edge	t5	2	–	–	ns	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 28. 100BASE-FX Receive Timing

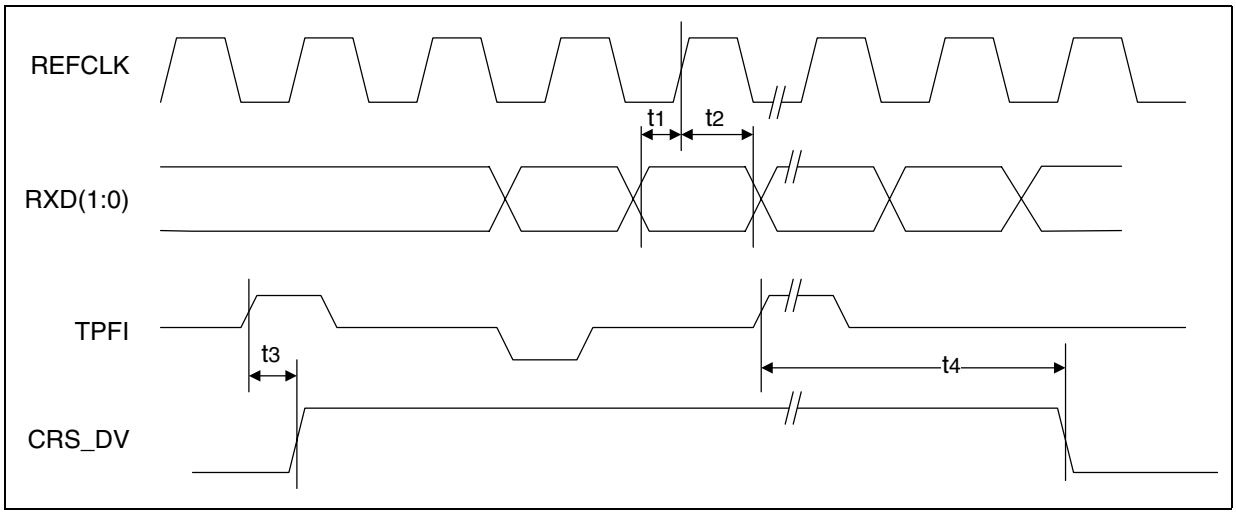


Table 25. 100BASE-FX Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD<1:0>, CRS_DV, RXER setup to REFCLK rising edge	t1	4	–	–	ns	–
RXD<1:0>, CRS_DV, RXER hold from REFCLK rising edge	t2	2	–	–	ns	–
Receive start of “J” to CRS_DV asserted	t3	–	12	–	BT	–
Receive start of “T” to CRS_DV de-asserted	t4	–	20	–	BT	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 29. 100BASE-FX Transmit Timing

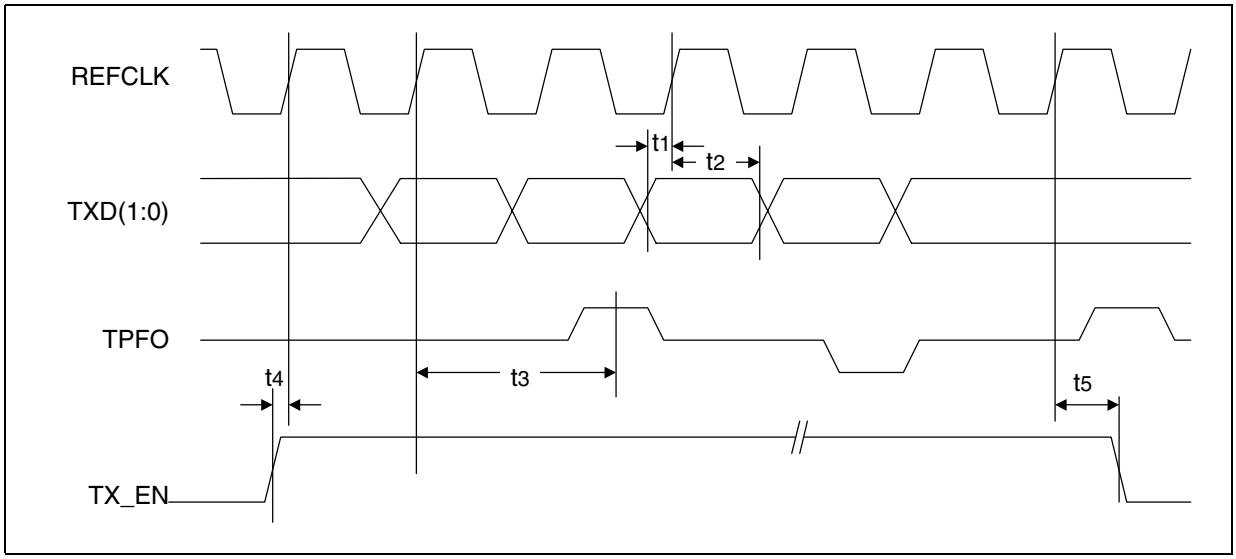


Table 26. 100BASE-FX Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD<1:0> setup to REFCLK rising edge	t1	4	–	–	ns	–
TXD<1:0> hold from REFCLK rising edge	t2	2	–	–	ns	–
TX_EN sampled to TPFO out (Tx latency)	t3	–	13	–	BT	–
TX_EN setup to REFCLK rising edge	t4	4	–	–	ns	–
TX_EN hold from REFCLK rising edge	t5	2	–	–	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 30. 10BASE-T Receive Timing

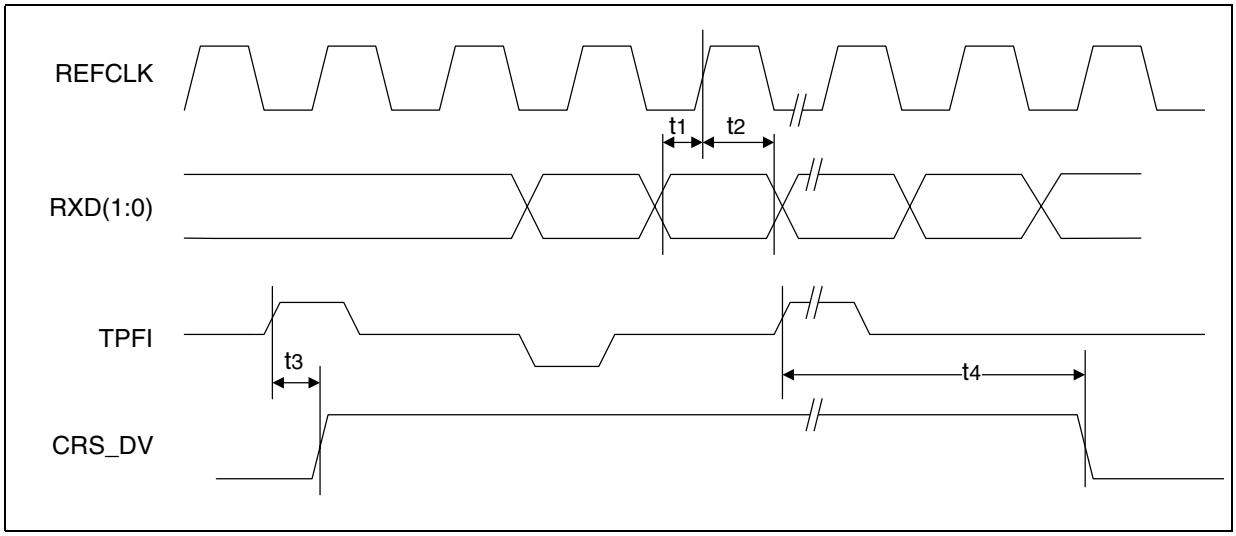


Table 27. 10BASE-T Receive Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
RXD<1:0>, CRS_DV setup to REFCLK rising edge	t1	4	–	–	ns	–
RXD<1:0>, RX_DV hold from REFCLK rising edge	t2	2	–	–	ns	–
TPFI in to CRS_DV asserted	t3	–	3	–	BT	–
TPFI quiet to CRS_DV de-asserted	t4	–	13	–	BT	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 31. 10BASE-T Transmit Timing

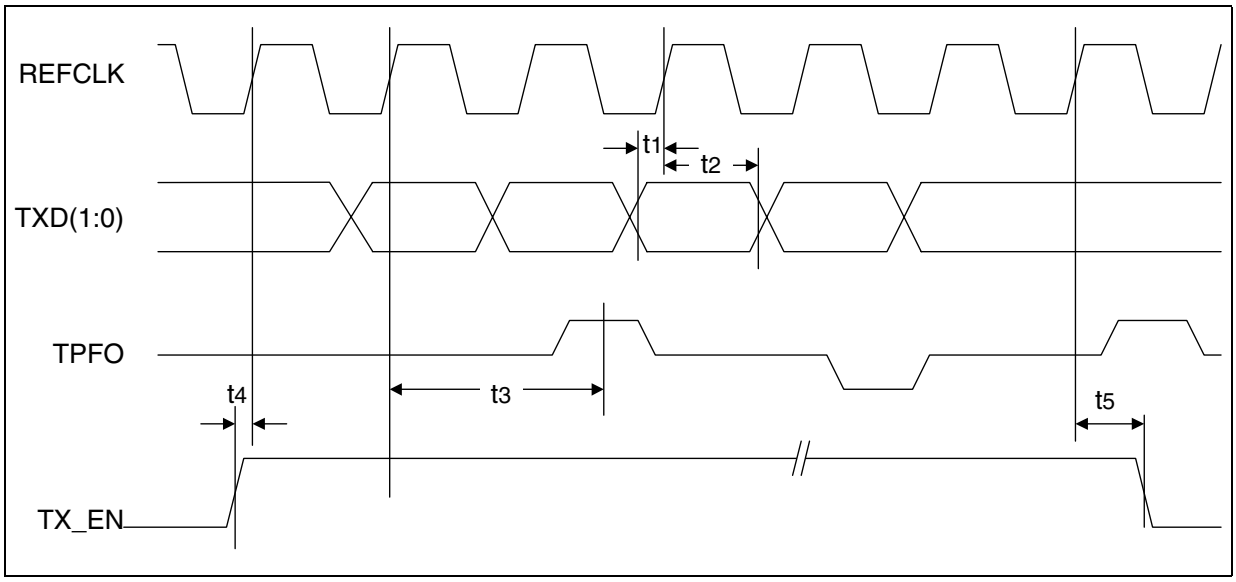


Table 28. 10BASE-T Transmit Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
TXD<1:0> setup to REFCLK rising edge	t1	4	–	–	ns	–
TXD<1:0> hold from REFCLK rising edge	t2	2	–	–	ns	–
TX_EN sampled to TPFO out (Tx latency)	t3	–	15	–	BT	–
TX_EN setup to REFCLK rising edge	t4	4	–	–	ns	–
TX_EN hold from REFCLK rising edge	t5	2	–	–	ns	–
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.						

Figure 32. Auto-Negotiation and Fast Link Pulse Timing

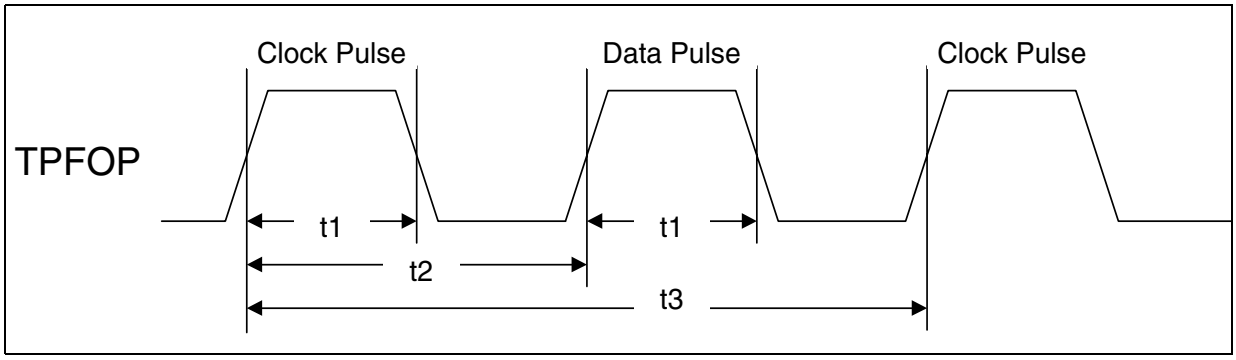


Figure 33. Fast Link Pulse Timing

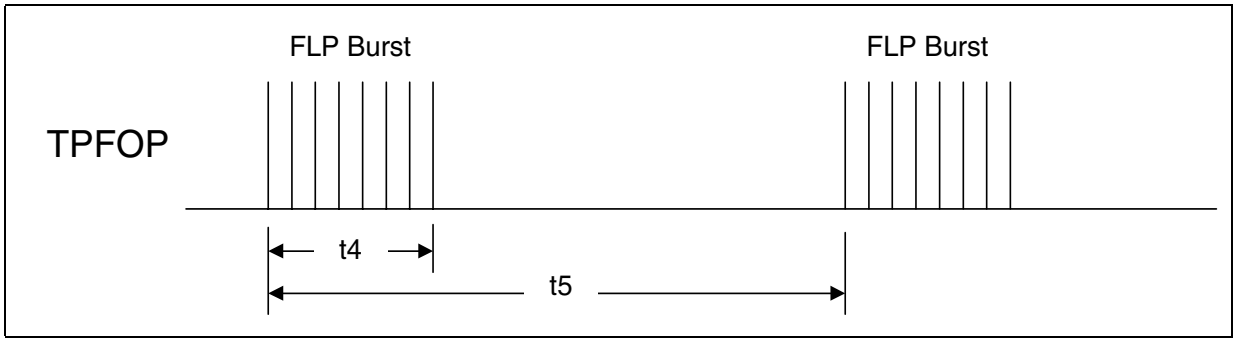


Table 29. Auto-Negotiation and Fast Link Pulse Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Clock/Data pulse width	t1	–	100	–	ns	–
Clock pulse to Data pulse	t2	55.5	–	69.5	µs	–
Clock pulse to Clock pulse	t3	111	–	139	µs	–
FLP burst width	t4	–	2	–	ms	–
FLP burst to FLP burst	t5	8	–	24	ms	–
Clock/Data pulses per burst	–	17	–	33	ea	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Figure 34. MDIO Write Timing (MDIO Sourced by MAC)

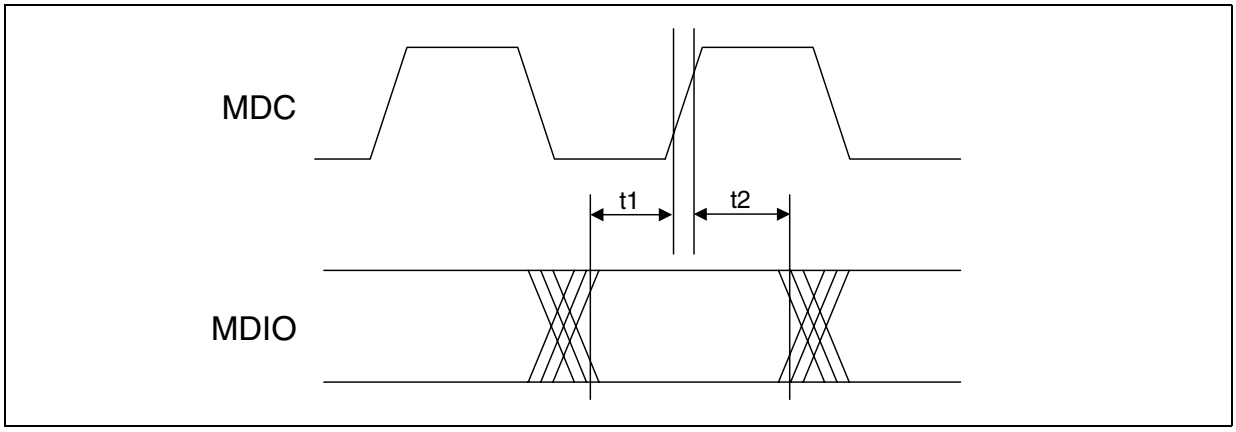


Figure 35. MDIO Read Timing (MDIO Sourced by PHY)

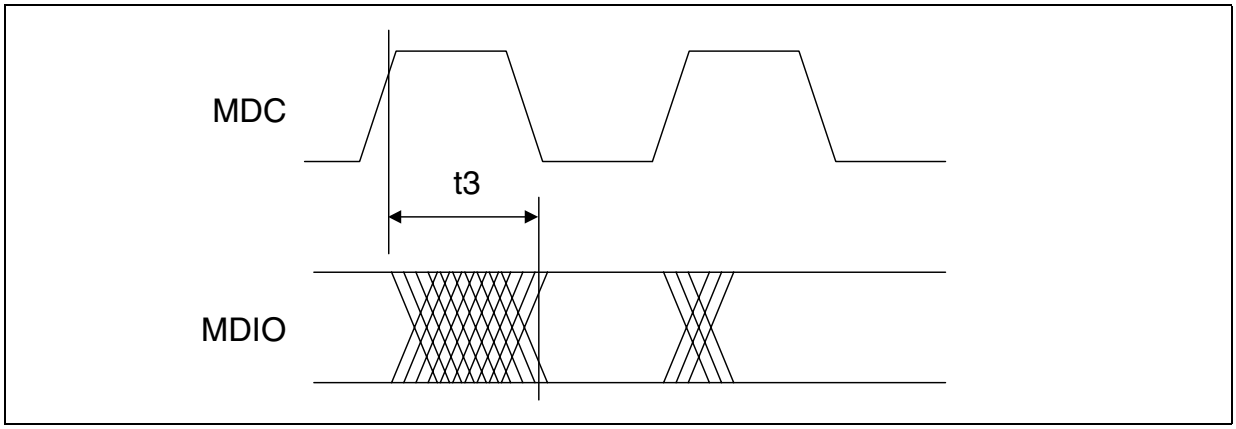


Table 30. MDIO Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
MDIO setup before MDC, sourced by STA	t1	10	–	–	ns	MDC = 2.5 MHz
		1	–	–	ns	MDC = 8 MHz
MDIO hold after MDC, sourced by STA	t2	10	–	–	ns	MDC = 2.5 MHz
		1	–	–	ns	MDC = 8 MHz
MDC to MDIO output delay, sourced by PHY	t3	10	–	300	ns	MDC = 2.5 MHz
		–	130	–	ns	MDC = 8 MHz

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 36. Power-Up Timing

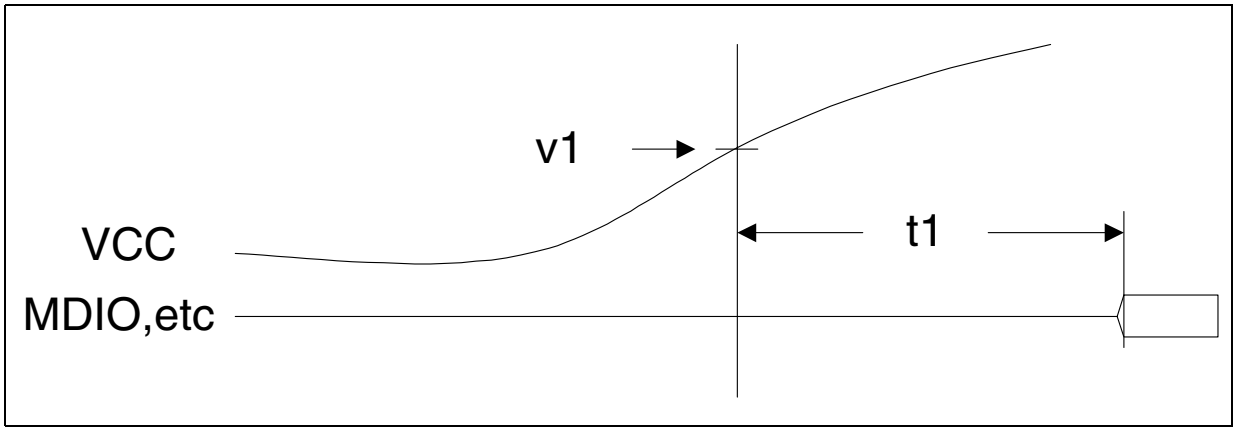


Table 31. Power-Up Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Voltage threshold	v1	–	2.9	–	V	–
Power Up delay	t1	–	–	500	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 37. $\overline{\text{RESET}}$ And Power-Down Recovery Timing

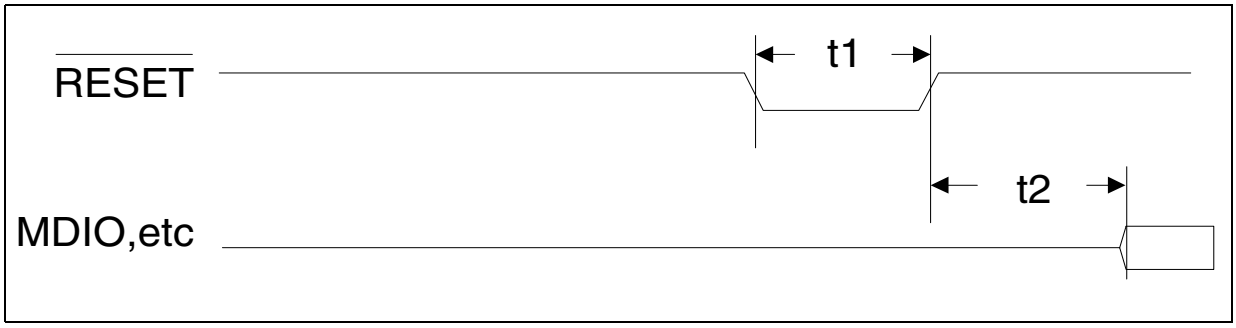


Table 32. $\overline{\text{RESET}}$ and Power-Down Recovery Timing Parameters

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
$\overline{\text{RESET}}$ pulse width	t1	10	–	–	ns	–
$\overline{\text{RESET}}$ recovery delay	t2	–	1	–	ms	–

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

5.0 Register Definitions

The LXT97x1 register set includes multiple 16-bit registers. Table 33 presents a complete register listing and Table 34 provides a consolidated memory map of all registers. Table 35 through Table 49 define individual registers.

- Base registers (0 through 8) are defined in accordance with the "Reconciliation Sublayer and Media Independent Interface" and "Physical Layer Link Signaling for 10/100 Mbps Auto-Negotiation" sections of the IEEE 802.3 specification.
- Additional registers (16 through 30) are defined in accordance with the IEEE 802.3 specification for adding unique chip functions.

Table 33. Register Set

Address	Register Name	Bit Assignments
0	Control Register	Refer to Table 35 on page 65
1	Status Register	Refer to Table 36 on page 65
2	PHY Identification Register 1	Refer to Table 37 on page 66
3	PHY Identification Register 2	Refer to Table 38 on page 67
4	Auto-Negotiation Advertisement Register	Refer to Table 39 on page 67
5	Auto-Negotiation Link Partner Base Page Ability Register	Refer to Table 40 on page 68
6	Auto-Negotiation Expansion Register	Refer to Table 41 on page 69
7	Auto-Negotiation Next Page Transmit Register	Refer to Table 42 on page 69
8	Auto-Negotiation Link Partner Received Next Page Register	Refer to Table 43 on page 70
9	1000BASE-T/100BASE-T2 Control Register	Not Implemented
10	1000BASE-T/100BASE-T2 Status Register	Not Implemented
15	Extended Status Register	Not Implemented
16	Port Configuration Register	Refer to Table 44 on page 70
17	Quick Status Register	Refer to Table 45 on page 71
18	Interrupt Enable Register	Refer to Table 46 on page 72
19	Interrupt Status Register	Refer to Table 47 on page 73
20	LED Configuration Register	Refer to Table 48 on page 74
21-24	Reserved	
25	Out of Band Signalling Register	Refer to Table 49 on page 75
26 - 27	Reserved	
28	Transmit Control Register #1	Refer to Table 50 on page 76
29	Reserved	
30	Transmit Control Register #2	Refer to Table 51 on page 76
31	Reserved	

Table 34. Register Bit Map

Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Control Register																	
Control	Reset	Loopback	Speed Select	A/N Enable	Power Down	Reserved	Re-start A/N	Duplex Mode	COL Test	Speed Select	Reserved						0
Status Register																	
Status	100Base-T4	100Base-X Full Duplex	100Base-X Half Duplex	10Mbps Full Duplex	10Mbps Half Duplex	100Base-T2 Full Duplex	100Base-T2 Half Duplex	Extended Status	Reserved	MF Preamble Suppress	A/N Complete	Remote Fault	A/N Ability	Link Status	Jabber Detect	Extended Capability	1
PHY ID Registers																	
PHY ID 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	2
PHY ID2	PHY ID No						MFR Model No					MFR Rev No					3
Auto-Negotiation Advertisement Register																	
A/N Advertise	Next Page	Reserved	Remote Fault	Reserved	Asymm Pause	Pause	100Base-T4	100Base-TX Full Duplex	100Base-TX	10Base-T Full Duplex	10Base-T	IEEE Selector Field					4
Auto-Negotiation Link Partner Base Page Ability Register																	
A/N Link Ability	Next Page	Ack	Remote Fault	Reserved	Asymm Pause	Pause	100Base-T4	100Base-TX Full Duplex	100Base-TX	10Base-T Full Duplex	10Base-T	IEEE Selector Field					5
Auto-Negotiation Expansion Register																	
A/N Expansion	Reserved										Base Page	Parallel Detect Fault	Link Partner Next Page Able	Next Page Able	Page Received	Link Partner A/N Able	6
Auto-Negotiation Next Page Transmit Register																	
A/N Next Page Txmit	Next Page	Reserved	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											7
Auto-Negotiation Link Partner Next Page Ability Register																	
A/N Link Next Page	Next Page	Ack	Message Page	Ack 2	Toggle	Message / Unformatted Code Field											8
Port Configuration Register																	
Port Config	Reserved	Link Disable	Txmit Disable	Bypass Scrambler (100TX)	Bypass 4B/5B (100TX)	Jabber (10T)	SQE (10T)	TP Loopback (10T)	Reserved	FIFO Size	PRE_EN	Reserved	Reserved	Far End Fault Tx Enable	Alternate Next Page	Fiber Select	16
Quick Status Register																	

Table 34. Register Bit Map (Continued)

Reg Title	Bit Fields																Addr
	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	
Quick Status	Reserved	10/100 Mode	Transmit Status	Receiver Status	Collision Status	Link	Duplex Mode	Auto-Neg	Auto-Neg Complete	Reserved	Polarity	Pause	Error	Reserved	Reserved	Reserved	17
Interrupt Enable Register																	
Interrupt Enable	Reserved							Reserved	Auto-Neg Mask	Speed Mask	Duplex Mask	Link Mask	Reserved	Reserved	Interrupt Enable	Test Interrupt	18
Interrupt Status Register																	
Interrupt Status	Reserved							Reserved	Auto-Neg Done	Speed Change	Duplex Change	Link Change	Reserved	MD Interrupt	Reserved	Reserved	19
LED Configuration Register																	
LED Config	LED1				LED2				LED3				LED Freq		Pulse Stretch	Invert Polarity	20
Programmable RMII Out of Band Signalling Register																	
RMII OOB Signalling	Reserved									Bit 1			Bit 0			Program RMII	25
Transmit Control Register #1																	
Analog #1	Line Length			Reserved									Bandwidth Control		Slew Control		28
Transmit Control Register #2																	
Analog #2	Reserved		Driver Amp	Reserved													30

Table 35. Control Register (Address 0)

Bit	Name	Description	Type [1]	Default
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC	0
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W	0
0.13	Speed Selection	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mbps (not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	R/W	Note 2 00
0.12	Auto-Negotiation Enable[3]	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process	R/W	Note 2 0
0.11	Power-Down	1 = power-down 0 = normal operation	R/W	0
0.10	Reserved	Write as zero. Ignore on read.	R/W	0
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = normal operation	R/W SC	0
0.8	Duplex Mode	1 = Full Duplex 0 = Half Duplex	R/W	Note 2 0
0.7	Collision Test	This bit is ignored by the LXT97x1. 1 = Enable COL signal test 0 = Disable COL signal test	R/W	0
0.6	Speed Selection 1000 Mb/s	0.6 0.13 1 1 = Reserved 1 0 = 1000 Mbps (not allowed) 0 1 = 100 Mbps 0 0 = 10 Mbps	R/W	00
0.5:0	Reserved	Write as 0, ignore on Read	R/W	00000

1. R/W = Read/Write
   RO = Read Only
   SC = Self Clearing
2. Default value of bits 0.12, 0.13 and 0.8 are determined by hardware pins.
3. Do not enable Auto-Negotiation if Fiber Mode is selected.

Table 36. Status Register (Address 1)

Bit	Name	Description	Type [1]	Default
1.15	100BASE-T4	1 = PHY able to perform 100BASE-T4 0 = PHY not able to perform 100BASE-T4	RO	0
1.14	100BASE-X Full Duplex	1 = PHY able to perform full-duplex 100BASE-X 0 = PHY not able to perform full-duplex 100BASE-X	RO	1
1.13	100BASE-X Half Duplex	1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X	RO	1

1. RO = Read Only
   LL = Latching Low
   LH = Latching High
2. Bit 1.4 is not valid if Auto-Negotiation is selected while operating in Fiber mode.

Table 36. Status Register (Address 1) (Continued)

Bit	Name	Description	Type [1]	Default
1.12	10 Mbps Full Duplex	1 = PHY able to operate at 10 Mbps in full-duplex mode 0 = PHY not able to operate at 10 Mbps full-duplex mode	RO	1
1.11	10 Mbps Half Duplex	1 = PHY able to operate at 10 Mbps in half-duplex mode 0 = PHY not able to operate at 10 Mbps in half-duplex	RO	1
1.10	100BASE-T2 Full Duplex	1 = PHY able to perform full-duplex 100BASE-T2 0 = PHY not able to perform full-duplex 100BASE-T2	RO	0
1.9	100BASE-T2 Half Duplex	1 = PHY able to perform half duplex 100BASE-T2 0 = PHY not able to perform half-duplex 100BASE-T2	RO	0
1.8	Extended Status	1 = Extended status information in register 15 0 = No extended status information in register 15	RO	0
1.7	Reserved	1 = ignore when read	RO	0
1.6	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed	RO	0
1.5	Auto-Negotiation complete	1 = Auto-negotiation complete 0 = Auto-negotiation not complete	RO	0
1.4	Remote Fault[2]	1 = Remote fault condition detected 0 = No remote fault condition detected	RO/LH	0
1.3	Auto-Negotiation Ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber condition detected 0 = Jabber condition not detected	RO/LH	0
1.0	Extended Capability	1 = Extended register capabilities 0 = Extended register capabilities	RO	1

1. RO = Read Only
   LL = Latching Low
   LH = Latching High
2. Bit 1.4 is not valid if Auto-Negotiation is selected while operating in Fiber mode.

Table 37. PHY Identification Register 1 (Address 2)

Bit	Name	Description	Type [1]	Default
2.15:0	PHY ID Number	The PHY identifier composed of bits 3 through 18 of the OUI.	RO	0013 hex

1. RO = Read Only

Table 38. PHY Identification Register 2 (Address 3)

Bit	Name	Description	Type [1]	Default
3.15:10	PHY ID number	The PHY identifier composed of bits 19 through 24 of the OUI.	RO	011110
3.9:4	Manufacturer's model number	6 bits containing manufacturer's part number.	RO	000111 (LXT9761) 001010 (LXT9781)
3.3:0	Manufacturer's revision number	4 bits containing manufacturer's revision number.	RO	XXXX

1. RO = Read Only

Figure 38. PHY Identifier Bit Mapping

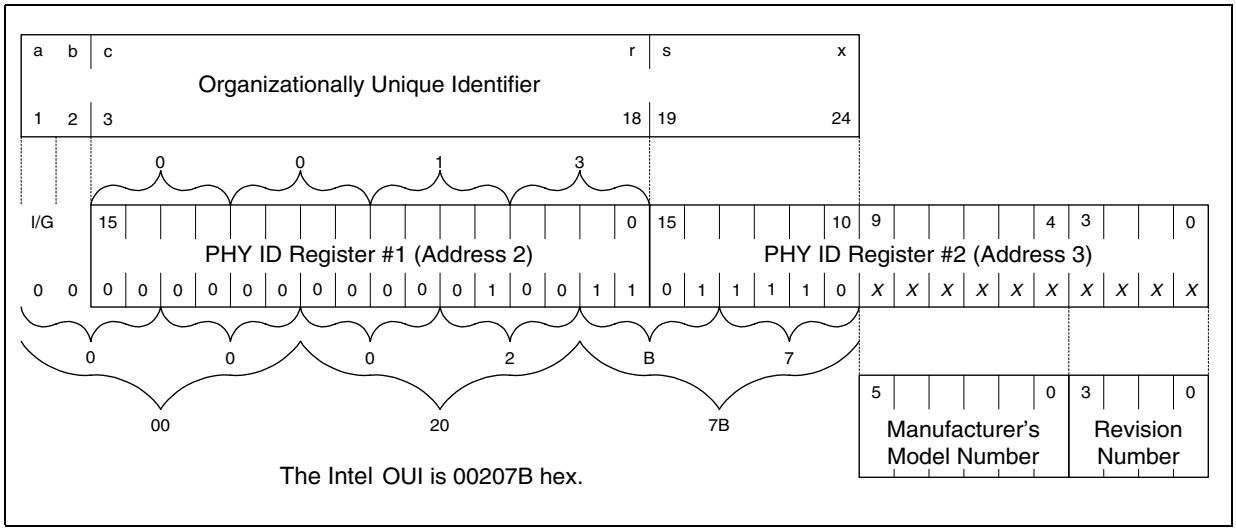


Table 39. Auto-Negotiation Advertisement Register (Address 4)

Bit	Name	Description	Type [1]	Default
4.15	Next Page	1 = Port has ability to send multiple pages. 0 = Port has no ability to send multiple pages.	R/W	0
4.14	Reserved	Ignore.	RO	0
4.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R/W	0
4.12	Reserved	Ignore.	R/W	0
4.11	Asymmetric Pause	Pause operation defined in Clause 40 and 27	R/W	0
4.10	Pause	1 = Pause operation enabled for full-duplex links. 0 = Pause operation disabled.	R/W	Note 2

1. R/W = Read/Write
   RO = Read Only
2. The default setting of bit 4.10 (PAUSE) is determined by pin 79.
3. Default settings for bits 4.5:8 are determined by LED?CFG pins as described in Table 9 on page 29.

Table 39. Auto-Negotiation Advertisement Register (Address 4) (Continued)

Bit	Name	Description	Type [1]	Default
4.9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. (The LXT97x1 does not support 100BASE-T4 but allows this bit to be set to advertise in the Auto-Negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W	0
4.8	100BASE-TX full duplex	1 = Port is 100BASE-TX full duplex capable. 0 = Port is not 100BASE-TX full duplex capable.	R/W	Note 2
4.7	100BASE-TX	1 = Port is 100BASE-TX capable. 0 = Port is not 100BASE-TX capable.	R/W	Note 2
4.6	10BASE-T full duplex	1 = Port is 10BASE-T full duplex capable. 0 = Port is not 10BASE-T full duplex capable.	R/W	Note 2
4.5	10BASE-T	1 = Port is 10BASE-T capable. 0 = Port is not 10BASE-T capable.	R/W	Note 2
4.4:0	Selector Field, S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future Auto-Negotiation development. <11111> = Reserved for future Auto-Negotiation development. Unspecified or reserved combinations should not be transmitted.	R/W	00001

1. R/W = Read/Write
   RO = Read Only
2. The default setting of bit 4.10 (PAUSE) is determined by pin 79.
3. Default settings for bits 4.5:8 are determined by LED?CFG pins as described in Table 9 on page 29.

Table 40. Auto-Negotiation Link Partner Base Page Ability Register (Address 5)

Bit	Name	Description	Type [1]	Default
5.15	Next Page	1 = Link Partner has ability to send multiple pages. 0 = Link Partner has no ability to send multiple pages.	RO	0
5.14	Acknowledge	1 = Link Partner has received Link Code Word from LXT97x1. 0 = Link Partner has not received Link Code Word from the LXT97x1.	RO	0
5.13	Remote Fault	1 = Remote fault. 0 = No remote fault.	RO	0
5.12	Reserved	Ignore.	RO	0
5.11	Asymmetric Pause	Pause operation defined in Clause 40 and 27. 1 = Link Partner is Pause capable. 0 = Link Partner is not Pause capable.	RO	0
5.10	Pause	1 = Link Partner is Pause capable. 0 = Link Partner is not Pause capable.	RO	0
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	RO	0
5.8	100BASE-TX full duplex	1 = Link Partner is 100BASE-TX full duplex capable. 0 = Link Partner is not 100BASE-TX full duplex capable.	RO	0
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	RO	0

1. RO = Read Only

Table 40. Auto-Negotiation Link Partner Base Page Ability Register (Address 5) (Continued)

Bit	Name	Description	Type [1]	Default
5.6	10BASE-T full duplex	1 = Link Partner is 10BASE-T full duplex capable. 0 = Link Partner is not 10BASE-T full duplex capable.	RO	0
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	RO	0
5.4:0	Selector Field S<4:0>	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future Auto-Negotiation development. <11111> = Reserved for future Auto-Negotiation development. Unspecified or reserved combinations shall not be transmitted.	RO	00000

1. RO = Read Only

Table 41. Auto-Negotiation Expansion (Address 6)

Bit	Name	Description	Type [1]	Default
6.15:6	Reserved	Ignore on read.	RO	0
6.5	Base Page	This bit indicates the status of the Auto_Negotiation variable, base page. It flags synchronization with the Auto_Negotiation state diagram allowing detection of interrupted links. This bit is only used if bit 16.1 (Alternate NP feature) is set. 1 = base_page = true 0 = base_page = false	RO	0
6.4	Parallel Detection Fault	1 = Parallel detection fault has occurred. 0 = Parallel detection fault has not occurred.	RO/ LH	0
6.3	Link Partner Next Page Able	1 = Link partner is next page able. 0 = Link partner is not next page able.	RO	0
6.2	Next Page Able	1 = Local device is next page able. 0 = Local device is not next page able.	RO	1
6.1	Page Received	1 = 3 identical and consecutive link code words have been received from link partner. 0 = 3 identical and consecutive link code words have not been received from link partner.	RO LH	0
6.0	Link Partner A/N Able	1 = Link partner is auto-negotiation able. 0 = Link partner is not auto-negotiation able.	RO	0

1. RO = Read Only
   LH = Latching High

Table 42. Auto-Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type [1]	Default
7.15	Next Page (NP)	1 = Additional next pages follow. 0 = Last page.	R/W	0
7.14	Reserved	Write as 0, ignore on read.	RO	0
7.13	Message Page (MP)	1 = Message page. 0 = Unformatted page.	R/W	1

1. R/W = Read Write
   RO = Read Only

Table 42. Auto-Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type [1]	Default
7.12	Acknowledge 2 (ACK2)	1 = Will comply with message. 0 = Can not comply with message.	R/W	0
7.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero. 0 = Previous value of the transmitted Link Code Word equalled logic one.	R/W	0
7.10:0	Message/Unformatted Code Field		R/W	00000000001

1. R/W = Read Write
   RO = Read Only

Table 43. Auto-Negotiation Link Partner Next Page Receive Register (Address 8)

Bit	Name	Description	Type [1]	Default
8.15	Next Page (NP)	1 = Link Partner has additional next pages to send. 0 = Link Partner has no additional next pages to send.	RO	0
8.14	Acknowledge (ACK)	1 = Link Partner has received Link Code Word from LXT97x1. 0 = Link Partner has not received Link Code Word from LXT97x1.	RO	0
8.13	Message Page (MP)	1 = Page sent by the Link Partner is a Message Page. 0 = Page sent by the Link Partner is an Unformatted Page.	RO	0
8.12	Acknowledge 2 (ACK2)	1 = Link Partner Will comply with the message. 0 = Link Partner can not comply with the message.	RO	0
8.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero. 0 = Previous value of the transmitted Link Code Word equalled logic one.	RO	0
8.10:0	Message/Unformatted Code Field		RO	0

1. RO = Read Only

Table 44. Port Configuration Register (Address 16, Hex 10)

Bit	Name	Description	Type [1]	Default
16.15	Reserved	Write as zero. Ignore on read.	R/W	0
16.14	Force Link Pass	1 = Force Link Pass. Sets appropriate registers and LEDs to Pass. 0 = Normal operation.	R/W	0
16.13	Transmit Disable	1 = Disable Twisted Pair transmitter. 0 = Normal Operation.	R/W	0
16.12	Bypass Scramble (100BASE-TX)	1 = Bypass Scrambler and Descrambler. 0 = Normal Operation.	R/W	0
16.11	Reserved	Write as zero. Ignore on read.	R/W	0
16.10	Jabber (10BASE-T)	1 = Disable Jabber. 0 = Normal operation.	R/W	0

1. R/W = Read /Write
2. The default value of bit 16.0 is determined by the SD/$\overline{\text{TP}}$*n* pin for the respective port.
   If SD/$\overline{\text{TP}}$*n* is tied Low, the default value of bit 16.0 = 0. If SD/$\overline{\text{TP}}$*n* is not tied Low, the default value of bit 16.0 = 1.

Table 44. Port Configuration Register (Address 16, Hex 10)

Bit	Name	Description	Type [1]	Default
16.9	SQE (10BASE-T)	This bit is ignored by the LXT97x1. 1 = Enable Heart Beat. 0 = Disable Heart Beat.	R/W	0
16.8	TP Loopback (10BASE-T)	1 = Disable TP loopback during half duplex operation. 0 = Normal Operation.	R/W	1
16.7	CRS Select (10BASE-T)	1 = CRS de-assert extends to RXDV de-assert. 0 = Normal operation.	R/W	1
16.6	FIFO Size	0 = FIFO allows packets up to 2 KBytes. 1 = FIFO allows packets up to 10 KBytes. Packet sizes assume a 450 ppm difference between the reference clock and the recovered clock.	R/W	0
16.5	PRE_EN (10BASE-T)	Preamble Enable. 0 = Set RX_DV high coincident with SFD. 1 = Set RX_DV high and RXD=preamble when CRS is asserted.	R/W	0
16.4	Reserved	Write as zero. Ignore on read.	R/W	0
16.3	Reserved	Write as zero. Ignore on read.	R/W	0
16.2	Far End Fault Transmit Enable	1 = Enable Far End Fault code transmission. 0 = Disable Far End Fault code transmission.	R/W	1
16.1	Alternate NP feature	1 = Enable alternate auto-negotiate next page feature. 0 = Disable alternate auto-negotiate next page feature.	R/W	0
16.0	Fiber Select	1 = Select fiber mode for this port. 0 = Select TP mode for this port.	R/W	Note 2

1. R/W = Read /Write
2. The default value of bit 16.0 is determined by the SD/$\overline{\text{TP}}$*n* pin for the respective port. If SD/$\overline{\text{TP}}$*n* is tied Low, the default value of bit 16.0 = 0. If SD/$\overline{\text{TP}}$*n* is not tied Low, the default value of bit 16.0 = 1.

Table 45. Quick Status Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default
17.15	Reserved	Always 0.	RO	0
17.14	10/100 Mode	1 = LXT97x1 is operating in 100BASE-TX mode. 0 = LXT97x1 is not operating 100BASE-TX mode.	RO	0
17.13	Transmit Status	1 = LXT97x1 is transmitting a packet. 0 = LXT97x1 is not transmitting a packet.	RO	0
17.12	Receive Status	1 = LXT97x1 is receiving a packet. 0 = LXT97x1 is not receiving a packet.	RO	0
17.11	Collision Status	1 = Collision is occurring. 0 = No collision.	RO	0
17.10	Link	1 = Link is up. 0 = Link is down.	RO	0
17.9	Duplex Mode	1 = Full duplex. 0 = Half duplex.	RO	0
17.8	Auto-Negotiation	1 = LXT97x1 is in Auto-Negotiation Mode. 0 = LXT97x1 is in manual mode.	RO	0

1. RO = Read Only

Table 45. Quick Status Register (Address 17, Hex 11)

Bit	Name	Description	Type [1]	Default
17.7	Auto-Negotiation Complete	1 = Auto-negotiation process completed. 0 = Auto-negotiation process not completed. This bit is only valid when auto-negotiate is enabled, and is equivalent to bit 1.5.	RO	0
17.6	Reserved	Reserved.	RO	0
17.5	Polarity	1= Polarity is reversed. 0= Polarity is not reversed.	RO	0
17.4	Pause	1 = The LXT97x1 is Pause capable. 0 = The LT97x1 is Not Pause capable.	RO	0
17:3	Error	1 = Error Occurred (Remote Fault, X,Y,Z). 0 = No error occurred.	RO	0
17:2:0	Reserved	Ignore.	RO	0
1. RO = Read Only				

Table 46. Interrupt Enable Register (Address 18, Hex 12)

Bit	Name	Description	Type [1]	Default
18.15:8	Reserved	Write as 0; ignore on read.	R/W	N/A
18.7	ANMSK	Mask for Auto-Negotiate Complete 1 = Enable event to cause interrupt. 0 = Do not allow event to cause interrupt.	R/W	0
18.6	SPEEDMSK	Mask for Speed Interrupt 1 = Enable event to cause interrupt. 0 = Do not allow event to cause interrupt.	R/W	0
18.5	DUPLEXMSK	Mask for Duplex Interrupt 1 = Enable event to cause interrupt. 0 = Do not allow event to cause interrupt.	R/W	0
18.4	LINKMSK	Mask for Link Status Interrupt 1 = Enable event to cause interrupt. 0 = Do not allow event to cause interrupt.	R/W	0
18.3	Reserved	Write as 0, ignore on read.	R/W	0
18.2	Reserved	Write as 0, ignore on read.	R/W	0
18.1	INTEN	1 = Enable interrupts on this port. 0 = Disable interrupts on this port.	R/W	0
18.0	TINT	1 = Force interrupt on MDINT. 0 = Normal operation.	R/W	0
1. R/W = Read /Write				

Table 47. Interrupt Status Register (Address 19, Hex 13)

Bit	Name	Description	Type [1]	Default
19.15:8	Reserved	Ignore	RO	N/A
19.7	ANDONE	Auto-Negotiation Status 1= Auto-Negotiation has completed. 0= Auto-Negotiation has not completed.	RO/SC	N/A
19.6	SPEEDCHG	Speed Change Status 1 = A Speed Change has occurred since last reading this register. 0 = A Speed Change has not occurred since last reading this register.	RO/SC	0
19.5	DUPLEXCHG	Duplex Change Status 1 = A Duplex Change has occurred since last reading this register. 0 = A Duplex Change has not occurred since last reading this register.	RO/SC	0
19.4	LINKCHG	Link Status Change Status 1 = A Link Change has occurred since last reading this register. 0 = A Link Change has not occurred since last reading this register.	RO/SC	0
19.3	Reserved	Ignore.	RO	0
19.2	MDINT	1 = RMII interrupt pending. 0 = No RMII interrupt pending.	RO/SC	0
19.1:0	Reserved	Ignore.	RO	0

1. R/W = Read/Write
   RO = Read Only
   SC = Self Clearing

Table 48. LED Configuration Register (Address 20, Hex 14)

Bit	Name	Description	Type [1]	Default
20.15:12	LED1 Programming bits	0000 = Display Speed Status (Continuous, Default). 0001 = Display Transmit Status (Stretched). 0010 = Display Receive Status (Stretched). 0011 = Display Collision Status (Stretched). 0100 = Display Link Status (Continuous). 0101 = Display Duplex Status (Continuous)[5]. 0110 =Reserved. 0111 = Display Receive or Transmit Activity (Stretched). 1000 = Test mode- turn LED on (Continuous). 1001 = Test mode- turn LED off (Continuous). 1010 = Test mode- blink LED fast (Continuous). 1011 = Test mode- blink LED slow (Continuous). 1100 = Display Link and Receive Status combined [2] (Stretched)[3] . 1101 = Display Link and Activity Status combined [2] (Stretched)[3]. 1110 = Display Duplex & Collision Status combined [4] (Stretched)[3,5]. 1111 = Reserved.	R/W	0000
20.11:8	LED2 Programming bits	0000 = Display Speed Status. 0001 = Display Transmit Status. 0010 = Display Receive Status. 0011 = Display Collision Status. 0100 = Display Link Status (Default). 0101 = Display Duplex Status[5]. 0110 = Reserved. 0111 = Display Receive or Transmit Activity. 1000 = Test mode- turn LED on. 1001 = Test mode- turn LED off. 1010 = Test mode- blink LED fast. 1011 = Test mode- blink LED slow. 1100 = Display Link and Receive Status combined [2] (Stretched)[3]. 1101 = Display Link and Activity Status combined [2] (Stretched)[3]. 1110 = Display Duplex & Collision Status combined [4] (Stretched)[3,5]. 1111 = Reserved.	R/W	0100
20.7:4	LED3 Programming bits	0000 = Display Speed Status. 0001 = Display Transmit Status. 0010 = Display Receive Status (Default). 0011 = Display Collision Status. 0100 = Display Link Status. 0101 = Display Duplex Status[5]. 0110 = Reserved. 0111 = Display Receive or Transmit Activity. 1000 = Test mode- turn LED on. 1001 = Test mode- turn LED off. 1010 = Test mode- blink LED fast. 1011 = Test mode- blink LED slow. 1100 = Display Link and Receive Status combined [2] (Stretched)[3]. 1101 = Display Link and Activity Status combined [2] (Stretched)[3]. 1110 = Display Duplex & Collision Status combined [4] (Stretched)[3,5]. 1111 = Reserved.	R/W	0010

1. R/W = Read /Write
   RO = Read Only
   LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up.
   The secondary LED driver (Receive or Activity) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full duplex.
   Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Duplex LED maybe active for a brief time after loss of link.

Table 48. LED Configuration Register (Address 20, Hex 14) (Continued)

Bit	Name	Description	Type [1]	Default
20.3:2	LEDFREQ	00 = Stretch LED events to 30 ms. 01 = Stretch LED events to 60 ms. 10 = Stretch LED events to 100 ms. 11 = Reserved.	R/W	00
20.1	PULSE-STRETCH	1 = Enable pulse stretching of all LEDs. 0 = Disable pulse stretching of all LEDs [2].	R/W	1
20.0	INVPOL	1 = Use active High polarity for serial LEDs. 0 = Use active Low polarity for serial LEDs.	R/W	0

1. R/W = Read /Write
   RO = Read Only
   LH = Latching High
2. Link status is the primary LED driver. The LED is asserted (solid ON) when the link is up.
   The secondary LED driver (Receive or Activity) causes the LED to change state (blink).
3. Combined event LED settings are not affected by Pulse Stretch bit 20.1. These display settings are stretched regardless of the value of 20.1.
4. Duplex status is the primary LED driver. The LED is asserted (solid ON) when the link is full duplex.
   Collision status is the secondary LED driver. The LED changes state (blinks) when a collision occurs.
5. Duplex LED maybe active for a brief time after loss of link.

Table 49. Out of Band Signaling Register (Address 25)

Bit	Name	Description	Type [1]	Default
25:15:7	Reserved	Reserved.	R/W	0
25:6:4	BIT1	These 3 bits select which status information is available on the RXD(1) bit of the RMII bus. 000 = Link 001 = Speed 010 = Duplex 011 = Auto-negotiation complete 100 = Polarity reversed 101 = Jabber detected 110 = Interrupt pending 111 = Reserved	R/W	000
25.3:1	BIT0	These 3 bits select which status information is available on the RXD(0) bit of the RMII bus. 000 = Link 001 = Speed 010 = Duplex 011 = Auto-negotiation complete 100 = Polarity reversed 101 = Jabber detected 110 = Interrupt pending 111 = Reserved	R/W	000
25.0	PROGRMII	1 = Enable programmable RMII Out of Band signalling. When enabled, bits 6:1 specify which status bits are available on the RMII RXD data bus. 0 = Disable Out of Band signalling.	R/W	0

1. R/W = Read/Write
   RO = Read Only

Table 50. Transmit Control Register #1 (Address 28)

Bit	Name	Description	Type[2]	Default
28.15:4	Reserved	Ignore.	R/W	N/A
28.3:2	Bandwidth Control	00 = Nominal Differential Amp Bandwidth 01 = Slower 10 = Fastest 11 = Faster	R/W	00
28.1:0	Risetime Control	00 = 2.5ns 01 = 3.1ns 10 = 3.7ns 11 = 4.3ns	R/W	Note 3

1. Transmit Control functions are approximations. They are not guaranteed and not subject to production testing.
2. RO = Read Only.
   R/W = Read/Write.
3. The default setting of bits 28.1:0 (Risetime) are determined by pins 91 and 94.

Table 51. Transmit Control Register #2 (Address 30)

Bit	Name	Description	Type	Default
30.15:14	Reserved		R/W	N/A
30.13	Increase Driver Amplitude	1 = Increase Driver Amplitude 5% in all modes. 0 = Normal operation.	R/W	0
30.12:0	Reserved		R/W	N/A

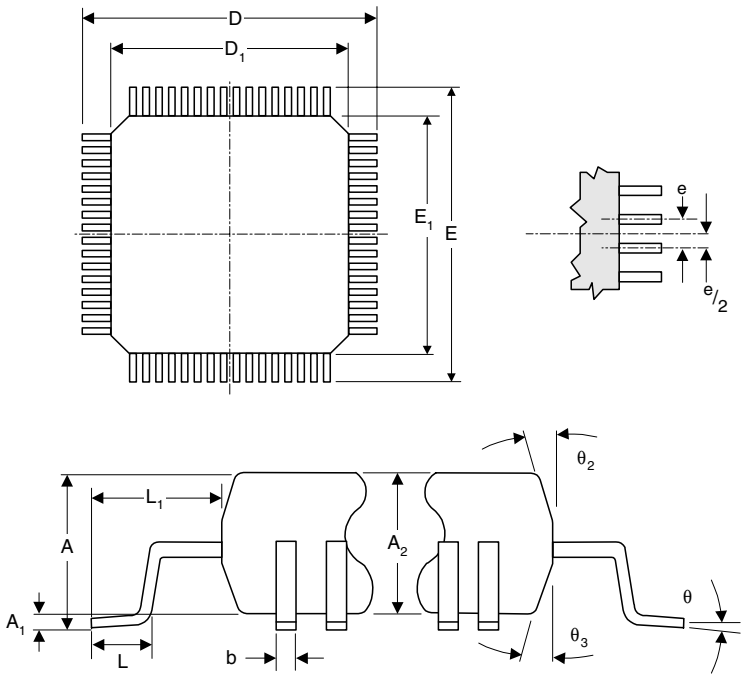
1. RO = Read Only.

6.0 Package Specifications

Figure 39. LXT97x1 PQFP Specification

208-Pin Plastic Quad Flat Package

- Part Number LXT9761HC (6-port model)
- Part Number LXT9781HC (8-port model)
- Commercial Temperature Range (0°C to 70°C)

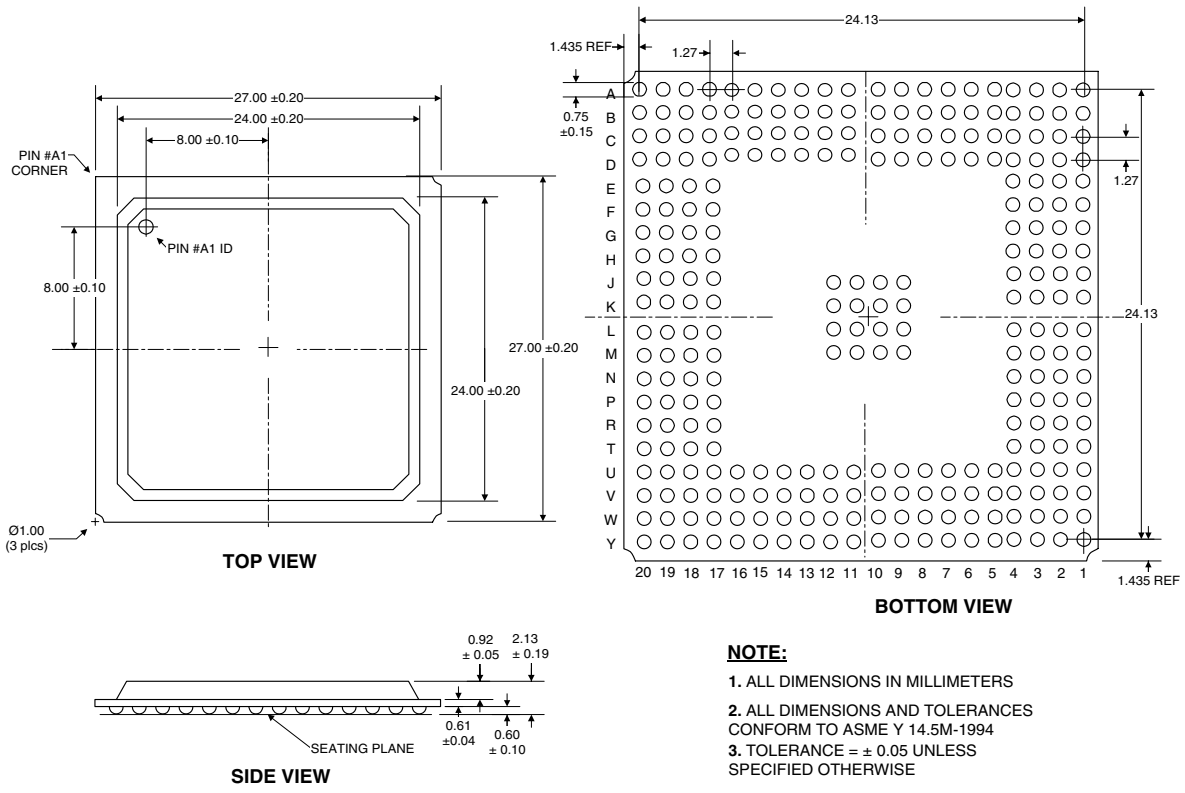


Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°

Figure 40. LXT9781 PBGA Specification

272-Lead Plastic Ball Grid Array

- Part Number LXT9781BC (8-port model)
- Commercial Temperature Range (0°C to 70°C)



NOTE:

1. ALL DIMENSIONS IN MILLIMETERS
2. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994
3. TOLERANCE = ± 0.05 UNLESS SPECIFIED OTHERWISE