Silicon-gate CMOS LSI

LC7215, 7215F, 7215FM

# **MW/LW PLL Frequency Synthesizers**

# Overview

The LC7215, LC7215F and LC7215FM are phase-locked-loop frequency synthesizer LSIs that provide accurate reference frequencies over the MW and LW bands, making them ideally suited for AM tuners.

# Features

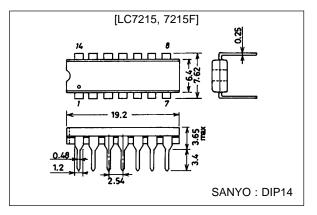
- PLL frequency synthesizer LSIs for MW and LW bands.
- Reference frequencies of 1, 5, 9 and 10 kHz.
- On-chip transistor for the low-pass filter amplifier.
- Single output pin (CMOS output)
- Controller clock output pin.
- Time-base output pin.
- All devices can be used for double conversion demodulation.
- The LC7215F and 7215FM have expanded input frequency ranges.

LC7215 0.5 to 13 MHz : (DIP14) LC7215F/FM 0.5 to 20 MHz : (DIP14/MFP14S)

# **Package Dimensions**

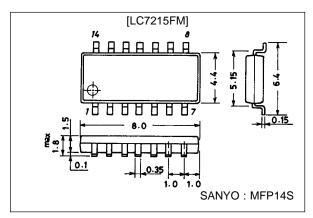
unit : mm

#### 3003A-DIP14





## 3111-MFP14S



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# **Specifications**

# Absolute Maximum Ratings at Ta = $25^{\circ}$ C, V<sub>SS</sub> = 0 V

Values in parentheses are for the LC7215F and LC7215FM.

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD</sub>	-0.3 to +6.5	V
Input voltage	V <sub>IN</sub> 1	All input pins	–0.3 to V <sub>DD</sub> +0.3	V
	V <sub>IN</sub> 2	CE, CL, DATA	(Note) -0.3 to +6.5	V
Output current	IOUT	AOUT	0 to 5	mA
Output voltage	V <sub>OUT</sub> 1	AOUT	-0.3 to +15	V
	V <sub>OUT</sub> 2	SYC, TB	-0.3 to +6.5	V
	V <sub>OUT</sub> 3	All output pins except V <sub>OUT</sub> 1 and V <sub>OUT</sub> 2	–0.3 to V <sub>DD</sub> +0.3	V
Allowable power dissipation	Pd max	Ta ≦ 85°C	150	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Note: Voltage that is applied to the resistors when resistors totaling at least 10 k $\Omega$  are connected to a pin in series.

## Allowable Operating Conditions at $\mathbf{V}_{SS}=\mathbf{0}~\mathbf{V}$

Values in parentheses are for the LC7215F and LC7215FM.

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltogo	V <sub>DD</sub> 1	V <sub>DD</sub>	(4.5)3.0		(5.5)5.5	V
Supply voltage	V <sub>DD</sub> 2	V <sub>DD</sub> (Crystal OSC oscillation guaranteed)	3.0		5.5	V
High-level input voltage	VIH	CE, CL, DATA	2.0		V <sub>DD</sub> 1	V
Low-level input voltage	VIL	CE, CL, DATA	0		0.5	V
	V <sub>OUT</sub> 1	AOUT			13	V
Output voltage	V <sub>OUT</sub> 2	SYC, TB			5.5	V
Input frequency	f <sub>IN</sub> 1	PIN: Sine wave, capacitive coupling V <sub>DD</sub> 1, *S = 1	(2.3)2.3		(20)13	MHz
	f <sub>IN</sub> 2	PIN: Sine wave, capacitive coupling $V_{DD}1$ , *S = 0	0.5		2.5	MHz
Oscillation guaranteed crystal oscillator	X'tal	XIN, XOUT: CI $\leq$ 30 $\Omega$		11.16	12.00	MHz
Input amplitude	V <sub>IN</sub> 1	PIN: Square wave, capacity connection V <sub>DD</sub> 1, *S = 1	100		1000	mVrms
	V <sub>IN</sub> 2	PIN: Square wave, capacity connection $V_{DD}1$ , *S = 0	100		1000	mVrms
Power supply	_	V <sub>DD</sub> , V <sub>SS</sub> : A capacitor of at least 1000 pF must be inserted.	1000			pF

#### **Electrical Characteristics** within the allowable operating ranges

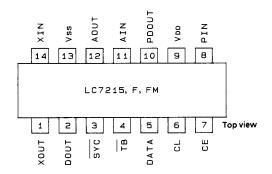
Values in parentheses are for LC7215F and LC7215FM.

Parameter	Symbol	Conditions	min	typ	max	Unit
High-level input currents	I <sub>IH</sub> 1	$XIN: V_I = V_{DD}$			20	μA
	I <sub>IH</sub> 2	PIN: $V_I = V_{DD}$			40	μA
Figh-level liput currents	I <sub>IH</sub> 3	CE, CL, DATA: V <sub>I</sub> = V <sub>DD</sub>			3.0	μA
	I <sub>IH</sub> 4	AIN: $V_I = V_{DD}$		0.01	1.0	μA
	I <sub>IL</sub> 1	$XIN: V_I = V_{SS}$			20	μA
Low-level input currents	I <sub>IL</sub> 2	PIN: $V_I = V_{SS}$			40	μA
Low-level input currents	I <sub>IL</sub> 3	CE, CL, DATA: V <sub>I</sub> = V <sub>SS</sub>			3.0	μA
	I <sub>IL</sub> 4	AIN: $V_I = V_{SS}$		0.01	1.0	μA
High-level output voltages	V <sub>OH</sub> 1	DOUT: I <sub>O</sub> = 1 mA	V <sub>DD</sub> -1.0			V
nigh-level output voltages	V <sub>OH</sub> 2	PDOUT: I <sub>O</sub> = 0.5 mA	V <sub>DD</sub> -1.0			V
	V <sub>OL</sub> 1	DOUT: I <sub>O</sub> = -1 mA			1.0	V
Low-level output voltages	V <sub>OL</sub> 2	PDOUT: $I_0 = -0.5 \text{ mA}$			1.0	V
Low-level output voltages	V <sub>OL</sub> 4	$\overline{\text{SYC}}, \overline{\text{TB}}: I_{O} = 0.5 \text{ mA}$			1.0	V
	V <sub>OL</sub> 5	AOUT: I <sub>O</sub> = 1 mA			1.0	V
Output off-state leakage	I <sub>OFF</sub> 1	$\overline{\text{SYC}}, \overline{\text{TB}}: V_{\text{O}} = V_{\text{DD}}$			3.0	μA
currents	I <sub>OFF</sub> 2	AOUT: V <sub>O</sub> = 13 V			5.0	μA
Tristate output High-level off-state leakage current	I <sub>OFF</sub> H	PDOUT: V <sub>O</sub> = V <sub>DD</sub>		0.01	1.0	nA
Tristate output Low-level off-state leakage current	I <sub>OFF</sub> L	PDOUT: V <sub>O</sub> = V <sub>SS</sub>		0.01	1.0	nA
High-level output voltage	V <sub>OH</sub> 3	XOUT: I <sub>O</sub> = -0.1 mA	V <sub>DD</sub> -1.0			V
Low-level output voltage	V <sub>OL</sub> 3	XOUT: I <sub>O</sub> = 0.1 mA			1.0	V
Supply current		V <sub>DD</sub> : f <sub>IN</sub> 1 = 13 MHz, *S = 1 (High speed) (Note 1)			10	mA
	I <sub>DD</sub> 1	f <sub>IN</sub> 1 = 20 MHz, *S = 1 (High speed) (Note 1)			(12)	mA
	I <sub>DD</sub> 2	V <sub>DD</sub> : f <sub>IN</sub> 1 = 2.5 MHz, *S = 0 (Low speed) (Note 1)			5	mA
		V <sub>DD</sub> : V <sub>DD</sub> = 5.5 V, *O = 0, P = 1 (Note 2)		1.2	2.0	mA
	I <sub>DD</sub> 3	V <sub>DD</sub> = 4.5 V, *O = 0, P = 1 (Note 2)		0.7	1.5	mA
		V <sub>DD</sub> = 3.0 V, *O = 0, P = 1 (Note 2)		0.4	1.0	mA

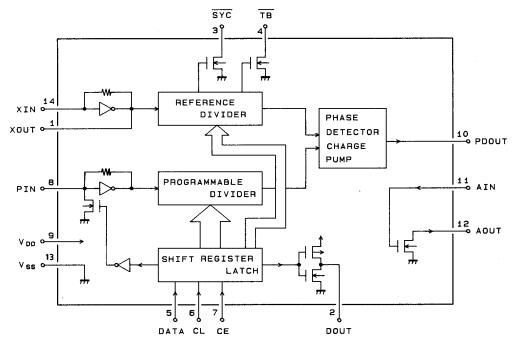
\* S, O and P are serial control bits.

- Note 1.  $V_{IN}1 = V_{IN}2 = 100$  mVms. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to  $V_{SS}$  and all other outputs are open.
  - 2. The 11.16 MHz crystal is connected to XIN and XOUT. All other inputs are connected to  $V_{DD}$  and all other outputs are open. (Backup mode when PLL is halted.)

#### **Pin Assignment**



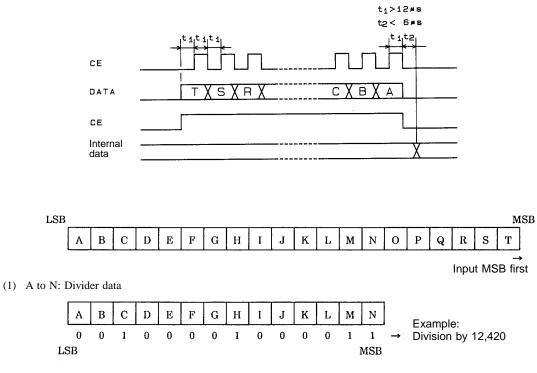
## **Block Diagram**



# **Pin Description**

Name	Description
XIN, XOUT	11.16 MHz crystal oscillator connection, feedback resistance built-in
PIN	Local oscillator signal input
V <sub>DD</sub> , V <sub>SS</sub>	Power supply
DATA, CL, CE	Data input
DOUT	Single bit data output
AIN, AOUT	Low-pass filter amplifier
PDOUT	Charge pump output
TB	8 Hz time-base output
SYC	60 kHz controller clock output

#### **Data Input**



(2) O, P: Mode selection

Mode	0	Р	DOUT	TB	Operation	
NOR1	0	0	Т	8 Hz Normal operation (with PLL operating)		
NOR2	0	1	Т	T 8 Hz Normal operation (backup when PLL is halted)		
TEST1	1	0	(Device test mode)			
TEST2	1	1	(Device test mode)			

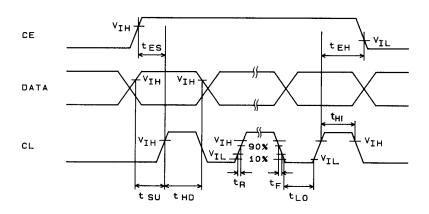
(3) Q, R: Reference frequency selection

Q	R	Reference frequency
0	0	9 kHz
0	1	10 kHz
1	0	1 kHz
1	1	5 kHz

- (4) S: Programmable divider input sensitivity switch
  S = 1: for High speed
  S = 0: for Low speed
- (5) T: Output to DOUT
  - T = 1: DOUT = 1T = 0: DOUT = 0

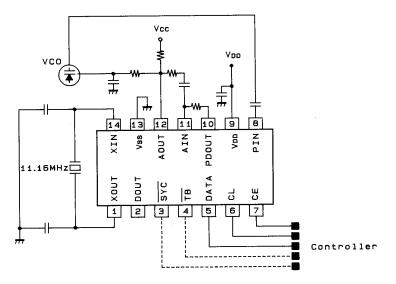
#### **Data Input Timing**

 $\label{eq:VII} \begin{array}{l} V_{IH} = 2.0 \mbox{ to } V_{DD}, \mbox{ } V_{IL} = 0 \mbox{ to } 0.5 \mbox{ V} \\ X'tal = 8.00 \mbox{ to } 11.16 \mbox{ (typ) to } 12.00 \mbox{ MHz} \\ Data \mbox{ latch: Rising edge of CL} \end{array}$ 

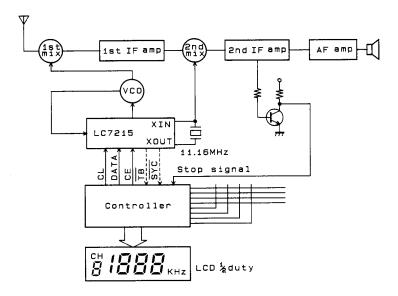


Item	Symbol	11.16 MHz crystal	Other crystal frequencies	Effective value
Enable setup time	t <sub>ES</sub>	At least 12 µs	At least $2 \times (1/fXtal \times 62)$	
Enable hold time	t <sub>EH</sub>	↑	$\uparrow$	
Data setup time	t <sub>SU</sub>	↑	$\uparrow$	1/2 of the value
Data hold time	t <sub>HD</sub>	↑	$\uparrow$	shown at left
Clock Low-level time	tLO	↑	$\uparrow$	
Clock High-level time	t <sub>HI</sub>	↑	$\uparrow$	
Rise time	t <sub>R</sub>	1 µs or less	1 µs or less	
Fall time	t <sub>F</sub>	↑	$\uparrow$	

#### (1) Sample Application Circuit



#### (2) Double-conversion Receiver



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