SONY

CXD3615R

Timing Generator for Frame Readout CCD Image Sensor

Description

The CXD3615R is a timing generator IC which generates the timing pulses for performing frame readout using the ICX432/434 CCD image sensor.

Features

- Base oscillation frequency 48.6/36.0MHz
- Electronic shutter function
- Supports draft, AF mode
- H/V driver for CCD

Applications

Digital still cameras

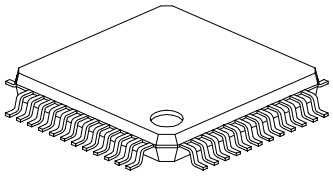
Structure

Silicon gate CMOS IC

Applicable CCD Image Sensors

- ICX432 (Type 1/2.7, 3240K pixels)
- ICX434 (Type 1/3.2, 2020K pixels)

48 pin LQFP (Plastic)



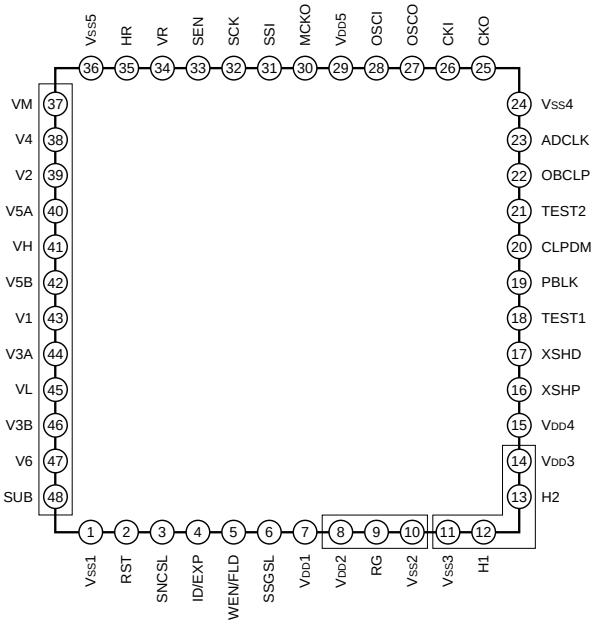
Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.3 to +7.0	V
	VL	–10.0 to V_{SS}	V
	VH	VL – 0.3 to +26.0	V
• Input voltage	V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
• Output voltage	V_{O1}	V_{SS} – 0.3 to V_{DD} + 0.3	V
	V_{O2}	VL – 0.3 to V_{SS} + 0.3	V
	V_{O3}	VL – 0.3 to VH + 0.3	V
• Operating temperature			
	Topr	–20 to +75	°C
• Storage temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}a, V_{DD}b, V_{DD}c		
		3.0 to 3.6	V
	VM	0.0	V
	VH	14.5 to 15.5	V
	VL	–7.0 to –8.0	V
• Operating temperature			
	Topr	–20 to +75	°C

Pin Configuration



* Groups of pins enclosed in the figure indicate sections for which power supply separation is possible.

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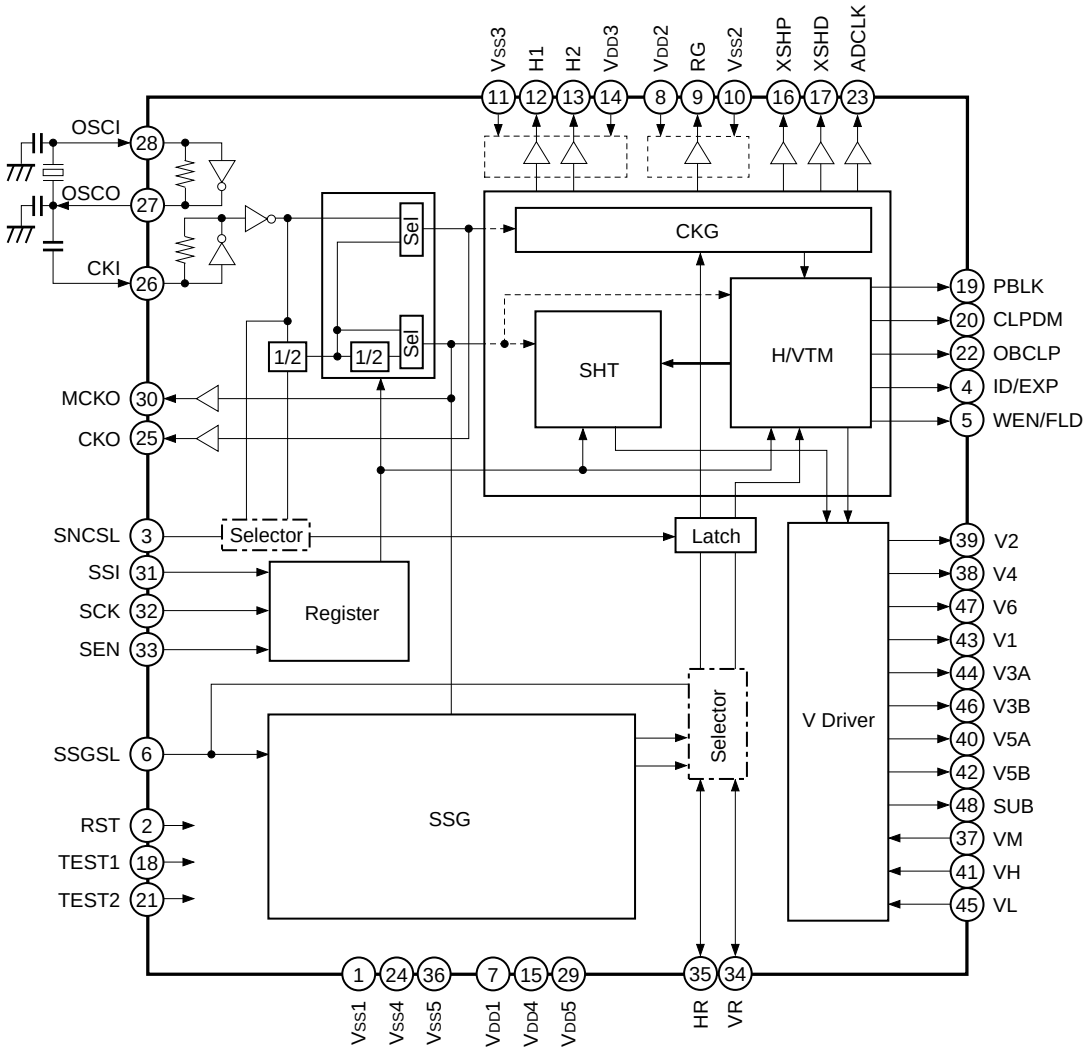
Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	$V_{SS}1$	—	GND
2	RST	I	Internal system reset input. High: Normal operation, Low: Reset control Normally apply reset during power-on. Schmitt trigger input
3	SNCSL	I	Control input used to switch sync system. High: CKI sync, Low: MCKO sync With pull-down resistor
4	ID/EXP	O	Vertical direction line identification pulse output/exposure time identification pulse output. Switching possible using the serial interface data. (Default: ID)
5	WEN/FLD	O	Memory write timing pulse output/field discrimination pulse output. Switching possible using the serial interface data. (Default: WEN)
6	SSGSL	I	Internal SSG enable. High: Internal SSG valid, Low: External sync valid With pull-down resistor
7	$V_{DD}1$	—	3.3V power supply. (Power supply for common logic block)
8	$V_{DD}2$	—	3.3V power supply. (Power supply for RG)
9	RG	O	CCD reset gate pulse output.
10	$V_{SS}2$	—	GND
11	$V_{SS}3$	—	GND
12	H1	O	CCD horizontal register clock output.
13	H2	O	CCD horizontal register clock output.
14	$V_{DD}3$	—	3.3V power supply. (Power supply for H1/H2)
15	$V_{DD}4$	—	3.3V power supply. (Power supply for CDS)
16	XSHP	O	CCD precharge level sample-and-hold pulse output.
17	XSHD	O	CCD data level sample-and-hold pulse output.
18	TEST1	I	IC test pin 1; normally fixed to GND. With pull-down resistor
19	PBLK	O	Pulse output for horizontal and vertical blanking period pulse cleaning
20	CLPDM	O	CCD dummy signal clamp pulse output.
21	TEST2	—	IC test pin 2; normally fixed to GND. With pull-down resistor
22	OBCLP	O	CCD optical black signal clamp pulse output. The horizontal/vertical OB pattern can be changed using the serial interface data.
23	ADCLK	O	Clock output for analog/digital conversion IC. Logical phase adjustment possible using the serial interface data.
24	$V_{SS}4$	—	GND
25	CKO	O	Inverter output.
26	CKI	I	Inverter input.
27	OSCO	O	Inverter output for oscillation. When not used, leave open or connect a capacitor.
28	OSCI	I	Inverter input for oscillation. When not used, fix to low.
29	$V_{DD}5$	—	3.3V power supply. (Power supply for common logic block)
30	MCKO	O	System clock output for signal processing IC.

Pin No.	Symbol	I/O	Description
31	SSI	I	Serial interface data input for internal mode settings. Schmitt trigger input
32	SCK	I	Serial interface clock input for internal mode settings. Schmitt trigger input
33	SEN	I	Serial interface strobe input for internal mode settings. Schmitt trigger input
34	VR	I/O	Vertical sync signal input/output.
35	HR	I/O	Horizontal sync signal input/output.
36	$V_{SS}5$	—	GND
37	VM	—	GND (GND for vertical driver)
38	V4	O	CCD vertical register clock output/V2 for ICX434.
39	V2	O	CCD vertical register clock output/open for ICX434.
40	V5A	O	CCD vertical register clock output/V3A for ICX434.
41	VH	—	15.0V power supply. (Power supply for vertical driver)
42	V5B	O	CCD vertical register clock output/V3B for ICX434.
43	V1	O	CCD vertical register clock output/open for ICX434.
44	V3A	O	CCD vertical register clock output//V1A for ICX434.
45	VL	—	–7.5V power supply. (Power supply for vertical driver)
46	V3B	O	CCD vertical register clock output/V1B for ICX434.
47	V6	O	CCD vertical register clock output//V4 for ICX434.
48	SUB	O	CCD electronic shutter pulse output.

Electrical Characteristics

DC Characteristics

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	$V_{DD}3$	$V_{DD}a$		3.0	3.3	3.6	V
Supply voltage 2	$V_{DD}2$	$V_{DD}b$		3.0	3.3	3.6	V
Supply voltage 3	$V_{DD}1$, $V_{DD}4$, $V_{DD}5$	$V_{DD}c$		3.0	3.3	3.6	V
Input voltage 1*1	RST, SSI, SCK, SEN	V_{t+}		0.8$V_{DD}c$			V
		V_{t-}				0.2$V_{DD}c$	V
Input voltage 2*2	TEST1, TEST2, SNCSL, SSGSL	V_{IH1}		0.7$V_{DD}c$			V
		V_{IL1}				0.3$V_{DD}c$	V
Input/output voltage	VR, HR	V_{IH2}		0.8$V_{DD}c$			V
		V_{IL2}				0.2$V_{DD}c$	V
		V_{OH1}	Feed current where I_{OH} = –1.2mA	$V_{DD}c$ – 0.8			V
		V_{OL1}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 1	H1, H2	V_{OH2}	Feed current where I_{OH} = –14.0mA	$V_{DD}a$ – 0.8			V
		V_{OL2}	Pull-in current where I_{OL} = 9.6mA			0.4	V
Output voltage 2	RG	V_{OH3}	Feed current where I_{OH} = –3.3mA	$V_{DD}b$ – 0.8			V
		V_{OL3}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 3	XSHP, XSHD, PBLK, OBCLP, CLPDM, ADCLK	V_{OH4}	Feed current where I_{OH} = –3.3mA	$V_{DD}c$ – 0.8			V
		V_{OL4}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 4	CKO	V_{OH5}	Feed current where I_{OH} = –6.9mA	$V_{DD}c$ – 0.8			V
		V_{OL5}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output voltage 5	MCKO	V_{OH6}	Feed current where I_{OH} = –3.3mA	$V_{DD}c$ – 0.8			V
		V_{OL6}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Output voltage 6	ID/EXP, WEN/FLD	V_{OH7}	Feed current where I_{OH} = –2.4mA	$V_{DD}c$ – 0.8			V
		V_{OL7}	Pull-in current where I_{OL} = 4.8mA			0.4	V
Output current 1	V1, V3A, V3B, V5A, V5B, V2, V4, V6	I_{OL}	V1, V2, V3A/B, V4, V5A/B, V6 = –8.25V	10.0			mA
		I_{OM1}	V1, V2, V3A/B, V4, V5A/B, V6 = –0.25V			–5.0	mA
		I_{OM2}	V1, V3A/B, V5A/B = 0.25V	5.0			mA
		I_{OH}	V1, V3A/B, V5A/B = 14.75V			–7.2	mA
Output current 2	SUB	I_{OSL}	SUB = –8.25V	5.4			mA
		I_{OSH}	SUB = 14.75V			–4.0	mA

*1 These input pins are Schmitt trigger inputs.

*2 This input pin is with pull-down register in the IC.

Inverter I/O Characteristics for Oscillation (Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	OSCI	LVth			$V_{DDC}/2$		V
Input voltage	OSCI	V_{IH}		$0.7V_{DDC}$			V
		V_{IL}				$0.3V_{DDC}$	V
Output voltage	OSCO	V_{OH}	Feed current where I_{OH} = –3.6mA	V_{DDC} – 0.8			V
		V_{OL}	Pull-in current where I_{OL} = 2.4mA			0.4	V
Feedback resistor	OSCI, OSCO	RFB	$V_{IN} = V_{DDC}$ or V_{SS}	500k	2M	5M	Ω
Oscillation frequency	OSCI, OSCO	f		20		50	MHz

Inverter Input Characteristics for Base Oscillation Clock Duty Adjustment

(Within the recommended operating conditions)

Item	Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logical Vth	CKI	LVth			$V_{DDC}/2$		V
Input voltage		V_{IH}		$0.7V_{DDC}$			V
		V_{IL}				$0.3V_{DDC}$	V
Input amplitude		V_{IN}	fmax 50MHz sine wave	0.3			Vp-p

Note) Input voltage is the input voltage characteristics for direct input from an external source. Input amplitude is the input amplitude characteristics in the case of input through a capacitor.

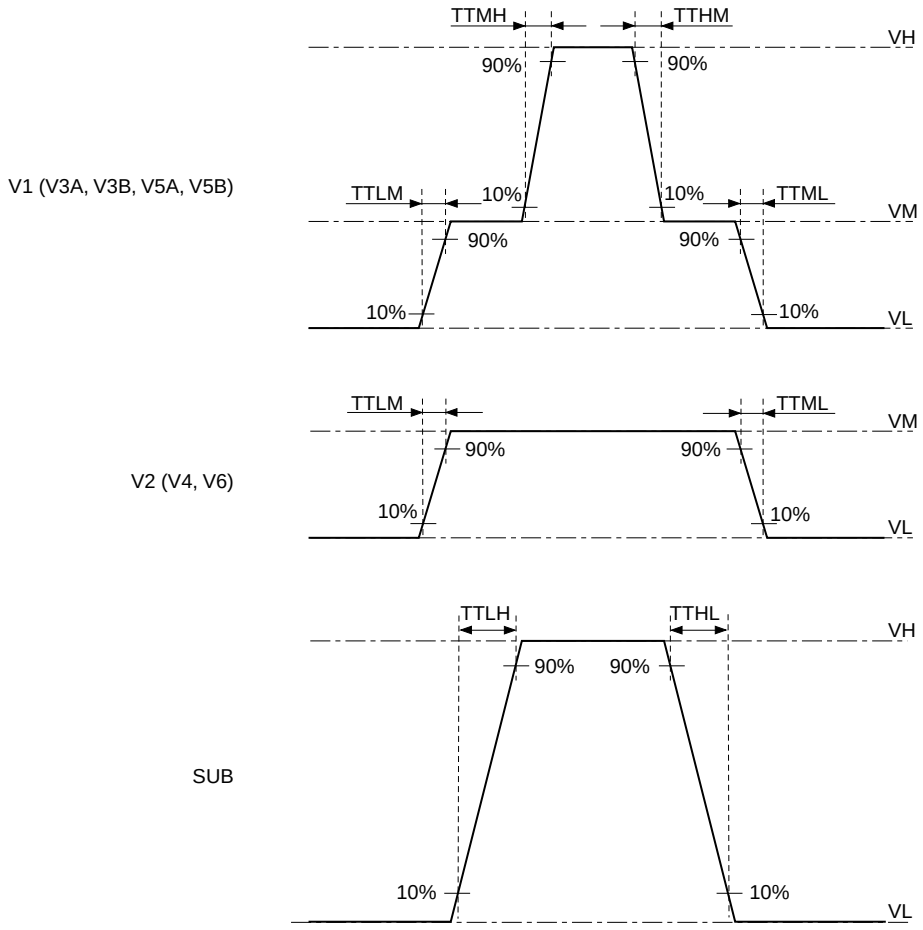
Switching Characteristics (VH = 15.0V, VM = GND, VL = –7.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Rise time	TTLM	VL to VM	200	350	500	ns
	TTMH	VM to VH	200	350	500	ns
	TTLH	VL to VH	30	60	90	ns
Fall time	TTML	VM to VL	200	350	500	ns
	TTHM	VH to VM	200	350	500	ns
	TTHL	VH to VL	30	60	90	ns
Output noise voltage	VCLH				1.0	V
	VCLL				1.0	V
	VCMH				1.0	V
	VCML				1.0	V

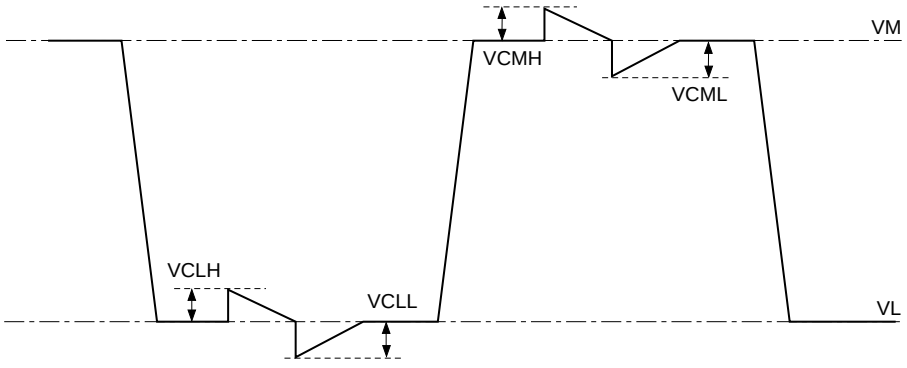
Notes)

1) The MOS structure of this IC has a low tolerance for static electricity, so full care should be given for measures to prevent electrostatic discharge.
2) For noise and latch-up countermeasures, be sure to connect a by-pass capacitor (0.1µF or more) between each power supply pin (VH, VL) and GND.
3) To protect the CCD image sensor, clamp the SUB pin output at VH before input to the CCD image sensor.

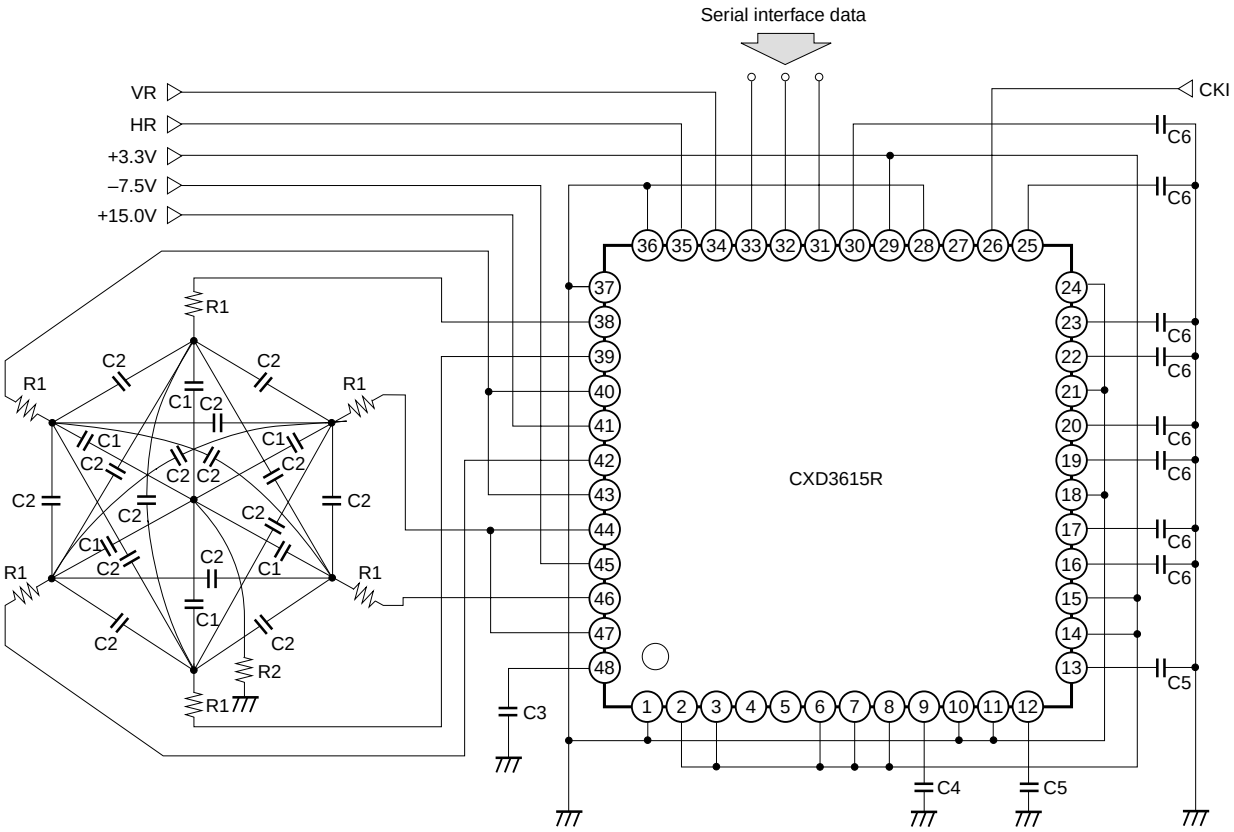
Switching Waveforms



Waveform Noise



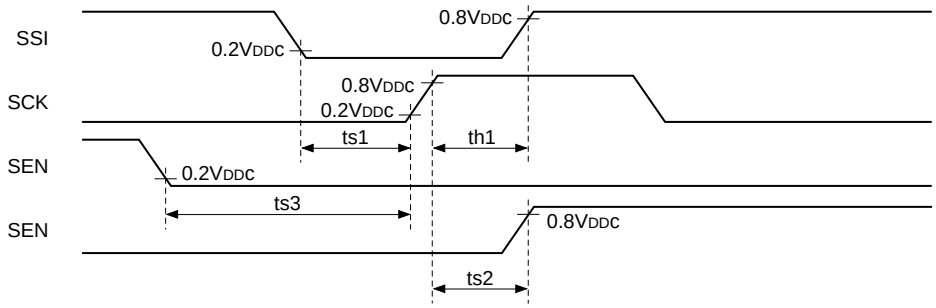
Measurement Circuit



C1: 3300pF C2: 560pF C3: 820pF C4: 8pF C5: 140pF C6: 10pF
R1: 30Ω R2: 10Ω

AC Characteristics

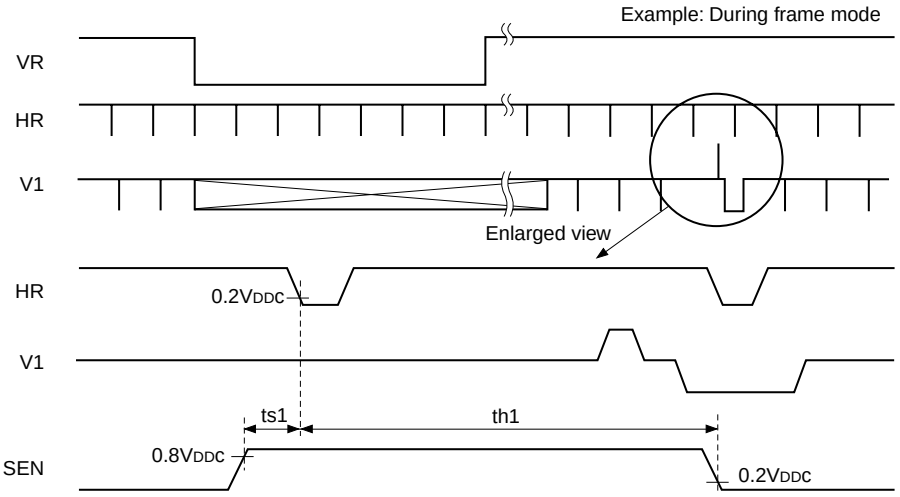
AC characteristics between the serial interface clocks



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SSI setup time, activated by the rising edge of SCK	20			ns
th1	SSI hold time, activated by the rising edge of SCK	20			ns
ts2	SCK setup time, activated by the rising edge of SEN	20			ns
ts3	SEN setup time, activated by the rising edge of SCK	20			ns

Serial interface clock internal loading characteristics (1)



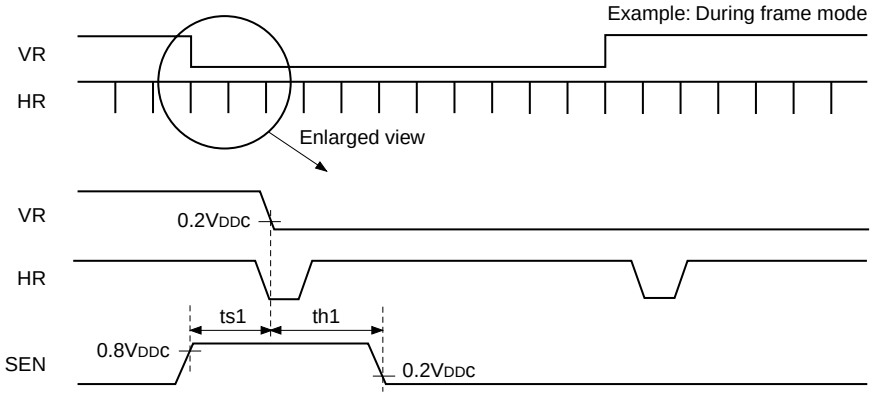
* Be sure to maintain a constantly high SEN logic level near the falling edge of the HR in the horizontal period during which V1, V3A/B and V5A/B values take the ternary value and during that horizontal period.

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN setup time, activated by the falling edge of HR	0			ns
th1	SEN hold time, activated by the falling edge of HR	123			µs

* Restriction for the ICX432 operating frequency of 24.3MHz in draft mode

Serial interface clock internal loading characteristics (2)



* Be sure to maintain a constantly high SEN logic level near the falling edge of VR.

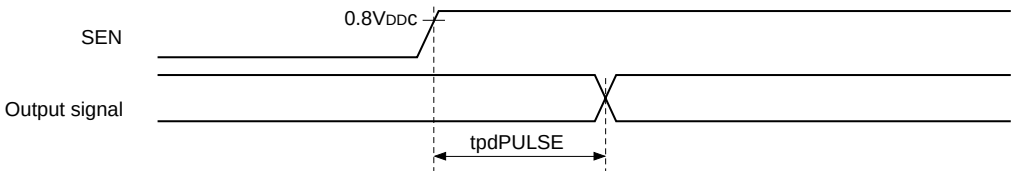
(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	SEN setup time, activated by the falling edge of VR	0			ns
th1	SEN hold time, activated by the falling edge of VR	200			ns

* Restriction for the ICX432 operating frequency of 24.3MHz in draft mode

Serial interface clock output variation characteristics

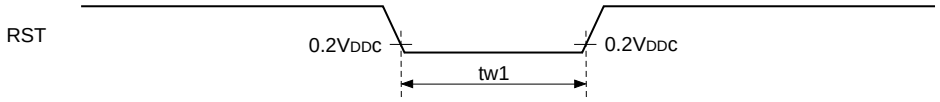
Normally, the serial interface data is loaded to the CXD3615R at the timing shown in "Serial interface clock internal loading characteristics (1)" above. However, one exception to this is when the data such as STB is loaded to the CXD3615R and controlled at the rising edge of SEN. See "Description of Operation".



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpdPULSE	Output signal delay, activated by the rising edge of SEN	5		100	ns

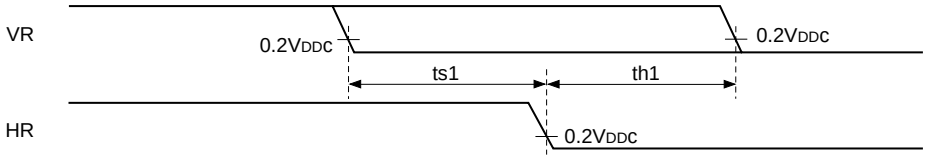
RST loading characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tw1	RST pulse width	35			ns

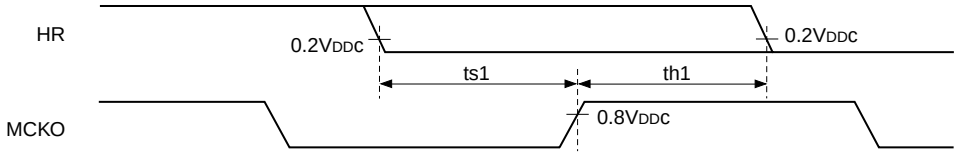
VR and HR phase characteristics



(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	VR setup time, activated by the falling edge of HR	0			ns
th1	VR hold time, activated by the falling edge of HR	0			ns

HR loading characteristics

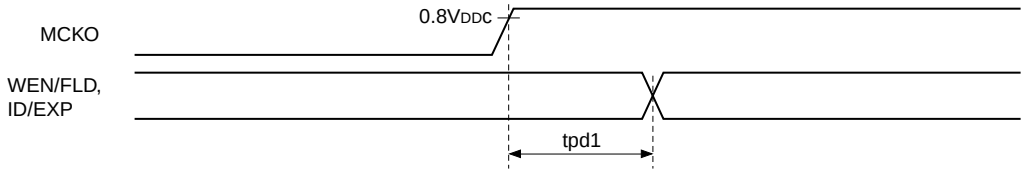


MCKO load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
ts1	HR setup time, activated by the rising edge of MCKO	13			ns
th1	HR hold time, activated by the rising edge of MCKO	0			ns

Output variation characteristics



WEN/FLD and ID/EXP load capacitance = 10pF

(Within the recommended operating conditions)

Symbol	Definition	Min.	Typ.	Max.	Unit
tpd1	Time until the above outputs change after the rise of MCKO	20		60	ns

Description of Operation

Pulses output from the CXD3615R are controlled mainly by the RST pin and by the serial interface data. The Pin Status Table is shown below, and the details of serial interface control are described on the following pages.

Pin Status Table

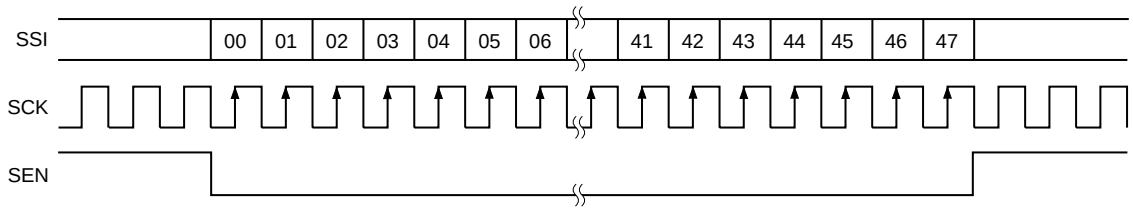
Pin No.	Symbol	CAM	SLP	SST	STB	RST	Pin No.	Symbol	CAM	SLP	SST	STB	RST
1	$V_{SS}1$	—					25	CKO	ACT	ACT	L	L	ACT
2	RST	ACT	ACT	ACT	ACT	L	26	CKI	ACT	ACT	ACT	ACT	ACT
3	SNCSL	ACT	ACT	ACT	ACT	ACT	27	OSCO	ACT	ACT	ACT	ACT	ACT
4	ID/EXP	ACT	L	L	L	L	28	OSCI	ACT	ACT	ACT	ACT	ACT
5	WEN/FLD	ACT	L	L	L	L	29	$V_{DD}5$	—				
6	SSGSL	ACT	ACT	ACT	ACT	ACT	30	MCKO	ACT	ACT	L	L	ACT
7	$V_{DD}1$	—					31	SSI	ACT	ACT	ACT	ACT	DIS
8	$V_{DD}2$	—					32	SCK	ACT	ACT	ACT	ACT	DIS
9	RG	ACT	L	L	L	ACT	33	SEN	ACT	ACT	ACT	ACT	DIS
10	$V_{SS}2$	—					34	VR*1	ACT	L	L	L	H
11	$V_{SS}3$	—					35	HR*1	ACT	L	L	L	H
12	H1	ACT	L	L	L	ACT	36	$V_{SS}5$	—				
13	H2	ACT	L	L	L	ACT	37	VM	—				
14	$V_{DD}3$	—					38	V4	ACT	VM	VM	VM	VM
15	$V_{DD}4$	—					39	V2	ACT	VM	VM	VM	VM
16	XSHP	ACT	L	L	L	ACT	40	V5A	ACT	VH	VM	VH	VL
17	XSHD	ACT	L	L	L	ACT	41	VH	—				
18	TEST1	—					42	V5B	ACT	VH	VM	VH	VL
19	PBLK	ACT	L	L	L	H	43	V1	ACT	VH	VM	VH	VM
20	CLPDM	ACT	L	L	L	H	44	V3A	ACT	VH	VM	VH	VM
21	TEST2	—					45	VL	—				
22	OBCLP	ACT	L	L	L	H	46	V3B	ACT	VH	VM	VH	VM
23	ADCLK	ACT	L	L	L	ACT	47	V6	ACT	VM	VM	VM	VL
24	$V_{SS}4$	—					48	SUB	ACT	VH	VL	VH	VL

*1 It is for output. For input, all items are “ACT”.

Note) ACT means that the circuit is operating, and DIS means that loading is stopped. L indicates a low output level, and H a high output level in the controlled status.
Also, VH, VM and VL indicate the voltage levels applied to VH (Pin 41), VM (Pin 37) and VL (Pin 45), respectively, in the controlled status.

Serial Interface Control

The CXD3615R basically loads and reflects the serial interface data sent in the following format in the readout portion at the falling edge of HR. Here, readout portion specifies the horizontal period during which V1, V3A/B and V5A/B, etc. take the ternary value.
Note that some items reflect the serial interface data at the falling edge of VR or the rising edge of SEN.



These are two categories of serial interface data: the CXD3615R drive control data (hereafter “control data”) and electronic shutter data (hereafter “shutter data”).
The details of each data are described below.

Control Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08	CTG	Category switching	See the category section.		0
D09 to D11	—	—	—	—	All 0
D12, D13	MODE	Drive mode switching	See the drive mode section.		0
D14, D15	—	—	—	—	0
D16	NTPL	Internal SSG function switching*1	NTSC	PAL	0
D17	CCD	CCD switching*1	ICX432	ICX434	0
D18, D19	—	—	—	—	0
D20	SMD	Electronic shutter mode switching*2	OFF	ON	0
D21	HTSG	HTSG control switching*2	OFF	ON	0
D22 to D30	—	—	—	—	All 0
D31	FLD	WEN/FLD output switching	WEN	FLD	0
D32	FGOB	Wide OBCLP generation switching	OFF	ON	0
D33	EXP	ID/EXP output switching	ID	EXP	0
D34, D35	PTOB	OBCLP waveform pattern switching	See the OBCLP waveform pattern section.		All 0
D36, D37	LDAD	ADCLK logic phase adjustment	See the ADCLK logic phase section.		All 0
D38, D39	STB	Standby control	See the standby section.		All 0
D40 to D47	—	—	—	—	All 0

*1 See the drive mode section.

*2 See the electronic shutter section.

Shutter Data

Data	Symbol	Function	Data = 0	Data = 1	RST
D00 to D07	CHIP	Chip enable	10000001 → Enabled Other values → Disabled		All 0
D08	CTG	Category switching	See the category section.		0
D09	—	—	—	—	0
D10 to D19	SVR	Electronic shutter vertical period specification	See the electronic shutter section.		All 0
D20 to D31	SHR	Electronic shutter horizontal period specification	See the electronic shutter section.		All 0
D32 to D41	SPL	High-speed shutter position specification	See the electronic shutter section.		All 0
D42 to D47	—	—	—	—	All 0

Detailed Description of Each Data

Shared data: D08 CTG [Category]

Of the data provided to the CXD3615R by the serial interface, the CXD3615R loads D09 and subsequent data to each data register as shown in the table below according to D08.

D08	Description of operation
0	Loading to control data register
1	Loading to shutter data register

Note that the CXD3615R can apply these categories consecutively within the same vertical period. However, care should be taken as the data is overwritten if the same category is applied.

Control data: D12 and D13 MODE [Drive mode]

The CXD3615R realizes various drive modes using control data D12 and D13 MODE, D16 NTPL and D17 CCD. The drive mode-related bits are loaded to the CXD3615R and reflected at the falling edge of VR. The details are described below.

First, the various basic drive modes are shown below. These modes are switched using control data D12 and D13 MODE.

D13	D12	Description of operation
0	0	Draft mode (default)
0	1	Frame mode
1	0	AF mode*1
1	1	Test mode

*1 These are both test mode for the ICX434.

Draft mode is the pulse elimination drive mode in the ICX432/434.

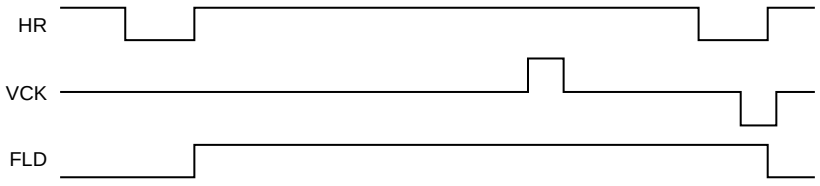
AF mode is the pulse eliminator drive mode based on draft mode, and is a high frame rate drive mode that can be used for purposes such as auto focus (AF).

Frame mode is the ICX432/434 drive mode in which the data for all lines are read.

In addition to these modes, the CXD3615R has functions for switching the applicable CCD with D17 CCD, and for switching VR/HR to NTSC equivalent or PAL equivalent with D16 NTPL.

Control data: D31 FLD [WEN/FLD output switching]

The WEN/FLD pin (Pin 5) output can be switched to the WEN pulse or the FLD pulse. The default is "WEN". See the Timing Charts for the WEN pulse. The FLD pulse rises in the readout block in the A Field, and falls in the horizontal period immediately thereafter. That is to say, FLD is a 1H high-active pulse. The transition points are the same as for ID/WEN.



Control data: D32 FGOB [Wide OBCLP generation]

This controls wide OBCLP generation during the vertical OPB period. When this function is on, the D34 and D35 PTOB setting is invalid for the output block. See the Timing Charts for the actual operation. The default is "OFF".

D32	Description of operation
0	Wide OBCLP generation OFF
1	Wide OBCLP generation ON

Control data D34 and D35 PTOB [OBCLP waveform pattern]

This designates the OBCLP waveform pattern. The default is "Normal". See the Timing Charts for details of the decoding values.

D35	D34	Waveform pattern	ICX432	ICX434
0	0	 (Normal)	20 to 44	19 to 45
0	1	 (Shifted rearward)	14 to 38	13 to 39
1	0	 (Shifted forward)	26 to 50	25 to 51
1	1	 (Wide)	14 to 50	13 to 51

Control data: D36 and D37 LDAD [ADCLK logic phase]

This indicates the ADCLK logic phase adjustment data. The default is "90°" relative to MCKO.

D37	D36	Degree of adjustment (°)
0	0	0
0	1	90
1	0	180
1	1	270

Control data: D38 and D39 STB [Standby]

The operating mode is switched as follows. However, the standby bits are loaded to the CXD3615R and control is applied immediately at the rising edge of SEN.

D39	D38	Symbol	Operating mode
0	0	CAM	Normal operating mode
0	1	SLP	Sleep mode
1	0	SST	Siesta mode
1	1	STB	Standby mode

See the Pin Status Table for the pin status in each mode.

Control data/shutter data: [Electronic shutter]

The CXD3615R realizes various electronic shutter functions by using control data D20 SMD and D21 HTSG and shutter data D10 to D19 SVR, D20 to D31 SHR and D32 to D41 SPL. These functions are described in detail below.

First, the various modes are shown below. These modes are switched using control data D20 SMD.

D20	Description of operation
0	Electronic shutter stopped mode
1	Electronic shutter mode

The electronic shutter data is expressed as shown in the table below using D20 to D31 SHR as an example. However, MSB (D31) is a reserved bit for the future specification, and is handled as a dummy bit on this IC.

MSB											LSB
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20
X	0	0	1	1	1	0	0	0	0	1	1
	↓				↓				↓		
	1				C				3		

→ SHR is expressed as 1C3h.

[Electronic shutter stopped mode]

During this mode, all shutter data items are invalid.

SUB is not output in this mode, so the shutter speed is the accumulation time for one field.

[Electronic shutter mode]

During this mode, the shutter data items have the following meanings.

Symbol	Data	Description
SVR	Shutter: D10 to D19	Number of vertical periods specification (000h ≤ SVR ≤ 3FFh)
SHR	Shutter: D20 to D31	Number of horizontal periods specification (000h ≤ SHR ≤ 7FFh)
SPL	Shutter: D32 to D41	Vertical period specification for high-speed shutter operation (000h ≤ SPL ≤ 3FFh)

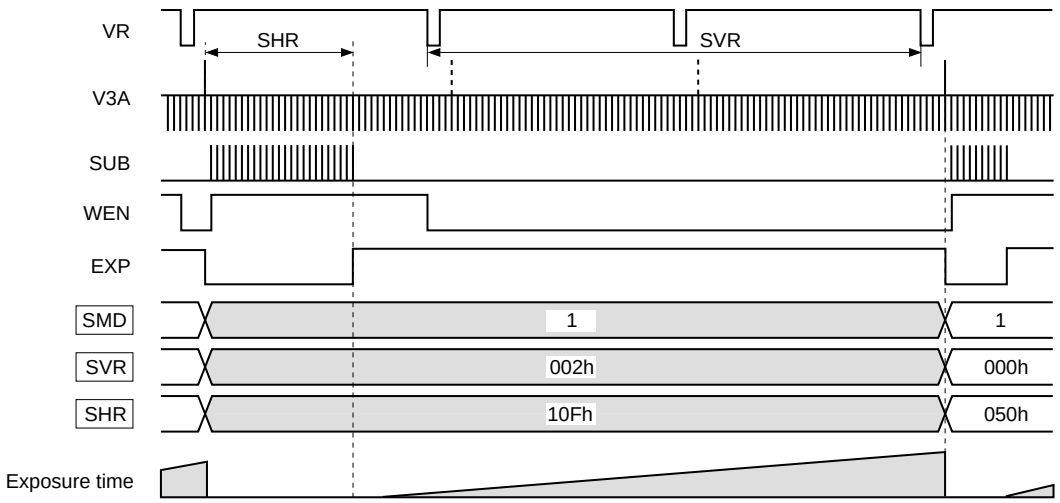
Note) The bit data definition area is assured in terms of the CXD3615R functions, and does not assure the CCD characteristics.

The period during which SVR and SHR are specified together is the shutter speed. An image of the exposure time calculation formula is shown below. In actual operation, the precise exposure time is calculated from the operating frequency, VR and HR periods, decoding value during the horizontal period, and other factors.

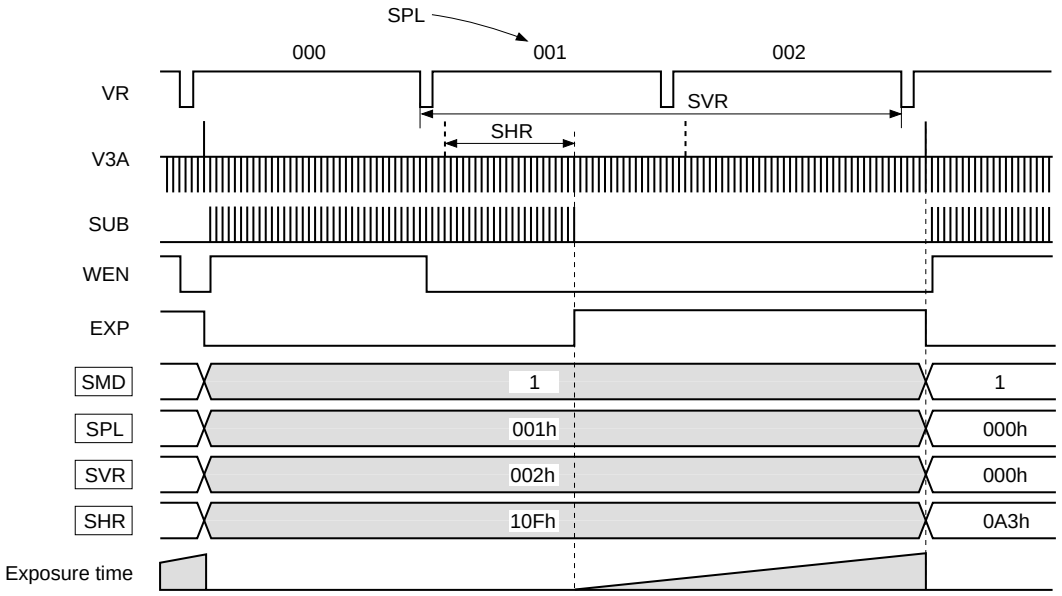
(Exposure time) = SVR × (1V period) + {(number of HR per 1V) – (SHR + 1)} × (1H period)
+ (distance from SUB to SG during the readout period)

Concretely, when specifying high-speed shutter, SVR is set to "000h". (See the figure.) During low-speed shutter, or in other words when SVR is set to "001h" or higher, the serial interface data is not loaded until this period is finished.

The vertical period indicated here corresponds to one field in each drive mode. In addition, the number of horizontal periods applied to SHR can be considered as (number of SUB pulses – 1). The readout period is normally the horizontal period during which V1, V3A/B and V5A/B (for the ICX432) are ternary values, and SG indicates these ternary level readout pulses.



Further, SPL can be used during this mode to specify the SUB output at the desired vertical period during the low-speed shutter period.
In the case below, SUB is output based on SHR at the SPL vertical period out of (SVR + 1) vertical periods.

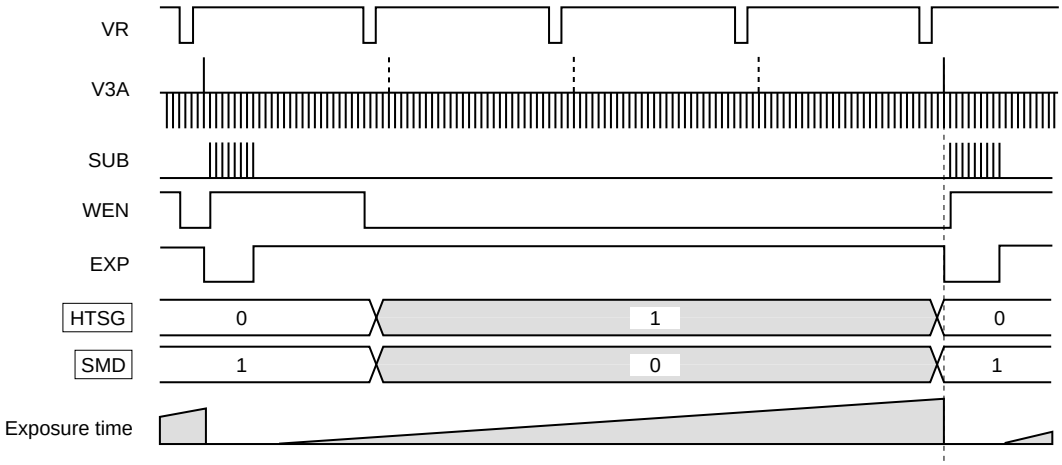


Incidentally, SPL is counted as "000h", "001h", "002h" and so on in conformance with SVR.
Using this function it is possible to achieve smooth exposure time transitions when changing from low-speed shutter to high-speed shutter or vice-versa.

[HTSG control mode]

This mode controls the V1, V3A/B and V5A/B (for the ICX432) ternary level outputs (readout pulse block) using D21 HTSG.

D21	Description of operation
0	Readout pulse (SG) normal operation
1	HTSG control mode



[EXP pulse]

The ID/EXP pin (Pin 4) output can be switched between the ID pulse or the EXP pulse using D33 EXP. The default is the "ID" pulse. See the Timing Charts for the ID pulse. The EXP pulse indicates the exposure time when it is high. In principle, the transition points are the last SUB pulse falling edge and the readout pulse falling edge, that is to say from the time the charge is completely discharged until transfer ends. However, when the readout pulse timing differs within the same readout block such as in draft mode, the average value is used. Then, when there is no SUB pulse in the next field, the readout pulse falling edge is defined as the start position. However, in this case the transition points overlap and disappear, so a tentative start position is defined.
This is shown below.

		SG ↓	Tentative start position
[ICX432]	Frame mode	1460	1480
	Draft/AF mode	1682	1784
[ICX434]	Frame mode	A: 1071	1091
		B: 1175	1195
	Draft mode	1123	1175

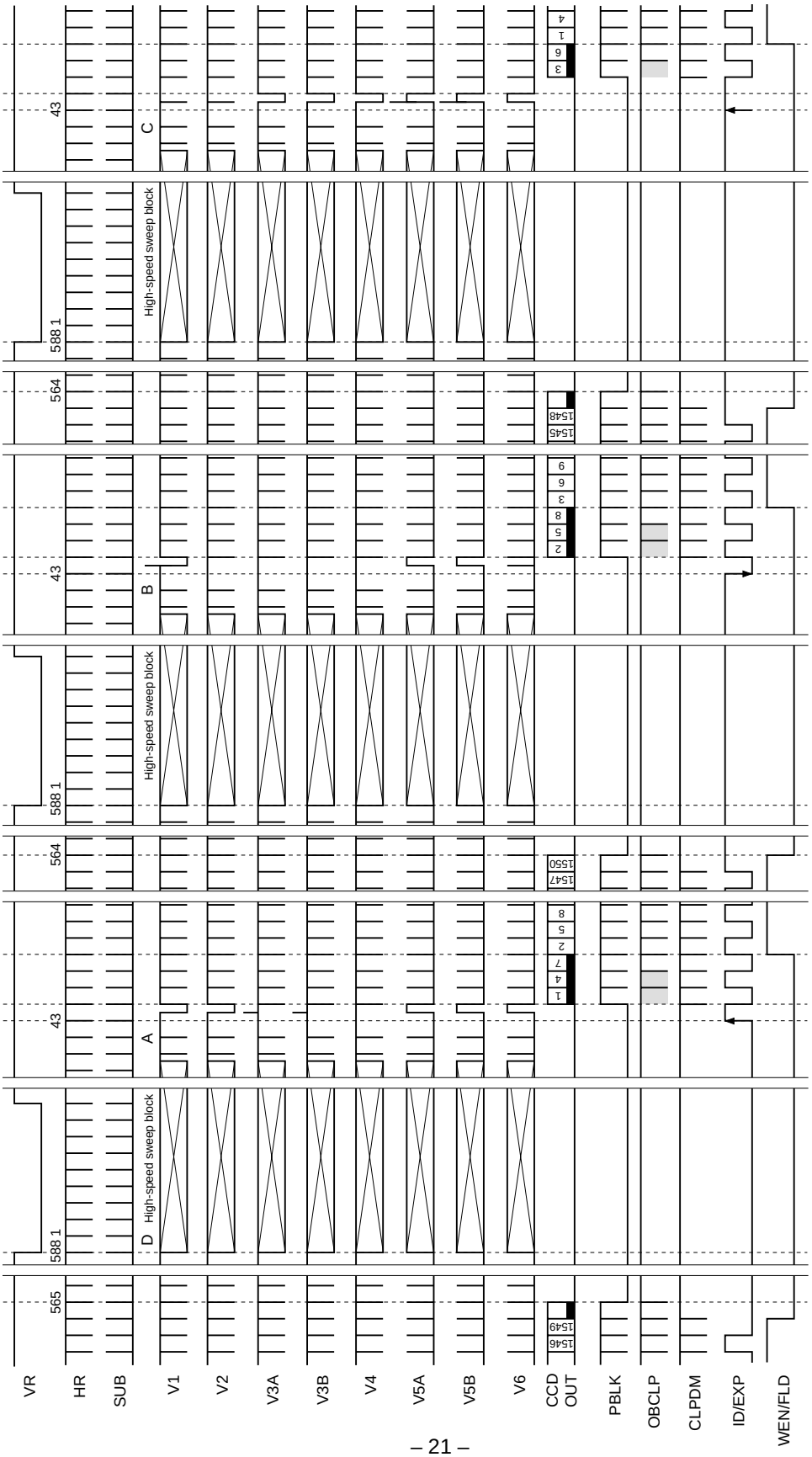
See the EXP pulse indicated in the explanatory diagrams under [Electronic shutter] for an image of operation.

Chart-A1 Vertical Direction Timing Chart

Applicable CCD image sensor

• ICX432

MODE **Frame mode**



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to (high, low, high) in the horizontal periods of each readout block (A, B, C).
* WEN/FLD of this chart shows WEN.
* The shaded portion of OBCLP shows the range over which the wide OBCLP can be set by the serial interface data.
* VR of this chart is NTSC equivalent pattern 587H (1H: 2760ck) + 1500ck units. For PAL equivalent pattern, it is 704H + 960ck units.

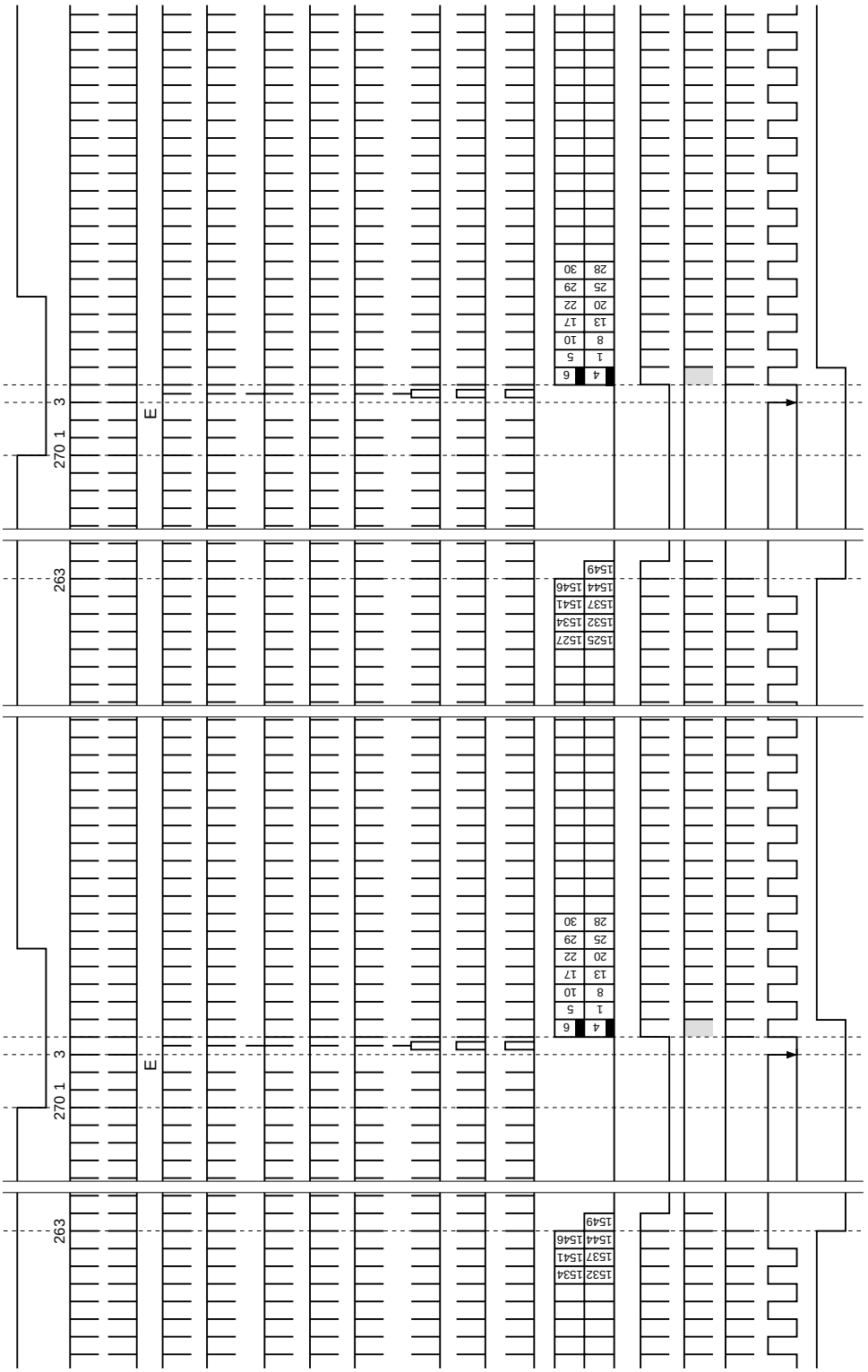
Chart-A2 Vertical Direction Timing Chart

MODE

Draft mode

Applicable CCD image sensor

• ICX432



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to low in the horizontal periods of each readout block (E).
* WEN/FLD of this chart shows WEN.
* The shaded portion of OBCLP shows the range over which the wide OBCLP can be set by the serial interface data.
* VR of this chart is NTSC equivalent pattern 269H (1H: 3004ck) + 2734ck units. For PAL equivalent pattern, it is 323H + 1708ck units.

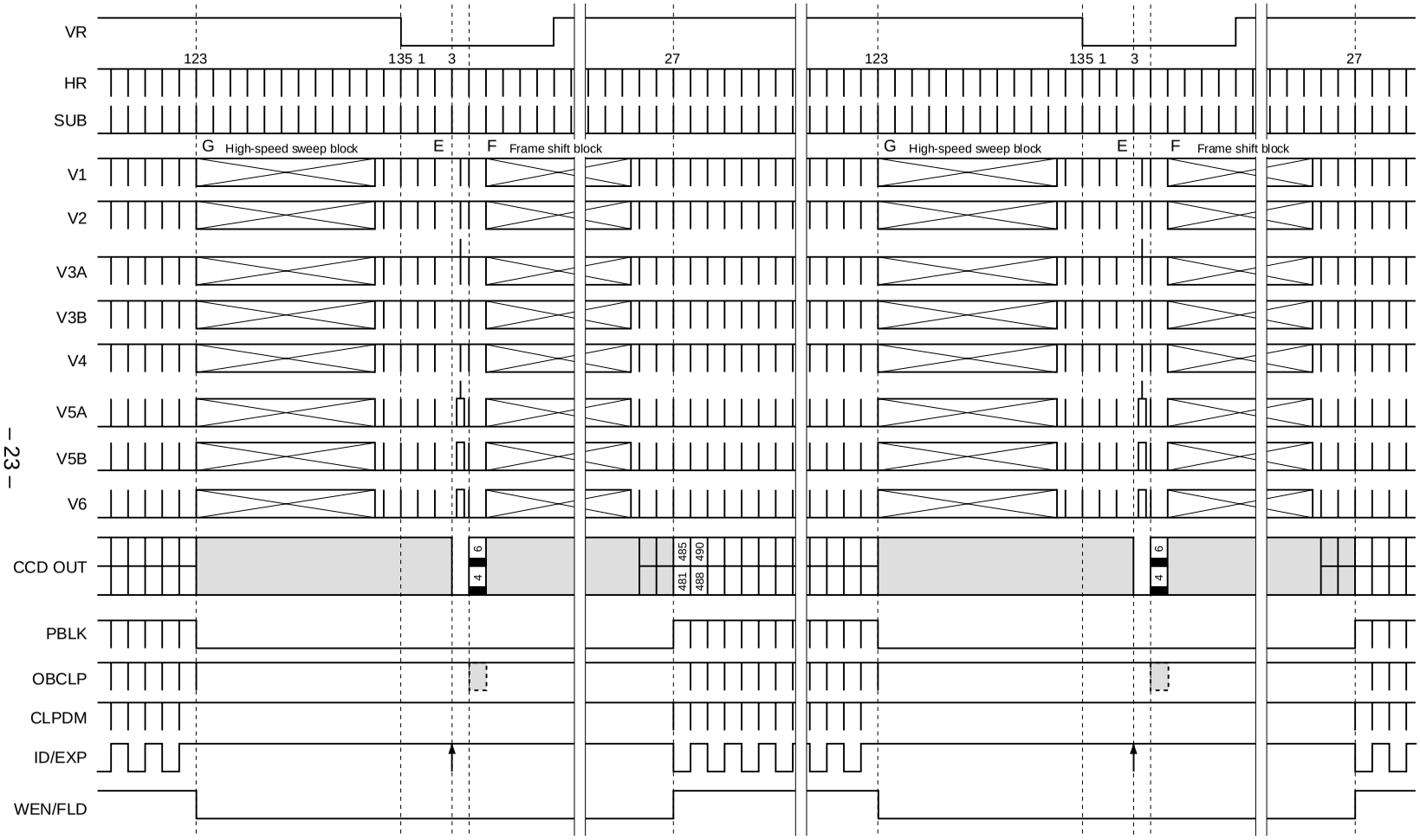
Chart-A3 Vertical Direction Timing Chart

MODE

AF mode

Applicable CCD image sensor

• ICX432



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to high in the horizontal periods of each readout block (E).
* WEN/FLD of this chart shows WEN.
* The shaded portion of OBCLP shows the range over which the wide OBCLP can be set by the serial interface data.
* VR of this chart is NTSC equivalent pattern 134H (1H: 3004ck) + 2869ck units. For PAL equivalent pattern, it is 161H + 2356ck units. In addition, for PAL equivalent pattern, the high-speed sweep block starts from 150H.

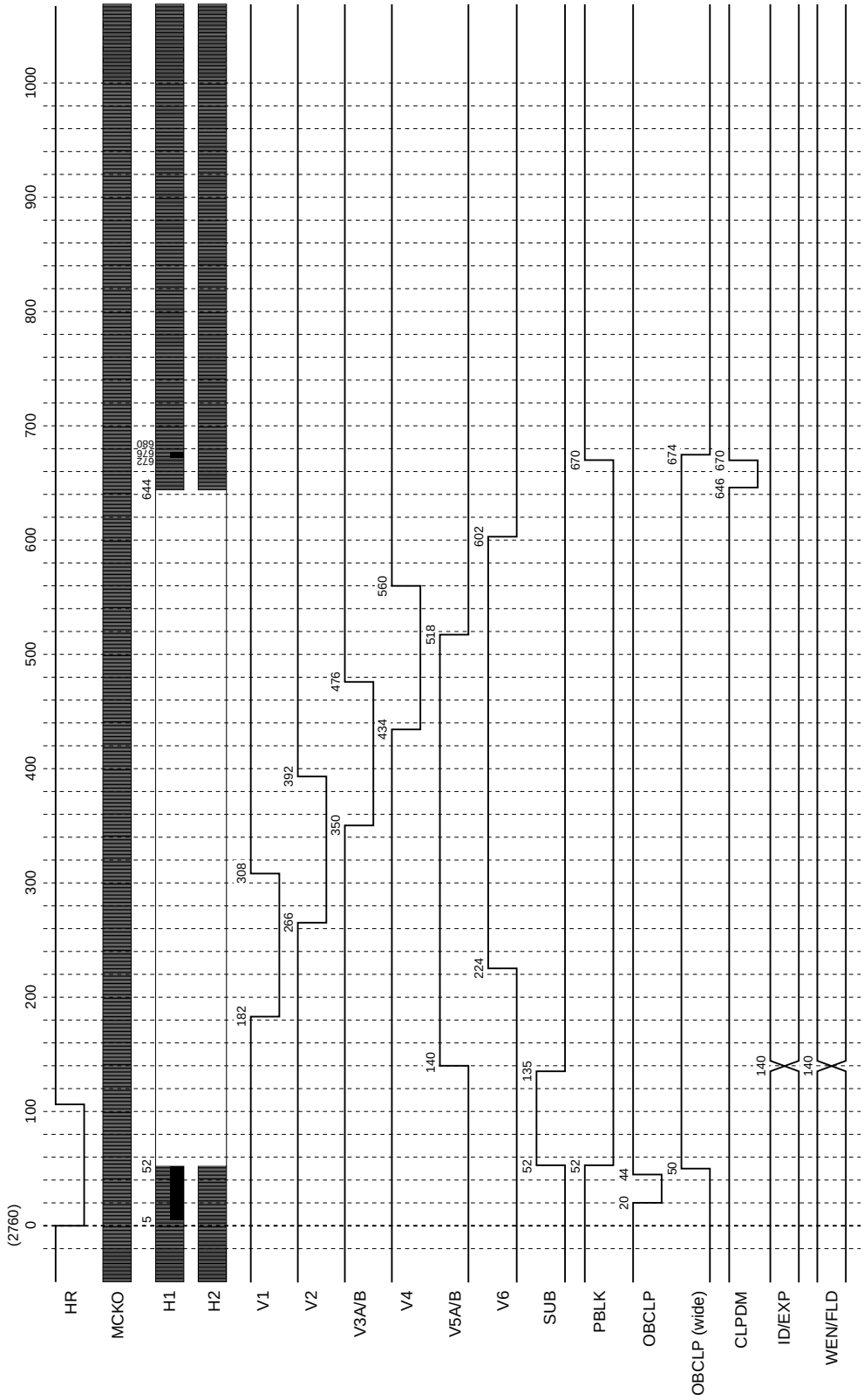
Chart-A4 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX432



* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-A1.
* OBCLP also has patterns of 14-38, 26-50 and 14-50 for a total of four patterns. OBCLP (wide) is output in the shaded portions shown in Chart-A1. These timings can be switched by the serial interface data.

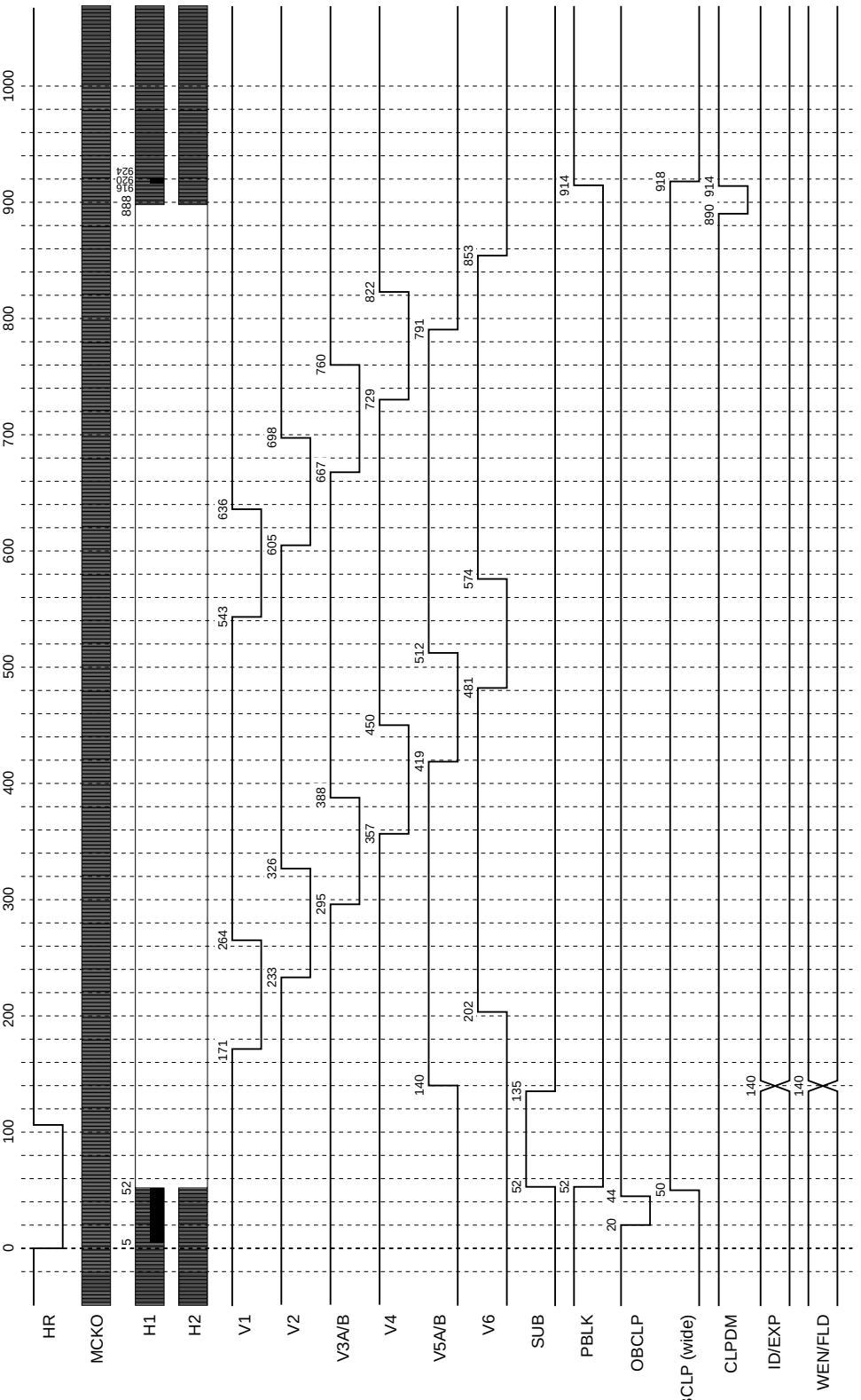
Chart-A5 Horizontal Direction Timing Chart

MODE

Draft/AF mode

Applicable CCD image sensor

• ICX432

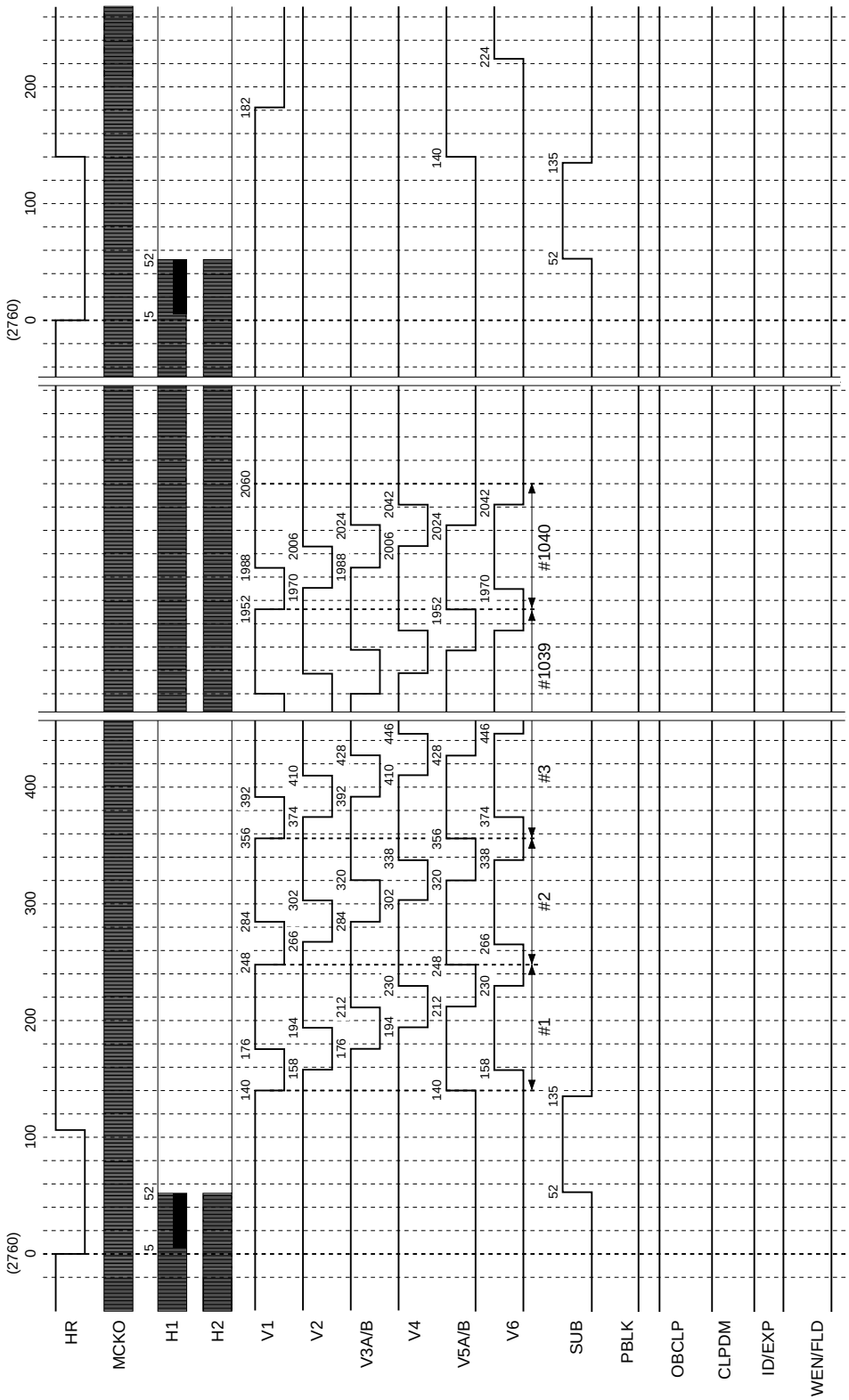


* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-A2 and A3.
* OBCLP also has patterns of 14-38, 26-50 and 14-50 for a total of four patterns. OBCLP (wide) is output in the shaded portions shown in Chart-A2 and A3. These timings can be switched by the serial interface data.

Chart-A6 Horizontal Direction Timing Chart
(High-speed sweep: D)

MODE
Frame mode

Applicable CCD image sensor
• ICX432

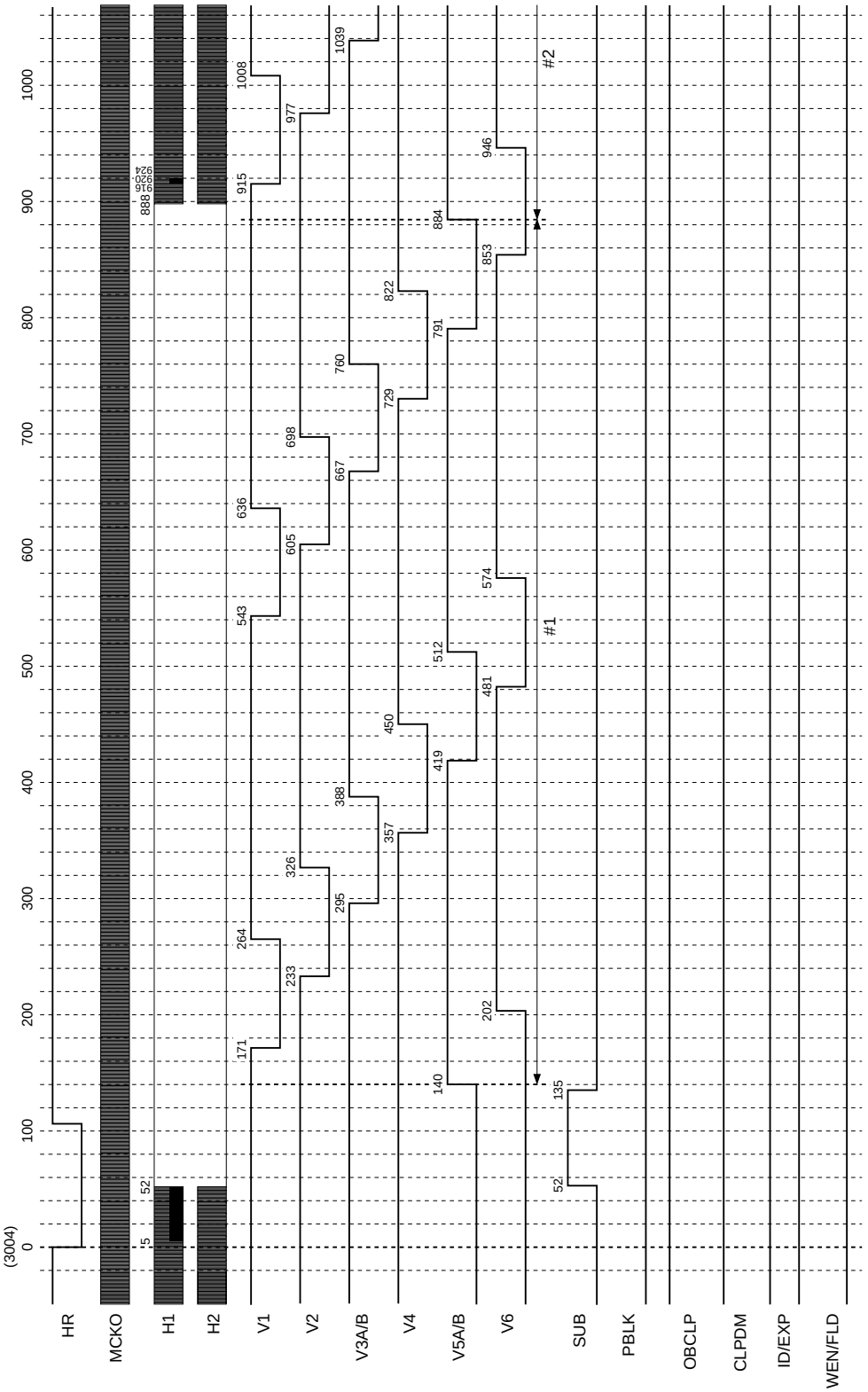


* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).

Chart-A7 Horizontal Direction Timing Chart
(Frame shift: F)

MODE
AF mode

Applicable CCD image sensor
• ICX432

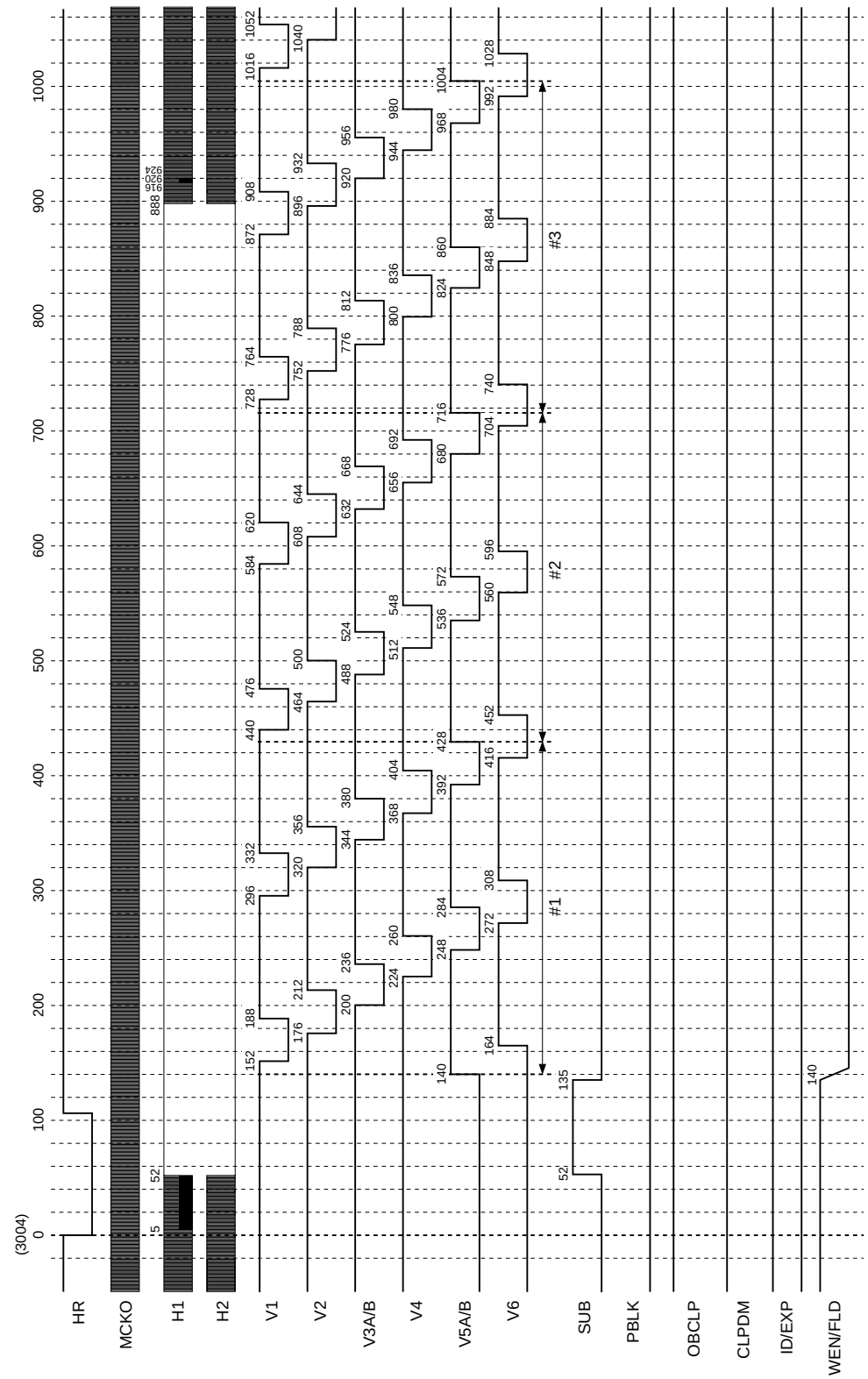


* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* Frame shift of V1, V2, V3A/B, V4, V5A/B and V6 is performed up to 24H 1096ck (#78).

Chart-A8 Horizontal Direction Timing Chart
(High-speed sweep: G)

MODE
AF mode

Applicable CCD image sensor
• ICX432

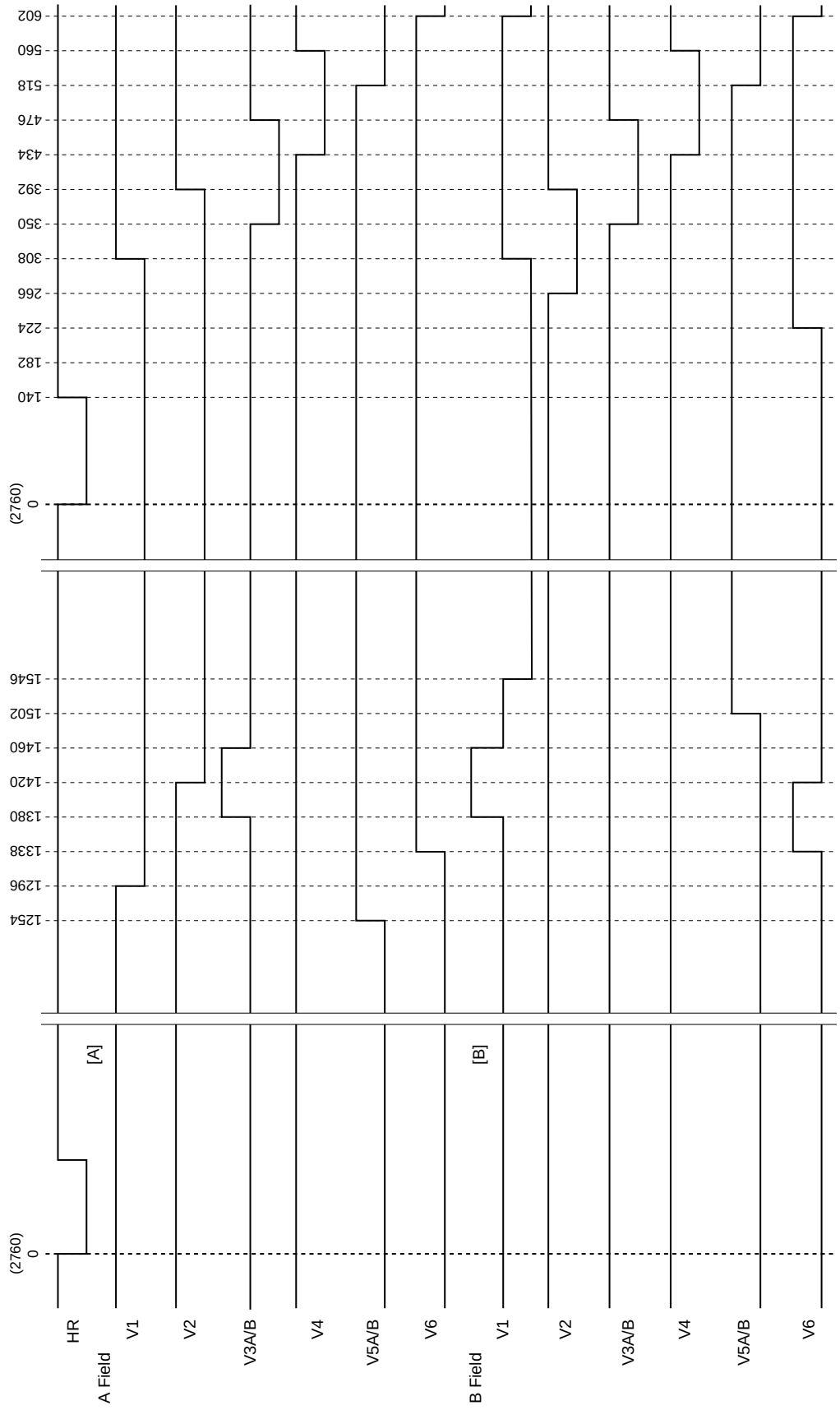


* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* High-speed sweep of V1, V2, V3A/B, V4, V5A/B and V6 is performed up to 133H 2932ck (#114).

Chart-A9a Horizontal Direction Timing Chart

MODE
Frame mode

Applicable CCD image sensor
• ICX432



* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).

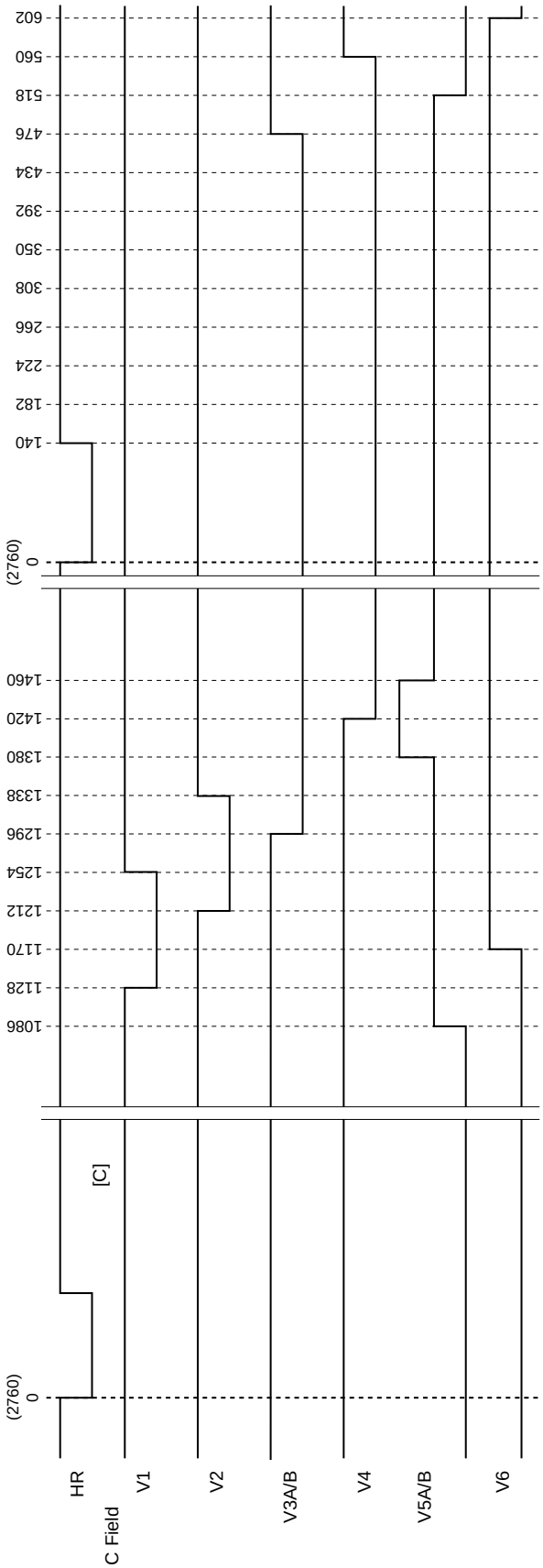
Chart-A9b Horizontal Direction Timing Chart

Applicable CCD image sensor

• ICX432

MODE

Frame mode

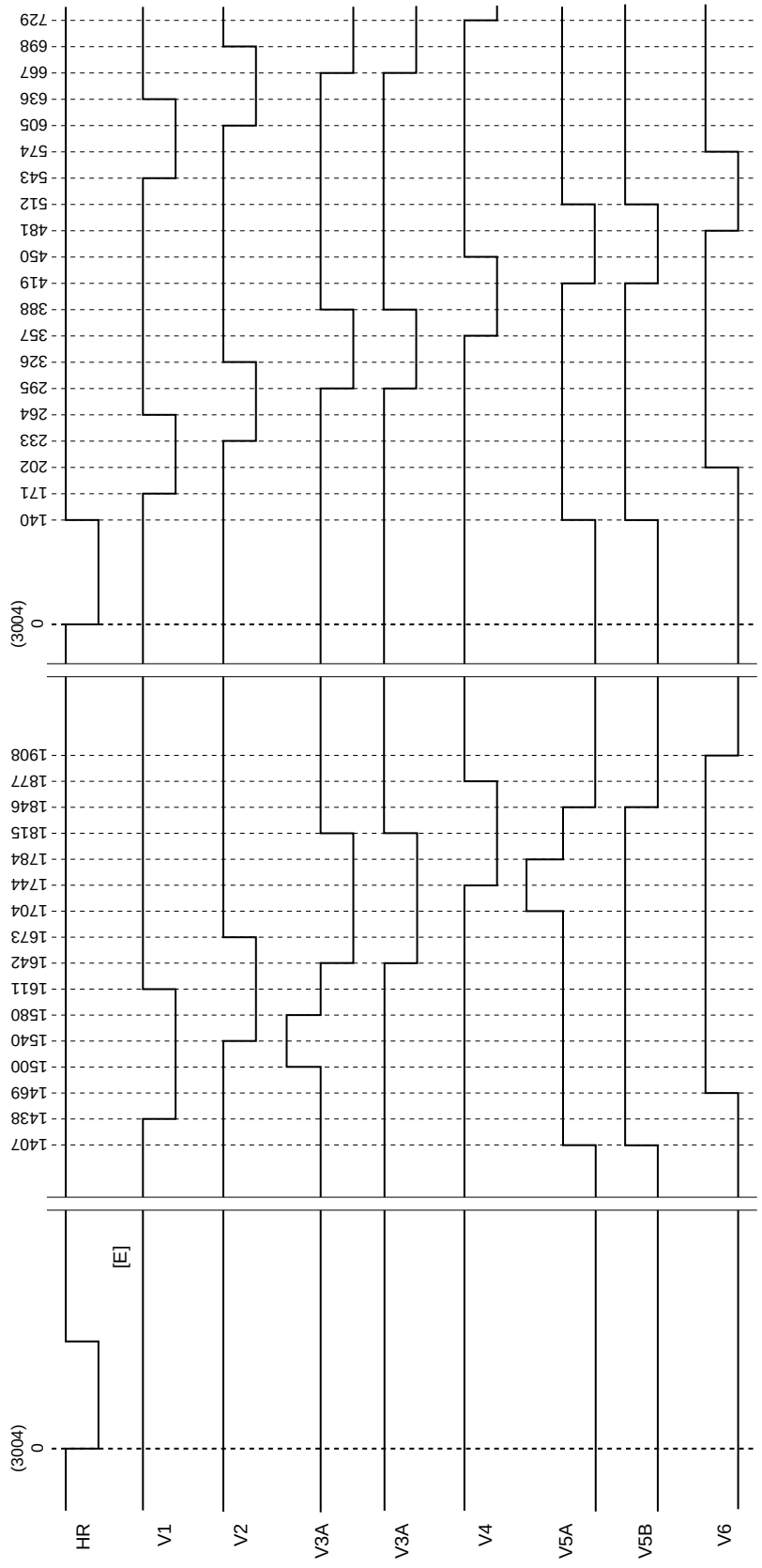


* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).

Chart-A10 Horizontal Direction Timing Chart

Applicable CCD image sensor
• ICX432

MODE
Draft/AF mode



* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 2.2 to 26.5µs (when the drive frequency is 24.3MHz). This chart shows a period of 104ck (4.3µs).

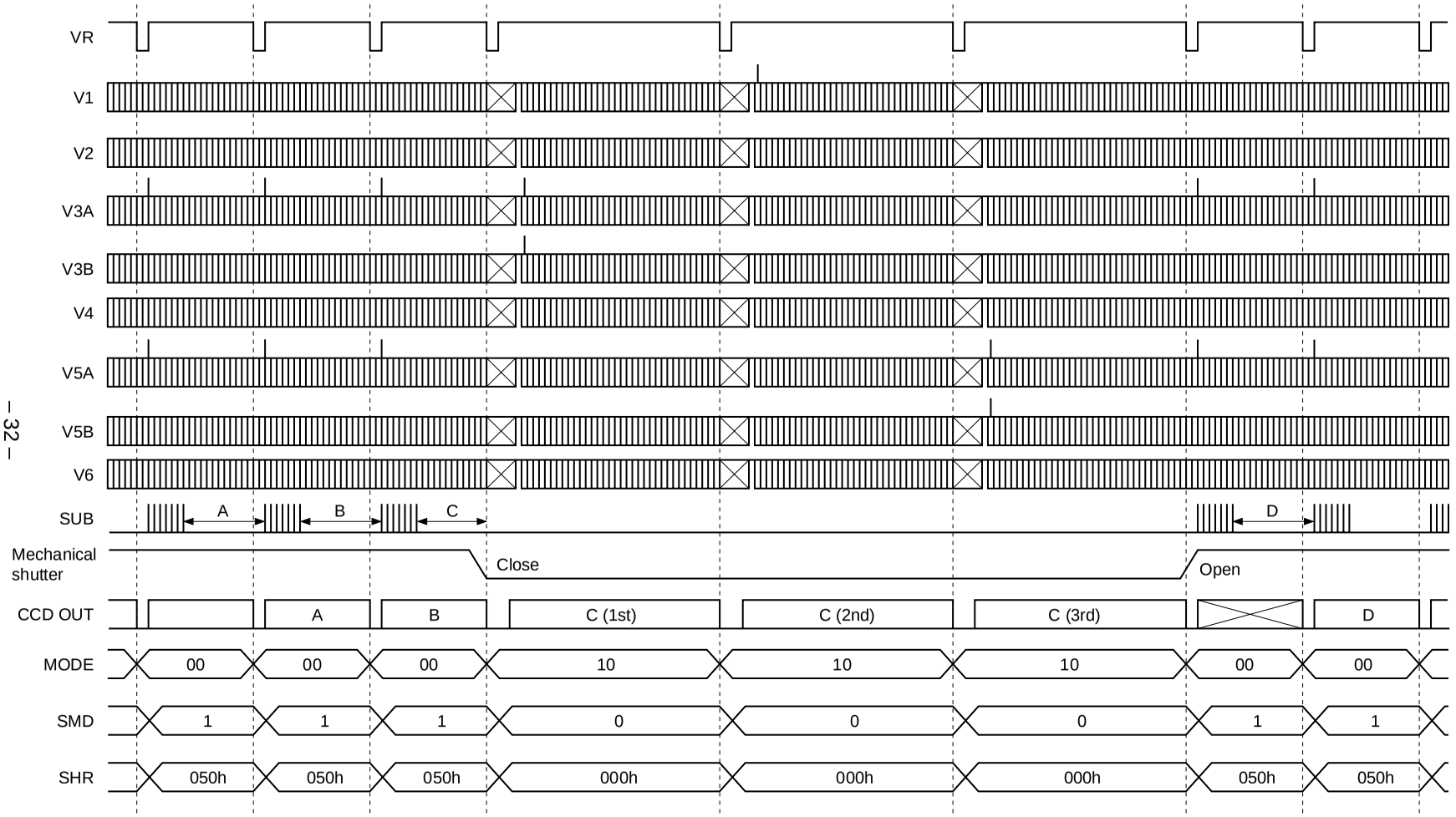
Chart-A11 Vertical Direction Sequence Chart

MODE

Draft → Frame → Draft

Applicable CCD image sensor

• ICX432



* This chart is a drive timing chart example of electronic shutter normal operation.
* Data exposed at B includes the blooming component. For details, see the CCD image sensor data sheet.
* The CXD3615R does not generate the pulse to control mechanical shutter operation.
* The switching timing of drive mode and electronic shutter data is not the same.

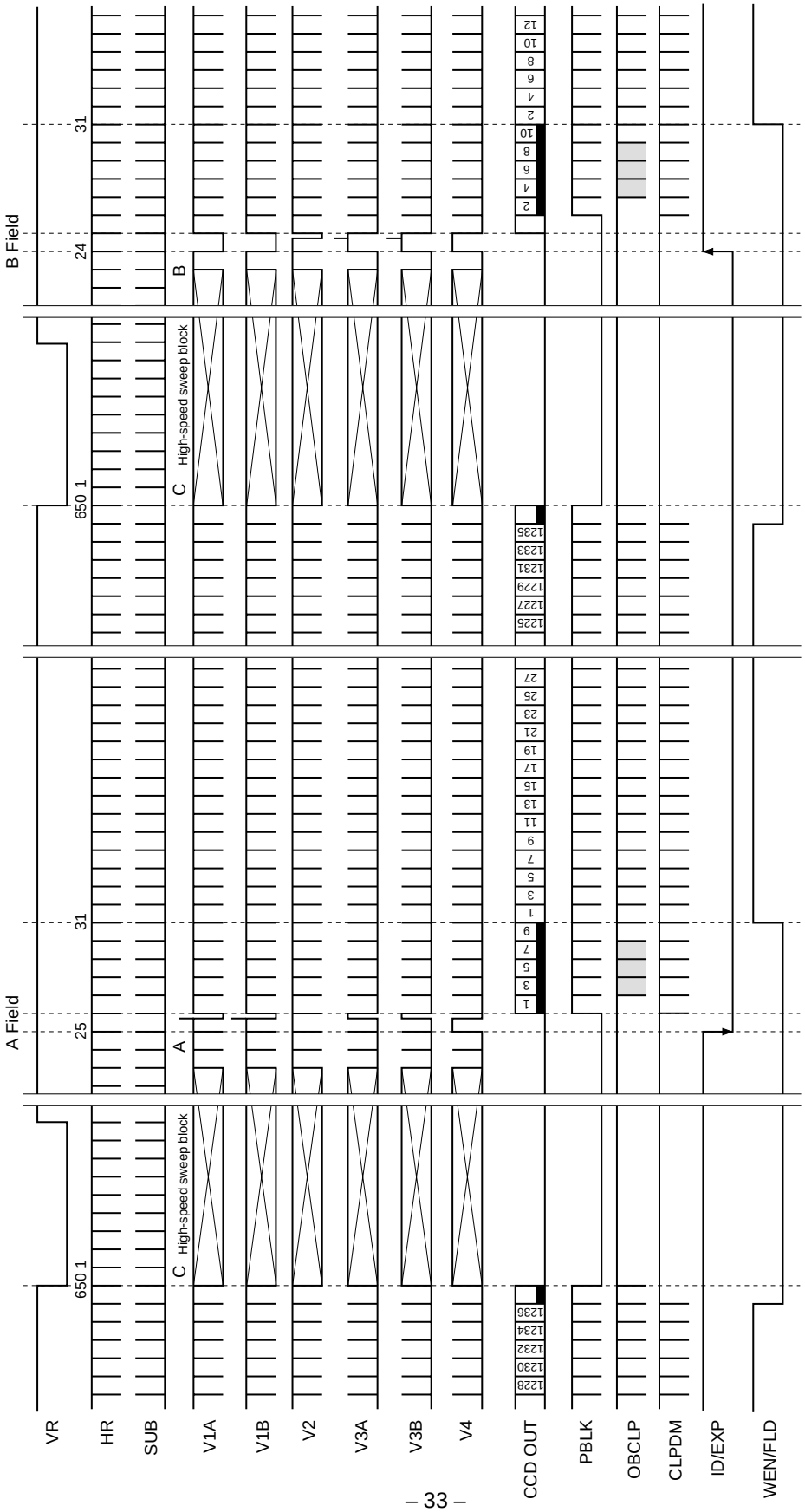
Chart-B1 Vertical Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX434



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to (low, high) in the horizontal periods of each readout portion (A, B).
* WEN/FLD of this chart shows WEN.
* VR of this chart is NTSC equivalent pattern 650H (1H: 1848ck) units. For PAL equivalent pattern, it is 779H + 408ck units.
* This chart shows the pin configuration for the ICX434. (See page 4.)

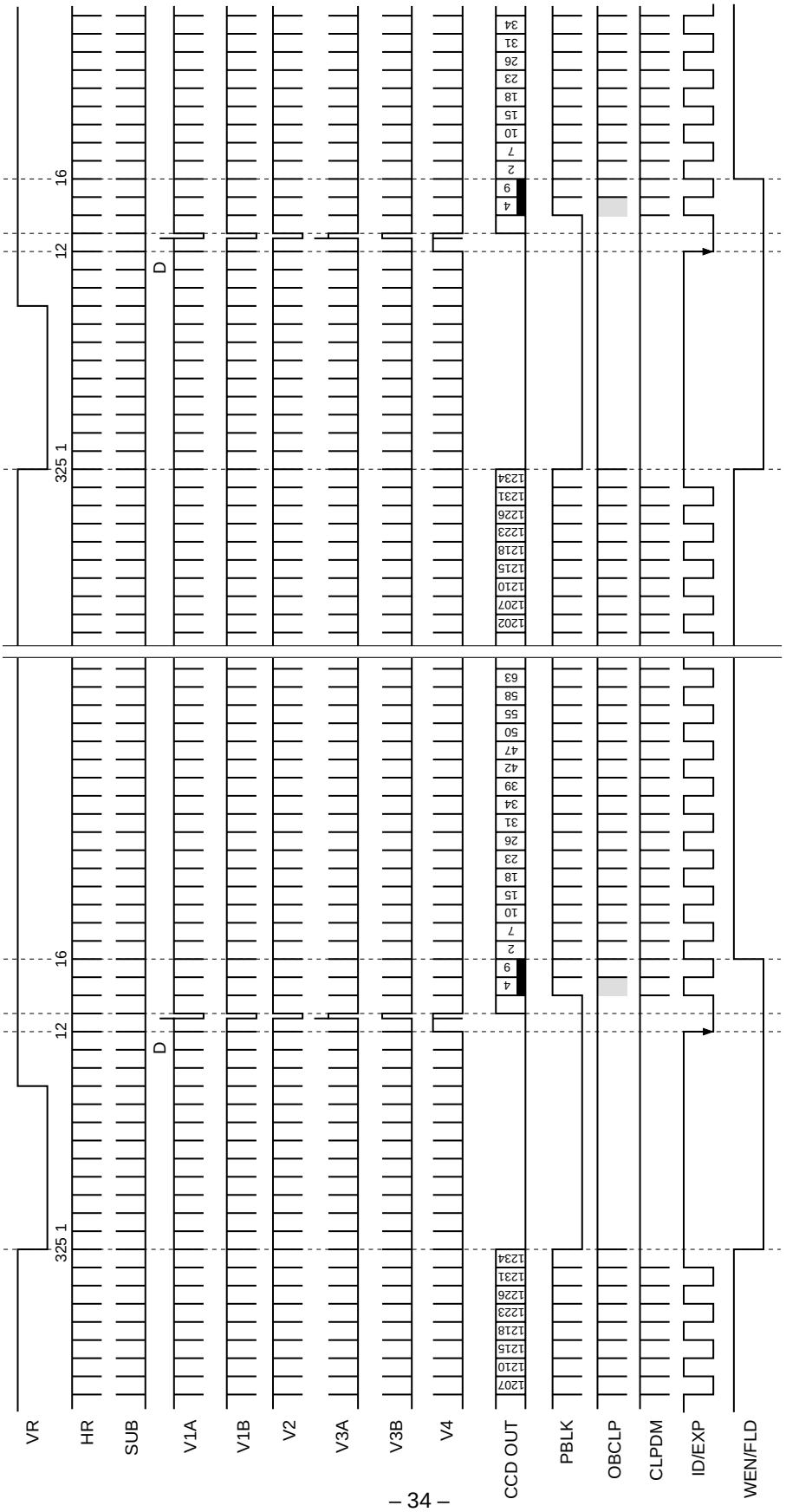
Chart-B2 Vertical Direction Timing Chart

MODE

Draft mode

Applicable CCD image sensor

• ICX434



* The number of SUB pulses is determined by the serial interface data. This chart shows the case where SUB pulses are output in each horizontal period.
* ID/EXP of this chart shows ID. ID is low for lines where CCD OUT contains the R component, and high for lines where CCD OUT contains the B component. In this drive mode, ID is reset to high in the horizontal period of the readout portion.
* WEN/FLD of this chart shows WEN.
* VR of this chart is NTSC equivalent pattern 325H (1H: 1848ck) units. For PAL equivalent pattern, it is 389H + 1128ck units.
* This chart shows the pin configuration for the ICX434. (See page 4.)

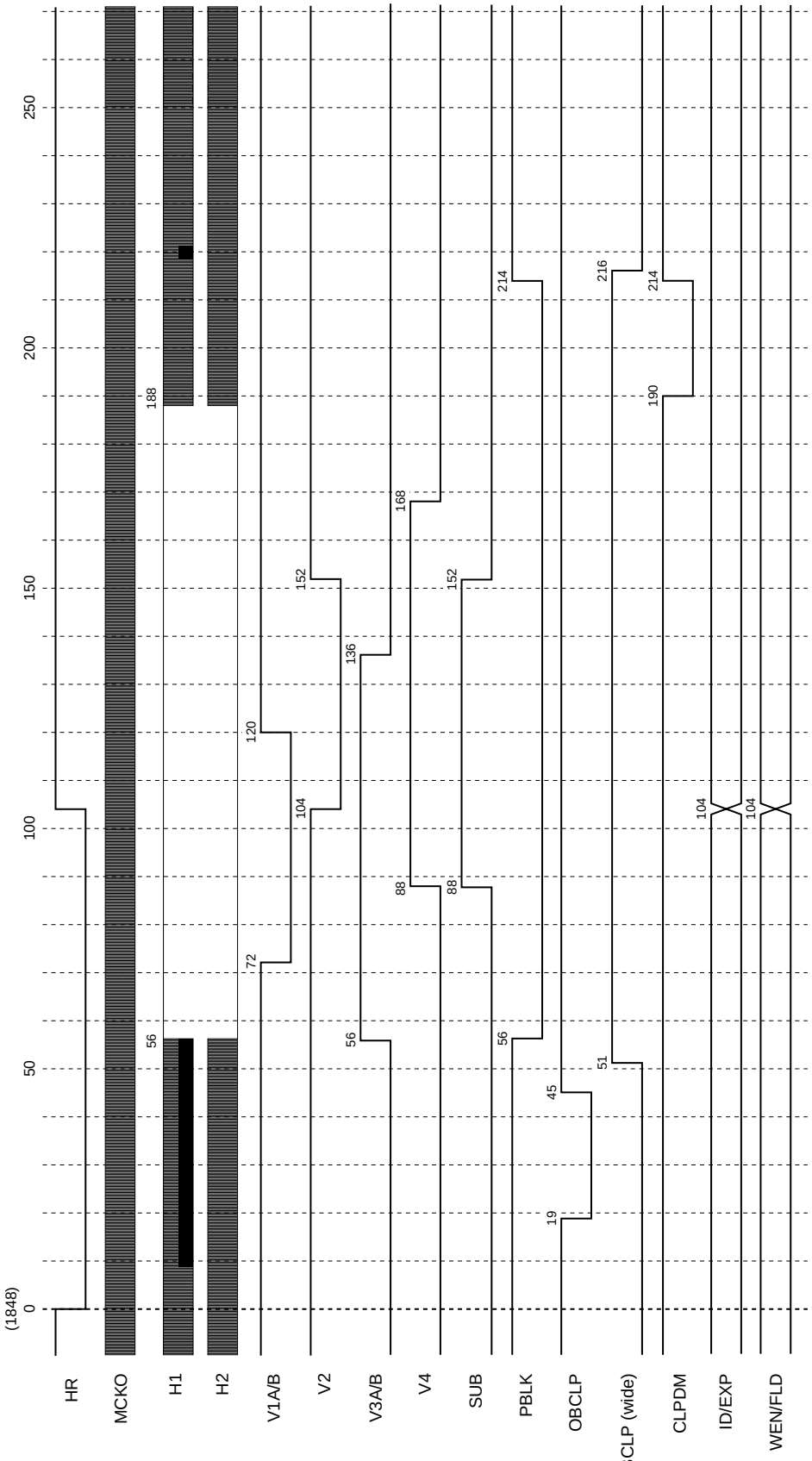
Chart-B3 Horizontal Direction Timing Chart

MODE

Frame mode

Applicable CCD image sensor

• ICX434



* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 3.1 to 10.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-B1.
* OBCLP also has patterns of 13-39, 25-51 and 13-51 for a total of four patterns. OBCLP (wide) is output in the shaded portions shown in Chart-B1. These timings can be switched by the serial interface data.
* This chart shows the pin configuration for the ICX434. (See page 4.)

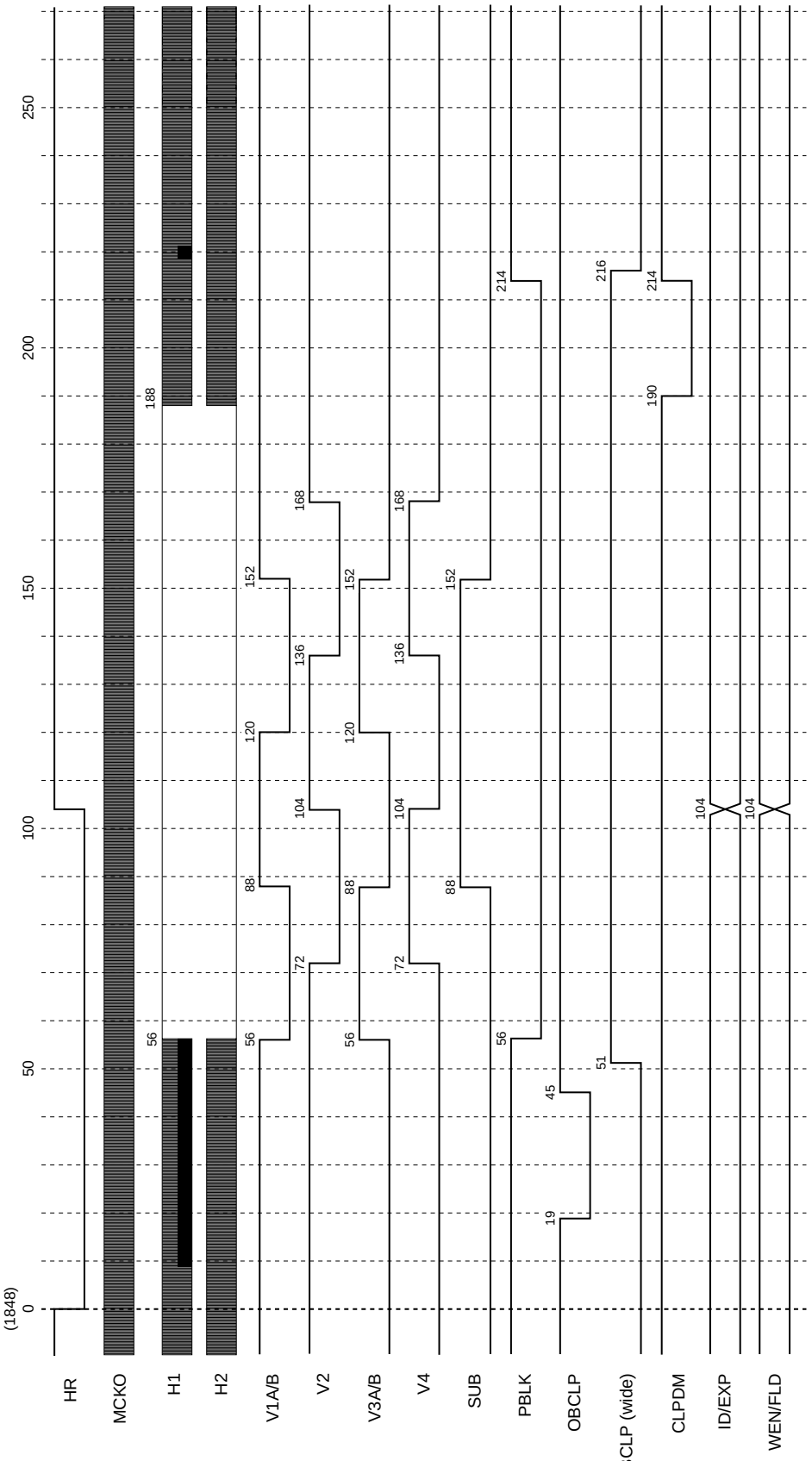
Chart-B4 Horizontal Direction Timing Chart

MODE

Draft mode

Applicable CCD image sensor

• ICX434

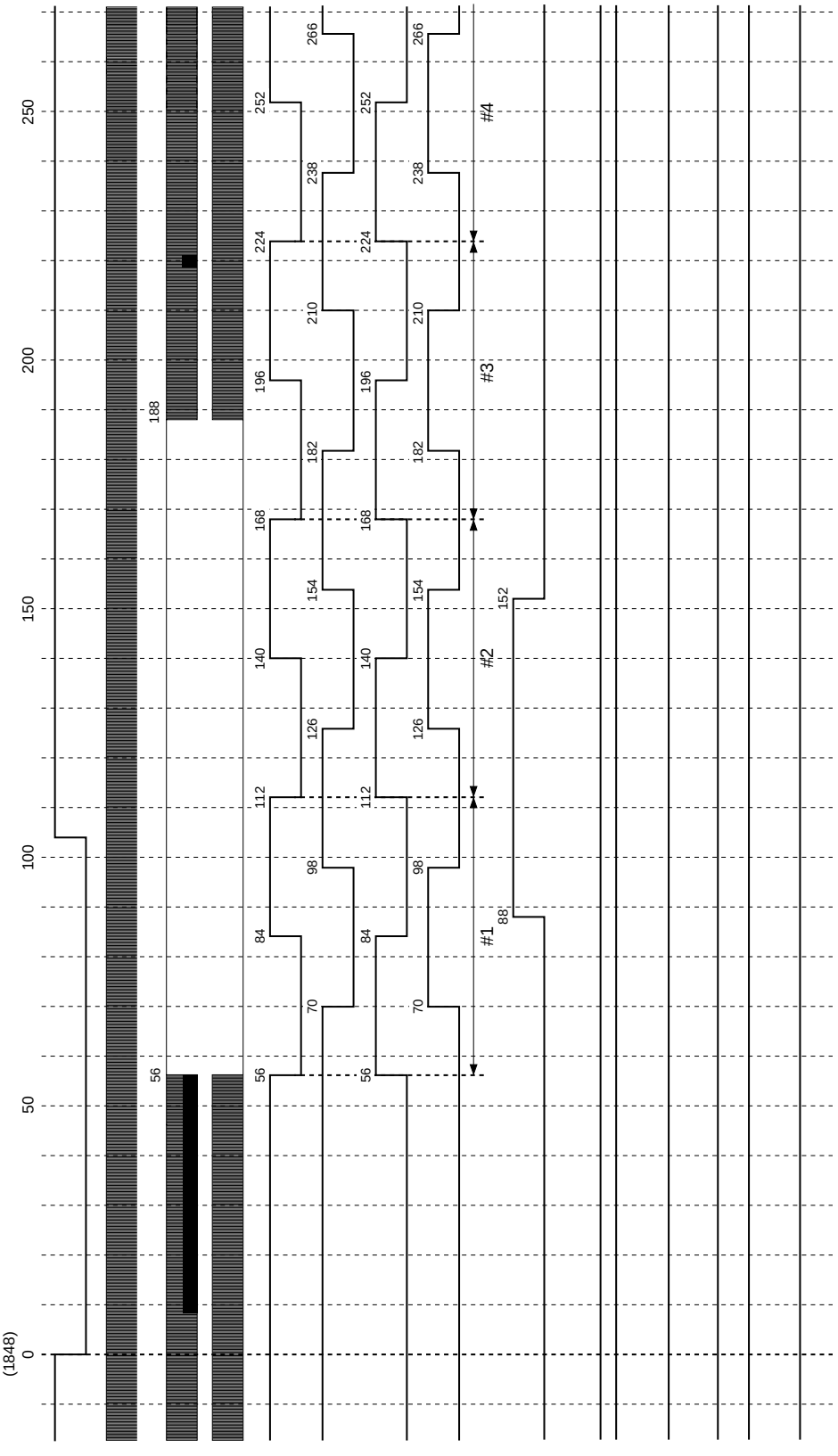


* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 3.1 to 10.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-B2.
* OBCLP also has patterns of 13-39, 25-51 and 13-51 for a total of four patterns. OBCLP (wide) is output in the shaded portions shown in Chart-B2. These timings can be switched by the serial interface data.
* This chart shows the pin configuration for the ICX434. (See page 4.)

Chart-B5 Horizontal Direction Timing Chart
(High-speed sweep: C)

MODE
Frame mode

Applicable CCD image sensor
• ICX434



* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 3.1 to 10.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* SUB is output at the timing shown above when output is controlled by the serial interface data.
* ID and WEN are output at the timing shown above at the position shown in Chart-B1.
* High-speed sweep of V1A/B, V2, V3A/B and V4 is performed up to 22H 1848ck (#758).
* This chart shows the pin configuration for the ICX434. (See page 4.)

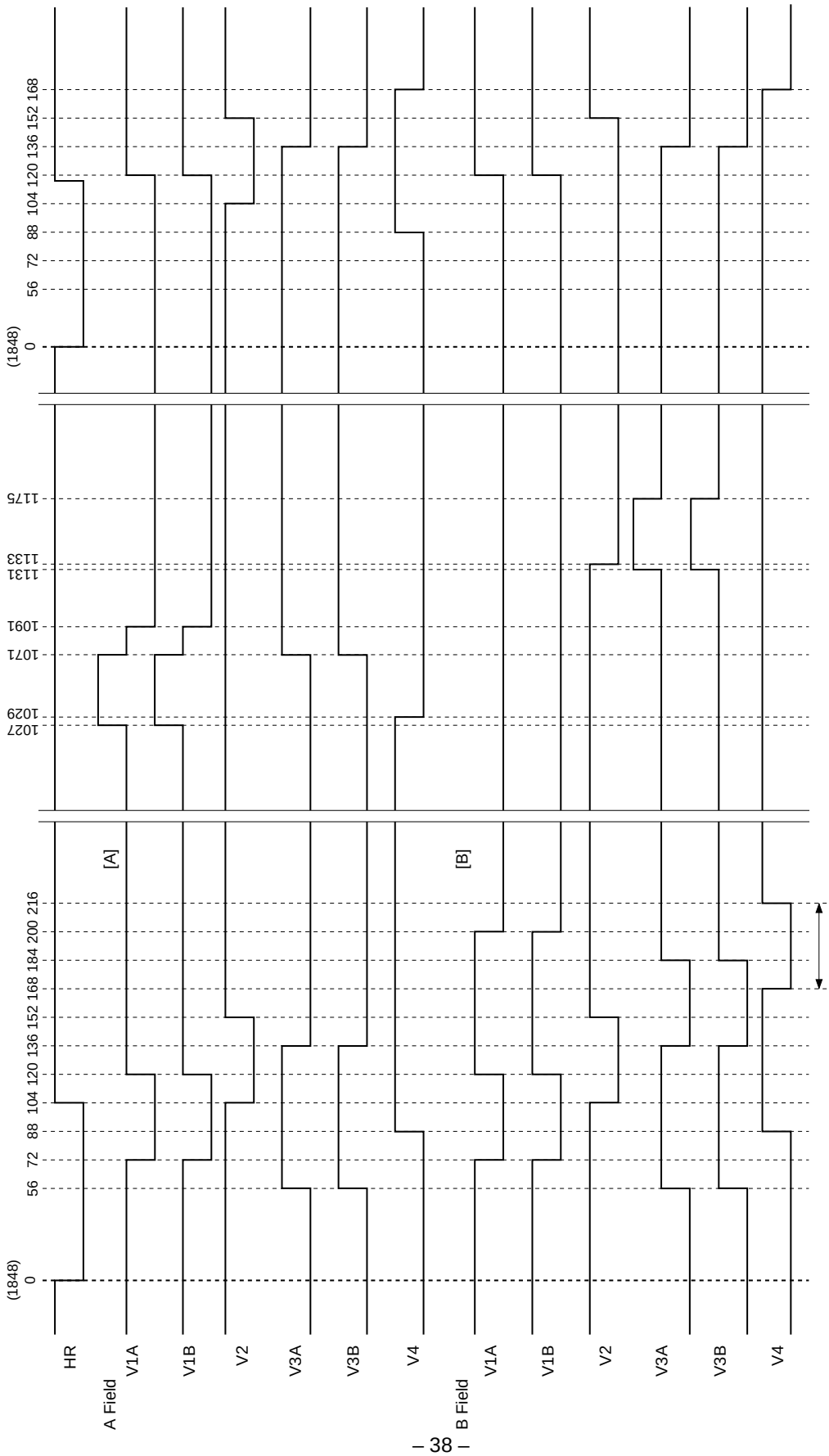
Chart-B6 Horizontal Direction Timing Chart

Applicable CCD image sensor

• ICX434

MODE

Frame mode



* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 3.0 to 13.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* This chart shows the pin configuration for the ICX434. (See page 4.)

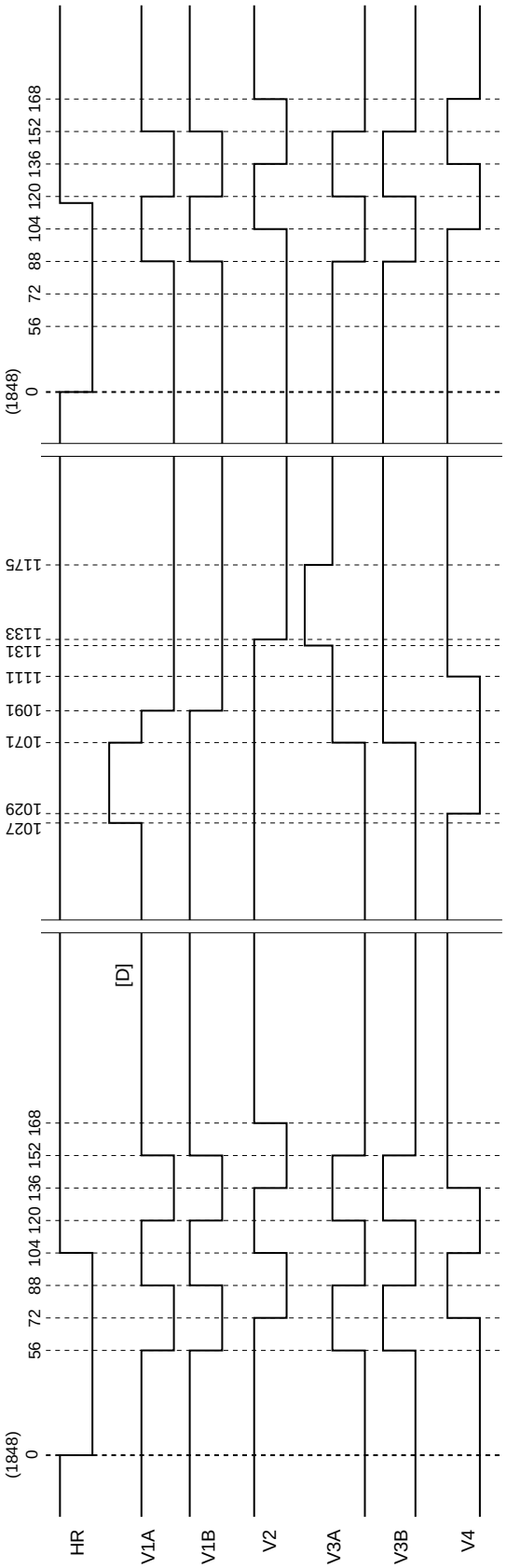
Chart-B7 Horizontal Direction Timing Chart

Applicable CCD image sensor

• ICX434

MODE

Draft mode



* HR of this chart indicates the actual CXD3615R load timing.
* The numbers at the output pulse transition points indicate the count at the MCKO rise from the fall of HR.
* The HR fall period should be between approximately 3.1 to 10.4µs (when the drive frequency is 18MHz). This chart shows a period of 104ck (5.8µs).
* This chart shows the pin configuration for the ICX434. (See page 4.)

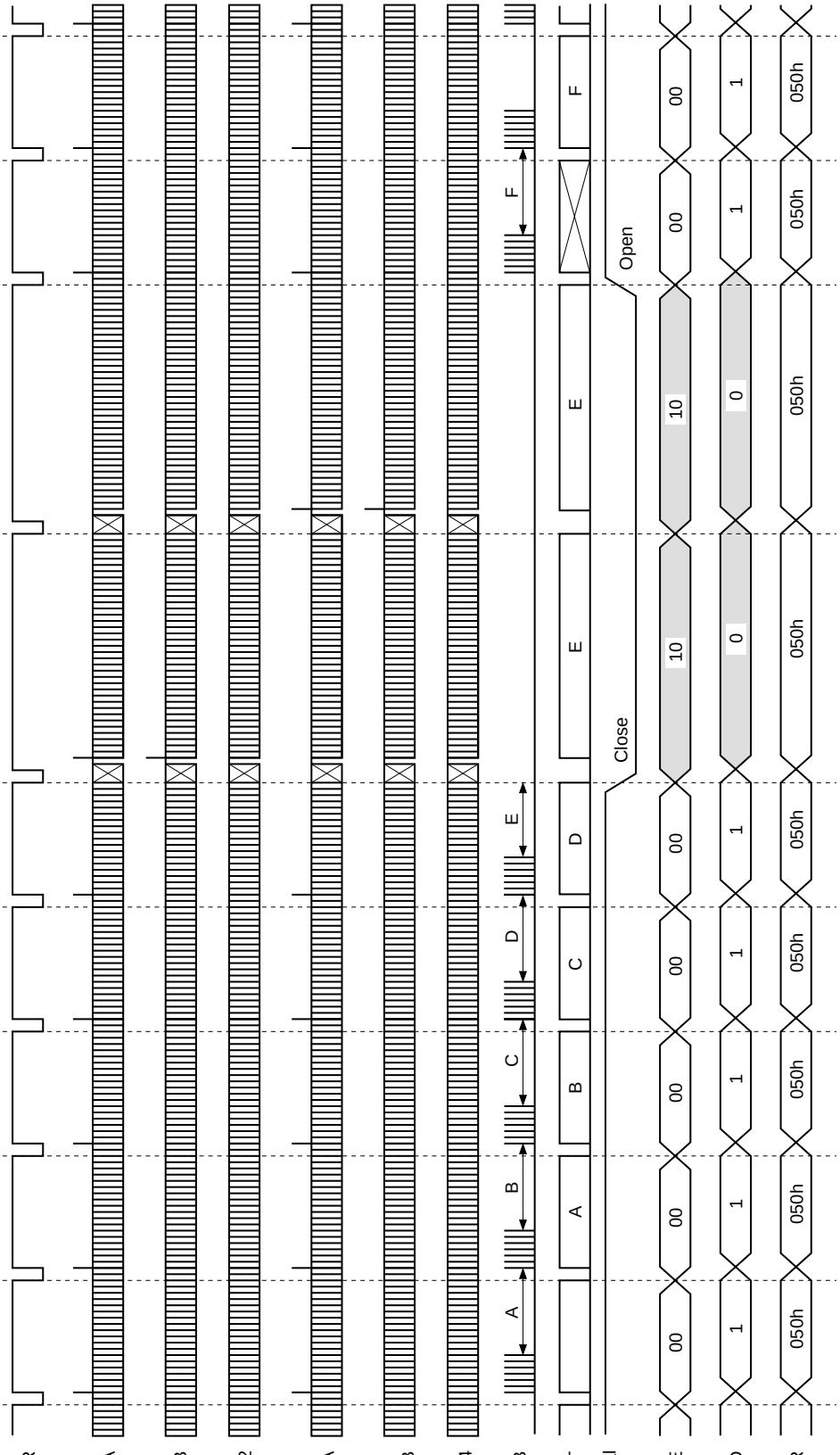
Chart-B8 Vertical Direction Sequence Chart

MODE

Draft → Frame → Draft

Applicable CCD image sensor

• ICX434



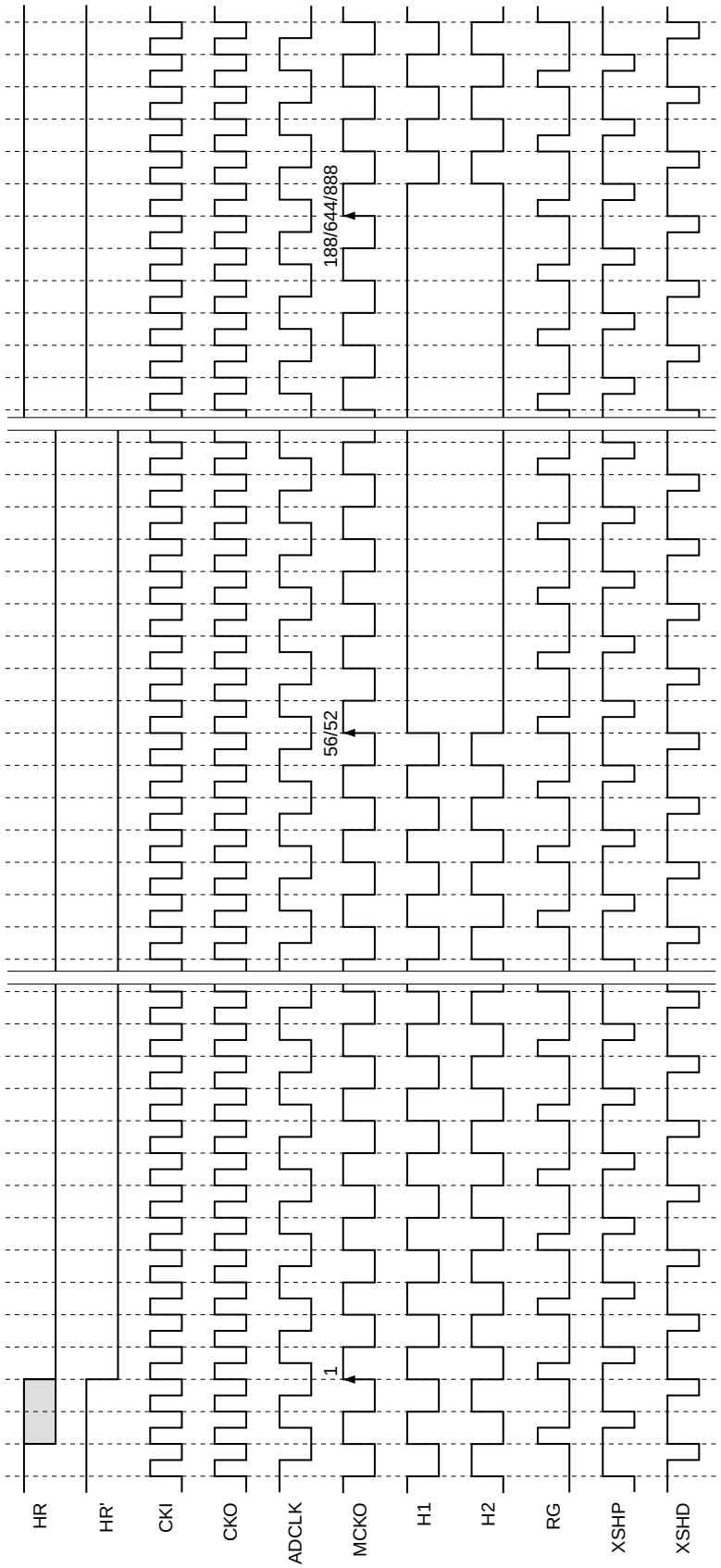
* This chart is a driving timing chart example of electronic shutter normal operation.
* Data exposed at D includes the blooming component. For details, see the CCD image sensor data sheet.
* The CXD3615R does not generate the pulse to control mechanical shutter operation.
* The switching timing of drive mode and electronic shutter data is not the same.
* This chart shows the pin configuration for the ICX434. (See page 4.)

Chart-Z High-Speed Phase Timing Chart

MODE

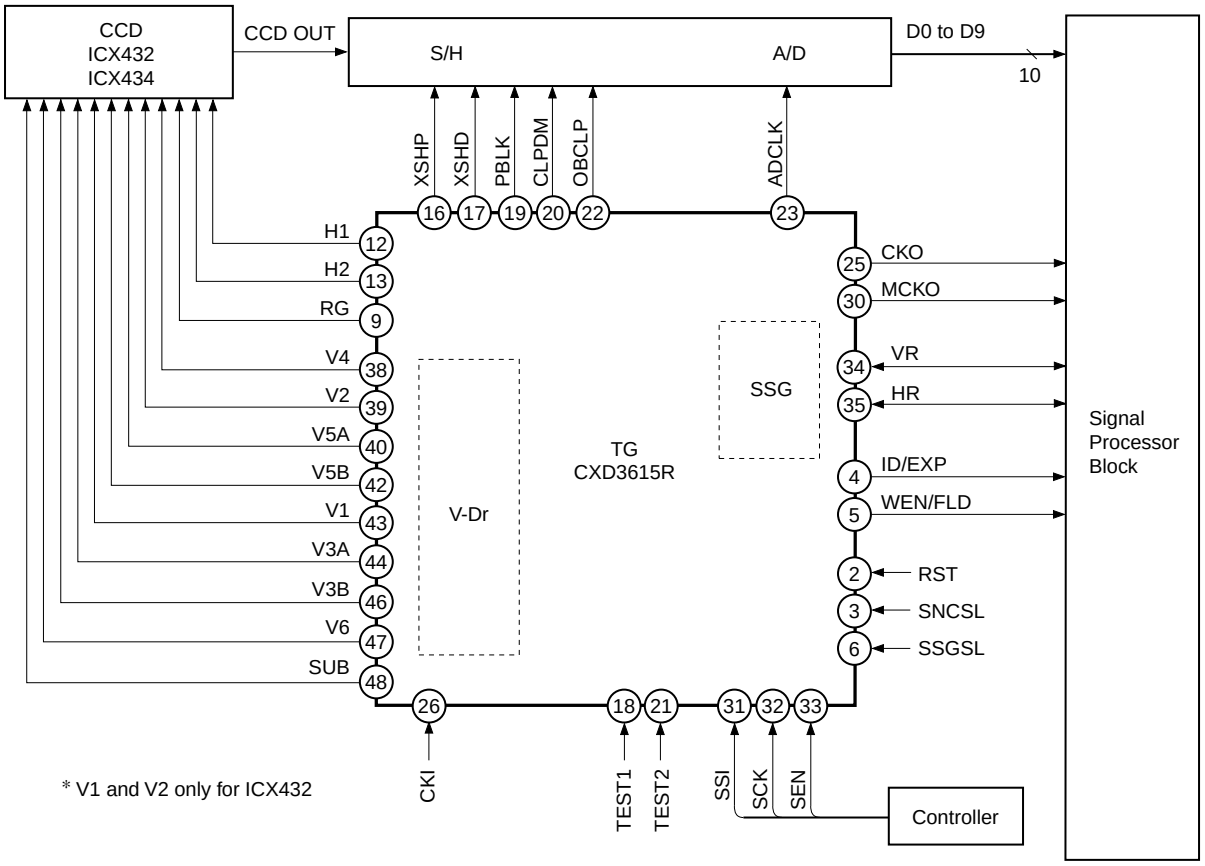
Applicable CCD image sensor

• ICX432/ICX434



* HR' indicates the HR which is the actual CXD3615R load timing.
* The phase relationship of each pulse shows the logical position relationship. For the actual output waveform, a delay is added to each pulse.
* The logical phase of ADCLK can be specified by the serial interface data.

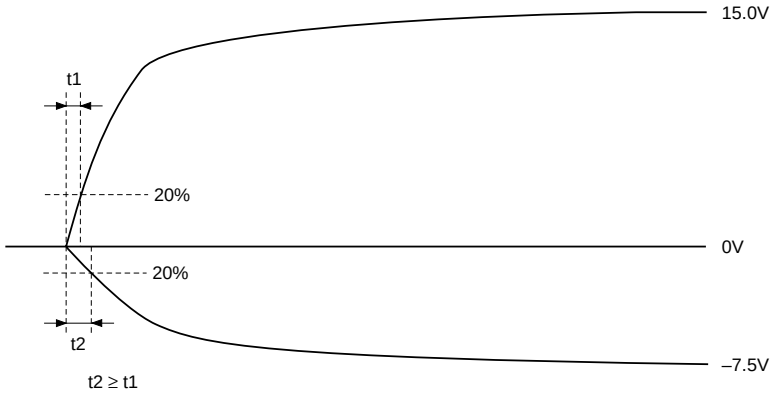
Application Circuit Block Diagram



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

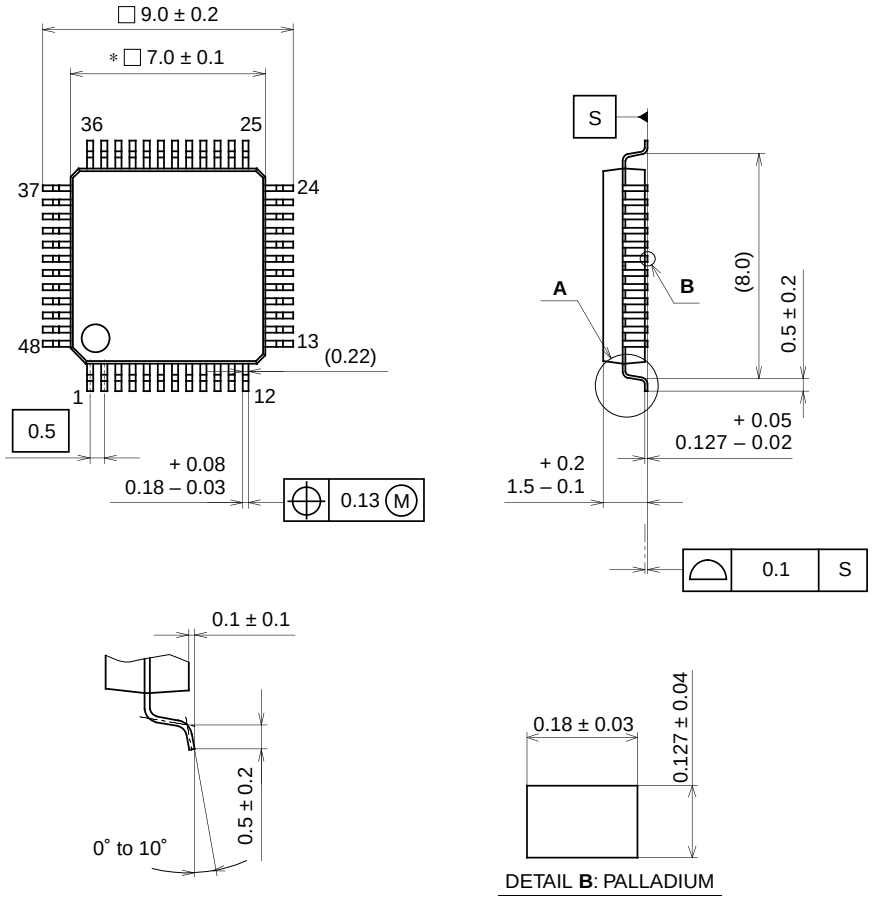
Notes for Power-on

Of the three –7.5V, +15.0V, +3.3V power supplies, be sure to start up the –7.5V and +15.0V power supplies in the following order to prevent the SUB pin of the CCD image sensor from going to negative potential.



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**: PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g