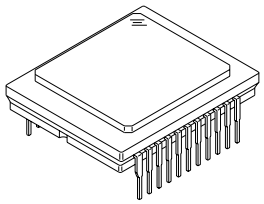
SONY

ICX415AL

Diagonal 8mm (Type 1/2) Progressive Scan CCD Solid-state Image Sensor with Square Pixel for CCIR B/W Cameras

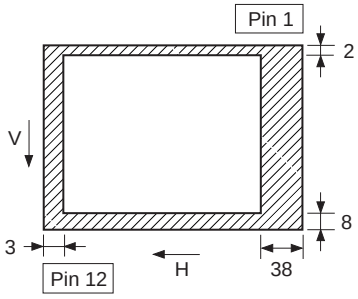
22 pin DIP (Cer-DIP)



Description

The ICX415AL is a diagonal 8mm (Type 1/2) interline CCD solid-state image sensor with a square pixel array suitable for CCIR black-and-white cameras. Progressive scan allows all pixel's signals to be output independently within approximately 1/50 second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter. Square pixel makes this device suitable for image input and processing applications. High sensitivity and low dark current are achieved through the adoption of the HAD (Hole-Accumulation Diode) sensors.

This chip is suitable for applications such as FA and surveillance cameras.



Optical black position
(Top View)

Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High vertical resolution (580 TV-lines) still images without a mechanical shutter
- Square pixel
- Horizontal drive frequency: 29.5MHz (Max.)
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- High resolution, high sensitivity, low dark current
- Continuous variable-speed shutter
- Low smear
- Excellent anti-blooming characteristics

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 8mm (Type 1/2)
- Number of effective pixels: 782 (H) × 582 (V) approx. 460K pixels
- Total number of pixels: 823 (H) × 592 (V) approx. 490K pixels
- Chip size: 7.48mm (H) × 6.15mm (V)
- Unit cell size: 8.3µm (H) × 8.3µm (V)
- Optical black: Horizontal (H) direction: Front 3 pixels, rear 38 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 19
  Vertical 5
- Substrate material: Silicon

E02116C3Z

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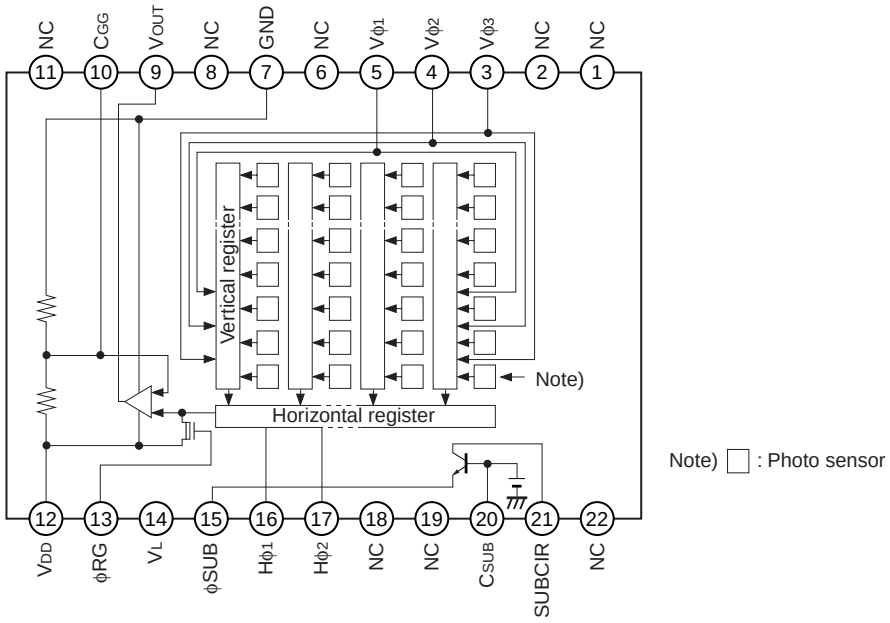
Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC		12	V_{DD}	Supply voltage
2	NC		13	φRG	Reset gate clock
3	Vφ3	Vertical register transfer clock	14	V_L	Protective transistor bias
4	Vφ2	Vertical register transfer clock	15	φSUB	Substrate clock
5	Vφ1	Vertical register transfer clock	16	Hφ1	Horizontal register transfer clock
6	NC		17	Hφ2	Horizontal register transfer clock
7	GND	GND	18	NC	
8	NC		19	NC	
9	V_{OUT}	Signal output	20	C_{SUB}	Substrate bias*2
10	C_{GG}	Output amplifier gate*1	21	SUBCIR	Supply voltage for the substrate voltage generation
11	NC		22	NC	

*1 DC bias is applied within the CCD, so that this pin should be grounded externally through a capacitance of 1µF or more.

*2 DC bias is applied within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF or more.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate clock φSUB – GND		–0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, C_{GG}, SUBCIR – GND	–0.3 to +18	V	
	V_{DD}, V_{OUT}, C_{GG}, SUBCIR – φSUB	–55 to +10	V	
Clock input voltage	Vφ1, Vφ2, Vφ3 – GND	–15 to +20	V	
	Vφ1, Vφ2, Vφ3 – φSUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*1
Voltage difference between horizongal clock input pins		to +17	V	
Hφ1, Hφ2 – Vφ3		–16 to +16	V	
Hφ1, Hφ2 – GND		–10 to +15	V	
Hφ1, Hφ2 – φSUB		–55 to +10	V	
V_L – φSUB		–65 to +0.3	V	
Vφ2, Vφ3 – V_L		–0.3 to +27.5	V	
RG – GND		–0.3 to +22.5	V	
Vφ1, Hφ1, Hφ2, GND – VL		–0.3 to +17.5	V	
Storage temperature		–30 to +80	°C	
Performance guarantee temperature		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +27V (Max.) when clock width < 10µs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for power-on and power-off.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	φSUB	*2				
Reset gate clock	φRG	*3				

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*2 Indications of substrate voltage setting value
Set SUBCIR pin to open when applying a DC bias the substrate clock pin.
Adjust the substrate voltage because the setting value of the substrate voltage is indicated on the back of image sensor by a special code when applying a DC bias the substrate clock pin.

V_{SUB} code – two characters indication □ □
↑ ↑
Integer portion Decimal portion

The integer portion of the code and the actual value correspond to each other as follows.

Integer portion of code	A	C	d	E	f	G	h	J
Value	5	6	7	8	9	10	11	12

[Example] "A5" → V_{SUB} = 5.5V

*3 Do not apply a DC bias to the reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

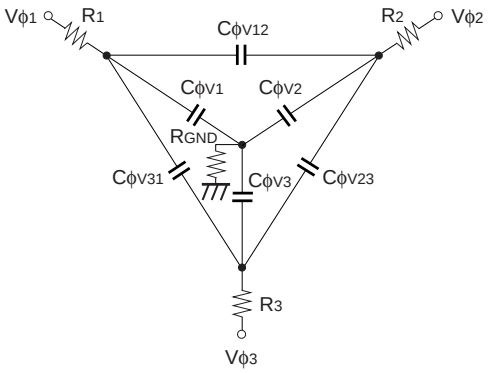
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}	4.0	7.0	9.0	mA	

Clock Voltage Conditions

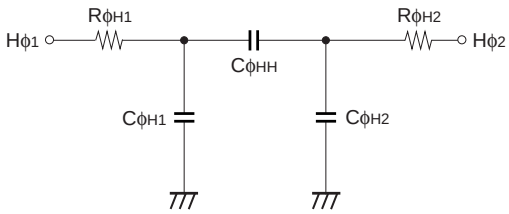
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform Diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH02}	–0.05	0	0.05	V	2	$V_{VH} = V_{VH02}$
	V_{VH1}, V_{VH2}, V_{VH3}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}	–7.8	–7.5	–7.2	V	2	$V_{VL} = (V_{VL1} + V_{VL3})/2$ (During 29.5MHz)
	V_{VL1}, V_{VL2}, V_{VL3}	–8.0	–7.5	–7.0	V	2	$V_{VL} = (V_{VL1} + V_{VL3})/2$ (During 14.75MHz)
	$V\phi_1$, $V\phi_2$, $V\phi_3$	6.8	7.5	8.05	V	2	
	$\lvert V_{VL1} - V_{VL3} \rvert$			0.1	V	2	
	V_{VHH}			0.5	V	2	High-level coupling
	V_{VHL}			0.5	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	0.8	2.5		V	3	Cross-point voltage
Reset gate clock voltage	$V\phi_{RG}$	4.5	5.0	5.5	V	4	
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	Low-level coupling
	$V_{RGL} - V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi_{SUB}$	21.5	22.5	23.5	V	5	

Clock Equivalent Circuit Constants

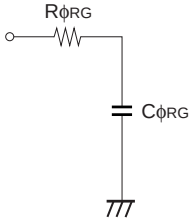
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		3900		pF	
	$C_{\phi V2}$		3300		pF	
	$C_{\phi V3}$		3300		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$		2200		pF	
	$C_{\phi V23}$		2200		pF	
	$C_{\phi V31}$		1800		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		30		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		6		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		390		pF	
Vertical transfer clock series resistor	R_1, R_2		27		Ω	
	R_3		22		Ω	
Vertical transfer clock ground resistor	R_{GND}		100		Ω	
Horizontal transfer clock series resistor	$R_{\phi H1}$, $R_{\phi H2}$		16		Ω	
Reset gate clock series resistor	$R_{\phi RG}$		36		Ω	



Vertical transfer clock equivalent circuit



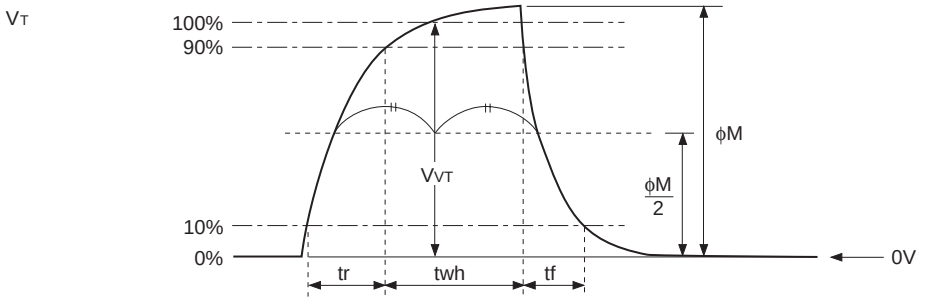
Horizontal transfer clock equivalent circuit



Reset gate clock equivalent circuit

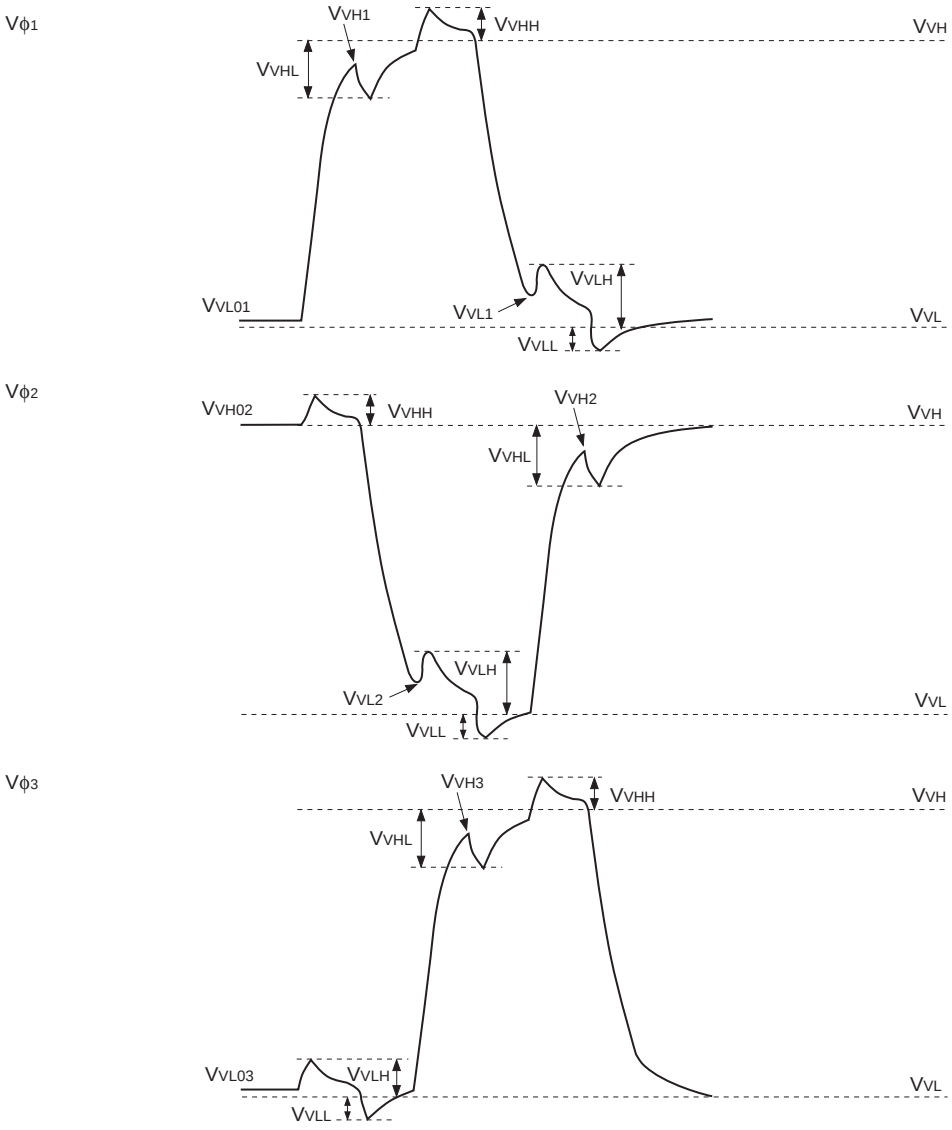
Drive Clock Waveform Conditions

(1) Readout clock waveform



Note) Readout clock is used by composing vertical transfer clocks Vϕ2 and Vϕ3.

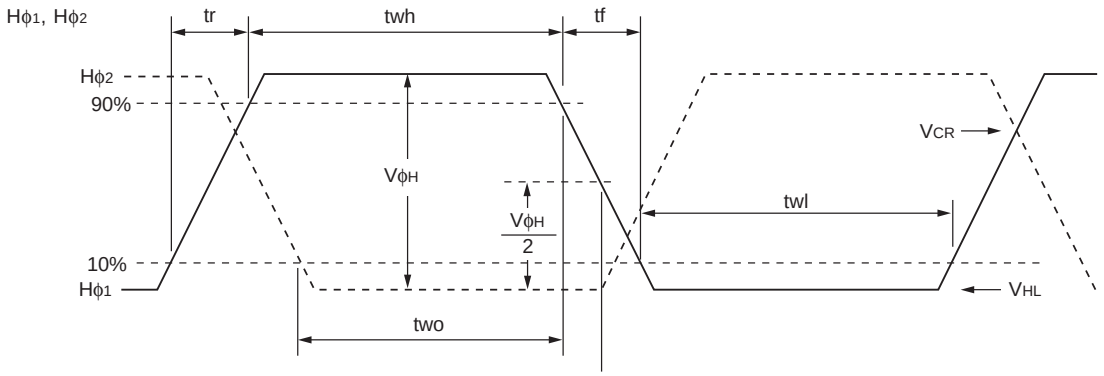
(2) Vertical transfer clock waveform



VVH = VVH02
VVL = (VVL01 + VVL03)/2
VVL3 = VVL03

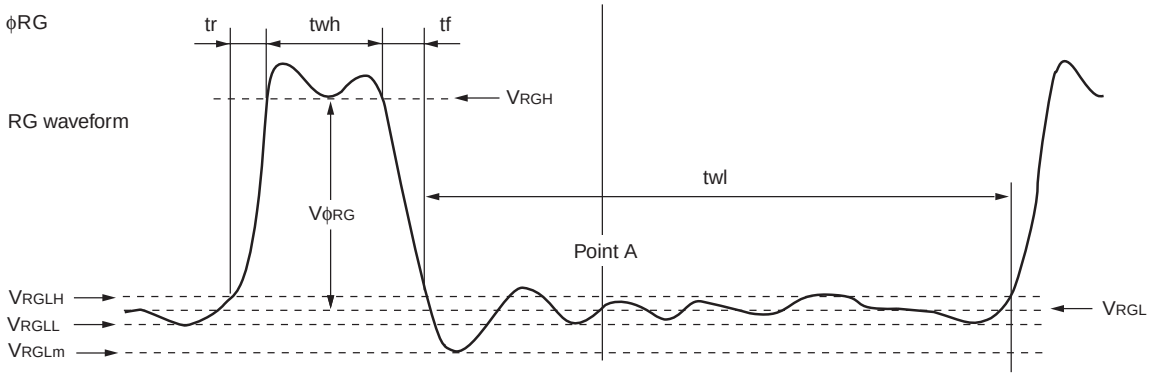
Vϕ1 = VVH1 – VVL01
Vϕ2 = VVH02 – VVL2
Vϕ3 = VVH3 – VVL03

(3) Horizontal transfer clock waveform



Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1 and Hϕ2 is two.

(4) Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

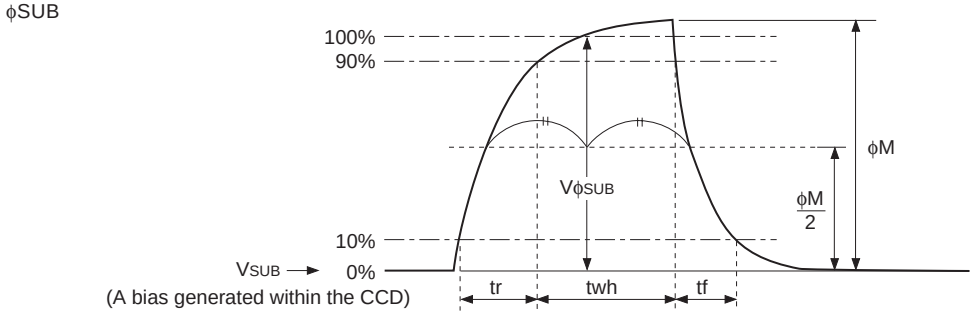
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is VRGLm.

(5) Substrate clock waveform



Clock Switching Characteristics (Horizontal drive frequency: 29.5MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.3	2.5						0.5			0.5		µs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$										15		250	ns	When using CXD3400N
Horizontal transfer clock	$H\phi_1$	9.5	12.0		9.5	12.0			5.0	7.5		5.0	7.5	ns	tf ≥ tr – 2ns
	$H\phi_2$	9.5	12.0		9.5	12.0			5.0	7.5		5.0	7.5		
Reset gate clock	ϕRG	4	7			22			2			3		ns	
Substrate clock	ϕSUB	0.7	0.8							0.5			0.5	µs	When draining charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	7.5	9.5		ns	*1

Clock Switching Characteristics (Horizontal drive frequency: 14.75MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	4.6	5.0						0.5			0.5		µs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$										15		350	ns	When using CXD3400N
Horizontal transfer clock	$H\phi_1$	18	23		21	26			10	17.5		10	17.5	ns	tf ≥ tr – 2ns
	$H\phi_2$	21	26		18	23			10	15		10	15		
Reset gate clock	ϕRG	11	14			49			2			2		ns	
Substrate clock	ϕSUB	1.4	1.6							0.4			0.4	µs	When draining charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	20	24		ns	*1

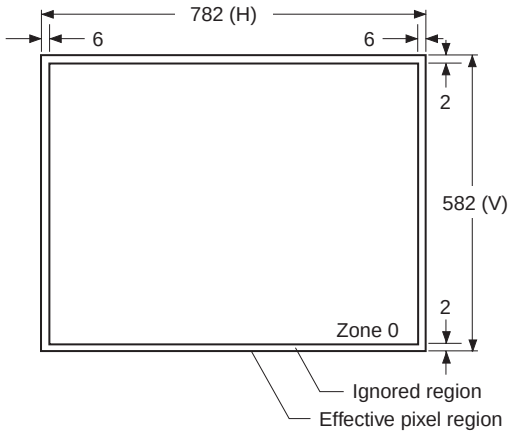
*1 The overlap period of twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is two.

Image Sensor Characteristics (Ta = 25°C)

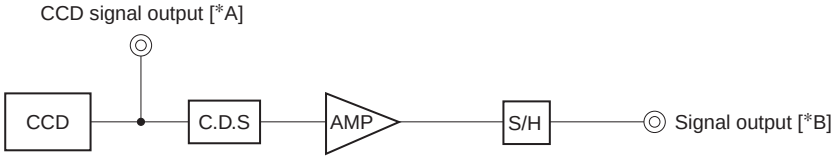
Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	650	820	1070	mV	1	1/25s accumulation conversion value
Saturation signal	Vsat	375			mV	2	Ta = 60°C
Smear	Sm		–100	–92	dB	3	
Video signal shading	SH			25	%	4	Zone 0
Dark signal	Vdt			2	mV	5	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	6	Ta = 60°C
Lag	Lag			0.5	%	7	

Note) All image sensor characteristic data noted above is for operation in 1/50s progressive scan mode.

Zone Definition of Video Signal Shading



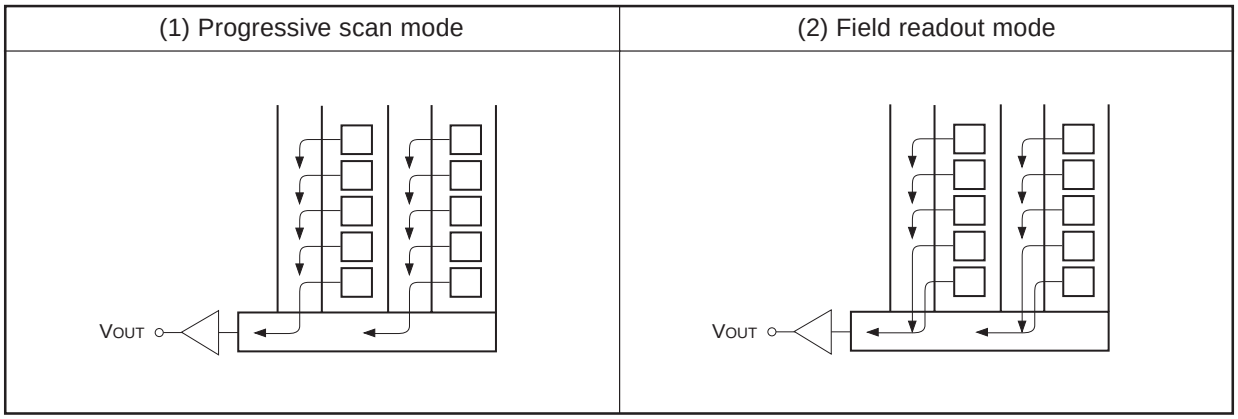
Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B] equals 1.

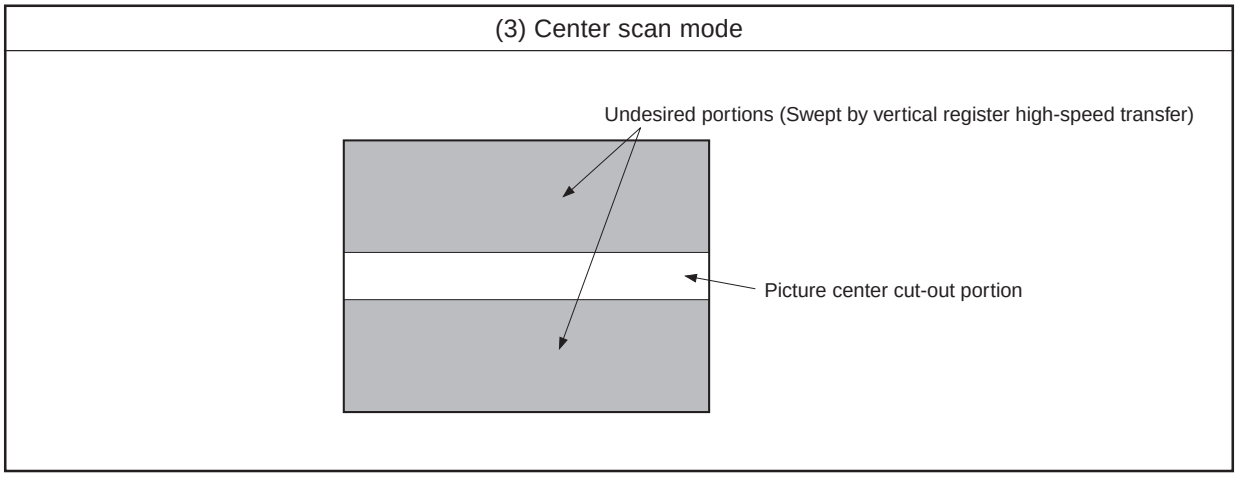
Image sensor readout mode

The diagram below shows the output methods for the following three readout modes.



1. Progressive scan mode
   In this mode, all pixel signals are output in non-interlace format in 1/50s.
   All pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. Field readout mode
   All pixels are readout, 2-line transfer is performed during H blanking period and 2 pixels are added by horizontal register. (However, guarantees only at the time of a 14.75MHz drive.)



3. Center scan mode
   This is the center scan mode using the progressive scan method.
   The undesired portions are swept by vertical register high-speed transfer, and the picture center portion is cut out.
   There are the mode (100 frames/s) which outputs 264 lines of an output line portion, and the mode (200 frames/s) which outputs 88 lines.

Image Sensor Characteristics Measurement Method

◎Measurement conditions

(1) In the following measurements, the substrate voltage is set to the value indicated on the device, and the device drive conditions are at the typical values of the bias and clock voltage conditions.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value measured at point [*B] of the measurement system.

(3) In the following measurements, this image sensor is operated in 1/50s progressive scan mode.

◎Definition of standard imaging conditions

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/250s, measure the signal voltage (Vs) at the center of the screen, and substitute the value into the following formula.

$$S = Vs \times \frac{250}{25} \text{ [mV]}$$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal output, 120mV, measure the minimum value of the signal output.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of signal output, 120mV. Then after the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (VSm [mV]) of the signal output and substitute the value into the following formula.

$$Sm = 20 \times \log\left(\frac{VSm}{120} \times \frac{1}{500} \times \frac{1}{10}\right) \text{ [dB] (1/10V method conversion value)}$$

4. Video signal shading
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 120mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (Vmax - Vmin)/120 \times 100 \text{ [\%]}$$

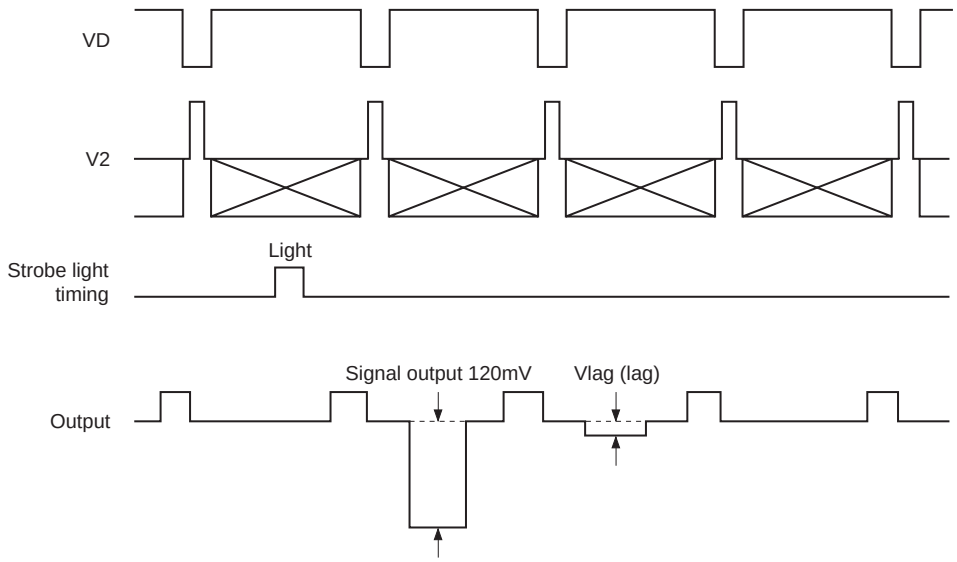
5. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

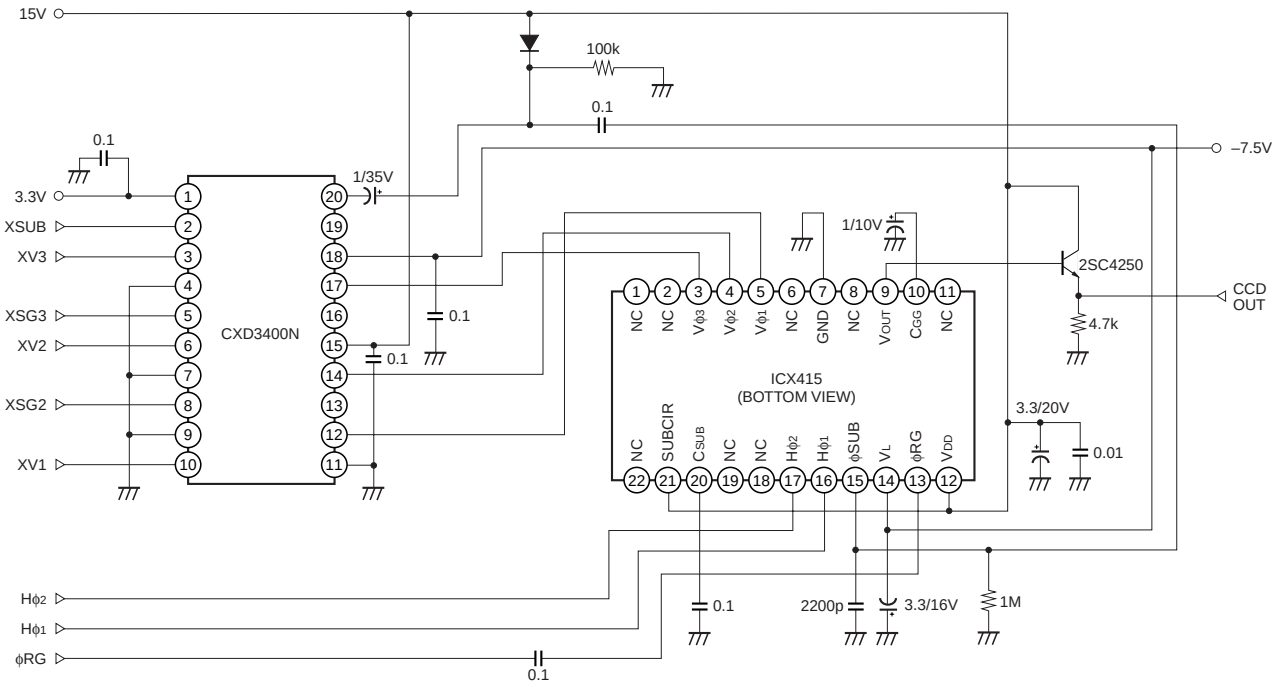
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Lag
   Adjust the signal output generated by strobe light to 120mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

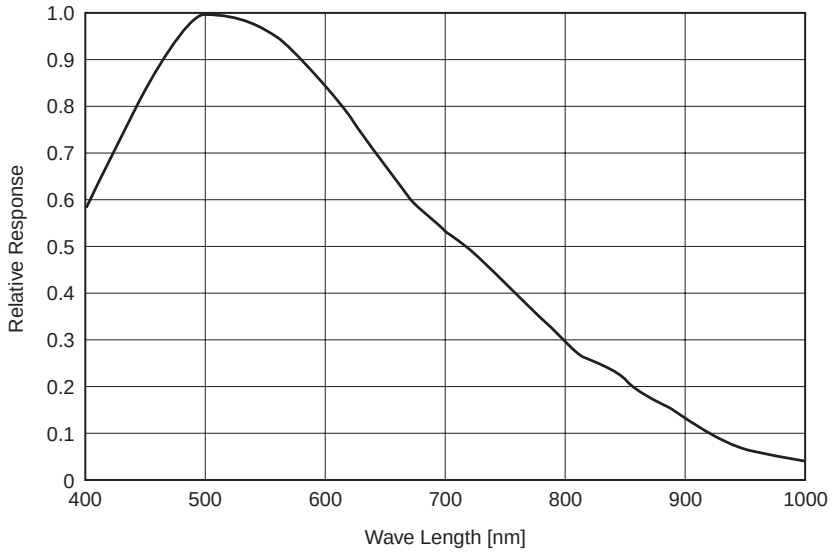
   $Lag = (Vlag/120) \times 100$ [%]



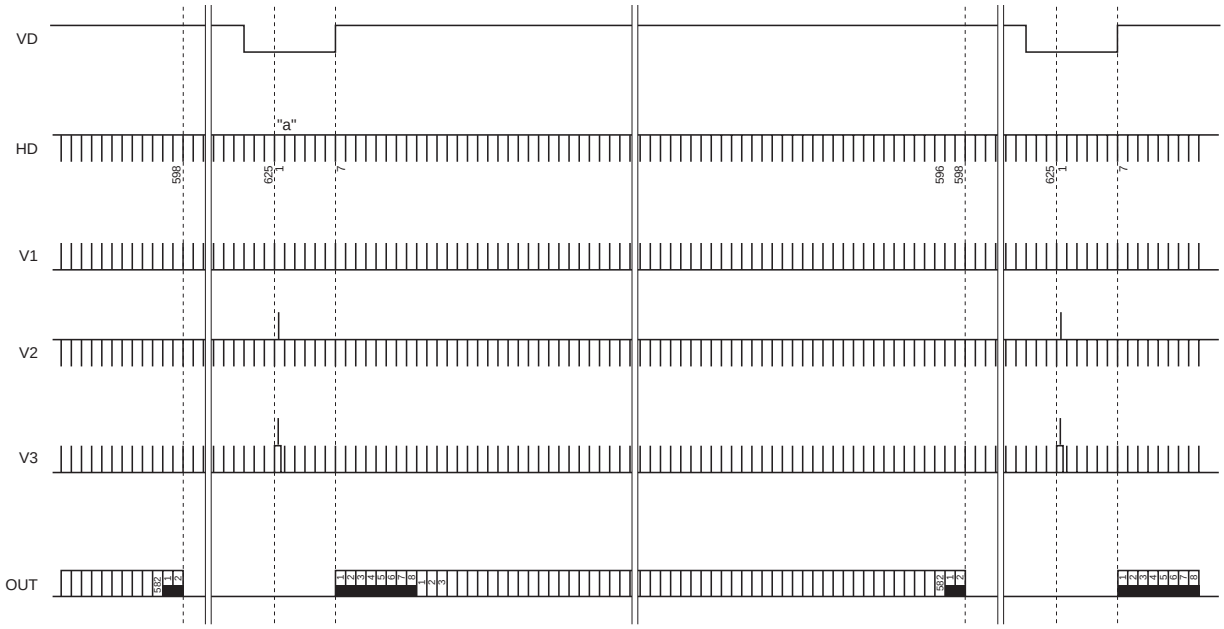
Drive Circuit



Spectral Sensitivity Characteristics (Excludes lens characteristics and light source characteristics)

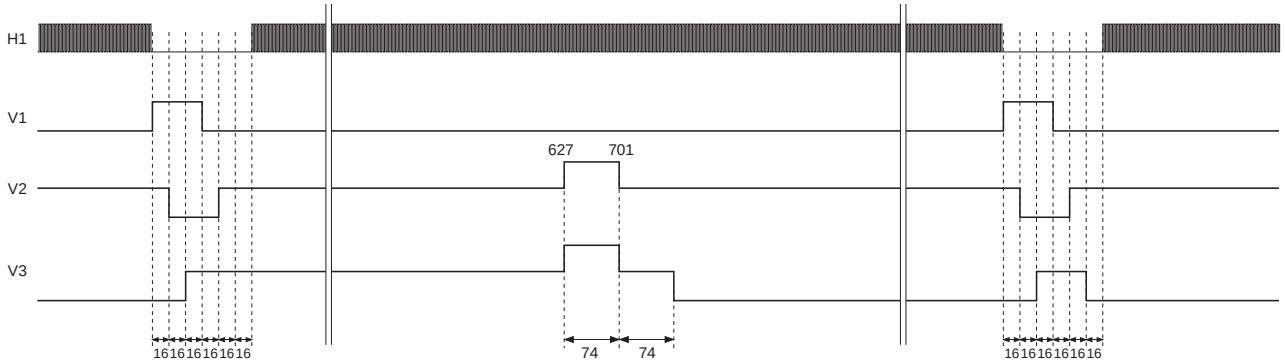


Drive Timing Chart (Vertical Sync) **Progressive Scan Mode**

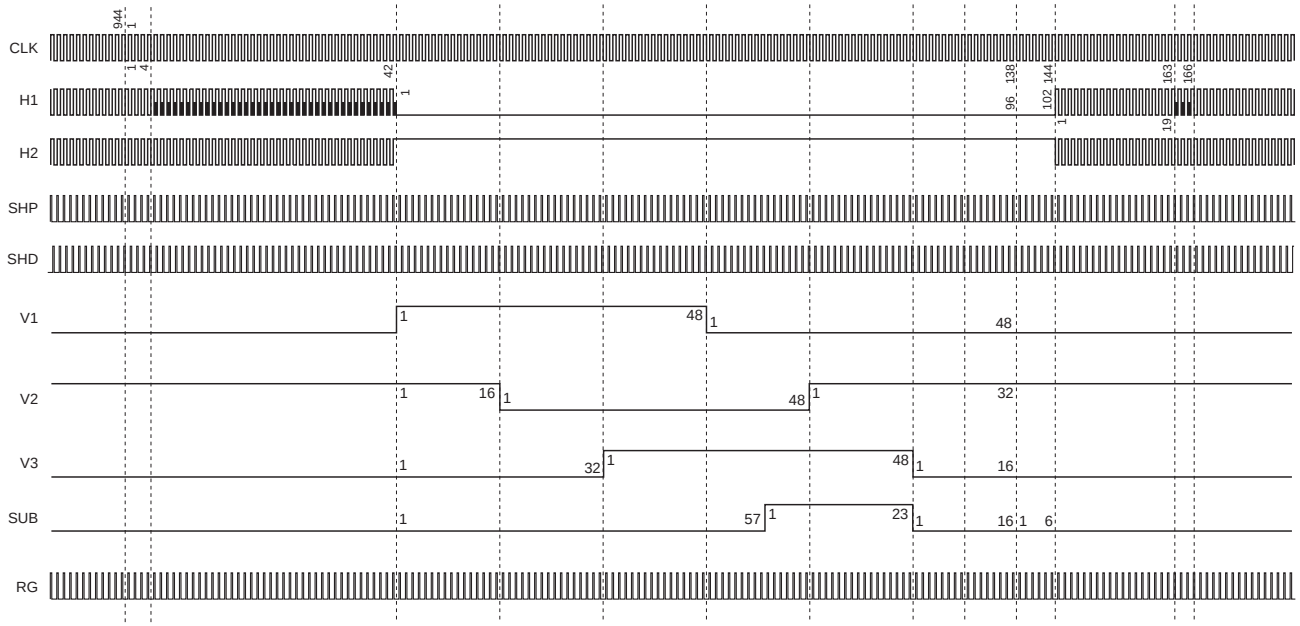


Drive Timing Chart (Vertical Sync "a" Enlarged) **Progressive Scan Mode/Center Scand Mode**

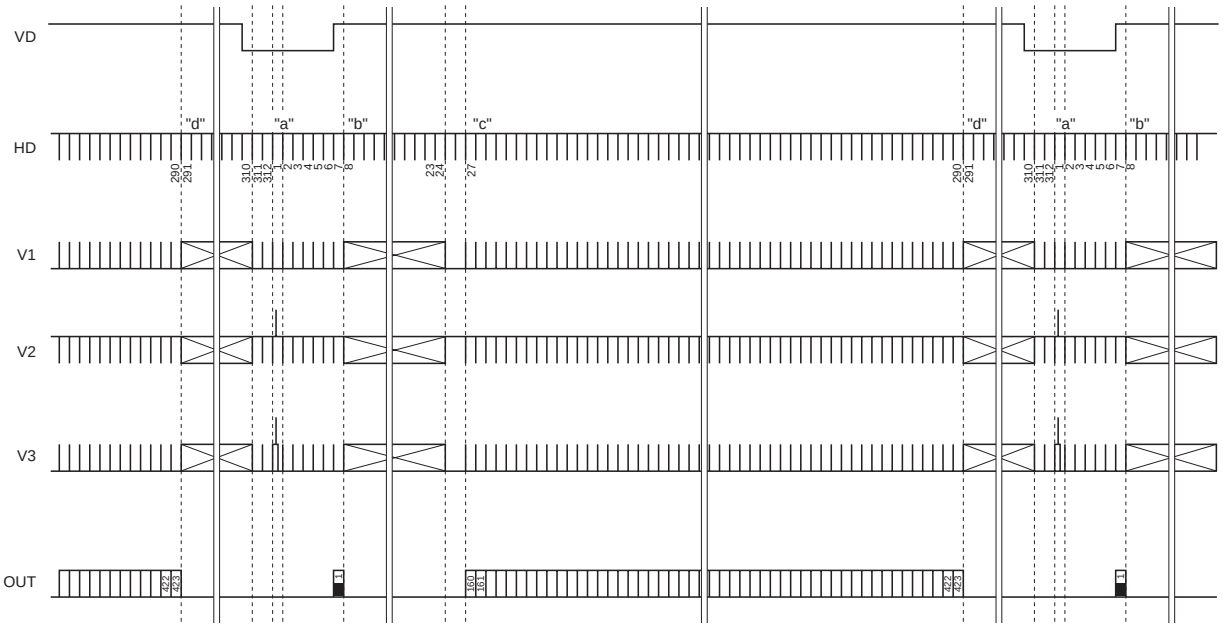
"a" Enlarged



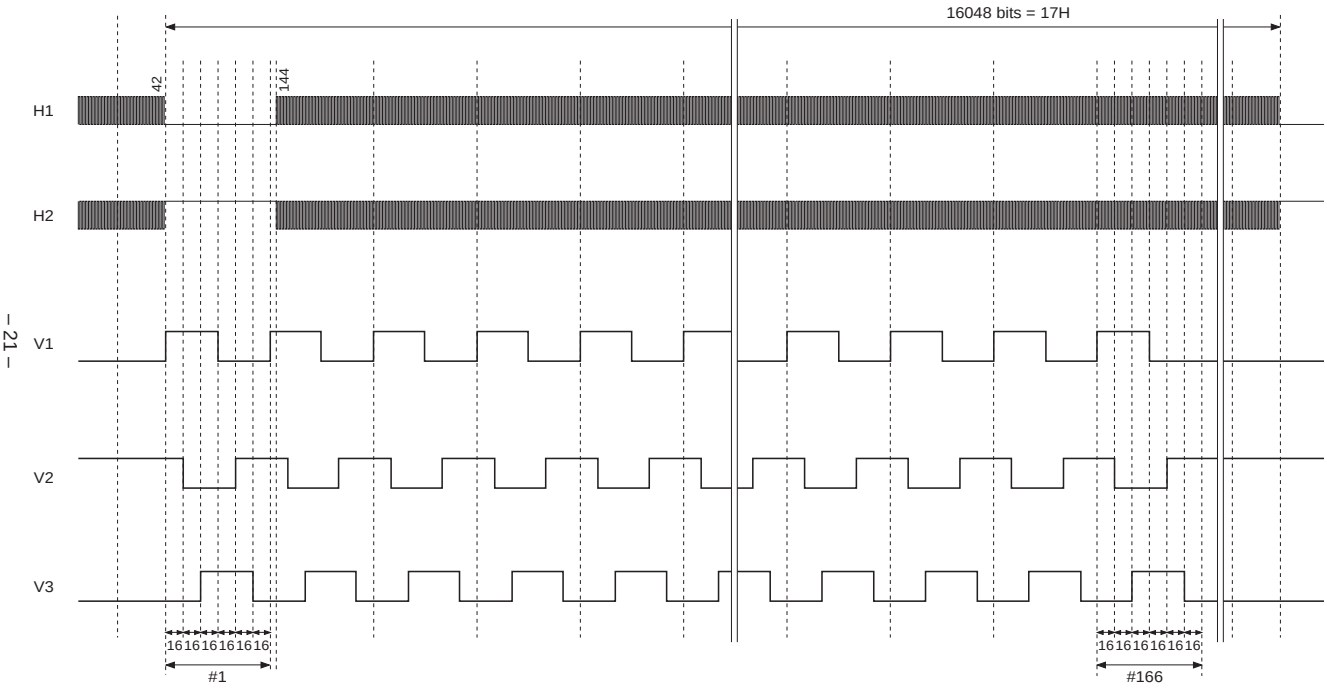
Drive Timing Chart (Horizontal Sync) **Progressive Scan Mode**



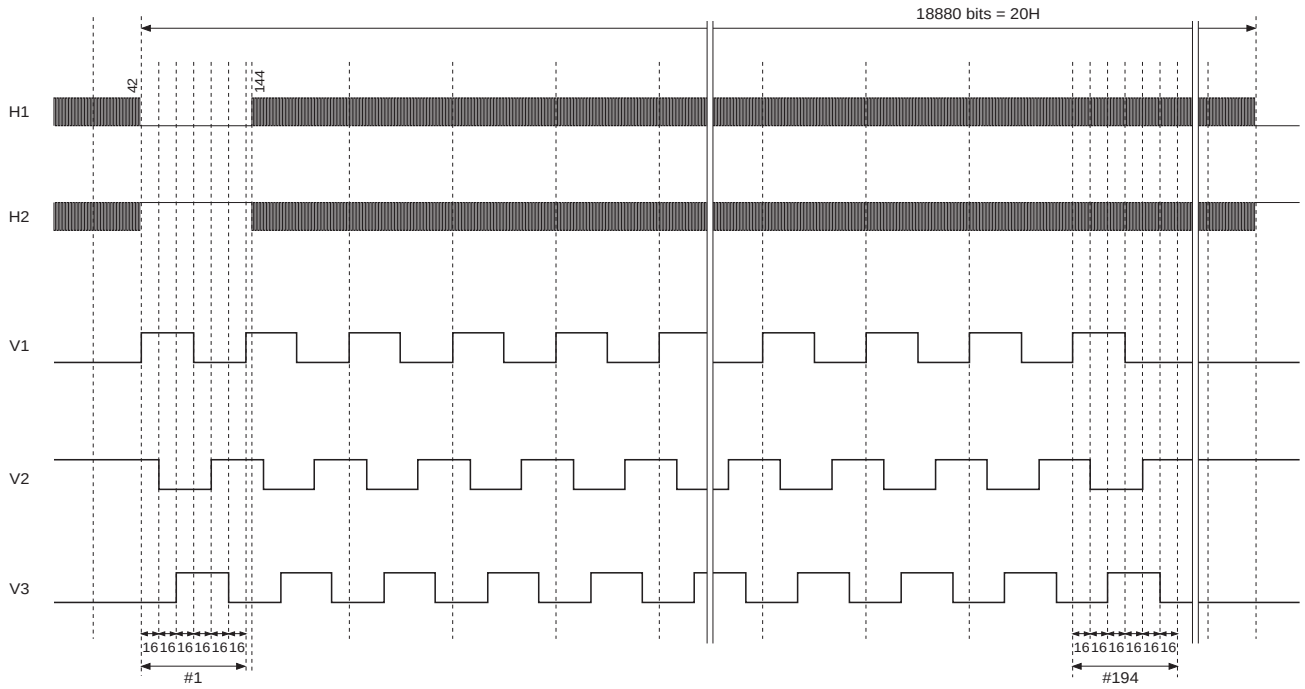
Drive Timing Chart (Vertical Sync) **Center Scan Mode 1**



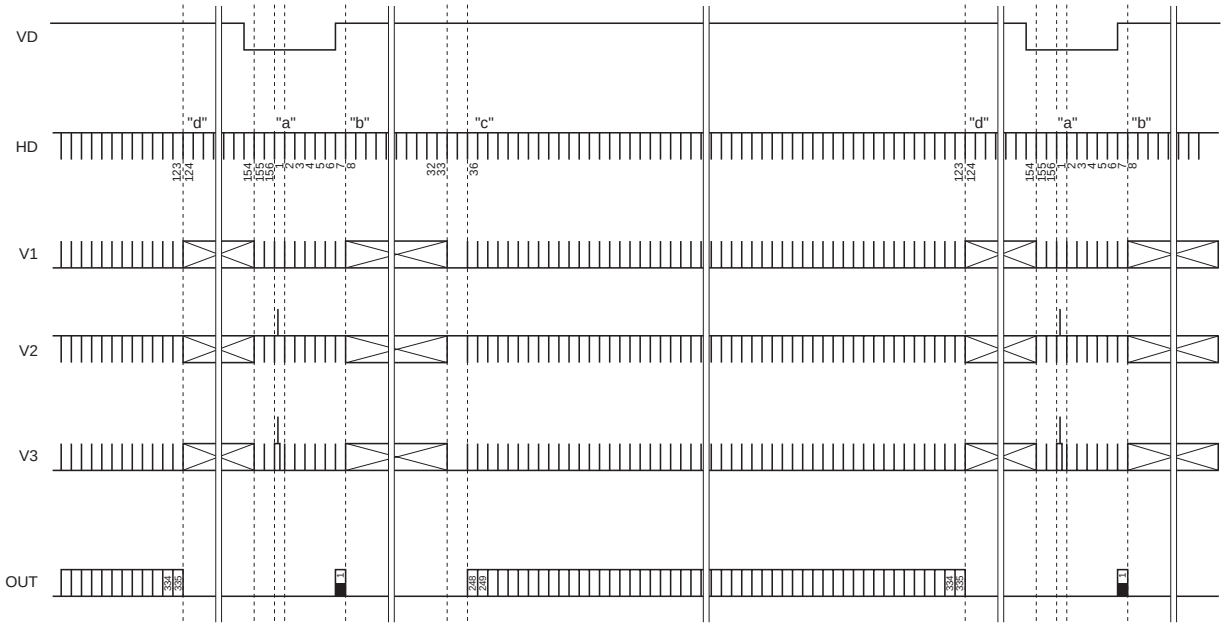
Drive Timing Chart (Horizontal Sync) **Center Scan Mode 1 (Frame Shift) ("b")**



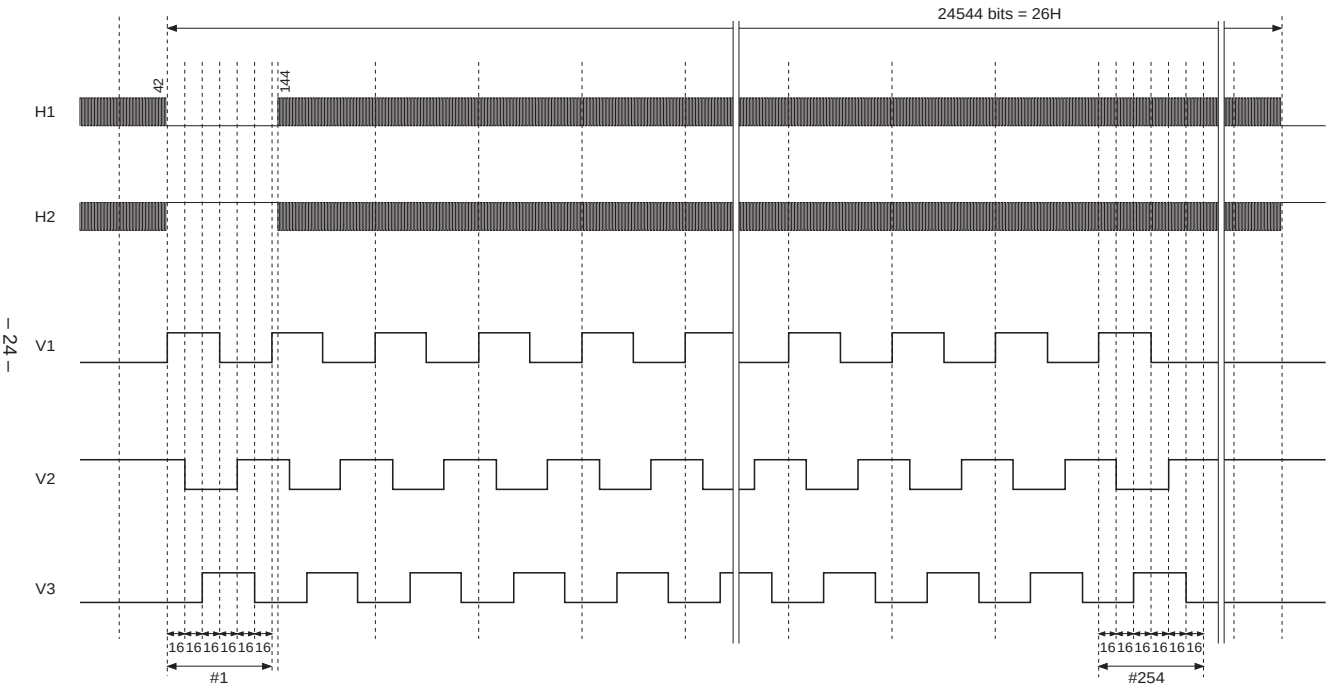
Drive Timing Chart (Horizontal Sync) **Center Scan Mode 1 (High-speed Sweep) ("d")**



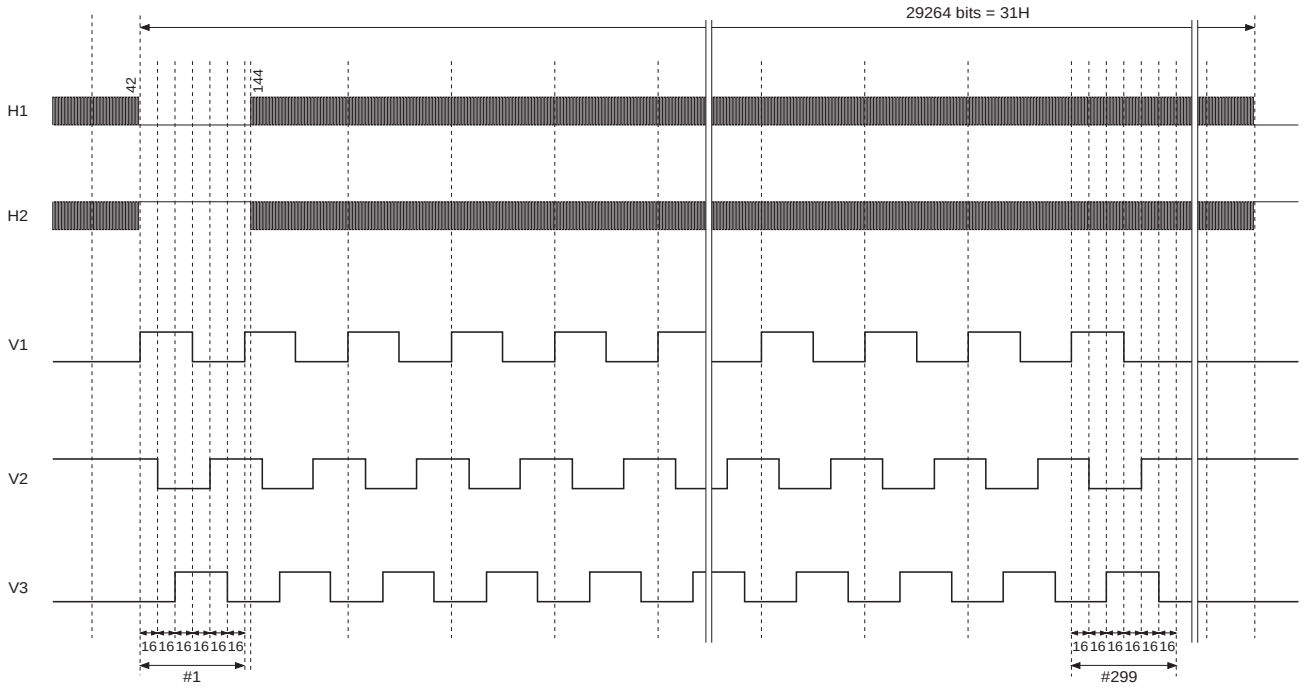
Drive Timing Chart (Vertical Sync) **Center Scan Mode 2**



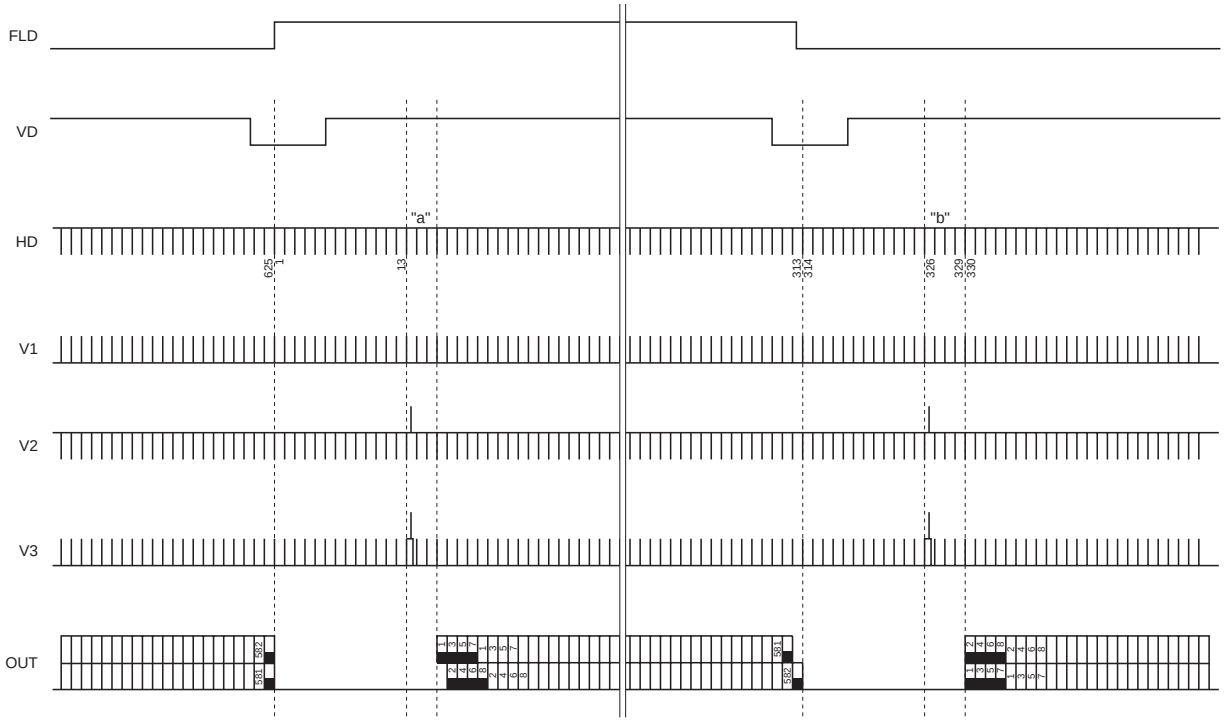
Drive Timing Chart (Horizontal Sync) **Center Scan Mode 2 (Frame Shift) ("b")**



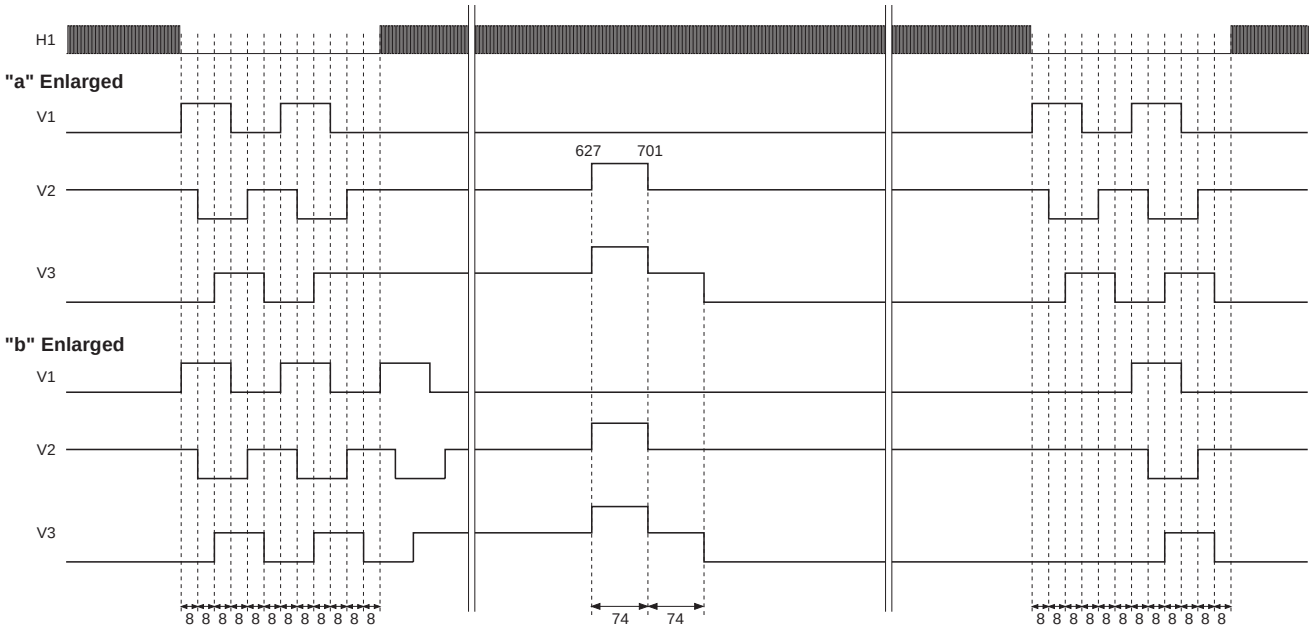
Drive Timing Chart (Horizontal Sync) Center Scan Mode 2 (High-speed Sweep) ("d")



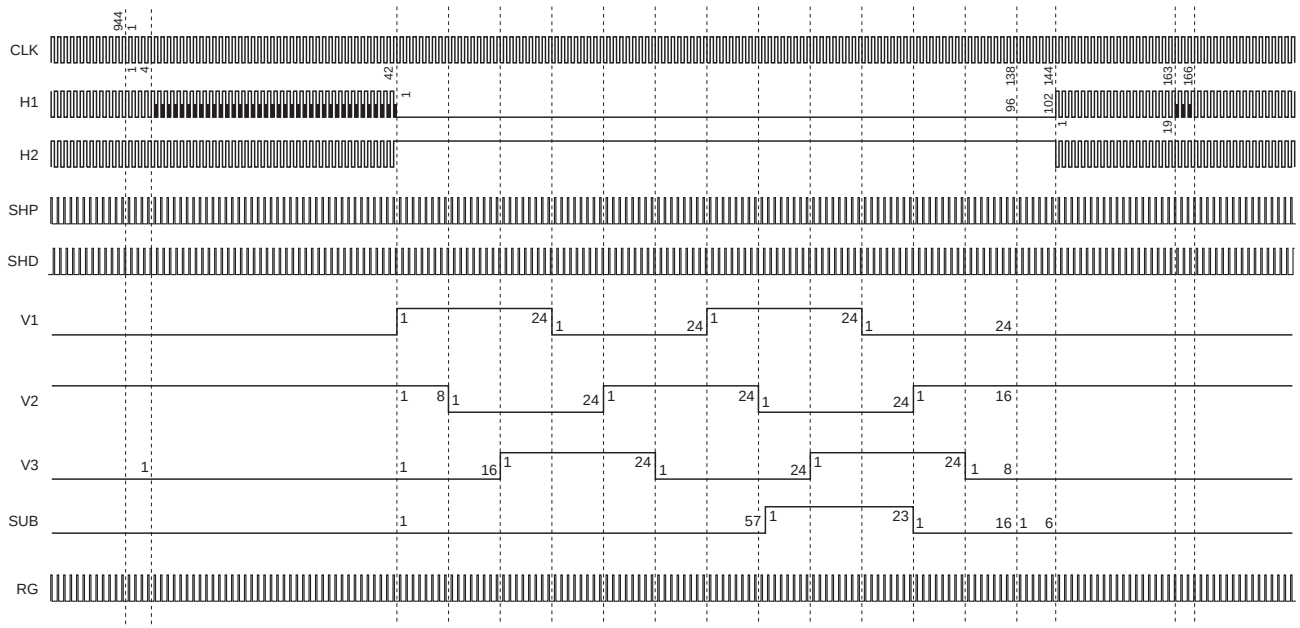
Drive Timing Chart (Vertical Sync) **Field Readout Mode**



Drive Timing Chart (Vertical Sync "a", "b" Enlarged) Field Readout Mode



Drive Timing Chart (Horizontal Sync) **Field Readout Mode**



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

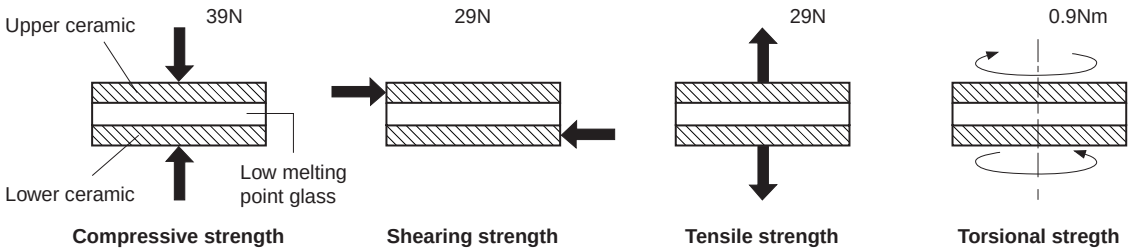
3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

a) Perform all assembly operations in a clean room (class 1000 or less).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)

a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



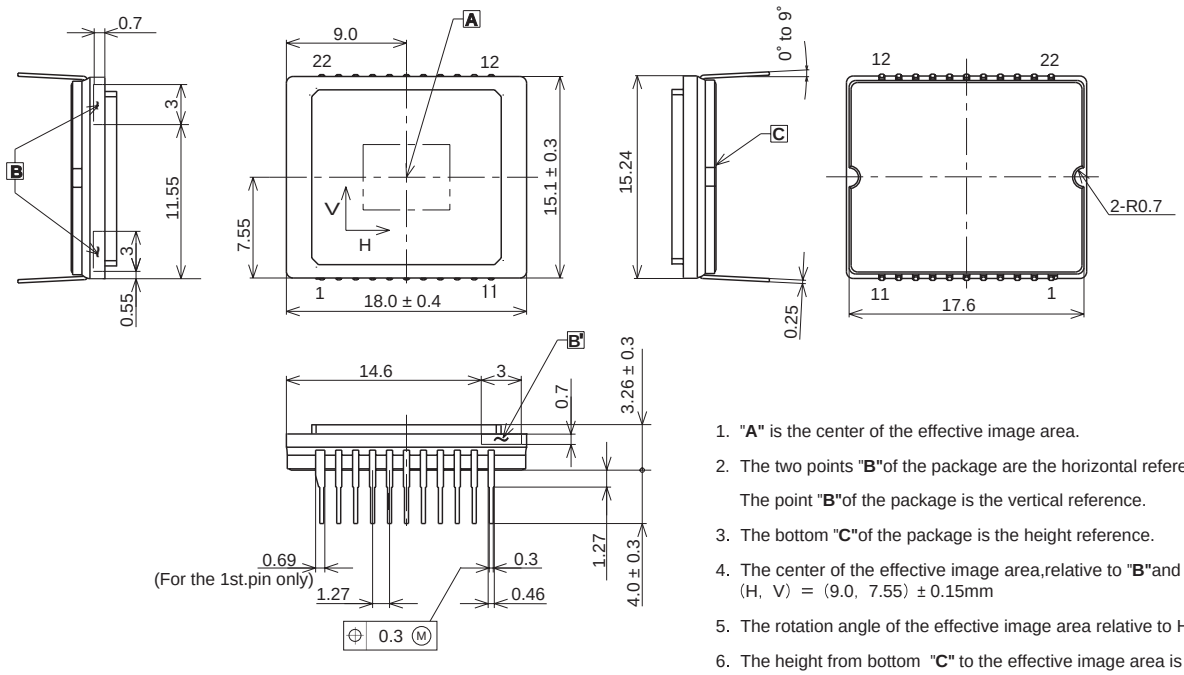
b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portions. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.
d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others
a) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

Package Outline Unit: mm

22 pin DIP (600mil)



PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	2.60g
DRAWING NUMBER	AS-B15-03(E)

1. "**A**" is the center of the effective image area.
2. The two points "**B**"of the package are the horizontal reference.
   The point "**B**"of the package is the vertical reference.
3. The bottom "**C**"of the package is the height reference.
4. The center of the effective image area,relative to "**B**"and "**B'**"is (H, V) = (9.0, 7.55) ± 0.15mm
5. The rotation angle of the effective image area relative to H and V is ± 1°
6. The height from bottom "**C**" to the effective image area is 1.41 ± 0.15mm
7. The tilt of the effective image area relative to the bottom "**C**" is less than 60µm.
8. The thickness of the cover glass is 0.75mm,and the refractive index is 1.5.
9. The notches on the bottom must not be used for reference of fixing.