

BRUSHLESS DC MOTOR COMMUTATOR/CONTROLLER

May 2011

FEATURES:

- Direct drive of PNP and NPN transistors
- Buffered drive of P-Channel and N-Channel FETs
- Six outputs for driving power switching bridge
- Open or closed loop motor control
- +5V to +28V operation ($V_{SS} - V_{DD}$)
- Externally selectable input to output code for 60°, 120°, 240°, or 300° electrical sensor spacing
- Three or four phase operation
- Analog speed control
- Direction control
- Output enable control
- Positive static braking
- Over-current sensing
- LS7262 (DIP), LS7262-S (SOIC), LS7262-TS (TSSOP)

DESCRIPTION:

The LS7262 is a MOS integrated circuit designed to generate the signals necessary to control a three phase or four phase brushless DC motor. LS7262 is the basic building block of a brushless DC motor controller. The circuit responds to changes at the SENSE inputs originating at the motor position sensors to provide electronic commutation of the motor windings. Pulse width modulation of outputs for motor speed control is accomplished through either the ENABLE input or through the Analog input (VTRIP) in conjunction with the OSCILLATOR input. Over-current circuitry is provided to protect the windings, associated drivers and power supply. The over-current circuitry causes the external output drivers to switch off immediately upon sensing the over-current condition and on again only when the over-current condition disappears and the positive edge of either the ENABLE input or the saw-tooth OSCILLATOR occurs. This limits the over-current sense cycling to the chopping rate of the ENABLE input or the saw-tooth OSCILLATOR.

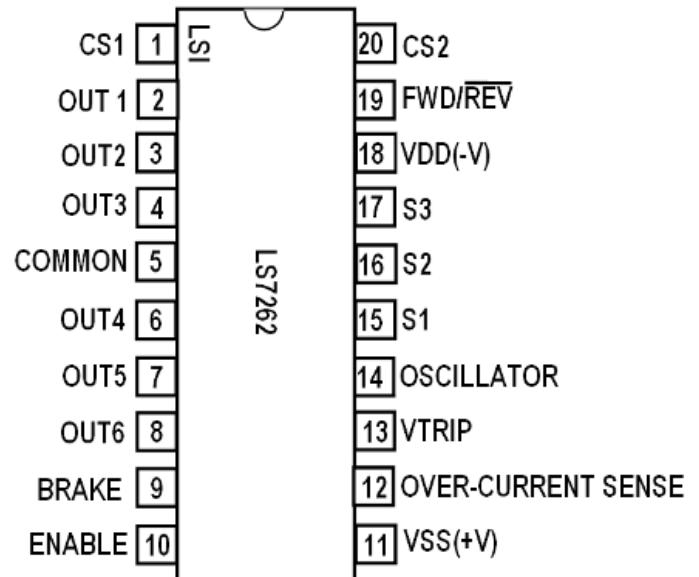
A positive braking feature is provided to effect rapid deceleration. The LS7262 is designed for driving NPN and PNP transistors. Using an additional CMOS driver, the LS7262 outputs are buffered to drive both NMOS and PMOS power FETs and will generate 12V drive for both the N-channel and P-channel devices when using a 12V power supply.

INPUT/OUTPUT DESCRIPTION:

COMMUTATION SELECTS (Pins 1, 20)

These inputs are used to select the proper sequence of outputs based on the electrical separation of the motor position sensors. See Table 3. Note that in all cases the external output drivers are disabled for invalid SENSE input codes. Internal pull down resistors are provided at Pins 1 and 20 causing a logic zero when these pins are left open.

PIN -ASSIGNMENT – TOP VIEW



FORWARD/REVERSE (Pin 19)

This input is used to select the proper sequence of outputs for the desired direction of rotation for the motor (See Table 3). An internal pull-up resistor holds the input high when left open.

SENSE INPUTS (Pins 15, 16, 17)

These inputs provide control of the output commutation sequence as shown in Table 3. S1, S2, S3 originate in the position sensors of the motor and must sequence in cycle code order. Hall switch pull-up resistors are provided at pins 15, 16 and 17. The positive supply of the Hall devices should be common to the chip V_{SS} .

BRAKE (Pin 9)

A high level at this input unconditionally turns off outputs OUT 1, 2 and 3 and turns on outputs OUT 4, 5 and 6 (See Fig. 2). Transistors Q101, Q102 and Q103 cut off and transistors Q104, Q105 and Q106 turn on, shorting the windings together. The BRAKE has priority over all other inputs. An internal pull-down resistor holds the input low when left open. (Center-tapped motor configuration requires a power supply disconnect transistor controlled by the BRAKE signal – See Figure 2A).

ENABLE (Pin 10)

A high level at this input permits the output to sequence as in Table 3, while a low disables all external output drivers. An internal pull-up

resistor holds the input high when left open. Positive edges at this input will reset the over-current flip-flop.

OVER-CURRENT SENSE (Pin 12)

This input provides the user a way of protecting the motor winding, drivers and power supply from an over-load condition. The user provides a fractional-ohm resistor between the negative supply and the common emitters of the NPN drivers or common sources of N-Channel FET drivers. This point is connected to one end of a potentiometer (e.g. 100k ohms), the other end of which is connected to the positive supply. The wiper pick-off is adjusted so that all outputs are disabled for currents greater than the limit. The action of the input is to disable all external output drivers. When BRAKE exists, OVER-CURRENT SENSE will be over-ridden. The over-current circuitry latches the over-current condition. The latch may be reset by the positive edge of either the saw-tooth OSCILLATOR or the ENABLE input. When using the ENABLE input as a chopped input, the OSCILLATOR input should be held at V_{SS} . When the ENABLE input is held high, the OSCILLATOR must be used to reset the over-current latch.

VTRIP (Pin 13)

This input is used in conjunction with the saw-tooth OSCILLATOR input. When the voltage level applied to VTRIP is more negative than the waveform at the OSCILLATOR input, the outputs will be enabled as shown in Table 3. When VTRIP is more positive than the saw-tooth OSCILLATOR waveform the external output drivers are disabled. The saw-tooth waveform at the OSCILLATOR input typically varies from $(0.4 \cdot V_{SS})$ to $(V_{SS} - 2V)$. The purpose of the VTRIP input in conjunction with the OSCILLATOR is to provide variable speed adjustment for the motor by means of PWM for V_{SS} greater than 7V. Below $V_{SS} = 7V$, the IC may only be used as a commutator. (See Note).

Note: Below $V_{SS} = 7V$, the OSCILLATOR saw-tooth amplitude is too small to allow proper operation of the PWM circuitry.

OSCILLATOR (Pin 14)

R and C connected to this input (See Figure 6) provide the timing components for a saw-tooth OSCILLATOR. The signal generated is used in conjunction with VTRIP to provide PWM for variable speed applications and to reset the over-current condition.

OUTPUTS 1,2,3 (Pins 2,3,4)

These open drain outputs are enabled as shown in Table 2 and provide base current to PNP transistors when COMMON is floating or gate drive to P-channel FET drivers when COMMON is tied to V_{SS} .

OUTPUTS 4,5,6 (Pins 6,7,8)

These open drain outputs are enabled in Table 2 and provide base current to NPN transistors when COMMON is floating or gate drive to N-Channel FET drivers when COMMON is tied to V_{SS} .

COMMON (Pin 5)

The COMMON is connected to V_{SS} when using P-Channel and N-Channel drivers (Figure 1). Pin 5 is left floating when using PNP and NPN transistors (Figure 2).

VSS, VDD (Pins 11, 18)

Supply voltage positive and negative terminals.

TYPICAL CIRCUIT OPERATION:

The oscillator is used for motor speed control as explained under VTRIP. Both upper and lower motor drive transistors are pulse width modulated (see Fig.1 or 2) during speed control. The outputs turn on in pairs (See Table 3). For example, in Figure 2, (see dotted line, Fig.2) Q8 and Q4 are on, thus enabling a path from the positive supply through Q101, Q8, Q4, R5 and the emitter-base junction of Q105 and the fractional-ohm resistor to ground. The current in the above described path is determined by the power supply voltage, the voltage across the base-emitter junctions of Q101 and Q105 (1.4V for single transistor or 2.8V for Darlington pairs), the impedance of Q8 and Q4 and the value of R5. Table 1 provides the recommended value for R5. R4 and R6 are the same value.

In Figure 1, the common (Pin 5) is tied to V_{SS} , the outputs still turn on in pairs. By adding external buffers (U1) for outputs O1, O2 and O3 the same sequence of motor winding conduction occurs as is the case for Figure 2. For example when Q8 and Q4 turn on, transistor Q101 and Q105 turn on which is the same as in Figure 2. The other external output pairs turn on similarly and the commutation sequence is identical to that of Figure 2 (as shown in Table 3).

MAXIMUM RATINGS:

| PARAMETER | SYMBOL | VALUE | UNIT |
|-------------------------------|-------------------|-------------|------|
| DC Supply Voltage | $V_{SS} - V_{DD}$ | +35 | V |
| Any Input Voltage to V_{SS} | V_{in} | -30 to +0.5 | V |
| Storage Temperature | T_{STG} | -65 to +150 | °C |
| Operating Temperature | T_A | -40 to +125 | °C |

DC ELECTRICAL CHARACTERISTICS:

(All Voltages Referenced to V_{DD} , $T_A = 25^\circ\text{C}$ unless otherwise specified)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|-------------------------------------|----------|-----|-----|-----|------|
| Supply Voltage | V_{SS} | 5 | - | 28 | V |
| Supply Current (Outputs not loaded) | I_{DD} | - | 4.5 | 6 | mA |

Input Specifications:

| | | | | | |
|--|----------|---------------------|-----|---------------------|-----------|
| BRAKE, ENABLE, CS1, CS2, S1, S2, S3, FWD/REV | R_{IN} | - | 150 | - | $k\Omega$ |
| Voltage (Logic 1) | V_{IH} | $V_{SS} - 1.5$ | - | V_{SS} | V |
| (Logic 0) | V_{IL} | 0 | - | $V_{SS} - 4.0$ | V |
| OVER-CURRENT SENSE (See Note) | | | | | |
| Threshold Voltage | V_{TH} | $(V_{SS}/2) - 0.25$ | | $(V_{SS}/2) + 0.25$ | V |

Oscillator:

| | | | | | |
|-------------------------|-----------|----|------|------|-----------|
| Frequency Range | F_{OSC} | 0 | 1/RC | 100 | KHz |
| External Resistor Range | R_{OSC} | 22 | - | 1000 | $k\Omega$ |

NOTE: Theoretical switching point of the OVER-CURRENT SENSE input is one half of the power supply determined by an internal bias network in manufacturing. Tolerances cause the switching point to vary $\pm 0.25\text{V}$. After manufacture, the switching point remains fixed within 10mV over time and temperature. The input switching sensitivity is a maximum of 50mV. There is no hysteresis on the OVER-CURRENT SENSE input.

TABLE 1
OUTPUT CURRENT LIMITING RESISTOR SELECTION TABLE
OUTPUT CURRENT(mA)

| POWER SUPPLY(V) | 20 | 15 | 10 | 7.5 | 5 | 2.5 | mA |
|-----------------|------|------|------|------|------|------|-----------------------------|
| 6 | ** | ** | ** | ** | ** | 0.24 | |
| 9 | ** | ** | ** | 0.43 | 0.86 | 2.2 | |
| 12 | 0.20 | 0.33 | 0.62 | 0.91 | 1.5 | 3.3 | |
| 15 | 0.36 | 0.56 | 0.91 | 1.3 | 2.2 | 4.3 | Resistance ($k\Omega$) |
| 18 | * | 0.75 | 1.2 | 1.6 | 2.7 | 5.1 | |
| 21 | * | * | 1.5 | 2.0 | 3.3 | 6.2 | |
| 24 | * | * | 1.8 | 2.3 | 3.6 | 7.5 | |
| 28 | * | * | * | 2.7 | 4.3 | 9.1 | |

*causes excessive power dissipation

**exceeds max current possible for this voltage

TABLE 2
For Power Supply 5V – 28V

| R1 ($k\Omega$) | Output Voltage |
|------------------|----------------|
| 10 | $V_{SS}-0.5$ |
| 4.0 | $V_{SS}-1.0$ |
| 1.5 | $V_{SS}-2.0$ |

TABLE 3.
OUTPUT COMMUTATION SEQUENCE FOR THREE PHASE OPERATION

| SEQUENCE SELECT | CS1 | CS2 | CS1 | CS2 | CS1 | CS2 | CS1 | CS2 | FWD/REV = 1 | | | | | | FWD/REV = 0 | | | | | | | | | |
|-----------------------|-------|-----|--------|-----|--------|-----|--------|-----|-----------------|----|---------|----|--------------|-----------------|-------------|---------|-----|----|--------------|-----|-----|-----|--|--|
| | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | OUTPUTS ENABLED | | DRIVERS | | | OUTPUTS ENABLED | | DRIVERS | | | | | | | | |
| ELECTRICAL SEPARATION | (60°) | | (120°) | | (240°) | | (300°) | | | | A | B | C | | | A | B | C | | | | | | |
| SENSE INPUTS | S1 | S2 | S3 | S1 | S2 | S3 | S1 | S2 | S3 | S1 | S2 | S3 | | | | | | | | | | | | |
| | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | O1 | O5 | + | - | Off | O2 | O4 | - | + | Off | | |
| | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | O3 | O5 | Off | - | + | O2 | O6 | Off | + | - | | |
| | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | O3 | O4 | - | Off | + | O1 | O6 | + | Off | - | | |
| | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | O2 | O4 | - | + | Off | O1 | O5 | + | - | Off | | |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | O2 | O6 | Off | + | - | O3 | O5 | Off | - | + | | |
| | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | O1 | O6 | + | Off | - | O3 | O4 | - | Off | + | | |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | ALL DISABLED | | | | | | ALL DISABLED | | | | | |
| | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | ALL DISABLED | | | | | | ALL DISABLED | | | | | |

The OVER-CURRENT input (BRAKE = low) enables external output drivers in normal sequence when more negative than VSS/2 and disables all external output drivers when more positive than VSS/2. The OVER-CURRENT is sensed continuously, and sets a flip-flop which is reset by the rising edge of the ENABLE input or the saw-tooth OSCILLATOR. (See description under OVER-CURRENT SENSE.)

The VTRIP input (BRAKE = low) enables the outputs in normal sequence when more negative than the OSC input and disables all outputs when more positive than the OSC input. The VTRIP input may be disabled by connecting it to VDD and the OSC input to VSS. (See description under VTRIP)

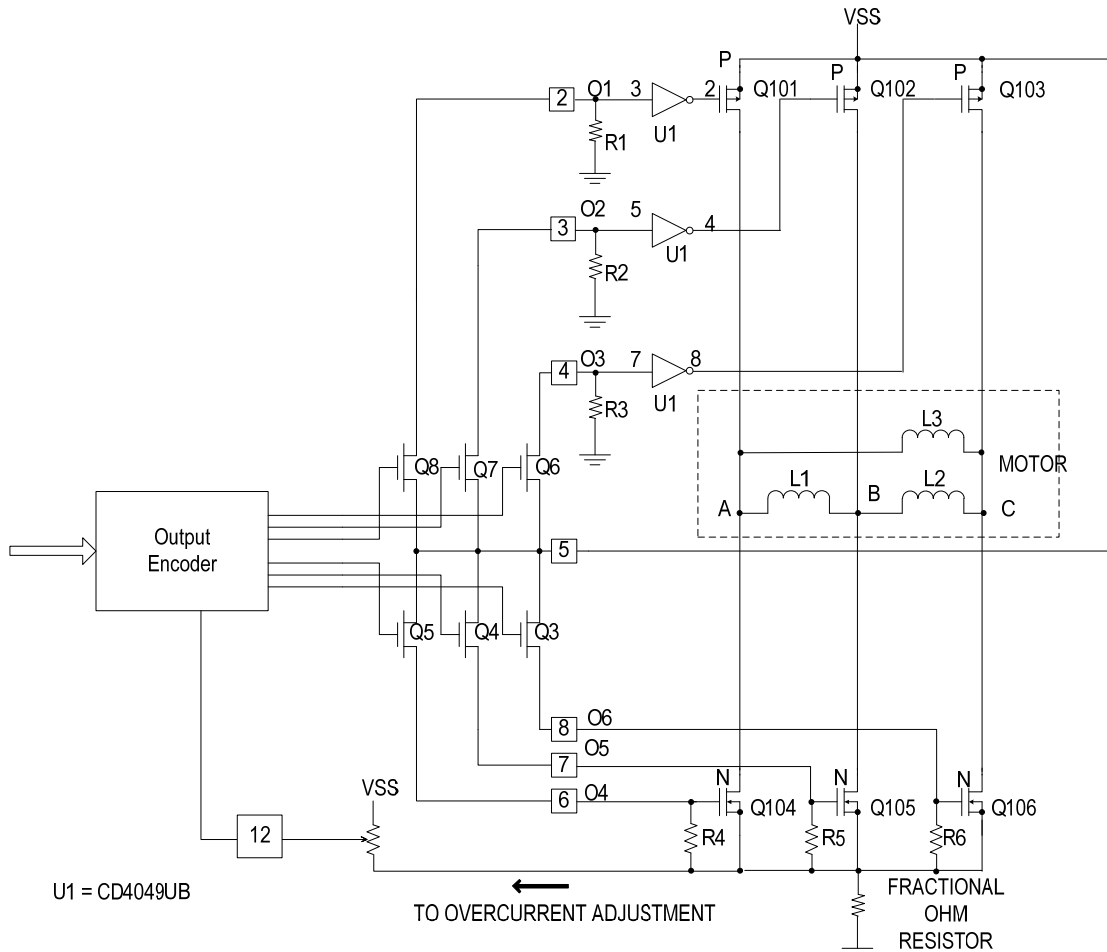


FIGURE 1. LS7262 THREE PHASE OUTPUT DRIVER CIRCUITRY

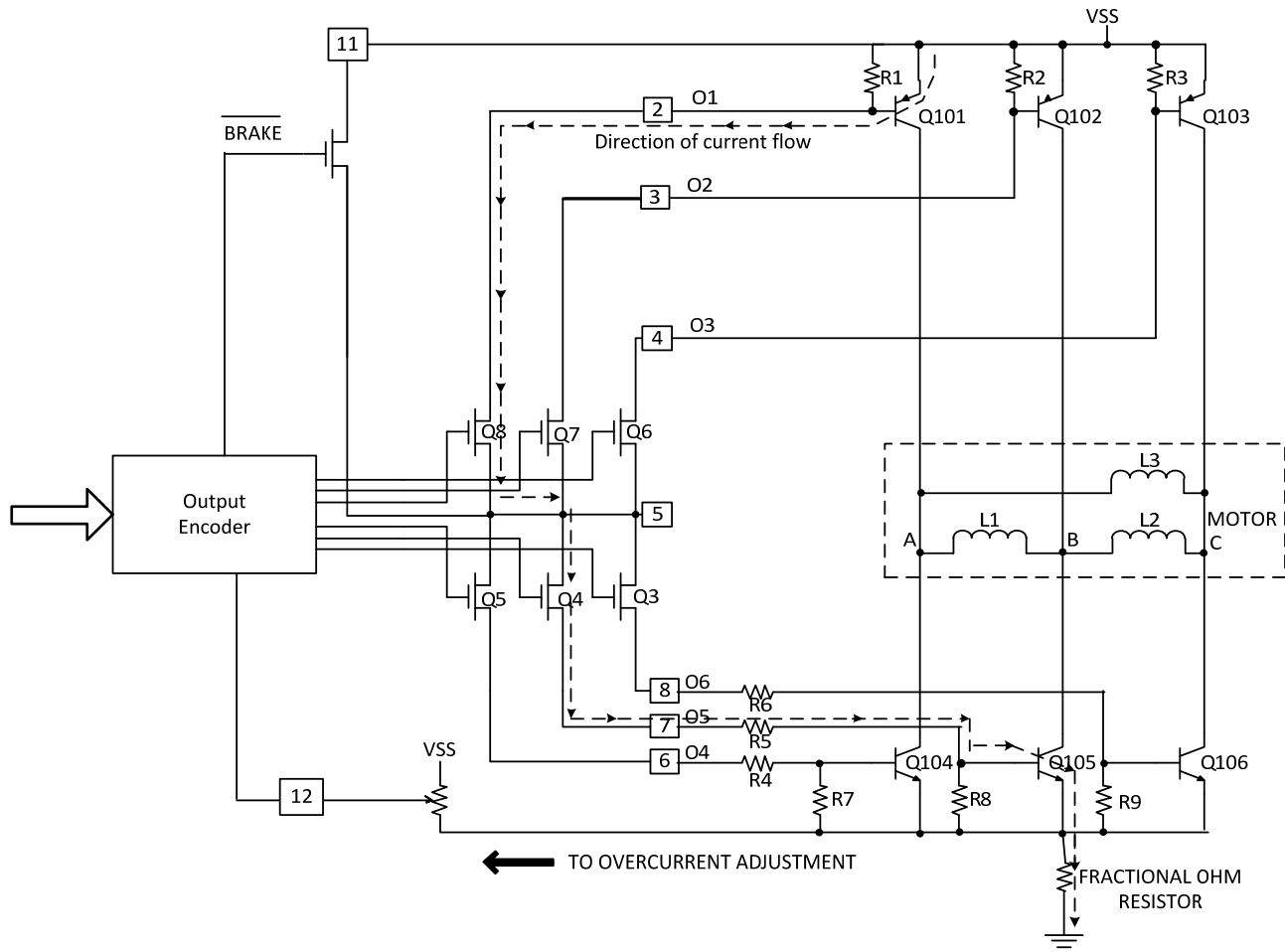


FIGURE 2. LS7262 THREE PHASE OUTPUT DRIVER CIRCUITRY

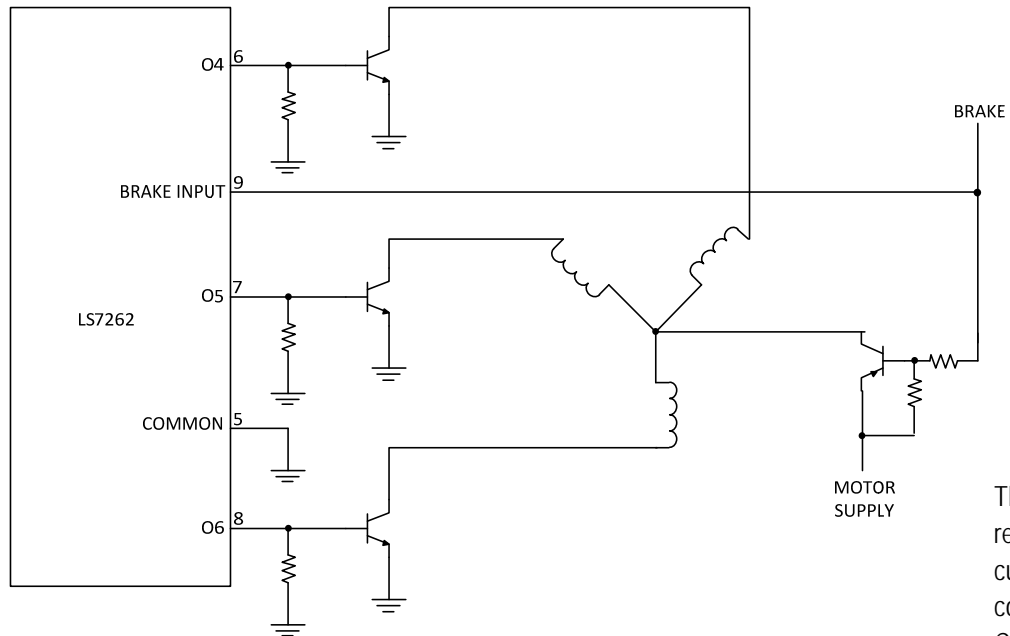


FIGURE 2A. SINGLE-ENDED DRIVER CIRCUIT

This configuration requires only one base current limiting resistor connected from the COMMON pin to VSS.

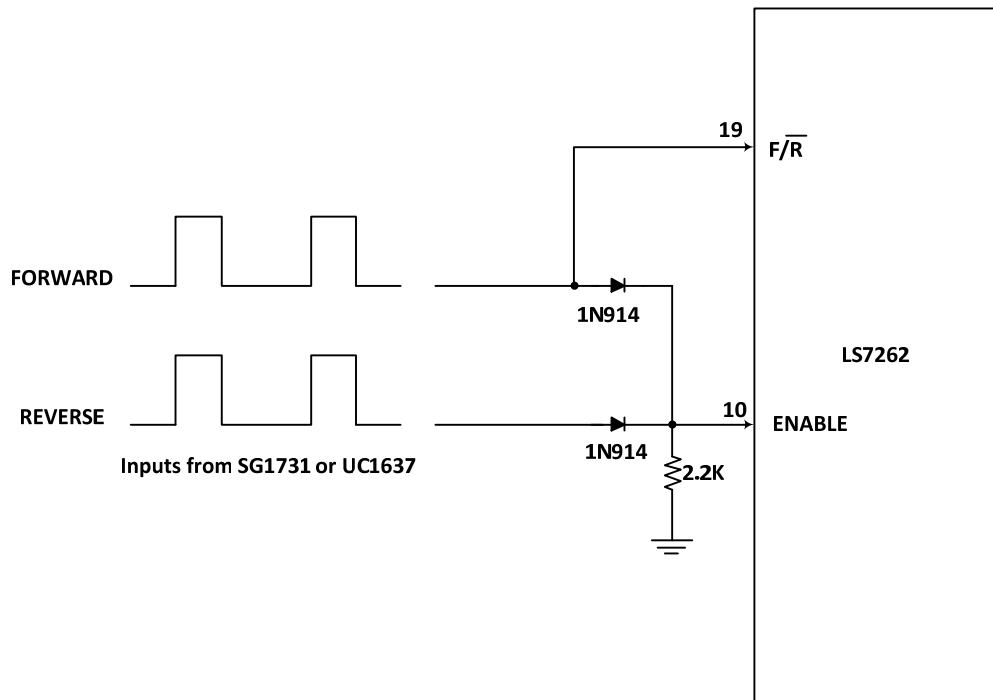


FIGURE 3. PRECISION CONTROL BRUSHLESS DC MOTOR DRIVE

For controlled acceleration and deceleration of motors in the forward or reverse directions, a motor control pulse width modulator circuit such as the SG1731 or UC1637 can be interfaced with the LS7262.

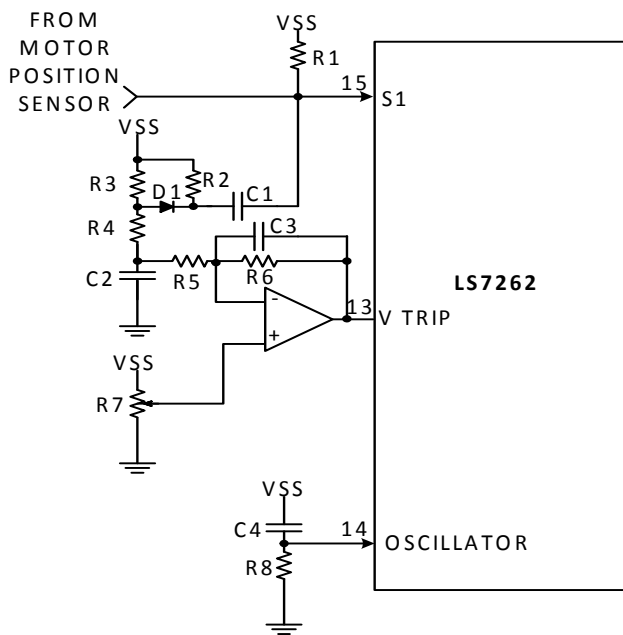
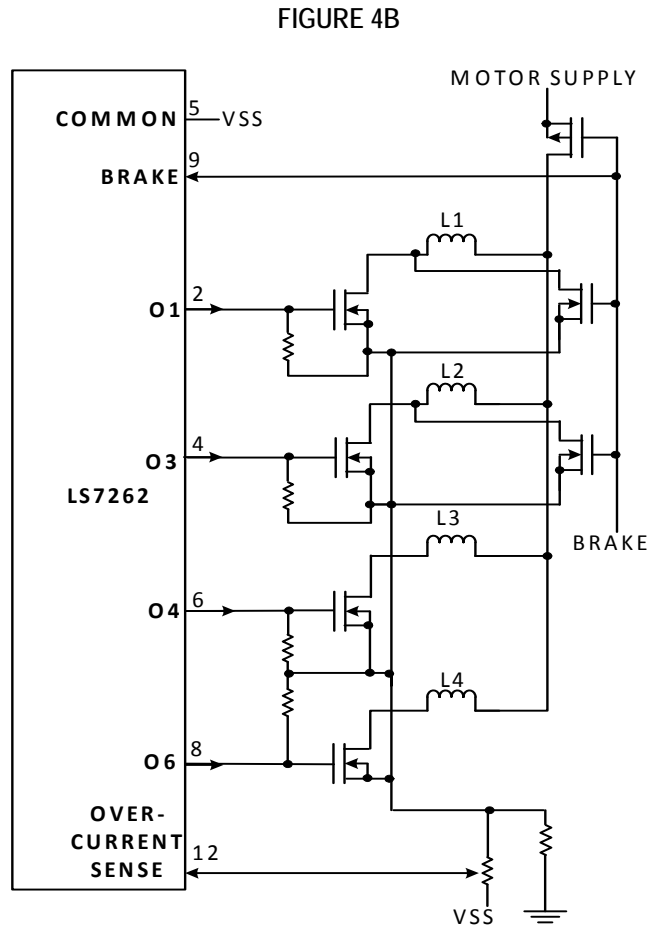
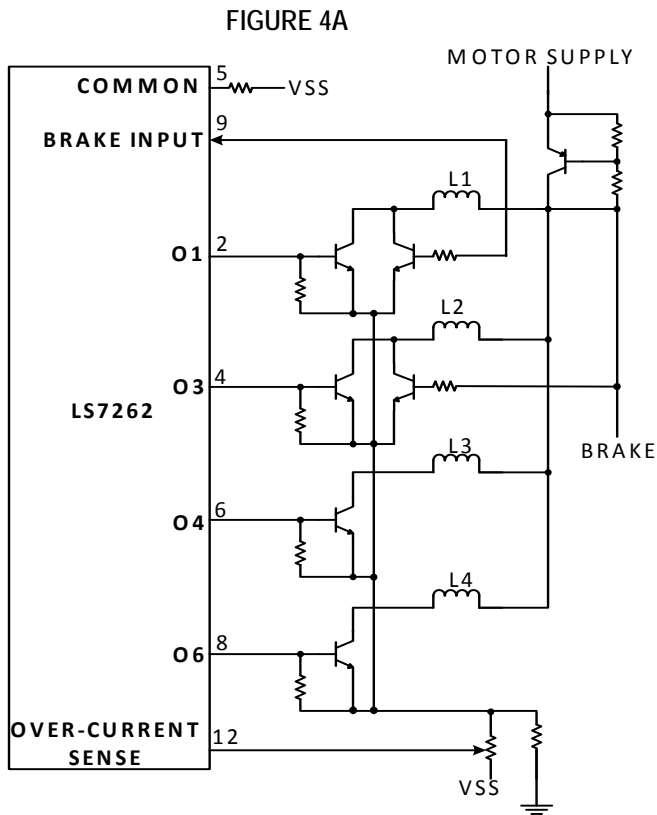
The logical OR gate made up of the resistor-diode network permits the LS7262 to be enabled when either the forward or reverse input is high. By applying the forward input directly to Pin 19, the motor can only operate in the forward direction when the forward input is high and only in the reverse direction when the reverse input is high. Motor direction is determined by relative pulse widths of the forward and reverse inputs while acceleration or deceleration is determined by variations of these widths.

TABLE 4.
OUTPUT COMMUTATION SEQUENCE FOR FOUR PHASE OPERATION
CS1=CS2=0 OUTPUTS ENABLED

| S1 | S2,S3 | FWD/REV=1 | FWD/REV=0 |
|----|-------|-----------|-----------|
| 0 | 0 | 01 | 04 |
| 1 | 0 | 03 | 06 |
| 1 | 1 | 04 | 01 |
| 0 | 1 | 06 | 03 |

For four phase commutation (See Fig.4), the COMMUTATION SELECT inputs must both be tied low. The S1 input is driven from one motor position sensor while the S2 and S3 inputs are connected together and driven by the second position sensor. The COMMON input must be connected to VSS. The sensors have an electrical separation of 90°. Figure 4A indicates the use of Bipolar Transistors. Figure 4B indicates the use of FETs.

FIGURE 4. FOUR PHASE OUTPUT DRIVER CIRCUITRY



A closed loop system can be configured by differentiating one of the motor position sense inputs and integrating only the negative pulses to form a DC voltage that is applied to the inverting input of an op-amp. The non-inverting input voltage is adjusted with a potentiometer until the resultant voltage at VTRIP causes the motor to run at desired speed. The R2-C1 differentiator, the R3-D1 negative pulse transmitter and the R4-C2 integrator form a frequency to voltage converter. An increase in motor speed above the desired speed causes VTRIP to increase which lowers the PWM and the resultant motor speed. A decrease in speed lowers VTRIP and raises the PWM and the resultant motor speed. For proper operation, both R5 and R6 should be greater than R4 and R4 in turn should be greater than both R2 and R3. Also, the R4-C2 time constant should be greater than the R2-C1 time constant. C3 may be added across R6 for additional VTRIP smoothing.

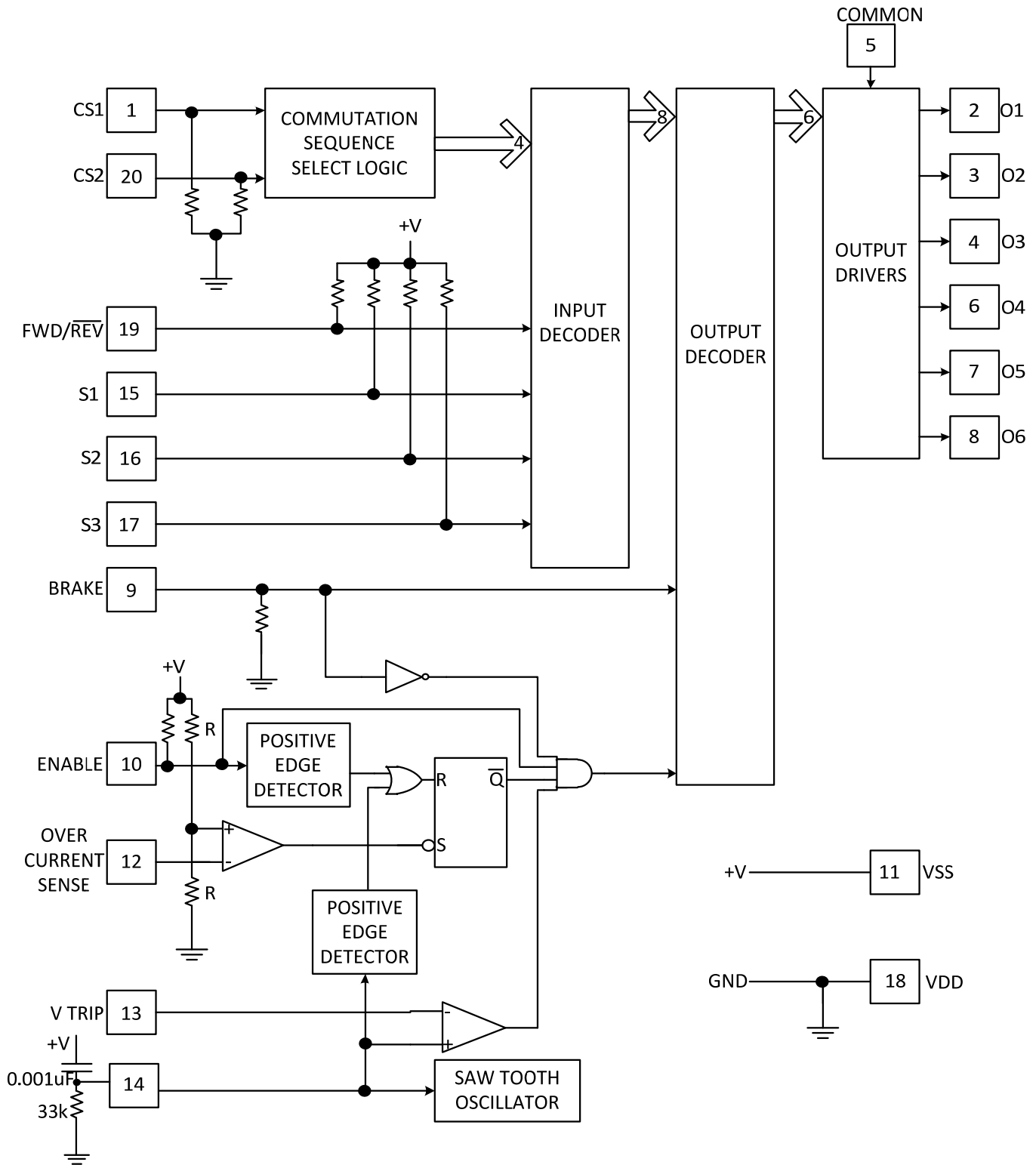


FIGURE 6. LS7262 BLOCK DIAGRAM

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc assumes no responsibilities for inaccuracies, or for any infringements of patent rights of others which may result from its use.