SONY

# ICX058AL

## 1/3-inch CCD Image Sensor for EIA Black-and-White Video Camera

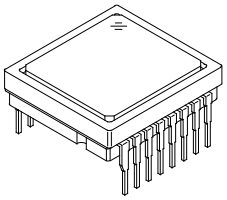
**For the availability of this product, please contact the sales office.**

### Description

The ICX058AL is an interline CCD solid-state image sensor suitable for EIA black-and-white video cameras. High sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

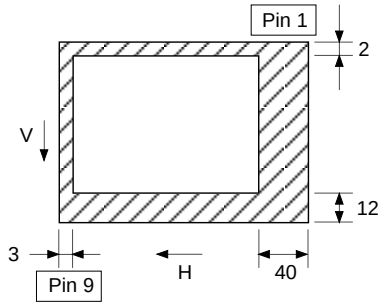
This chip features a field period readout system and an electronic shutter with variable charge-storage time.

16 pin DIP (Plastic)



### Features

- High resolution, high sensitivity and low dark current
- Continuous variable-speed shutter
  1/60s (Typ.), 1/100s to 1/10000s
- Low smear
- Excellent antiblooming characteristics
- Horizontal register: 5V drive
- Reset gate: 5V drive




**Optical black position (Top View)**

### Device Structure

- Optical size: 1/3-inch format
- Number of effective pixels: 768 (H) × 494 (V) approx. 380K pixels
- Number of total pixels: 811 (H) × 508 (V) approx. 410K pixels
- Interline CCD image sensor
- Chip size: 6.00mm (H) × 4.96mm (V)
- Unit cell size: 6.35µm (H) × 7.40µm (V)
- Optical black: Horizontal (H) direction: Front 3 pixels, rear 40 pixels
  Vertical (V) direction: Front 12 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 22
  Vertical 1 (even field only)
- Substrate material: Silicon

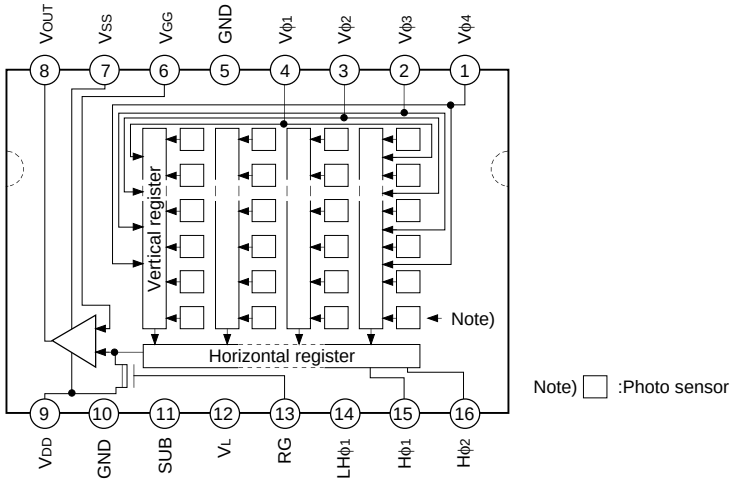




E92210C5Z-PS

## Block Diagram and Pin Configuration

(Top View)




## Pin Description

| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---|---|---|---|---|---|
| 1 | $V\phi_4$ | Vertical register transfer clock | 9 | $V_{DD}$ | Output amplifier drain supply |
| 2 | $V\phi_3$ | Vertical register transfer clock | 10 | GND | GND |
| 3 | $V\phi_2$ | Vertical register transfer clock | 11 | SUB | Substrate (Overflow drain) |
| 4 | $V\phi_1$ | Vertical register transfer clock | 12 | $V_L$ | Protective transistor bias |
| 5 | GND | GND | 13 | RG | Reset gate clock |
| 6 | $V_{GG}$ | Output amplifier gate bias | 14 | $LH\phi_1$ | Horizontal register final stage transfer clock |
| 7 | $V_{SS}$ | Output amplifier source | 15 | $H\phi_1$ | Horizontal register transfer clock |
| 8 | $V_{OUT}$ | Signal output | 16 | $H\phi_2$ | Horizontal register transfer clock |

## Absolute Maximum Ratings

| Item | | Ratings | Unit | Remarks |
|---|---|---|---|---|
| Substrate voltage SUB – GND | | –0.3 to +55 | V | |
| Supply voltage | $V_{DD}$, $V_{OUT}$, $V_{SS}$ – GND | –0.3 to +18 | V | |
| | $V_{DD}$, $V_{OUT}$, $V_{SS}$ – SUB | –55 to +10 | V | |
| Vertical clock input voltage | $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ – GND | –15 to +20 | V | |
| | $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ – SUB | to +10 | V | |
| Voltage difference between vertical clock input pins | | to +15 | V | *1 |
| Voltage difference between horizontal clock input pins | | to +17 | V | |
| $H\phi_1$, $H\phi_2$ – $V\phi_4$ | | –17 to +17 | V | |
| $H\phi_1$, $H\phi_2$, $LH\phi_1$, RG, $V_{GG}$ – GND | | –10 to +15 | V | |
| $H\phi_1$, $H\phi_2$, $LH\phi_1$, RG, $V_{GG}$ – SUB | | –55 to +10 | V | |
| $V_L$ – SUB | | –65 to +0.3 | V | |
| $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $V_{DD}$, $V_{OUT}$ – $V_L$ | | –0.3 to +30 | V | |
| RG – $V_L$ | | –0.3 to +24 | V | |
| $V_{GG}$, $V_{SS}$, $H\phi_1$, $H\phi_2$, $LH\phi_1$ – $V_L$ | | –0.3 to +20 | V | |
| Storage temperature | | –30 to +80 | ℃ | |
| Operating temperature | | –10 to +60 | ℃ | |

*1 +27V (Max.) when clock width < 10µs, clock duty factor < 0.1%.

**Bias Conditions**

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Output amplifier drain voltage | $V_{DD}$ | 14.55 | 15.0 | 15.45 | V | |
| Output amplifier gate voltage | $V_{GG}$ | 3.8 | 4.2 | 4.65 | V | |
| Output amplifier source | $V_{SS}$ | Grounded with 820Ω resistor | | | | ±5% |
| Substrate voltage adjustment range | $V_{SUB}$ | 9.0 | | 18.5 | V | *1 |
| Fluctuation range after substrate voltage adjustment | $\Delta V_{SUB}$ | –3 | | +3 | % | |
| Reset gate clock voltage adjustment range | $V_{RGL}$ | 1.0 | | 4.0 | V | *1, *6 |
| Fluctuation range after reset gate clock voltage adjustment | $\Delta V_{RGL}$ | –3 | | +3 | % | |
| Protective transistor bias | $V_L$ | *2 | | | | |

**DC Characteristics**

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Output amplifier drain current | $I_{DD}$ | | 5 | | mA | |
| Input current | $I_{IN1}$ | | | 1 | μA | *3 |
| Input current | $I_{IN2}$ | | | 10 | μA | *4 |

*1 Indications of substrate voltage ($V_{SUB}$) · reset gate clock voltage ($V_{RGL}$) setting value.
The setting values of substrate voltage and reset gate clock voltage are indicated on the back of the image sensor by a special code. Adjust substrate voltage ($V_{SUB}$) and reset gate clock voltage ($V_{RGL}$) to the indicated voltage. Fluctuation range after adjustment is ±3%.

$V_{SUB}$ code one character indication □ □
$V_{RGL}$ code one character indication ↑ ↑
$V_{RGL}$ code $V_{SUB}$ code

Code and optimal setting correspond to each other as follows.

| $V_{RGL}$ code | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| Optimal setting | 1.0 | 1.5 | 2.0 | 2.5 | 3.0 | 3.5 | 4.0 |

| $V_{SUB}$ code | E | f | G | h | J | K | L | m | N | P | Q | R | S | T | U | V | W | X | Y | Z |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Optimal setting | 9.0 | 9.5 | 10.0 | 10.5 | 11.0 | 11.5 | 12.0 | 12.5 | 13.0 | 13.5 | 14.0 | 14.5 | 15.0 | 15.5 | 16.0 | 16.5 | 17.0 | 17.5 | 18.0 | 18.5 |

<Example> "5L" → $V_{RGL}$ = 3.0V
$V_{SUB}$ = 12.0V

*2 $V_L$ setting is the $V_{VL}$ voltage of the vertical transfer clock waveform.

*3
1) Current to each pin when 18V is applied to $V_{DD}$, $V_{OUT}$, Vss and SUB pins, while pins that are not tested are grounded.
2) Current to each pin when 20V is applied sequentially to $V\phi_1$, $V\phi_2$, $V\phi_3$ and $V\phi_4$ pins, while pins that are not tested are grounded. However, 20V is applied to SUB pin.
3) Current to each pin when 15V is applied sequentially to RG, $LH\phi_1$, $H\phi_1$, $H\phi_2$ and $V_{GG}$ pins, while pins that are not tested are grounded. However, 15V is applied to SUB pin.
4) Current to $V_L$ pin when 30V is applied to $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $V_{DD}$ and $V_{OUT}$ pins or when, 24V is applied to RG pin or when, 20V is applied to $V_{GG}$, Vss, $H\phi_1$, $H\phi_2$ and $LH\phi_1$ pins, while $V_L$ pin is grounded. However, GND and SUB pins are left open.

*4 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

**Clock Voltage Conditions**

| Item | Symbol | Min. | Typ. | Max. | Unit | Waveform diagram | Remarks |
|---|---|---|---|---|---|---|---|
| Readout clock voltage | $V_{VT}$ | 14.55 | 15.0 | 15.45 | V | 1 | |
| Vertical transfer clock voltage | $V_{VH1}$, $V_{VH2}$ | –0.05 | 0 | 0.05 | V | 2 | $V_{VH} = (V_{VH1} + V_{VH2})/2$ |
| | $V_{VH3}$, $V_{VH4}$ | –0.2 | 0 | 0.05 | V | 2 | |
| | $V_{VL1}$, $V_{VL2}$, $V_{VL3}$, $V_{VL4}$ | –9.0 | –8.5 | –8.0 | V | 2 | $V_{VL} = (V_{VL3} + V_{VL4})/2$ |
| | $V\phi_V$ | 7.8 | 8.5 | 9.05 | V | 2 | $V\phi_V = V_{VHn} – V_{VLn}$ (n = 1 to 4) |
| | $\lvert V_{VH1} – V_{VH2} \rvert$ | | | 0.1 | V | 2 | |
| | $V_{VH3} – V_{VH}$ | –0.25 | | 0.1 | V | 2 | |
| | $V_{VH4} – V_{VH}$ | –0.25 | | 0.1 | V | 2 | |
| | $V_{VHH}$ | | | 0.5 | V | 2 | High-level coupling |
| | $V_{VHL}$ | | | 0.5 | V | 2 | High-level coupling |
| | $V_{VLH}$ | | | 0.5 | V | 2 | Low-level coupling |
| | $V_{VLL}$ | | | 0.5 | V | 2 | Low-level coupling |
| Horizontal transfer clock voltage | $V\phi_H$, $V\phi_{LH}$ | 4.75 | 5.0 | 5.25 | V | 3 | *5 |
| | $V_{HL}$, $V_{LHL}$ | –0.05 | 0 | 0.05 | V | 3 | *5 |
| Reset gate clock voltage | $V\phi_{RG}$ | 4.5 | 5.0 | 5.5 | V | 4 | *6 |
| | $V_{RGLH} – V_{RGLL}$ | | | 0.8 | V | 4 | Low-level coupling |
| Substrate clock voltage | $V\phi_{SUB}$ | 22.5 | 23.5 | 24.5 | V | 5 | |

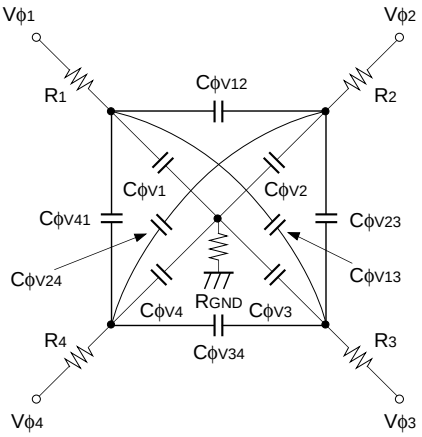
*5 The horizontal final stage transfer clock input pin $LH\phi_1$ is connected to the horizontal transfer clock input pin $H\phi_1$.

*6 The reset gate clock voltage need not be adjusted when reset gate clock is driven when the specifications are as given below. In this case, the reset gate clock voltage setting indicated on the back of the image sensor has not significance.

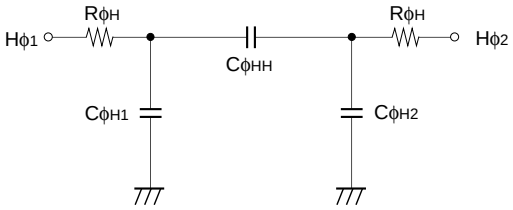
| Item | Symbol | Min. | Typ. | Max. | Unit | Waveform diagram | Remarks |
|---|---|---|---|---|---|---|---|
| Reset gate clock voltage | $V_{RGL}$ | –0.2 | 0 | 0.2 | V | 4 | |
| | $V\phi_{RG}$ | 8.5 | 9.0 | 9.5 | V | 4 | |

**Clock Equivalent Circuit Constant**

| Item | Symbol | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| Capacitance between vertical transfer clock and GND | $C_{\phi V1}$, $C_{\phi V3}$ | | 1000 | | pF | |
| | $C_{\phi V2}$, $C_{\phi V4}$ | | 560 | | pF | |
| Capacitance between vertical transfer clocks | $C_{\phi V12}$, $C_{\phi V34}$ | | 470 | | pF | |
| | $C_{\phi V23}$, $C_{\phi V41}$ | | 330 | | pF | |
| | $C_{\phi V13}$ | | 220 | | pF | |
| | $C_{\phi V24}$ | | 100 | | pF | |
| Capacitance between horizontal transfer clock and GND | $C_{\phi H1}$, $C_{\phi H2}$ | | 47 | | pF | |
| Capacitance between horizontal transfer clocks | $C_{\phi HH}$ | | 43 | | pF | |
| Capacitance between horizontal final stage transfer clock and GND | $C_{\phi LH}$ | | 8 | | pF | |
| Capacitance between reset gate clock and GND | $C_{\phi RG}$ | | 8 | | pF | |
| Capacitance between substrate clock and GND | $C_{\phi SUB}$ | | 270 | | pF | |
| Vertical transfer clock series resistor | $R_1$, $R_2$, $R_3$, $R_4$ | | 80 | | Ω | |
| Vertical transfer clock ground resistor | $R_{GND}$ | | 15 | | Ω | |
| Horizontal transfer clock series resistor | $R_{\phi H}$ | | 15 | | Ω | |



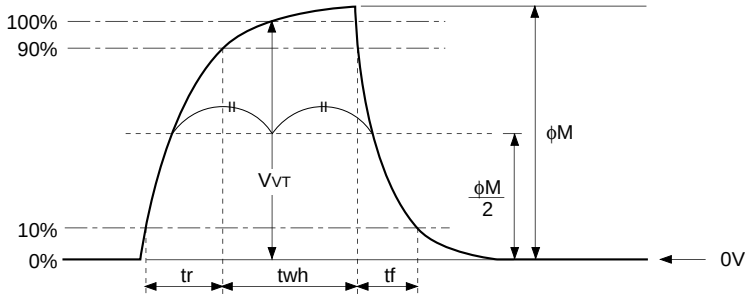

**Vertical transfer clock equivalent circuit**



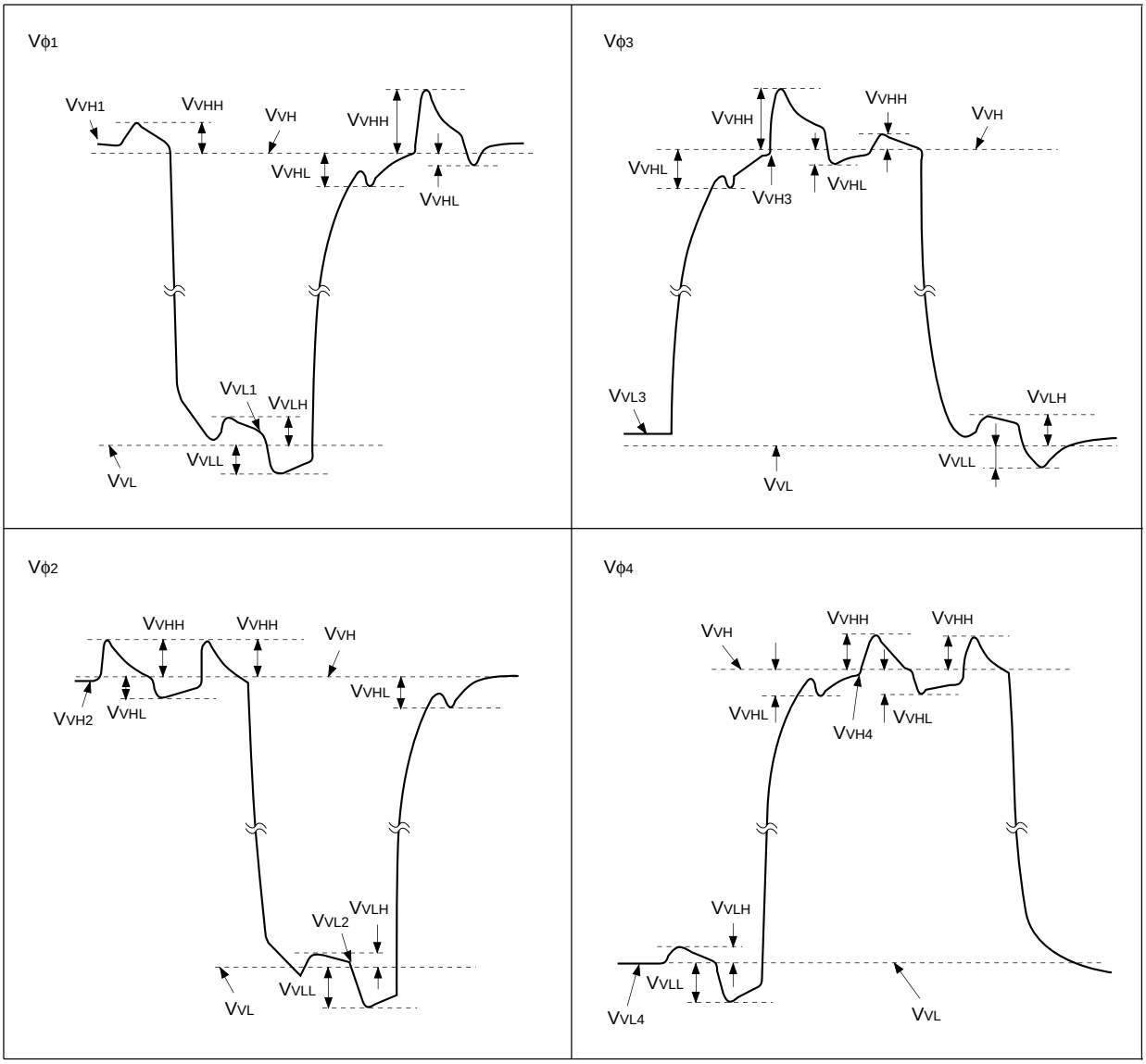

**Horizontal transfer clock equivalent circuit**

## Drive Clock Waveform Conditions

### (1) Readout clock waveform




### (2) Vertical transfer clock waveform

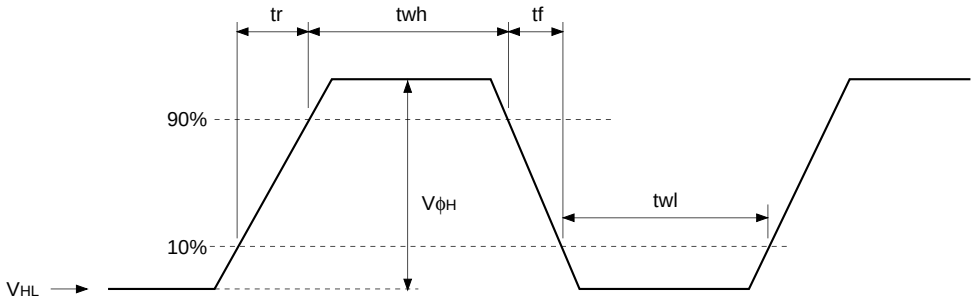



$V_{VH} = (V_{VH1} + V_{VH2})/2$

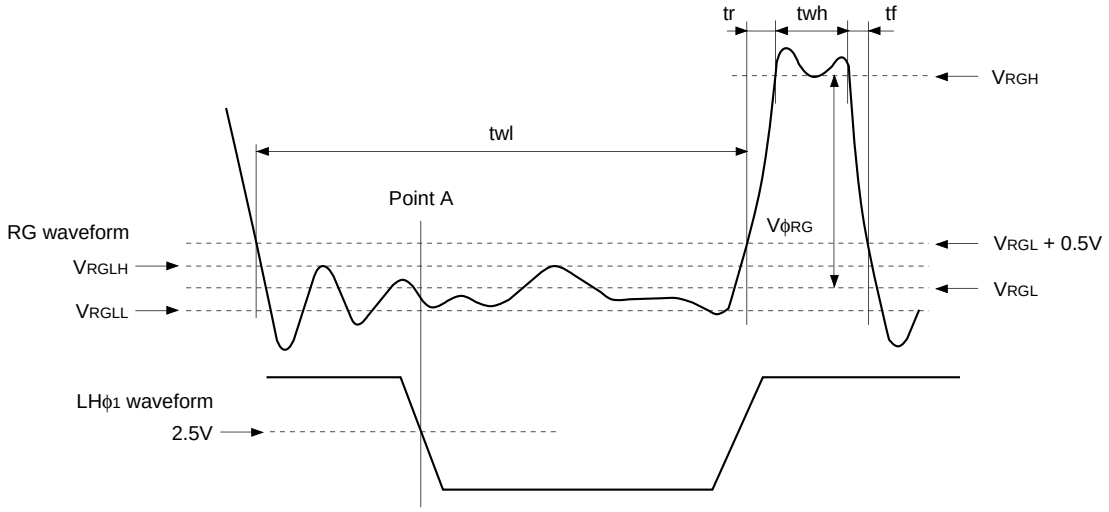
$V_{VL} = (V_{VL3} + V_{VL4})/2$

$V_{\phi V} = V_{VH}n - V_{VL}n$ (n = 1 to 4)

### (3) Horizontal transfer clock waveform




### (4) Reset gate clock waveform




$V_{RGLH}$ is the maximum value and $V_{RGLL}$ is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.

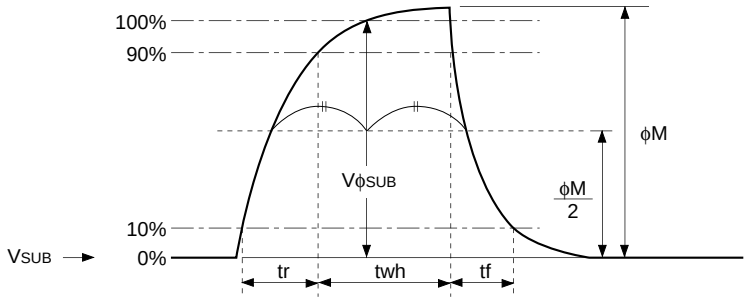
In addition, $V_{RGL}$ is the average value of $V_{RGLH}$ and $V_{RGLL}$.

$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming $V_{RGH}$ is the minimum value during the interval twh, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

**(5) Substrate clock waveform**




**Clock Switching Characteristics**

**Note)** Because the horizontal final stage transfer clock LHφ1 is connected to the horizontal transfer clock Hφ1, specifications will be the same as Hφ1.

| Item | | Symbol | twh | | | twl | | | tr | | | tf | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Readout clock | | VT | 2.3 | 2.5 | | | | | | 0.5 | | | 0.5 | | µs | During readout |
| Vertical transfer clock | | Vφ1, Vφ2, Vφ3, Vφ4 | | | | | | | | | | 15 | | 250 | ns | *1 |
| Horizontal transfer clock | During imaging | Hφ1, LHφ1 | 18 | 24 | | 19.5 | 26 | | | 10 | 17.5 | | 10 | 17.5 | ns | *2 |
| | | Hφ2 | 21 | 26 | | 19 | 24 | | | 10 | 15 | | 10 | 15 | | |
| | During parallel-serial conversion | Hφ1, LHφ1 | | 5.38 | | | | | | 0.01 | | | 0.01 | | µs | |
| | | Hφ2 | | | | | 5.38 | | | 0.01 | | | 0.01 | | | |
| Reset gate clock | | φRG | 11 | 13 | | | 51 | | | 3 | | | 3 | | ns | |
| Substrate clock | | φSUB | 1.5 | 1.8 | | | | | | | 0.5 | | | 0.5 | µs | During drain charge |

*1 When vertical transfer clock driver CXD1250 is used.

*2 tf ≥ tr – 2ns, and the cross-point voltage (VCR) for the Hφ1 · LHφ1 rising side of the Hφ1 · LHφ1 and Hφ2 waveforms must be at least 2.5V.

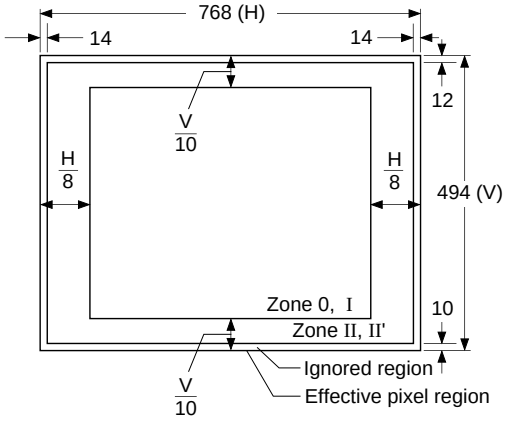
| Item | Symbol | two | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Horizontal transfer clock | Hφ1 · LHφ1, Hφ2 | 16 | 20 | | ns | *3 |

*3 The overlap period for twh and twl of horizontal transfer clocks Hφ1 · LHφ1 and Hφ2 is two.

**Image Sensor Characteristics** (Ta = 25°C)

| Item | Symbol | Min. | Typ. | Max. | Unit | Measurement method | Remarks |
|---|---|---|---|---|---|---|---|
| Sensitivity | S | 240 | 300 | | mV | 1 | |
| Saturation signal | Vsat | 600 | | | mV | 2 | Ta = 60°C |
| Smear | Sm | | 0.009 | 0.015 | % | 3 | |
| Video signal shading | SH | | | 20 | % | 4 | Zone 0 and I |
| | | | | 25 | % | 4 | Zone 0 to II' |
| Dark signal | Vdt | | | 2 | mV | 5 | Ta = 60°C |
| Dark signal shading | ΔVdt | | | 1 | mV | 6 | Ta = 60°C |
| Flicker | F | | | 2 | % | 7 | |
| Lag | Lag | | | 0.5 | % | 8 | |

**Zone Definition of Video Signal Shading**



## Image Sensor Characteristics Measurement Method

### ◎ Measurement conditions

1) In the following measurements, the substrate voltage and the reset gate clock voltage are set to the values indicated on the device, and the device drive conditions are at the typical values of the bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, and the value measured at point [*A] in the drive circuit example is used.

### ◎ Definition of standard imaging conditions

1) Standard imaging condition I:
Use a pattern box (luminance 706cd/$m^2$, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (Vs) at the center of the screen and substitute the value into the following formula.

$$S = Vs \times \frac{250}{60} \text{ [mV]}$$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with average value of the signal output, 200mV, measure the minimum value of the signal output.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of the signal output, 200mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value VSm [mV] of the signal output and substitute the value into the following formula.

$$Sm = \frac{VSm}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [\%] (1/10V method conversion value)}$$

4. Video signal shading
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 200mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (Vmax - Vmin)/200 \times 100 \text{ [\%]}$$

5. Dark signal
Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading

After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

$\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Flicker

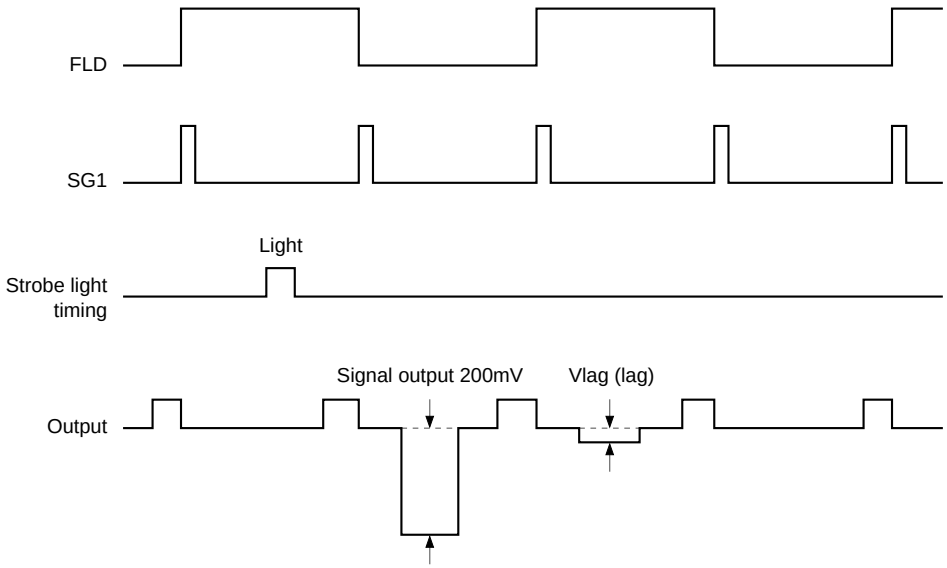
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the signal output is 200mV, and then measure the difference in the signal level between fields ($\Delta Vf$ [mV]). Then substitute the value into the following formula.

$F = (\Delta Vf/200) \times 100$ [%]

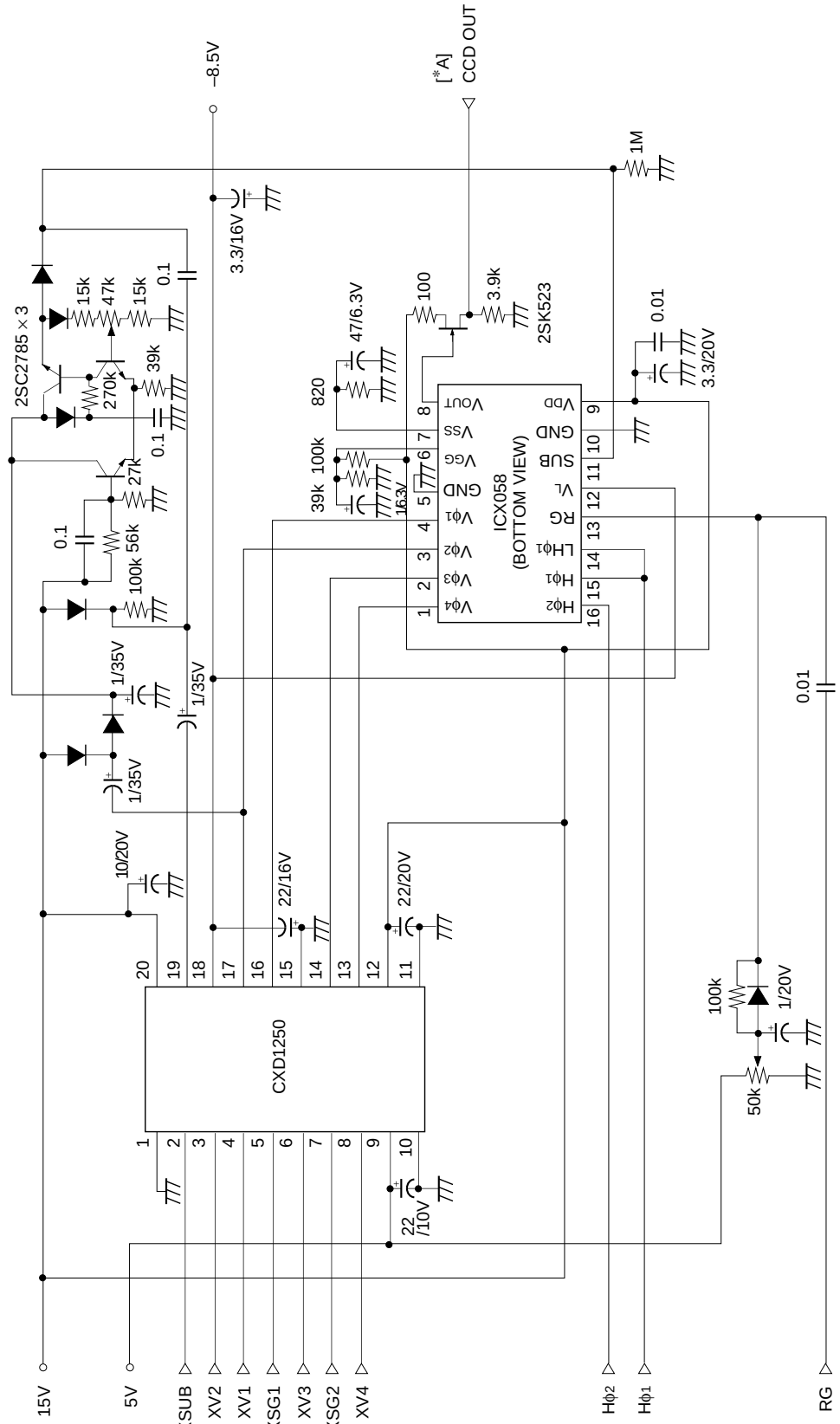
8. Lag

Adjust the signal output value generated by strobe light to 200mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

$Lag = (Vlag/200) \times 100$ [%]

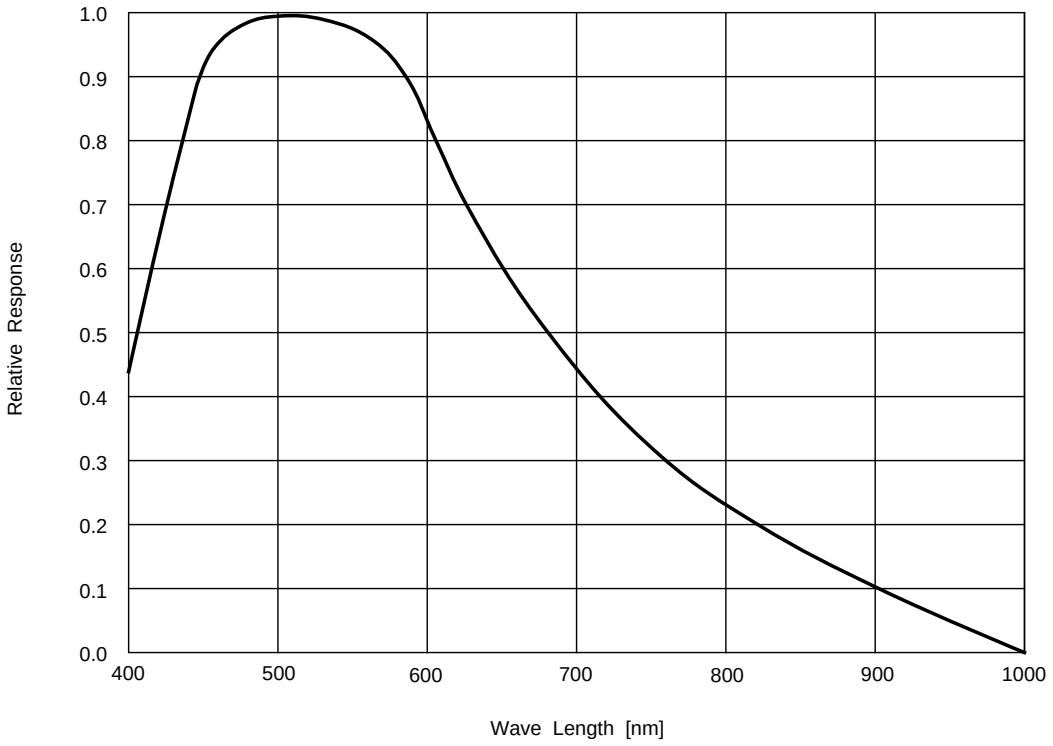


**Drive Circuit**

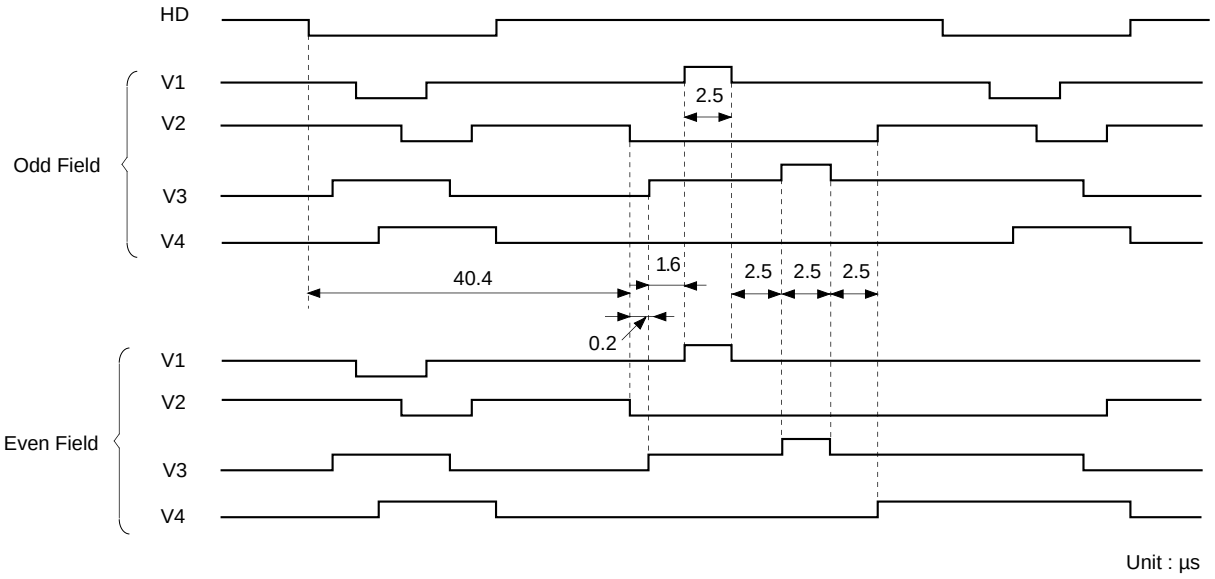


**Spectral Sensitivity Characteristics**

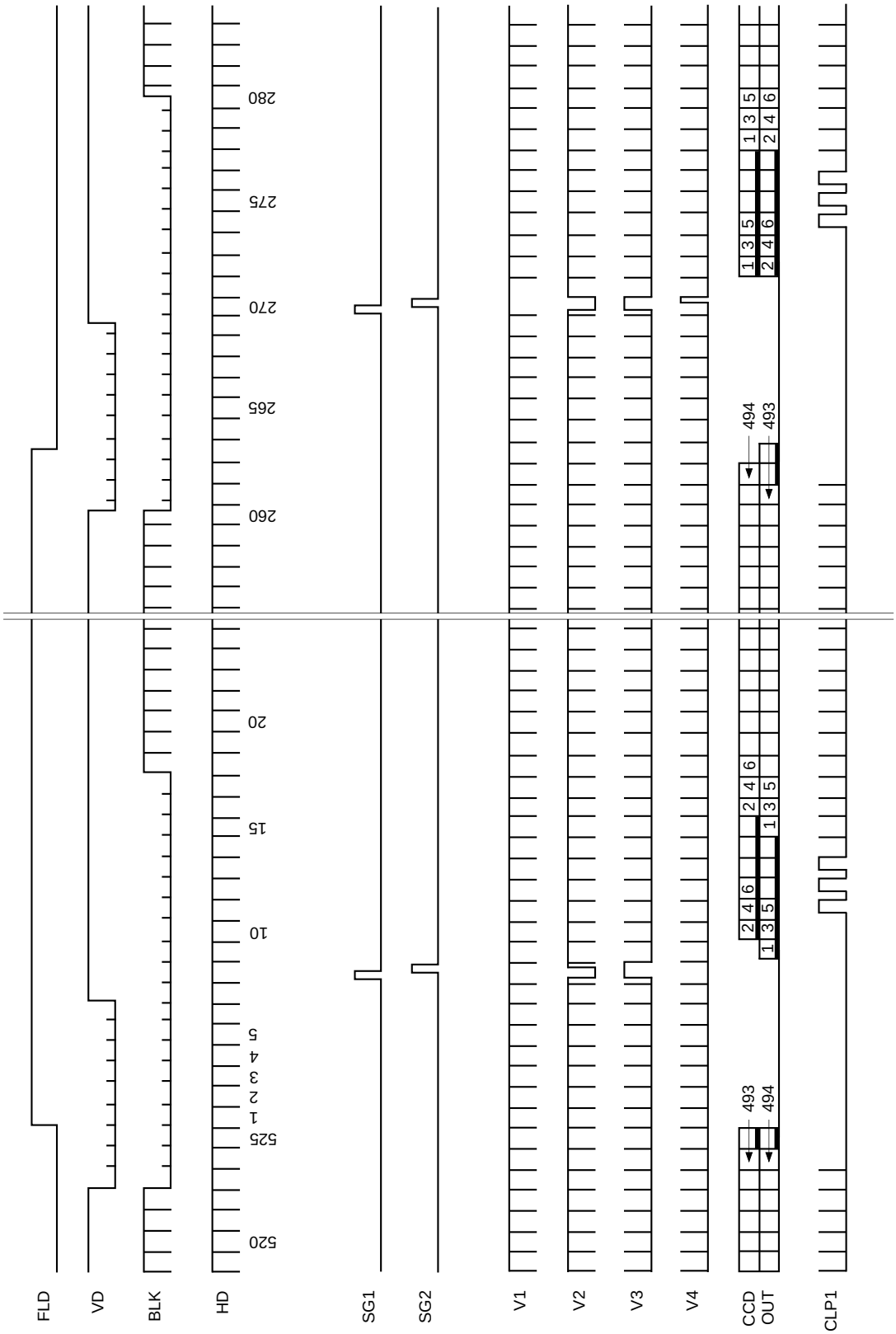
(Includes lens characteristics, excludes light source characteristics)



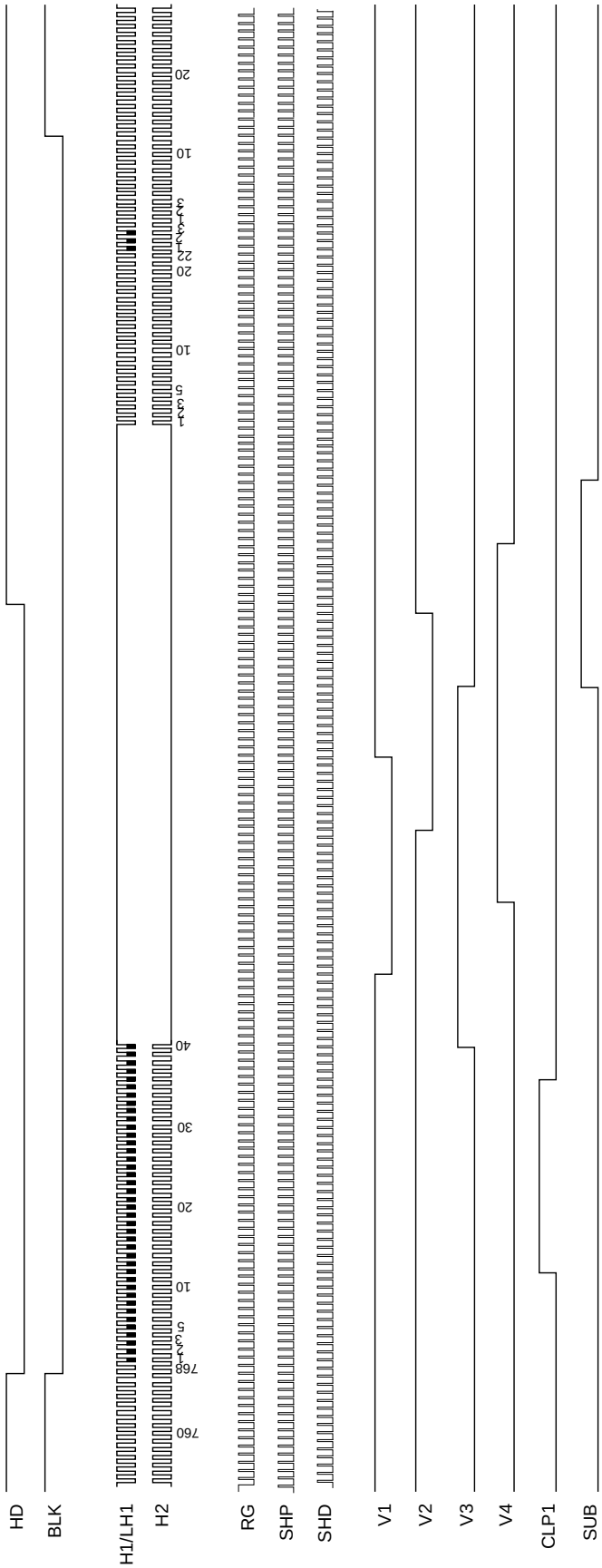

**Sensor Readout Clock Timing Chart**



## Drive Timing Chart (Vertical Sync)



**Drive Timing Chart (Horizontal Sync)**



**Notes on Handling**

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material.
   Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

a) Operate in clean environments (around class 1000 is appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

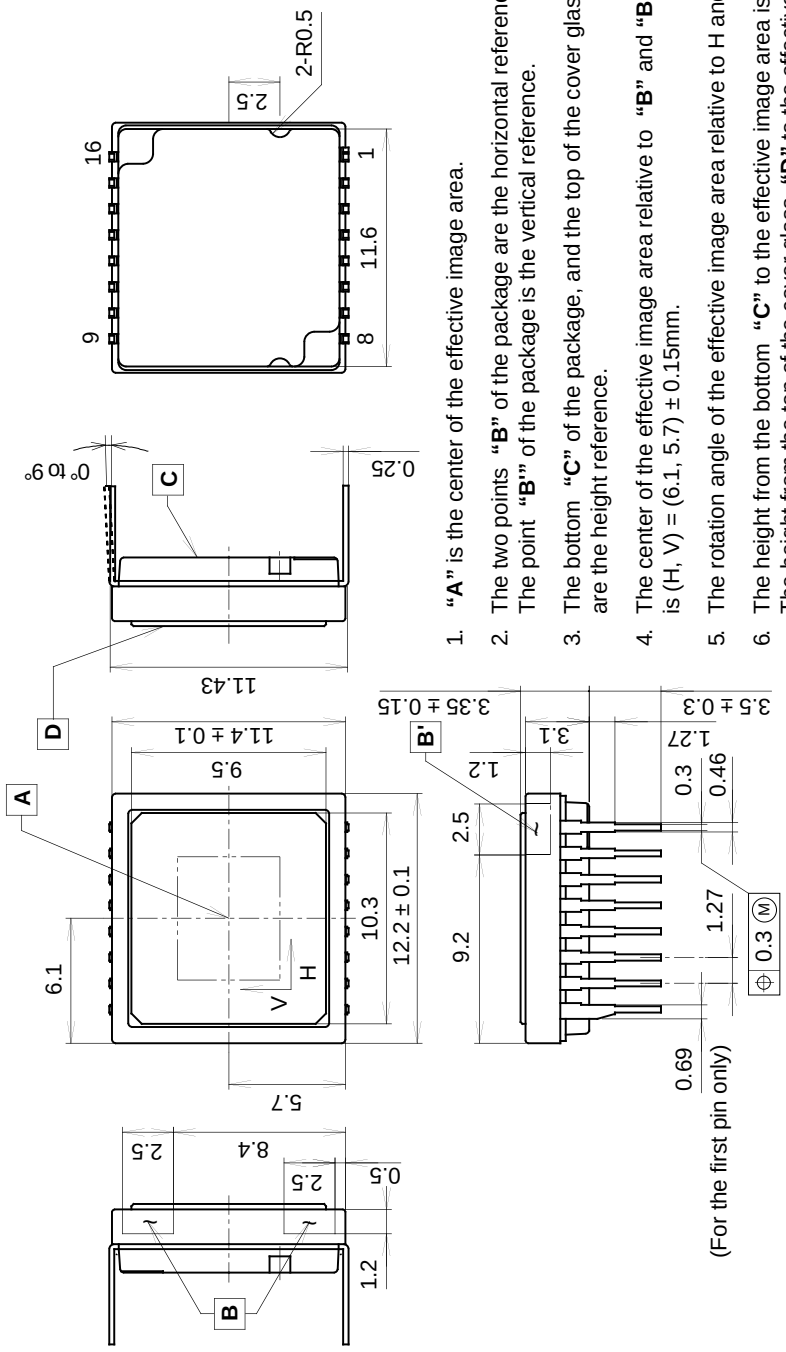
4) Do not expose to strong light (sun rays) for long periods.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

**Package Outline** Unit: mm

16pin DIP (450mil)




1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference. The point **"B"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (6.1, 5.7) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm. The height from the top of the cover glass **"D"** to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 50µm. The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | Plastic |
| LEAD TREATMENT | GOLD PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE WEIGHT | 0.9g |