Ordering number : ENA0250

SANYO Semiconductors
DATA SHEET

LA75693M

Monolithic Linear IC
For use in TV/VTR Applications
IF Signal Processing (VIF+SIF)

Overview

The LA75693M is a PAL/NTSC multichannel audio VIF/SIF signal-processing IC that makes the minimum number of adjustments possible. The system is designed so that VCO adjustment makes AFT adjustment unnecessary, thus simplifying the adjustment steps in endproduct manufacturing. PLL detection is adopted in the FM detector, allowing the LA75693VA to support multichannel detection for the audio signal. In addition, it also incorporates a buzz canceller that suppresses Nyquist buzz for improved audio quality.

Functions

- VIF Block : VIF Amplifier, Buzz Canceller, PLL Detector, IF AGC, RF AGC, AFT, Equalizer Amplifier

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Circuit voltage	V_{13}, V_{17}		V_{CC}	V
Circuit current	I_6		-3	mA
	I_{10}		-10	mA
Allowable dissipation	Pd max	Ta≤50°C, Independent IC	420	mW
		Mounted on a substrate *	720	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

*When mounted on a 65×72×1.6mm^3, glass epoxy substrate

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Operating supply voltage	V_{CC} op		4.5 to 5.5	V

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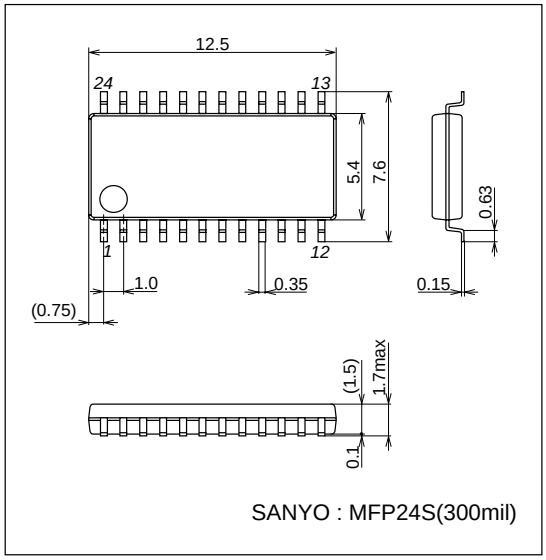
Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

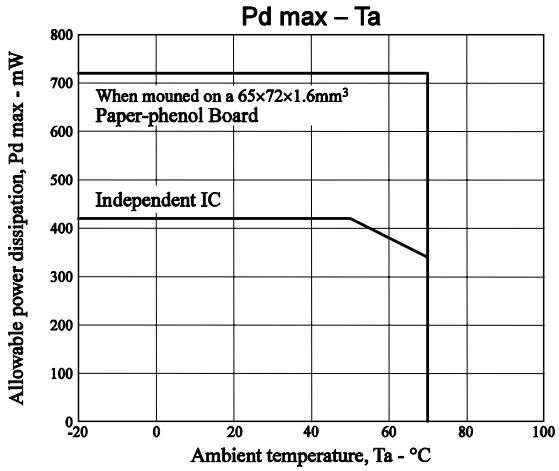
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[VIF block]						
Circuit current	I_5		32	40	48	mA
Maximum RF AGC voltage	$V_{14}H$		V_{CC}-0.5	V_{CC}		V
Minimum RF AGC voltage	$V_{14}L$			0	0.5	V
Input sensitivity	V_I	S1 = OFF	32	38	44	dBμV
AGC range	GR		58	63		dB
Maximum allowable input	V_I max		95	100		dBμV
No-signal video output voltage	V_6		2.3	2.6	2.9	V
Sync. signal tip voltage	V_6tip		0.75	1.0	1.25	V
Video output level	V_O		1.15	1.35	1.55	Vp-p
Black noise threshold voltage	V_{BTH}		0.4	0.7	1.0	V
Black noise clamp voltage	V_{BCL}		1.2	1.5	1.8	V
Video S/N	S/N		48	52		dB
C-S beat	IC-S		38	43		dB
Frequency characteristics	fc	6MHz	-3	-1.5		dB
Differential gain	DG			3.0	6.5	%
Differential phase	DP			3	5	deg
No-signal AFT voltage	V_{13}		2.0	2.5	3.0	V
Maximum AFT voltage	$V_{13}H$		4.0	4.4	5.0	V
Minimum AFT voltage	$V_{13}L$		0	0.18	1.0	V
AFT detection sensitivity	Sf		28	40	52	mV/kHz
VIF input resistance	Ri	45.75MHz		1.5		kΩ
VIF input capacitance	Ci	45.75MHz		3		pF
APC pull-in range (U)	fpu		1.3	2.0		MHz
APC pull-in range (L)	fpl			-2.0	-1.4	MHz
AFT tolerance frequency 1	ΔFa1		-150	0	+150	kHz
VCO1 maximum variable range (U)	dfu		1.5	2.0		MHz
VCO1 maximum variable range (L)	dfl			-2.0	-1.5	MHz
VCO control sensitivity	β		1.3	2.7	5.4	kHz/mV
4.5MHz Output Level	Vsout	SIF IN 80dBμV	87	94	101	dBμV

Package Dimensions

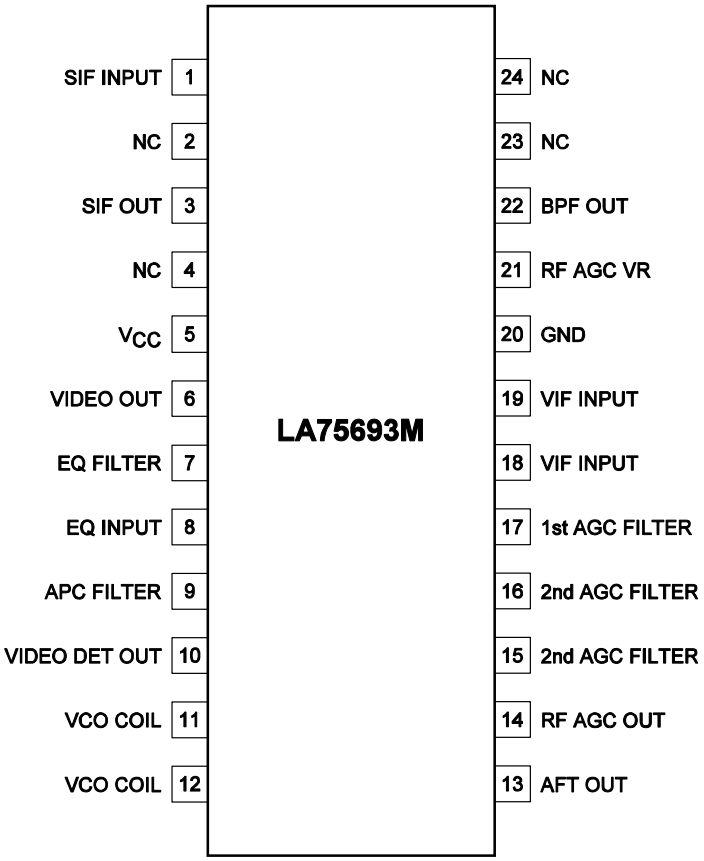
unit : mm

3112B





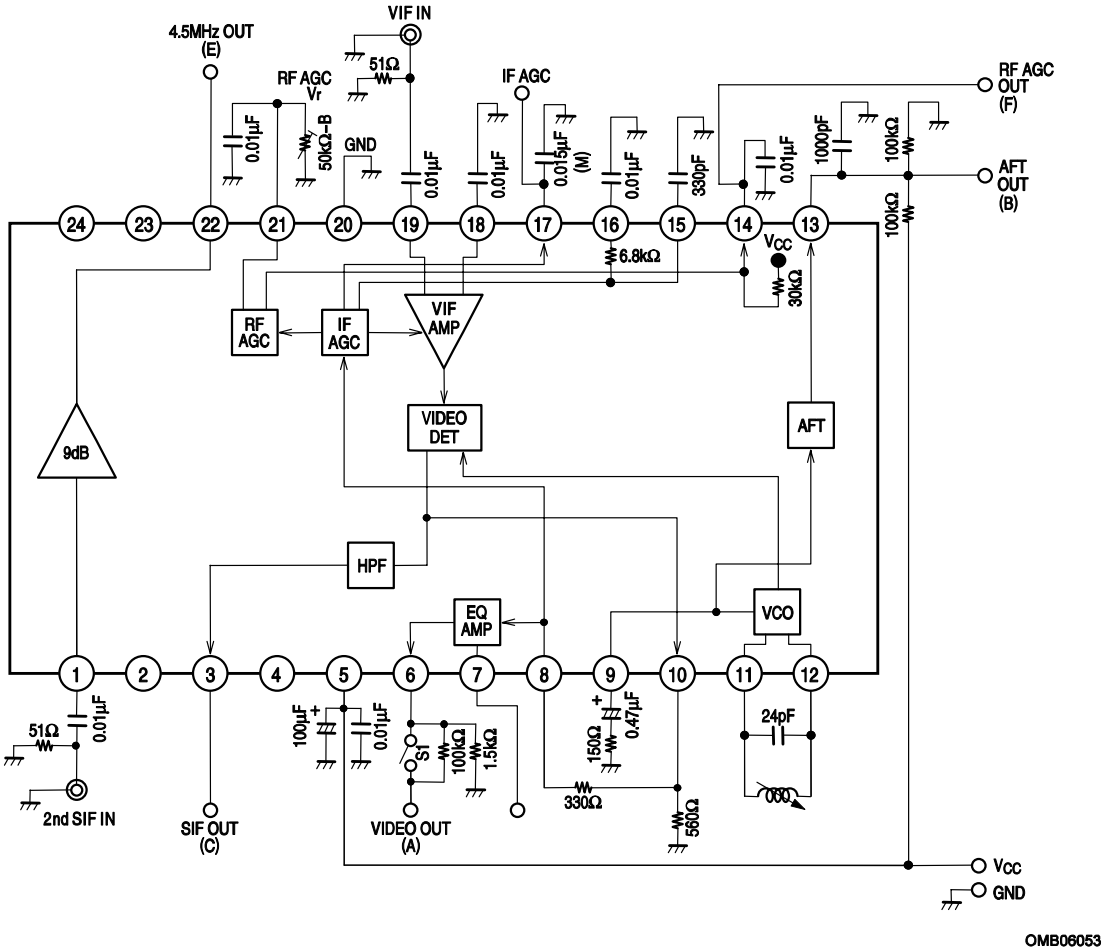
Pin Assignment



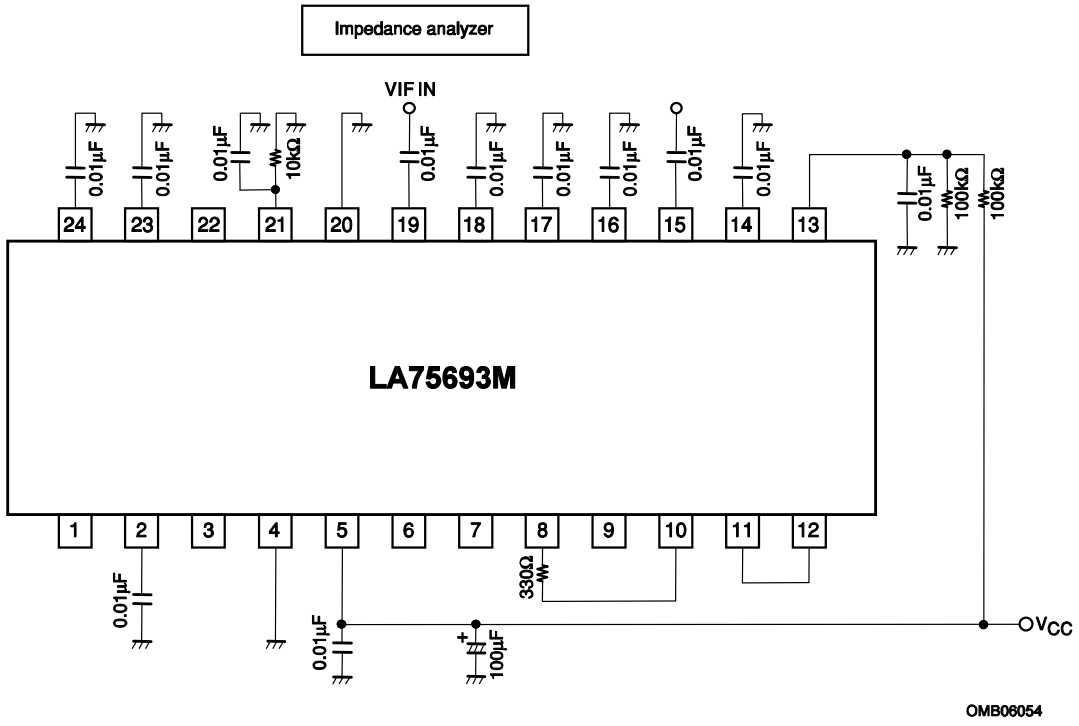
Top view

OMP06137

Block Diagram and AC Characteristics Test Circuit



Input Impedance Test Circuit



Test Conditions

V1. Circuit current [I_5]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) RF AGC Vr MAX
(4) Connect an ammeter to the V_{CC} and measure the incoming current.

V2. V3. Maximum RF AGC voltage, Minimum RF AGC voltage [$V_{14}H$, $V_{14}L$]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Adjust the RF AGC Vr (resistance max.) and measure the maximum RF AGC voltage. ⋯ F
(4) Adjust the RF AGC Vr (resistance min.) and measure the minimum RF AGC voltage. ⋯ F

V4. Input sensitivity [V_i]
(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) Turn off the S1 and put 100kΩ through.
(4) VIF input level at which the 15kHz detection output level at test point A becomes V_O - 3dB.

V5. AGC range [GR]
(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) In the same manner under the same conditions as for V4 (input sensitivity), measure the VIF input level at which the detection output level becomes V_O - 3dB. ⋯Vil
(3) GR = Vil - Vi

V6. Maximum allowable input [V_i max]
(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) VIF input level at which the detection output level at test point A becomes video output (V_O) ±1dB.

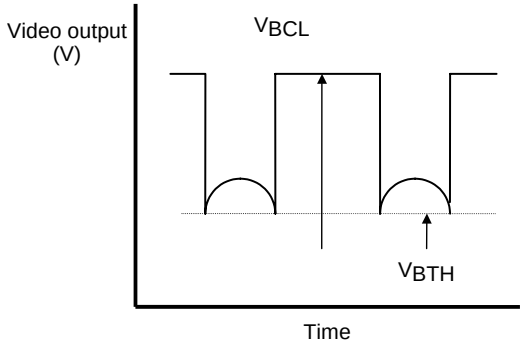
V7. No-signal video output voltage [V_6]
(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Measure the DC voltage at the VIDEO output (A).

V8. Sync. signal tip voltage [V_6tip]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Measure the DC voltage at the VIDEO output (A).

V9. Video output level [V_O]
(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM V_i = 10mVrms (VIF input)
(3) Measure the peak value of the detection output level at test point A. (Vp-p)

V10. V11 Black noise threshold level and clamp voltage [V_{BTH}, V_{BCL}]

(1) Apply DC voltage to the external AGC, IF AGC (pin 17) and vary it.
(2) fp = 45.75MHz 15kHz 78% AM10mVrms (VIF input)
(3) Adjust the IF AGC (pin 17) voltage to operate the noise canceller.
Measure the V_{BTH}, V_{BCL} at test point A.



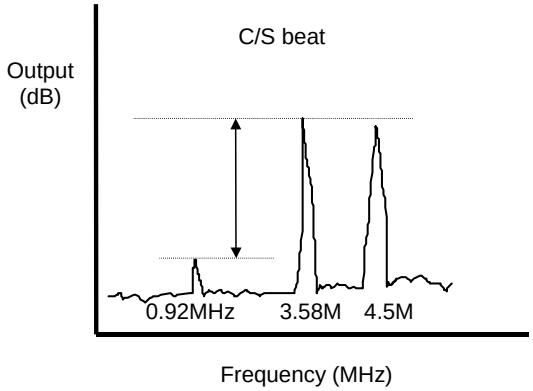
V12. Video S/N [S/N]

(1) Internal AGC
(2) fp = 45.75MHz CW = 10mVrms(VIF input)
(3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
……Noise voltage (N)

(4) $S/N = 20\log\frac{\text{Video position (Vp-p)}}{\text{Noise voltage (Vrms)}} = 20\log\frac{1.12\text{Vp-p}}{\text{Noise voltage}}$ (dB)

V13. C/S beat [IC-S]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and vary it.
(2) fp = 45.75MHz CW;10mVrms
fc = 42.17MHz CW;10mVrms - 10dB
fs = 41.25MHz CW;10mVrms - 10dB
(3) Adjust the IF AGC (pin 17) voltage so that the output level at test point A becomes 1.3Vp-p.
(4) Measure the difference between the levels for 3.58MHz and 0.92MHz components at test point A.



V14. Frequency characteristics [fc]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and vary it.
(2) SG1:45.75MHz continuous wave 10mVrms
SG2:45.65MHz to 39.75MHz continuous wave 2mVrms
Add the SG1 and SG2 signals using a T pat and adjust each SG signal level so that the above-mentioned levels are reached and input the added signals to the VIF IN.
(3) First set the SG2 frequency to 45.65MHz, and then adjust the IF AGC voltage (V_{17}) so that the output level at test point A becomes 0.5Vp-p. ……V1
(4) Set the SG2 frequency to 39.75MHz and measure the output level. ……V2
(5) Calculate as follows: $fc = 20\log\frac{V2}{V1}(dB)$

V15. V16. Differential gain, differential phase [DG, DP]

(1) Internal AGC
(2) fp = 45.75MHz APL50% 87.5% modulation video signal V_i = 10mVrms
(3) Measure the DG and DP at test point A

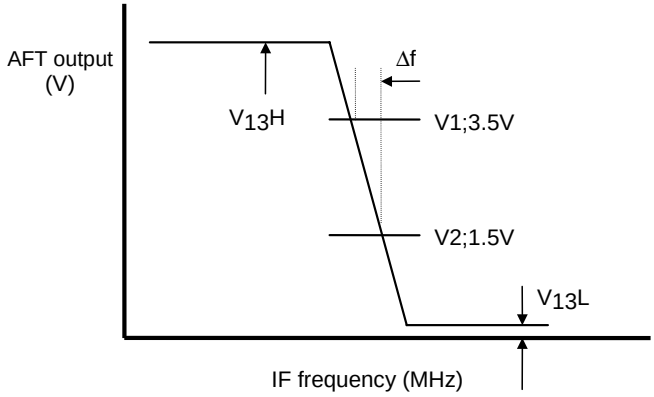
V17. No-signal AFT voltage [V_{13}]

(1) Internal AGC
(2) Measure the DC voltage at the AFT output (B).

V18.V19.V20 Maximum minimum AFT output voltage, AFT detection sensitivity [V_{13}H, V_{13}L, Sf]

(1) Internal AGC
(2) fp = 45.75MHz ±1.5MHz Sweep = 10mVrms (VIF input)
(3) Maximum voltage …… V_{13}H, minimum voltage …… V_{13}L
(4) Measure the frequency deviation at which the voltage at test point B changes from V1 to V2 …… Δf

$$Sf = \frac{2000(mV)}{\Delta f(kHz)} mV/kHz$$



V21.V22 VIF input resistance, Input capacitance [R_i, C_i]

(1) Referring to the input impedance Test Circuit, measure R_i and C_i with an impedance analyzer.

V23.V24 APC pull-in range [fpu, fpl]

(1) Internal AGC
(2) fp = 39MHz to 51MHz CW ; 10mVrms
(3) Adjust the SG signal frequency to be higher than fp = 45.75MHz to bring the PLL to unlocked state.
Note; The PLL is assumed to be in unlocked state when a beat signal appears at test point A.
(4) When the SG signal frequency is lowered, the PLL is brought to locked state again. ····· f1
(5) Lower the SG signal frequency to bring the PLL to unlocked state.
(6) When the SG signal frequency is raised, the PLL is brought to locked state again. ····· f2
(7) Calculate as follows:

fpu = f1 - 45.75MHz
fpl = f2 - 45.75MHz

V25. AFT tolerance frequency 1 [ΔFa1]

(1) Internal AGC
(2) SG1:43.75MHz to 47.75MHz variable CW 10mVrmns
(3) Adjust the SG1 signal frequency so that the AFT output DC voltage (test point B) becomes 2.5V; that SG1 signal frequency is f1.
(4) External AGC (Adjust the V_{17}.)
(5) Apply 9V to the IFAGC (pin 17) and then pick up the VCO oscillation frequency from the GND, etc.; that frequency is f2.
(6) Calculate as follows: AFT tolerance frequency ΔFa1 = f2 - f1 (kHz)

V26.V27 VCO Maximum variable range (U, L) [dfu, dfl]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) fl is taken as the frequency when 1V is applied to the APC pin (pin 9). In the same manner, fu is taken as the frequency when 5V is applied to the APC pin (pin 9).

dfu = fu - 45.75MHz
dfl = fl - 45.75MHz

V28. VCO control sensitivity [β]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) f1 is taken as the frequency when 2.8V is applied to the APC pin (pin 9). In the same manner, f2 is taken as the frequency when 3.0V is applied to the APC pin (pin 9).

$$\beta = \frac{f2 - f1}{400} \left(\mathrm{kHz}/\mathrm{mV}\right)$$

S1. 4.5MHz output level [Vsout]

(1) Internal AGC ($V_{17} = V_{CC}$)
(2) fs = 4.5MHz NO MOD V_i = 10mVrms
(3) Measure the output level at test point E. ·····Vsout

Note 1) Unless otherwise specified for VIF test, apply the V_{CC} voltage to the IF AGC and adjust the VCO coil so that oscillation occurs at 45.7MHz.
Note 2) Unless otherwise specified, leave the SW1 turned ON.