

CDS for CCD camera

Description

The CXA1439M is an IC for CDS (Correlated Double Sampling) to be used in a CCD camera.

Features

- Single power supply (4.8V)
- Low power consumption (57mW)
- Requires less external parts.
- High S/N ratio
- A smaller-size package requiring less mounting space
- Built-in two amplifiers.

Application

CCD camera

Structure

Bipolar silicon monolithic IC

8pin SOP (Plastic)



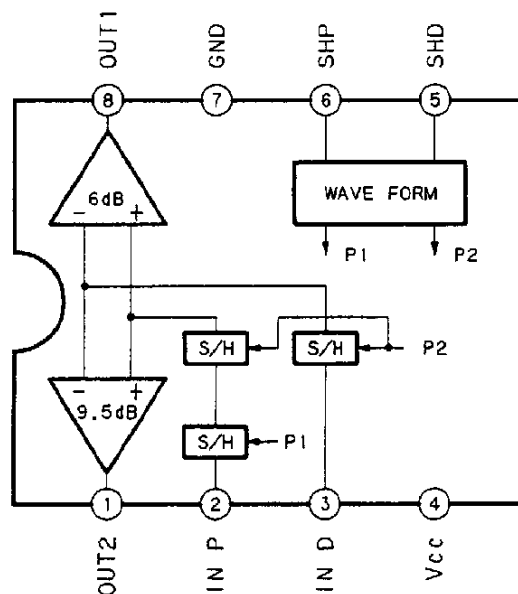
Absolute Maximum Ratings

• Supply voltage	V_{CC}	10	V
• Operating temperature	T_{opr}	-20 to +75	°C
• Storage temperature	T_{stg}	-60 to +150	°C
• Allowable power dissipation	P_D	300	mW

Operating Condition

Supply voltage	4.6 to 5.2	V
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Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Pin Voltage	Equivalent Circuit	Description
1	OUT2	Black level 1.6V		CDS signal output pin. 9.5dB amplifier output.
2	IN P	Black level 2.6V		Output signal from CCD to be input. To be input by capacitance coupling. Input at low impedance.
3	IN D	Black level 2.6V		Output signal from CCD to be input. Normally, coupled with Pin 2 when used. Input at low impedance.
4	V _{CC}	4.8V		V _{CC}
5	SHD	 H...2V or more L...1V or less		Sample and hold high speed pulse to be input. (Active: Hi) V _{TH} =1.5V
6	SHP	 H...2V or more L...1V or more		Sample and hold high speed pulse to be input. (Active: Hi) V _{TH} =1.5V
7	GND			GND
8	OUT1	Black level 1.6V		CDS signal output pin 6dB amplifier output.

Electrical Characteristics ($V_{CC}=4.8V$, $T_a=25^{\circ}C$)

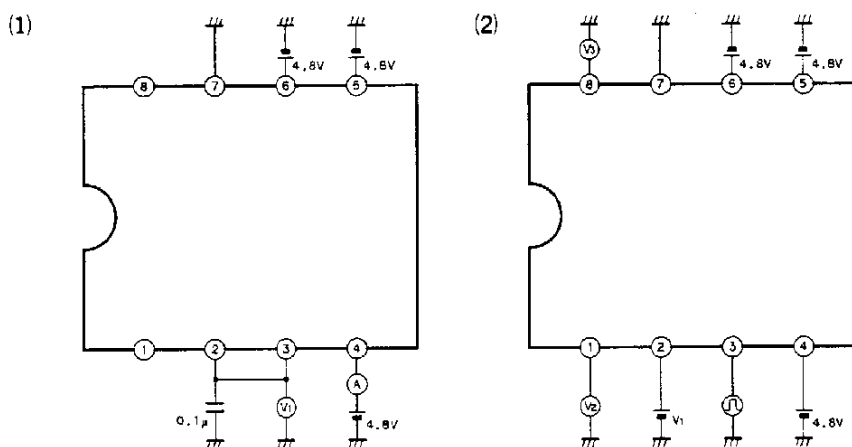
No.	Item	Symbol	Test Circuit	Condition	Min.	Typ.	Max.	Unit
1	Power consumption	P	(1)	V_{CC} value \times V_{CC} current value	40	57	80	mW
2	Gain (6dB)	G1	(2)	Input - OUT1 gain IN D input level=300mV	5	6	7	dB
3	Gain (9.5dB)	G2	(2)	Input - OUT2 gain IN D input level=300mV	8.5	9.5	10.5	dB
4	Output D range (6dB)	O DR1	(2)	OUT1 dynamic range IN D input level=1.5V	1.4	1.7		V
5	Output D range (9.5dB)	O DR2	(2)	OUT2 dynamic range IN D input level=1.5V	1.4	1.7		V
6	Amplifier CMRR (6dB)	CMRR1	—	6dB amplifier CMRR 10MHz		-40^{*1}		dB
7	Amplifier CMRR (9.5dB)	CMRR2	—	9.5dB amplifier CMRR 10MHz		-40^{*1}		dB
8	Amplifier frequency response	Fcut	—	3dB down point		100^{*1}		MHz
9	Sample and hold pulse width	T_w	—	Threshold level (1.5V)		17.5^{*2}		nS

Note) Both * 1 and * 2 are design reference values.

* 1 : Stand-alone characteristics of amplifier

* 2 : Sampling pulse width which enable the level to change over 800mV at 6dB amplifier output.

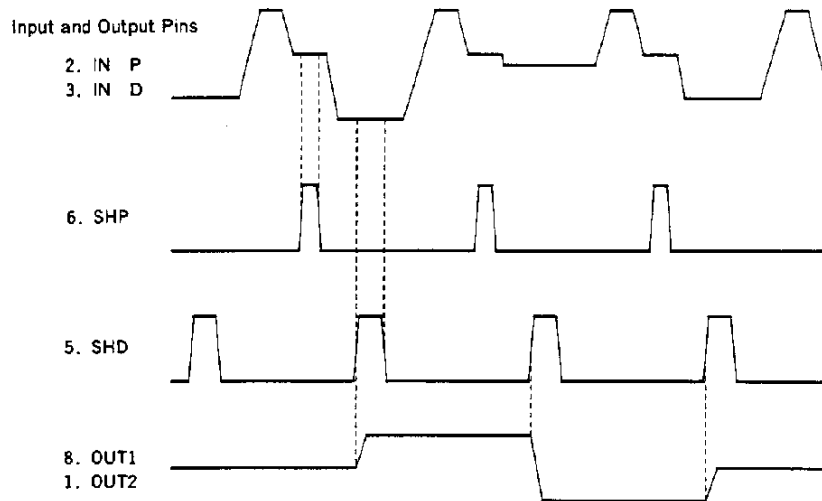
Electrical Characteristics Test Circuit



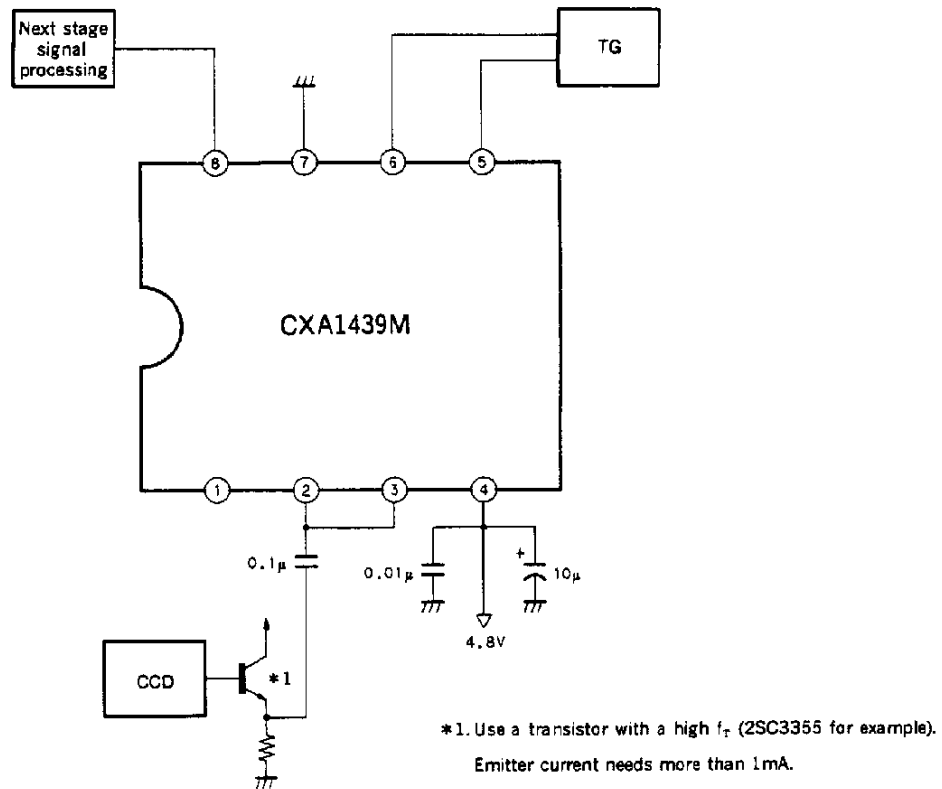
Note 1) The DC value of V1 is the measured value (V1) in (1).

Note 2) The input signal to IN D is V1.

Input and Output Waveform Diagram



Application Circuit (6dB amplifier only to be used)



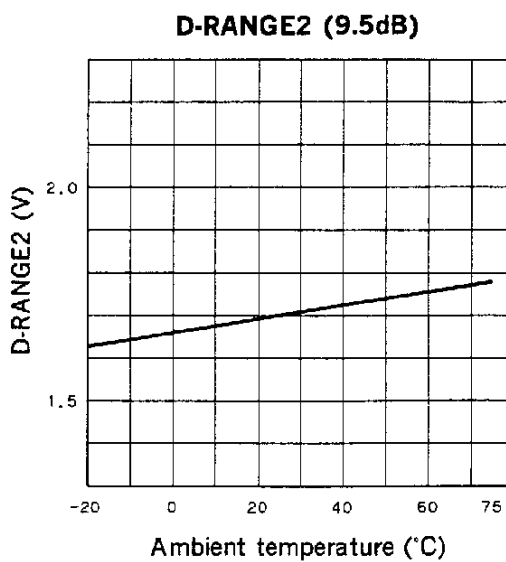
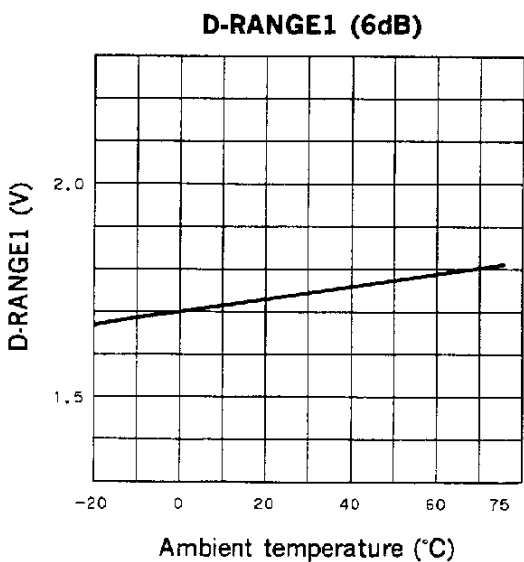
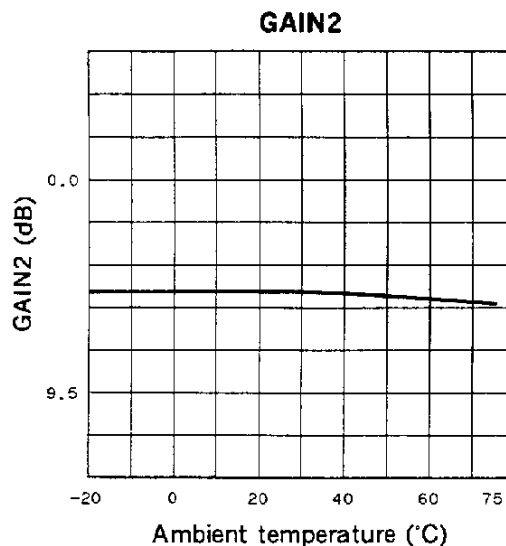
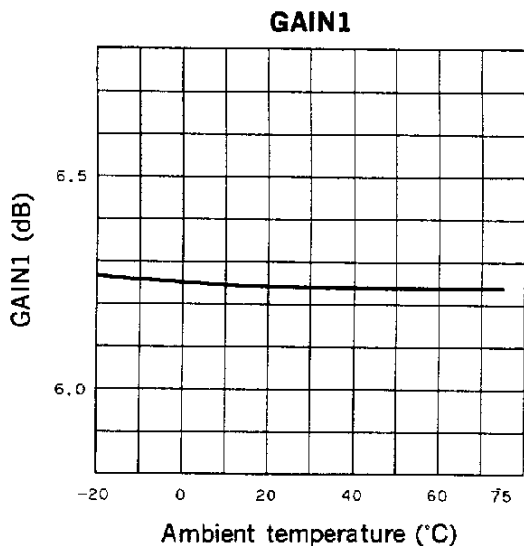
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

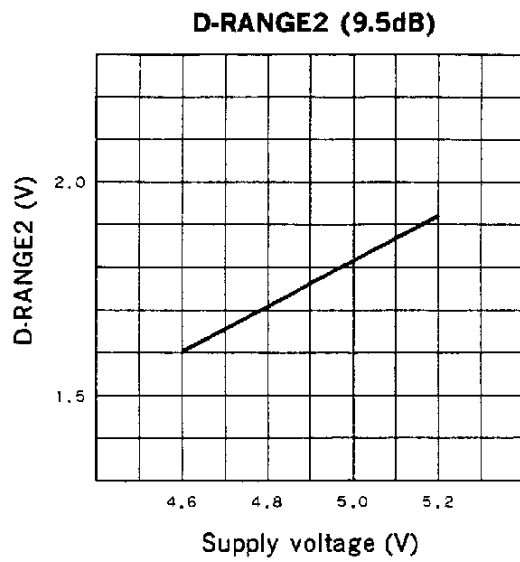
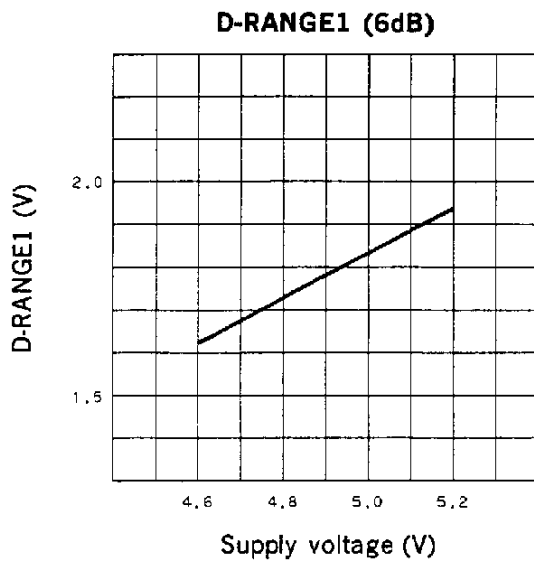
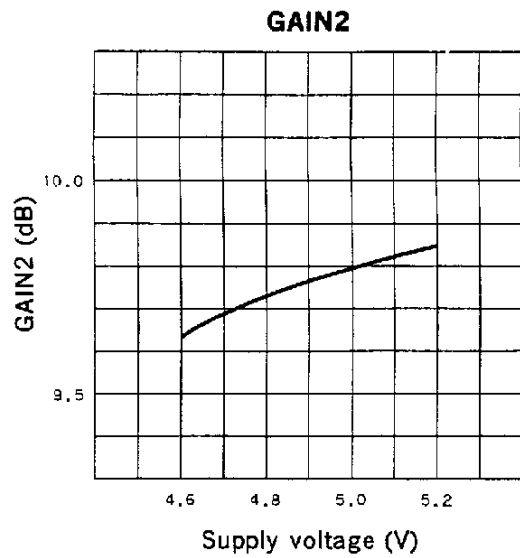
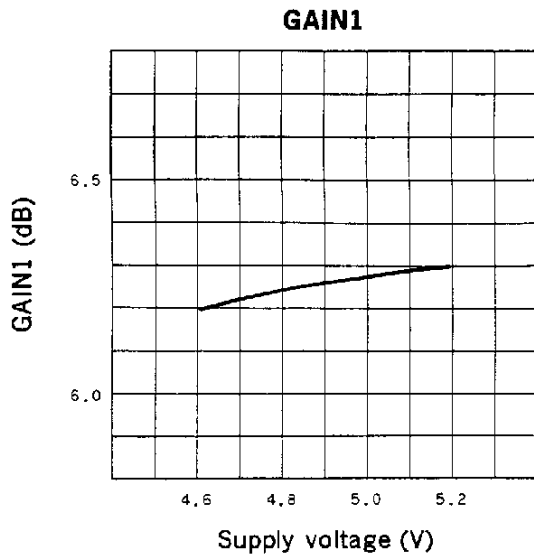
- (1) Make short the distance between CXA1439M and a timing IC (TG) in order to reduce the impedance of Vcc and GND.
- (2) Make impedance of input signal line (output signal from CCD) low and the length of that minimum.
- (3) Make short the sample and hold pulse line, not to have coupling between other elements.

Examples of Typical Characteristics

I. Temperature Characteristics ($V_{CC}=4.8V$)



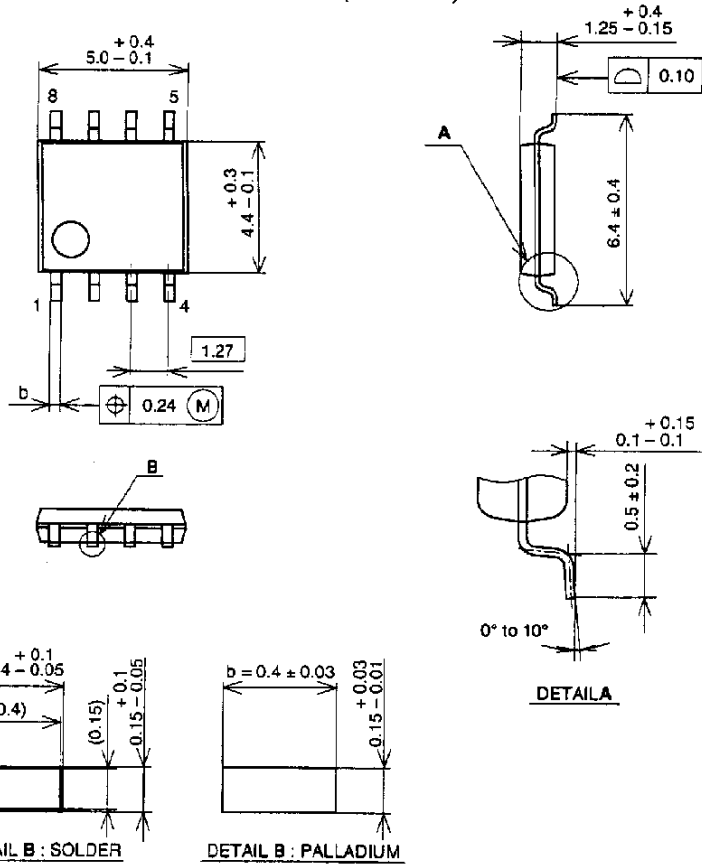
II. Supply Voltage Characteristics (Ta = 25°C)



Package Outline

Unit : mm

8PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-8P-L03
EIAJ CODE	SOP008-P-0225
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).