SONY

CXA1946AQ/AR

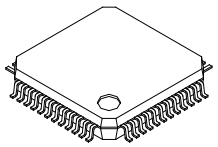
Electronic Volume

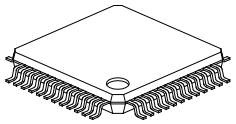
For the availability of this product, please contact the sales office.

Description

The CXA1946AQ/AR is a serial control electronic volume IC designed for use in audio systems.

48 pin QFP (Plastic) 48 pin LQFP (Plastic)





Features

- Loudness
- Volume control (0dB to –87dB in 1dB step, –∞dB)
- Balance
- Tone control (15 steps, 2 bands, –16dB to +16dB)
- Fader
  (2dB-step to –20dB, –25dB, –35dB, –45dB, –60dB, –∞dB)
- Input selector (4 channels)
- Gain can be set for each input channel (common for channels 3 and 4)
- Serial data control (DATA, CLK, CE)
- Single 8V power supply
- Zero-cross detection circuit (with timer)
- Power-off mute
- Volume control and tone control input/output pins are separate.

Absolute Maximum Ratings

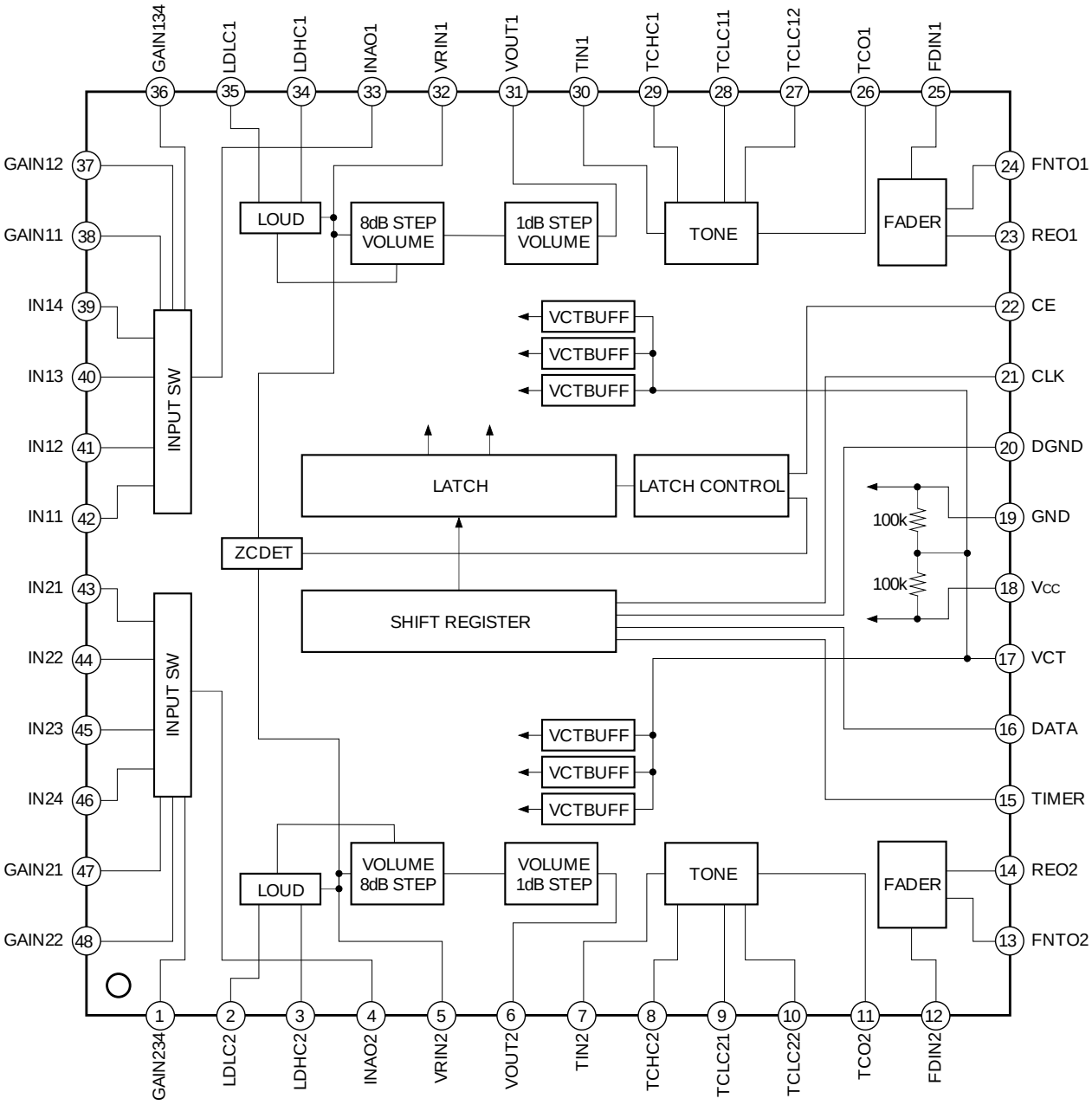
• Supply voltage	V_{CC}		13	V	
• Operating temperature	Topr		–40 to +85	℃	
• Storage temperature	Tstg		–65 to +150	℃	
• Allowable power dissipation	P_D	QFP	350	mW	(Ta = 85°C)
		LQFP	180	mW	(Ta = 85°C)

Operating Conditions

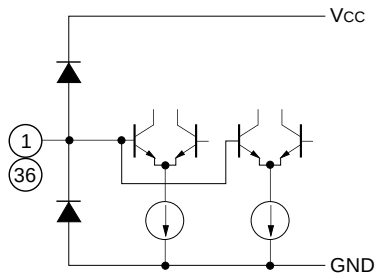
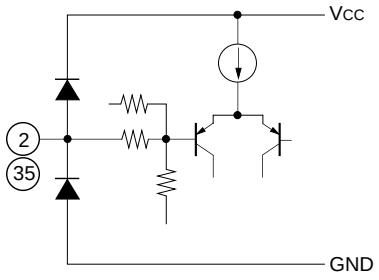
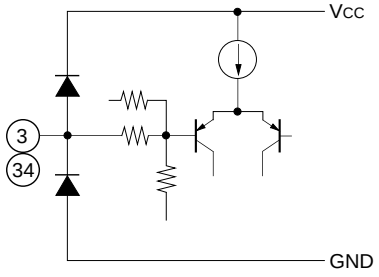
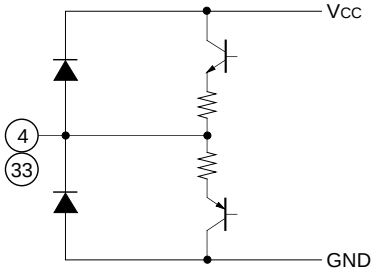
Supply voltage	V_{CC}	6 to 12	V

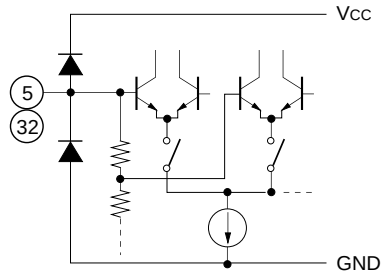
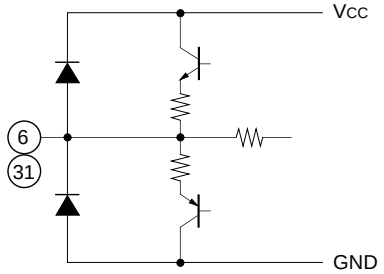
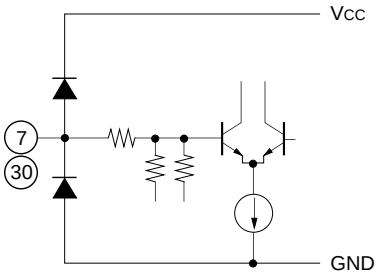
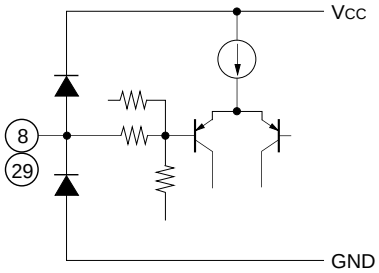
E95602D7Y

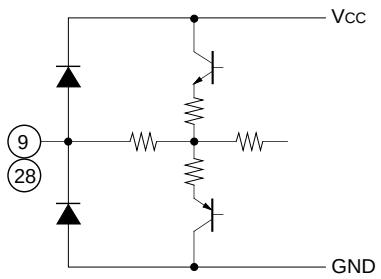
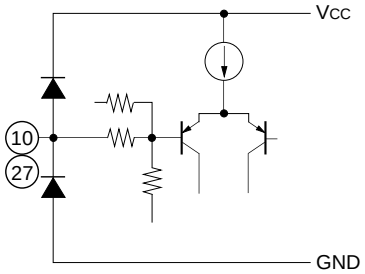
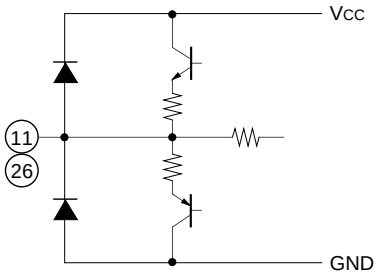
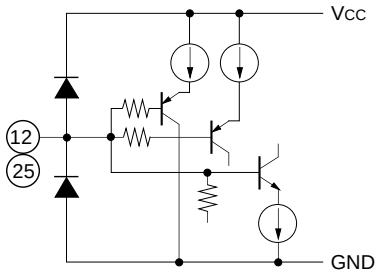
Block Diagram and Pin Configuration

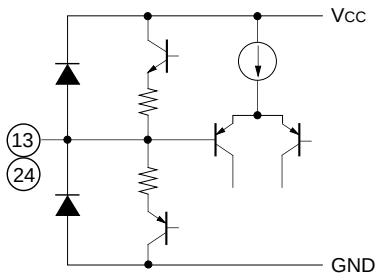
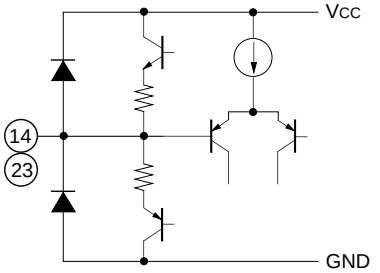
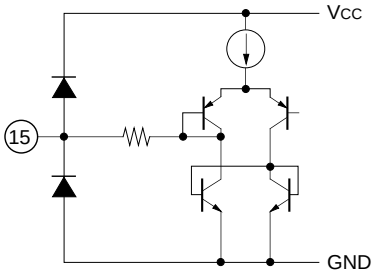
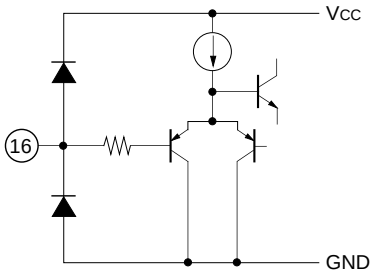


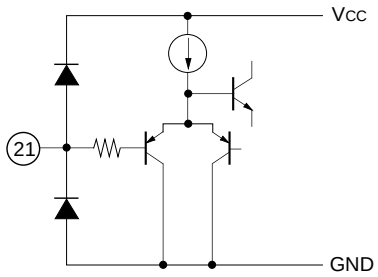
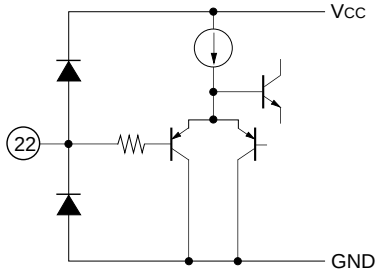
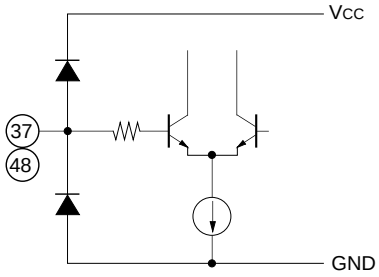
Pin Description

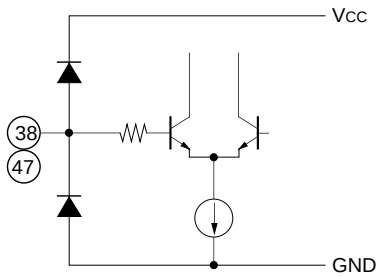
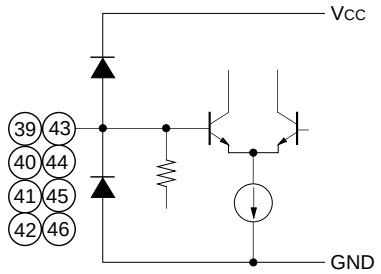
Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
1 36	GAIN234 GAIN134	≃∞ VCT		Sets gain for IN3 and IN4.
2 35	LDLC2 LDLC1	6.18kΩ VCT		Sets loudness low cut-off frequency.
3 34	LDHC2 LDHC1	8.92kΩ VCT		Sets loudness high cut-off frequency.
4 33	INAO2 INAO1	— VCT		Input selector output

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
5 32	VRIN2 VRIN1	9.5kΩ VCT		Volume input
6 31	VOUT2 VOUT1	— VCT		Volume output
7 30	TIN2 TIN1	19kΩ VCT		Tone input
8 29	TCHC2 TCHC1	5kΩ VCT		Sets tone high frequency.

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
9 28	TCLC21 TCLC11	8kΩ VCT		Sets tone low frequency.
10 27	TCLC22 TCLC12	8kΩ VCT		Sets tone low frequency.
11 26	TCO2 TCO1	— VCT		Tone control output
12 25	FDIN2 FDIN1	24kΩ VCT		Fader input

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
13 24	FNTO2 FNTO1	— VCT		Front output
14 23	REO2 REO1	— VCT		Rear output
15	TIMER	— —		Sets timer.
16	DATA	≃ ∞ —		Serial data input

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
17	VCT	— VCT		Center electric potential
18	Vcc	Vcc		+ power supply
19	GND	GND		GND
20	DGND	—		Digital GND
21	CLK	≃∞ —		Serial clock input
22	CE	≃∞ —		Latch enable input
37 48	GAIN12 GAIN22	≃∞ VCT		Sets gain for IN2.

Pin No.	Symbol	I/O resistance Pin voltage	Equivalent circuit	Description
38 47	GAIN11 GAIN21	≃ ∞		Sets gain for IN1.
39 40 41 42 43 44 45 46	IN14 IN13 IN12 IN11 IN21 IN22 IN23 IN24	50kΩ VCT		Signal input

Data Format

(a) Data allocation

FAST BIT	D1 D2	NOP	MSB
	D3 D4	ISW	
	D5	LOUD	
	D6 D7 D8 D9	VRC1	
	D10 D11 D12	VRF1	
	D13 D14 D15 D16	VRC2	
	D17 D18 D19	VRF2	
	D20 D21 D22 D23	TONE BASS	
	D24 D25 D26 D27	TONE TREBLE	
	D28 D29 D30 D31	FADER	
LAST BIT	D32	FADER SELECT	LSB

(b) Setting table

• NOP

Setting value	D1	D2
—	0	0

• ISW

Setting value	D3	D4
IN14/IN24	1	1
IN13/IN23	1	0
IN12/IN22	0	1
IN11/IN21	0	0

• LOUD

Setting value	D5
ON	1
OFF	0

• VRC1/VRC2

Setting value	D6/D13	D7/D14	D8/D15	D9/D16
0	1	1	1	1
–8	1	1	1	0
–16	1	1	0	1
–24	1	1	0	0
–32	1	0	1	1
–40	1	0	1	0
–48	1	0	0	1
–56	1	0	0	0
–64	0	1	1	1
–72	0	1	1	0
–80	0	1	0	1
–∞	0	1	0	0
–∞	0	0	0	0

• VRF1/VRF2

Setting value	D10/D17	D11/D18	D12/D19
0	1	1	1
–1	1	1	0
–2	1	0	1
–3	1	0	0
–4	0	1	1
–5	0	1	0
–6	0	0	1
–7	0	0	0

• **TONE BASS/TREBLE**

Setting value	D20/D24	D21/D25	D22/D26
14	1	1	1
12	1	1	0
10	1	0	1
8	1	0	0
6	0	1	1
4	0	1	0
2	0	0	1
0	0	0	0

• **BOOST/CUT**

Setting value	D23/D27
BOOST	1
CUT	0

• **FADER**

Setting value	D28	D29	D30	D31
–∞	1	1	1	1
–60	1	1	1	0
–45	1	1	0	1
–35	1	1	0	0
–25	1	0	1	1
–20	1	0	1	0
–18	1	0	0	1
–16	1	0	0	0
–14	0	1	1	1
–12	0	1	1	0
–10	0	1	0	1
–8	0	1	0	0
–6	0	0	1	1
–4	0	0	1	0
–2	0	0	0	1
0	0	0	0	0

• **FADER SELECT**

Setting value	D32
Attenuation of front signal	1
Attenuation of rear signal	0

• **RESET**

Reset is performed automatically when power is first supplied to the IC; there is no reset pin.

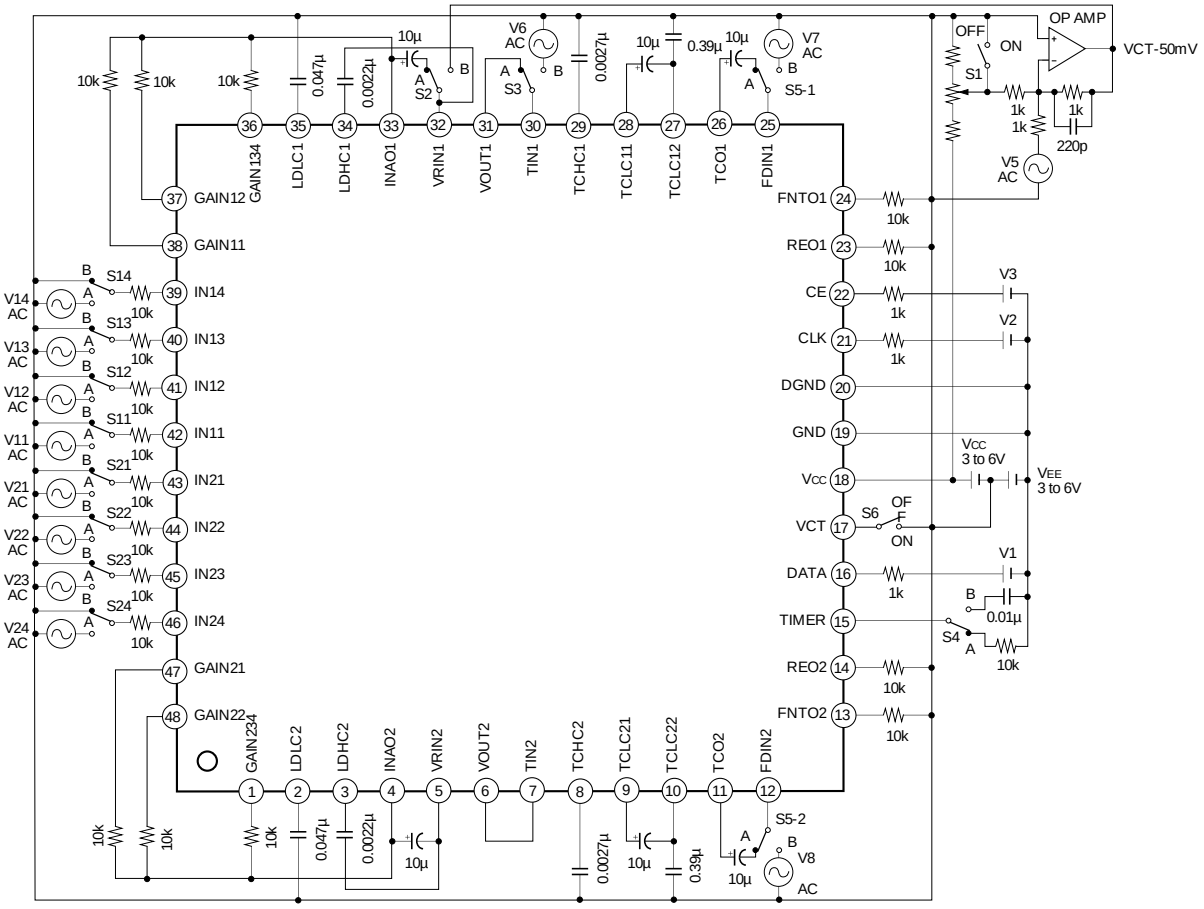
The following table shows the respective statuses of various settings after a reset has been performed. However, from the time when power is first supplied until the first data transfer, keep CE high by pulling it up to Vcc, etc.

MODE	Setting value
INPUT	1
VRC1	–∞
VRF1	–7dB
VRC2	–∞
VRF2	–7dB
LOUD	OFF
TONE BASS	0dB
TONE TREBLE	0dB
FADER	0dB, REAR

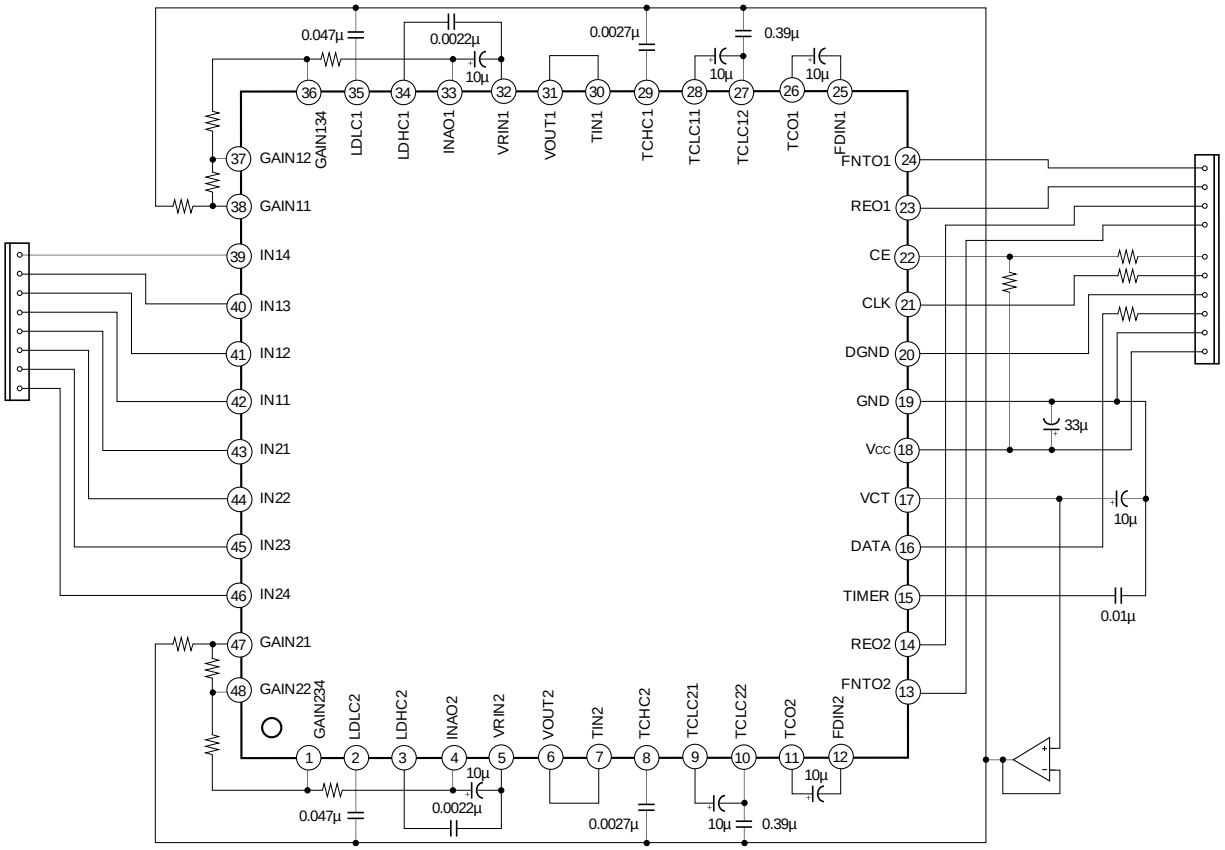
Electrical Characteristics (Unless otherwise specified, Vcc = 8V, Ta = 25°C)

Item		Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption		Icc	No signal	—	20	25	mA
Total harmonic distortion		THD	1kHz, 5dBm output	—	0.005	0.01	%
Output noise voltage		Vn	input shorted, A weight	—	7	10	µVrms
Maximum output voltage		Vom	1kHz	8	—	—	dBm
Separation		CS	1kHz	72	90	—	dB
Volume maximum attenuation		ATTm	1kHz	85	90	—	dB
Loudness	Low	Glb	100Hz, VRC = –16dB	7	8	9	dB
	High	Glh	10kHz, VRC = –16dB	5	6	7	dB
Bass max. boost gain		Gbb		14	16	18	dB
Bass max. cut gain		Gbc		14	16	18	dB
Treble max. boost gain		Gtb		14	16	18	dB
Treble max. cut gain		Gtc		14	16	18	dB
Input voltage	Low	Vsl	DATA, CLK, CE	0	—	1.5	V
	High	Vsh		3	—	6	V
Input voltage range		Vin	IN11 to 14, IN21 to 24, VRIN1, VRIN2, TIN1, TIN2, FDIN1, FDIN2	1	—	Vcc–1	V

Electrical Characteristics Measurement Circuit

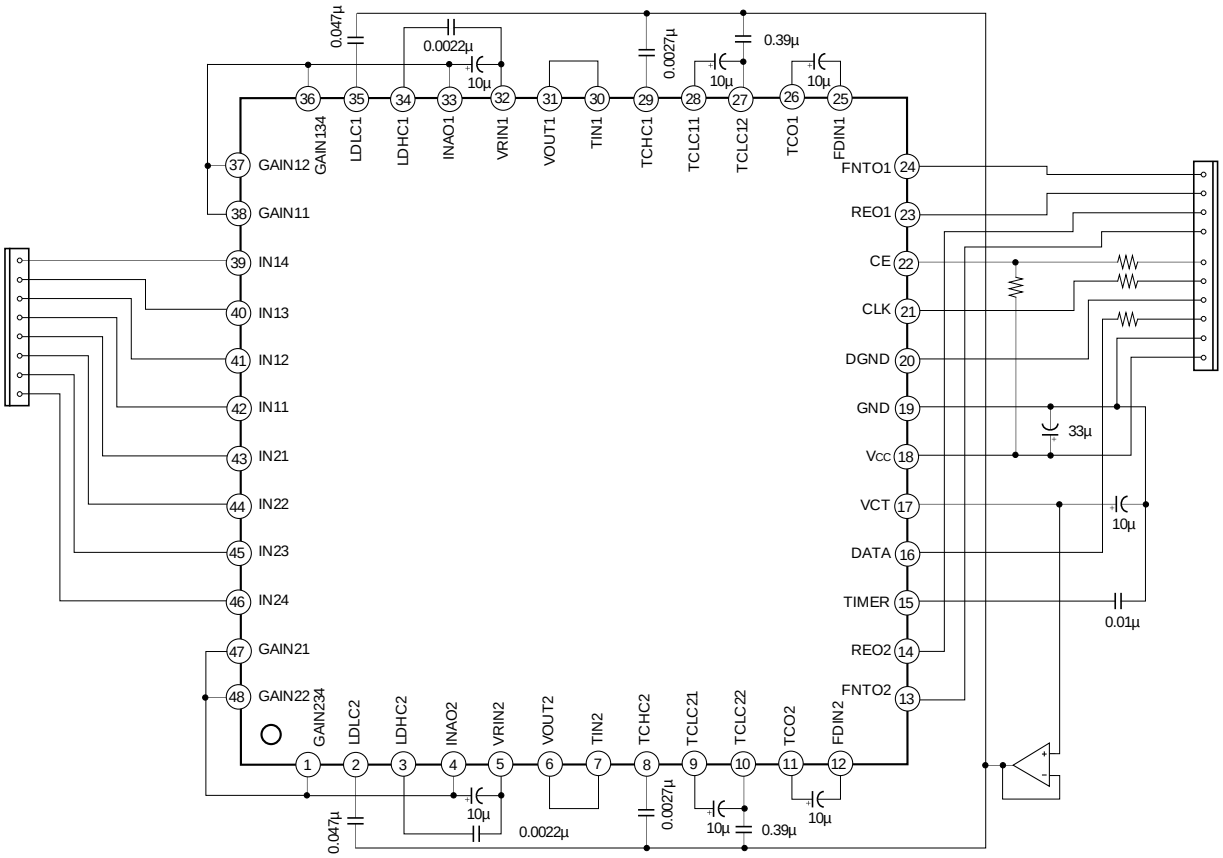


Application Circuit 1



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2



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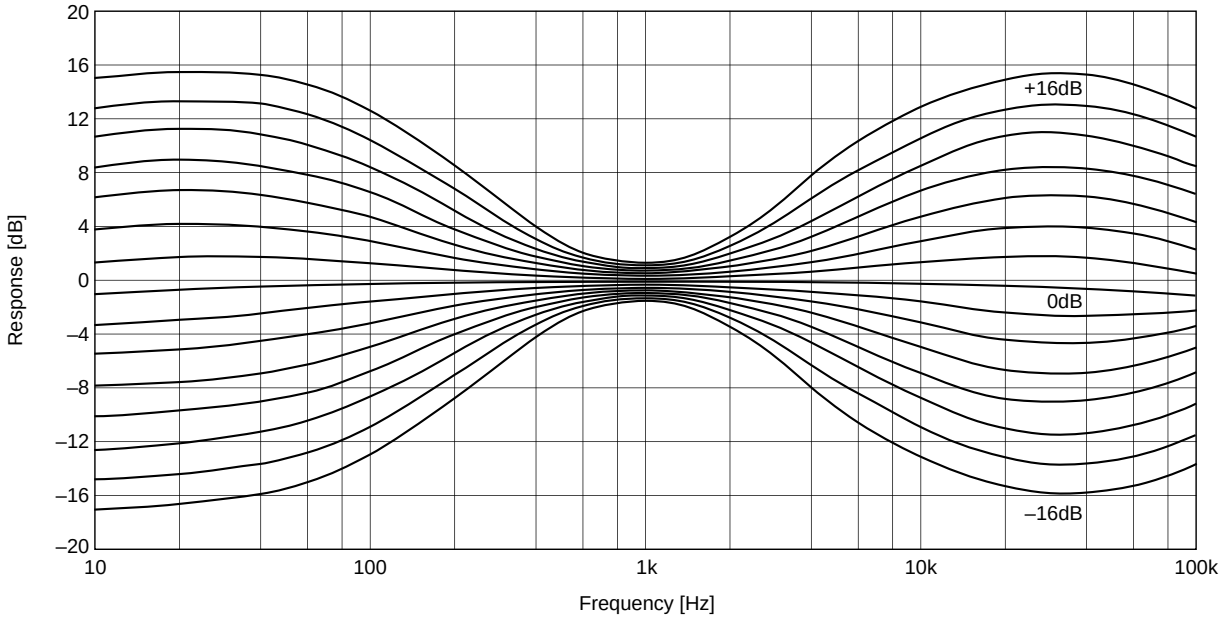
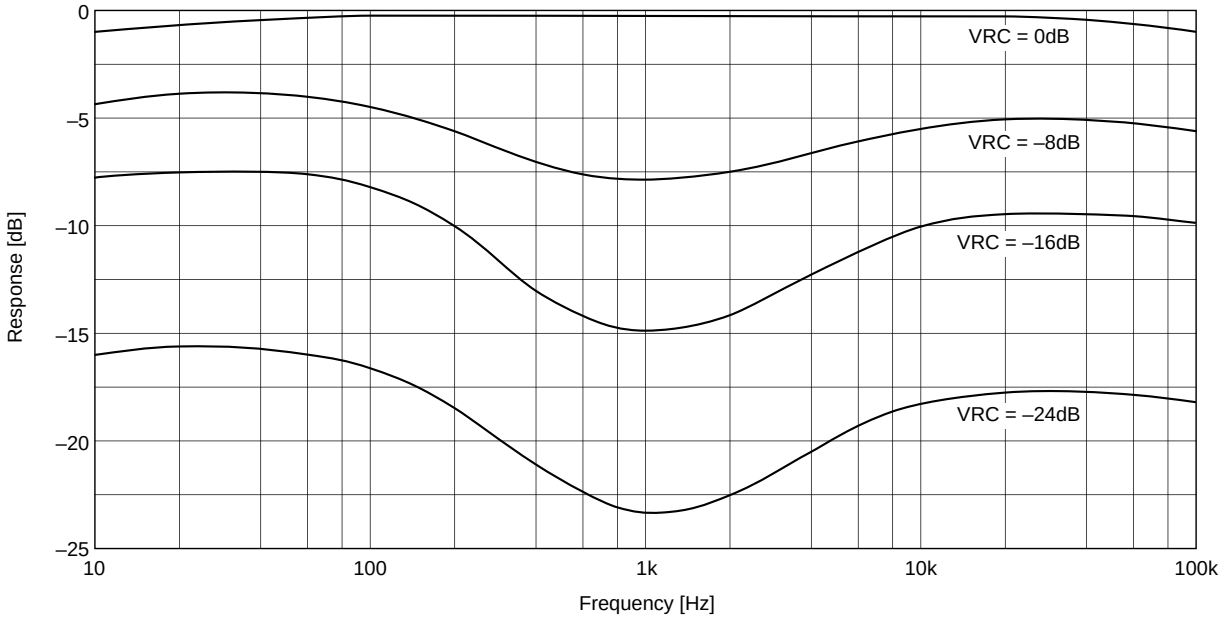
Tone control characteristics



Loudness characteristics



Description of Operation

The CXA1946AQ/AR is a serial control electronic volume IC designed for use in audio systems.
The internal circuit of the IC consists of the following blocks:

1. Input selector
2. Volume
3. Loudness
4. Tone control
5. Fader
6. VCT buffer
7. Serial data I/O
8. Zero-cross detector (with timer)
9. Power-off mute

The operation of each block and notes on their use are described below.
Note that when the circuits for channels 1 and 2 are identical, the suffix "X" is added to pin names and device names in order to distinguish between the two channels.

1. Input selector
   There are two channels (stereo), each with four systems of input pins; the input selector selects one of those input systems.
   The gain between the input pins and the output pin of the input selector can be set independently for each input system, except the gain for inputs 3 and 4 is common.
   Determine the gain for each system through the settings of the feedback circuit constants as shown in Figs. 1 and 2. When each input gain is set to × 1, short INAOX and GAIN × 1,GAIN × 2,GAIN × 34.
   The input impedance is 50kΩ (typ.) for each input.
   The output impedance for INAO1 and INAO2 is low impedance (roughly 0Ω). The gain is not affected by the load impedance.

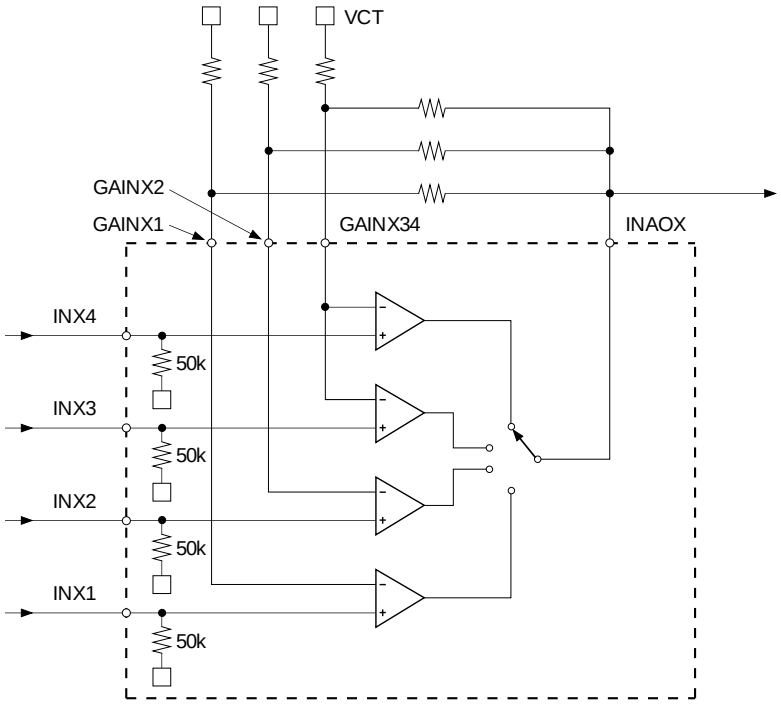


Fig. 1. Input Selector (1)

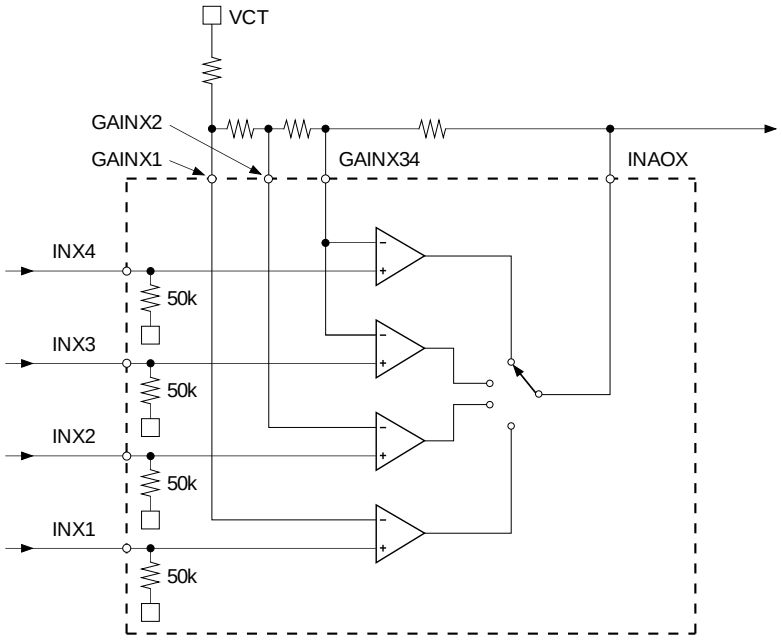


Fig. 2. Input Selector (2)

2. Volume

The volume circuit consists of two sections, an 8dB/step section and a 1dB/step section, as shown in Fig. 3. This circuit also serves as a balance control because the volume for channel 1 and channel 2 can be set independently.

To mute the output signal, send –∞dB data.

The input impedance is 9.5kΩ (typ.) for VRIN1 and VRIN2.

The output impedance for VOUT1 and VOUT2 is low impedance (roughly 0Ω). The volume step width and gain are not affected by the load impedance.

3. Loudness

The configuration of the loudness circuit is shown in Fig. 3. C_{LDHCX} and C_{LDLCX} are connected externally, and the loudness frequency characteristics are determined by these constants. The relationships between C_{LDHCX}/C_{LDLCX} and the frequency characteristics are as follows:

$1/f_L = 2\pi C_{LDLCX} R_1$

$1/f_H = 2\pi C_{LDHCX} R_2$

The loudness characteristics are not affected by the load impedance of VOUT1 and VOUT2.

Loudness is turned on and off by serial data bit D5.

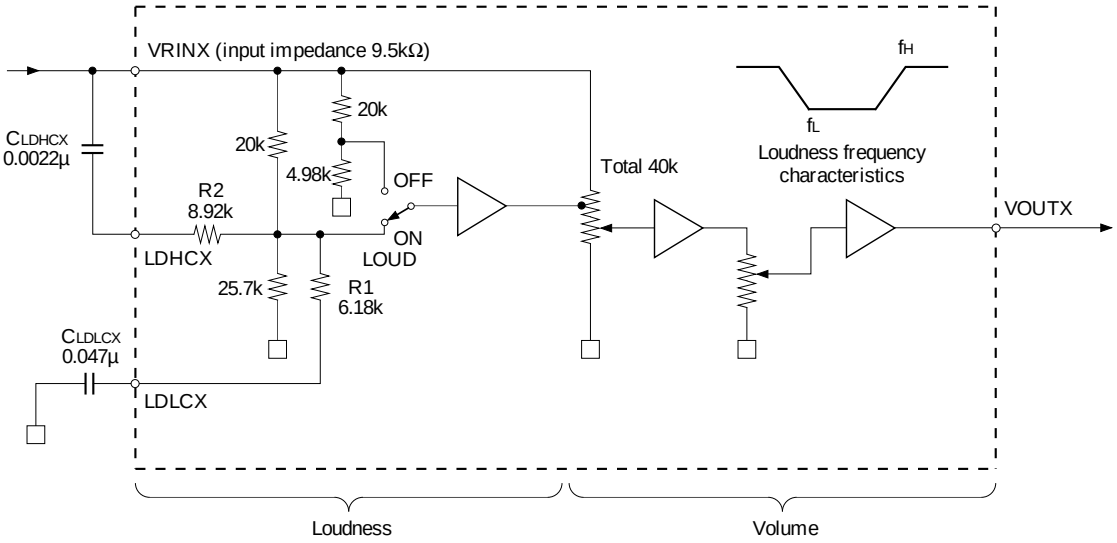


Fig. 3. Volume and Loudness

4. Tone control

The configuration of the tone control circuit is shown in Fig. 4. C_{TCLCX2} and C_{TCHCX} are connected externally, and the tone control frequency characteristics can be changed by changing these constants. The relationships between C_{TCLCX2}/C_{TCHCX} and the frequency characteristics are as follows:

$1/f_L = 2\pi C_{TCLCX2} (R_3//R_4)$

$1/f_H = 2\pi C_{TCHCX} R_5$

The maximum bass boost and cut can be made smaller than in the Application Circuit by connecting an external resistance to the TCLCX1 pin in series, or else connecting an external resistance to C_{TCLCX2} in parallel. (See Fig. 5.) Furthermore, the maximum treble boost and cut can be made smaller than in the Application Circuit by connecting an external resistance to C_{TCHCX} in series. (See Fig. 6.) However, when these methods are used, variations in the absolute value of the CXA1946A internal resistance (±20% max.) and in the external resistance will cause variations in the tone control characteristics. Set these constants after studying all considerations carefully. Note that when the method illustrated in the Application Circuit is used, variations in the internal resistance of the CXA1946A have no effect on the tone control characteristics.

The input impedance is 19kΩ (typ.) for TIN1 and TIN2.

The output impedance for TCO1 and TCO2 is low impedance (roughly 0Ω). The tone step width and gain are not affected by the load impedance.

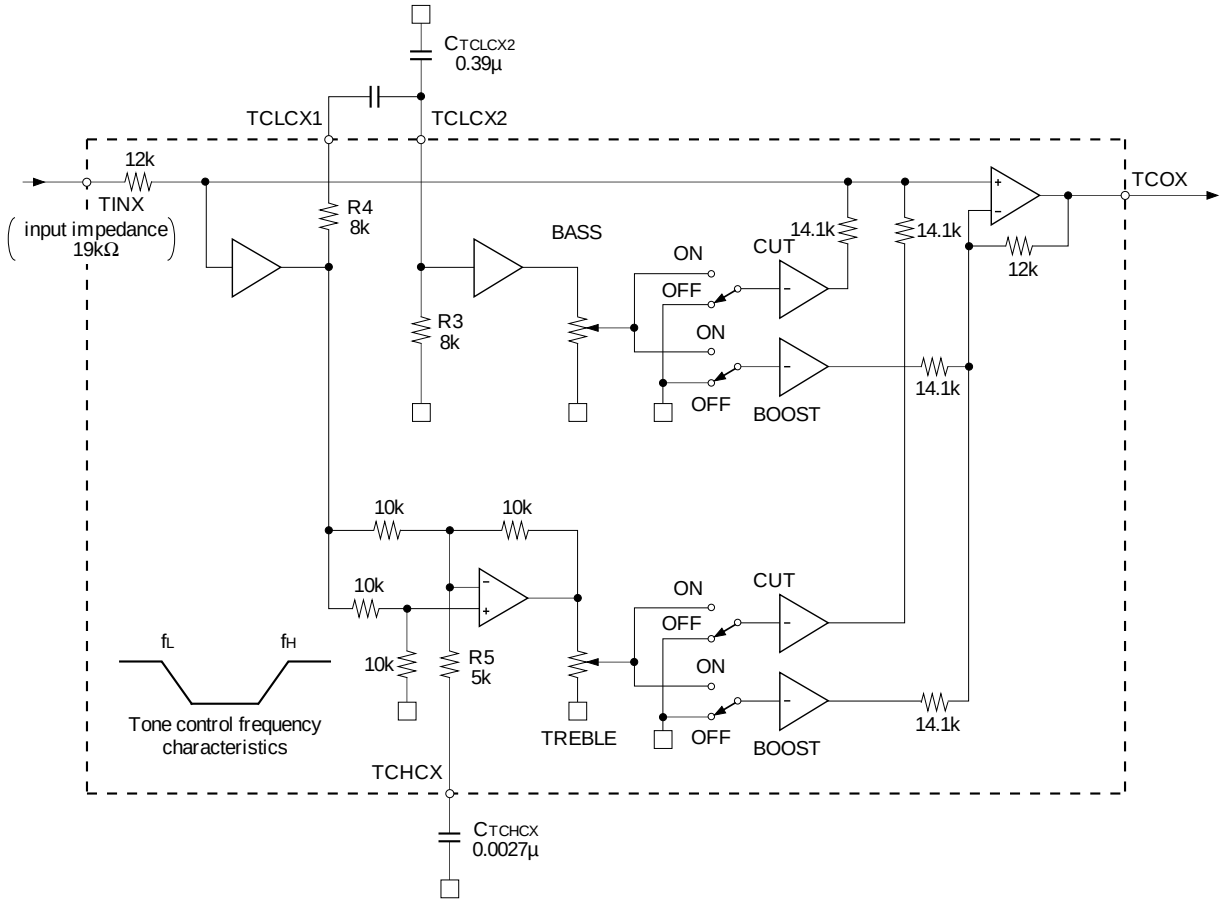


Fig. 4. Tone Control

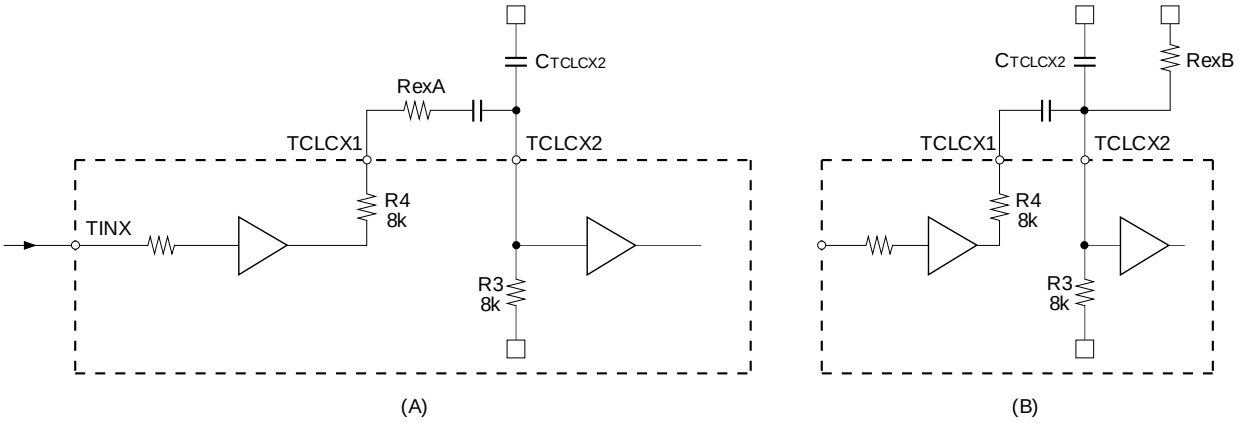


Fig. 5. Method for Reducing Bass Boost/Cut

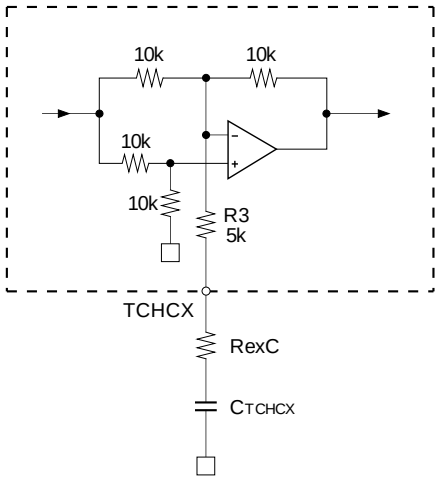


Fig. 6. Method for Reducing Treble Boost/Cut

5. Fader

The configuration of the fader circuit is shown in Fig. 7. The fader operates by specifying the amount of attenuation for either the front or rear output signal and by specifying which output signal (front or rear) is to be attenuated.

The input impedance is 24kΩ (typ.) for FDIN1 and FDIN2.

The output impedance for FNTO1, FNTO2, REO1, and REO2 is low impedance (roughly 0Ω). The gain and fader step width are not affected by the load impedance.

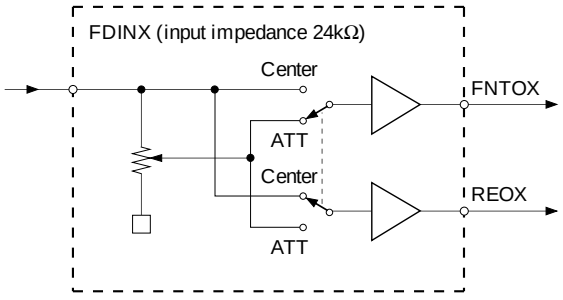


Fig. 7. Fader

6. VCT buffer

The internal circuit for the VCT pin is shown in Fig. 8.

This circuit generates the electric potential for the center between Vcc and GND (Vcc/2). The IC internal operation reference potential is equal to the output potential of VCT buffer. The impedance for the VCT pin (Pin 17) is high since it is connected to a bypass capacitor. Add an external buffer when using the electric potential of the VCT pin as the external reference potential for the CXA1946.

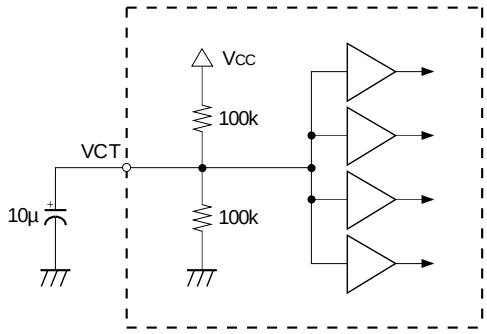


Fig. 8. VCT Buffer

7. Serial data I/O

The serial data has a 32-bit structure as indicated in the specifications. Data input is conducted using three inputs: DATA, CLK, and CE. DATA is shifted in the CXA1946A internal shift register at the rising edge of CLK. The data in the shift register is latched at the falling edge of CE. Refer to this specification for details on the timing.

The CXA1946A does not have a reset (initialize) pin. The internal shift register and latch are reset automatically when power is first supplied to the IC. To execute a reset at other times, send the data (statuses after reset) shown in the item "RESET" of this specification to the CXA1946A.

8. Zero-cross detector (with timer)

Using the zero-cross detector, the internal latch data is overwritten the first time the input signal becomes roughly 0 after serial data is sent (after CE goes low). This operation reduces noise when overwriting data. Although there are usually no problems when a normal audio signal is input, in rare cases there may be nothing except a large-amplitude input signal of the high band, causing the slew rate to become abnormally high; the zero-cross detection signal is not output in such a case because the zero-cross detector response speed is too slow. Another rare situation would be that the zero-cross detection signal is output very infrequently because the input signal frequency is extremely low. In these types of instances, it is conceivable that the internal latch data will not be overwritten after data is sent, or that it will take much time until the data is overwritten. Therefore, to an external observer it will appear that the data is not being overwritten regardless of the fact that data is being sent.

As a countermeasure, the IC is designed to permit the internal latch data to be forcibly overwritten if the zero-cross detection signal is not output within a certain waiting period after the data is sent (after CE goes low). This function is called the “timer.” If the zero-cross detection signal is output within a certain waiting period, the internal latch data is overwritten in synchronization with the zero-cross of the input signal.

The waiting period mentioned above can be changed according to the value of the external capacitor connected to the TIMER pin. When the value of the capacitor is 0.01µF, the waiting period is approximately 500µs.

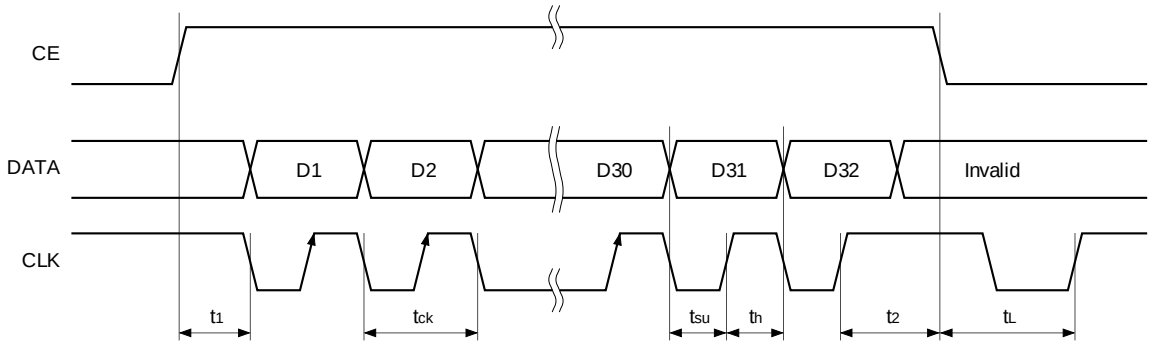
9. Power-off mute

When Vcc goes below 5V, the output stage bias of the fader output pins FNTO1, FNTO2, REO1, and REO2 is turned off and the pins go to high impedance. This operation prevents popping noises caused by the output pin potential deviating from Vcc/2 when the power is turned off.

Connections and Characteristics of Each Block

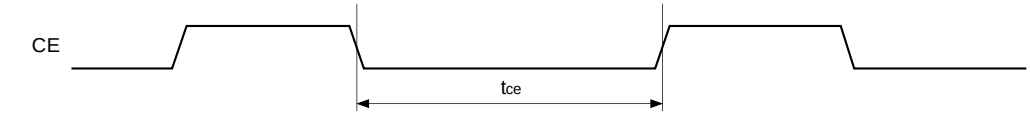
In the Application Circuit, the signal path goes from the input selector to the volume (+loudness) to the tone control to the fader. The sequence of the blocks in the signal path can be changed because the I/O pins for each block are independent of each other. For example, it is possible to switch the sequence of the volume circuit and the tone control so that the signal path goes from the input selector to the tone control to the volume (+loudness) to the fader. When this connection method is used, the noise voltage in the fader output can be reduced in actual use because the noise and signal up to the tone control are attenuated by the volume. However, because the maximum output amplitude of the tone control circuit is limited by the supply voltage, care should be given to the setting of the input signal level.
Although blocks in the Application Circuit are linked either by coupling capacitors or by direct connection, it is also possible to insert external circuits between blocks. In this case, the gain will change according to the input impedance of the following block and the impedance of the external circuit. In addition, the input impedance of each block can vary by ±20% due to the characteristics of the IC. Consequently, the overall gain also varies. Give careful consideration to the effects of this variation when setting the constants. The step widths (control characteristics) of the volume, tone control, and fader are not affected.

Timing Chart



$t_1 \geq 0.5\mu s$
$t_2 \geq 0.5\mu s$
$t_{ck} \geq 1.0\mu s$
$t_{su} \geq 0.5\mu s$
$t_h \geq 0.5\mu s$

$t_L \geq t_T + 0.5\mu s$
(t_T is the maximum value for the timer operation time)



$t_{ce} \geq 4.0\mu s$

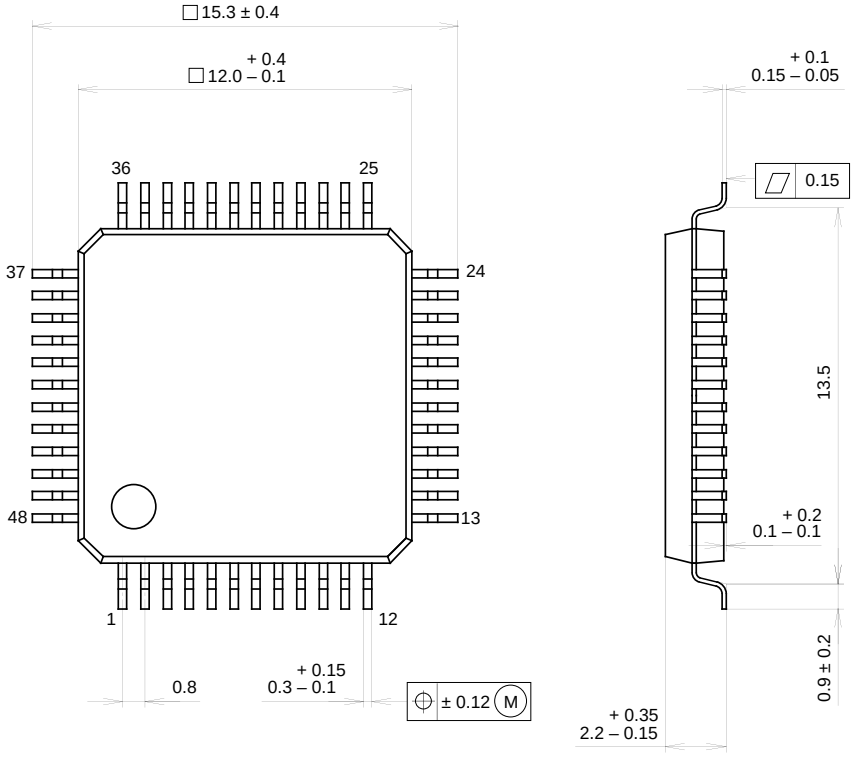
Timer Waiting Period Setting Chart (Vcc = 6 to 12V, operating temperature = –35°C to 85°C)

TIMER pin capacitance C	Waiting peroid		
	Min.	Typ.	Max.
C = 100pF	3µs	5µs	9µs
C = 0.001µF	30µs	50µs	90µs
C = 0.01µF	300µs	500µs	900µs
C = 0.1µF	3ms	5ms	9ms
C = 1µF	30ms	50ms	90ms
C = 10µF	300ms	500ms	900ms

Package Outline Unit: mm

CXA1946AQ

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	————

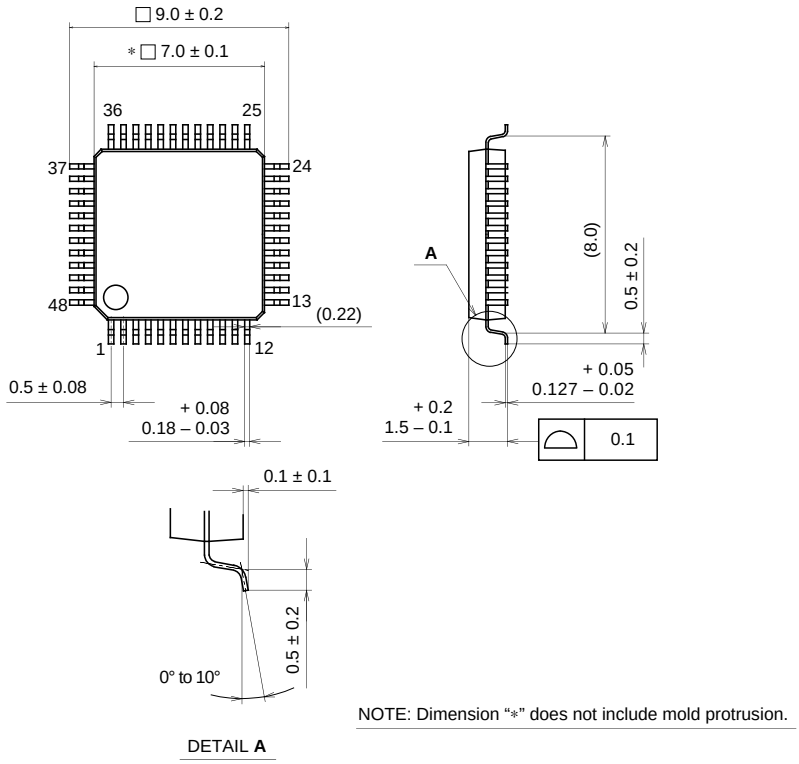
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

CXA1946AR

48PIN LQFP (PLASTIC)



DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	∗QFP048-P-0707-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g