SONY

CXA1999N

IF Amplifier for M-ary FSK Pagers

Description

The CXA1999N is a low current consumption FM IF amplifier which employs the newest bipolar process. It is suitable for M-ary FSK pagers.

Features

- Low current consumption: 1.16 mA (typ. at V_{CC} = 1.4 V)
- Low voltage operation: V_{CC} = 1.1 to 4.0 V
- Small package 20-pin SSOP
- Second mixer and oscillator
- Needless of IF decoupling capacitor
- Reference power supply for operational amplifier and comparator
- IF input, V_{CC} standard

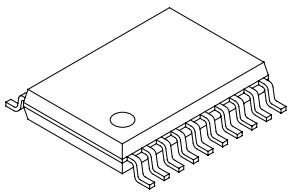
Applications

- M-ary FSK pagers
- Double conversion pagers

Structure

- Bipolar silicon monolithic IC

20 pin SSOP (Plastic)



Absolute Maximum Ratings

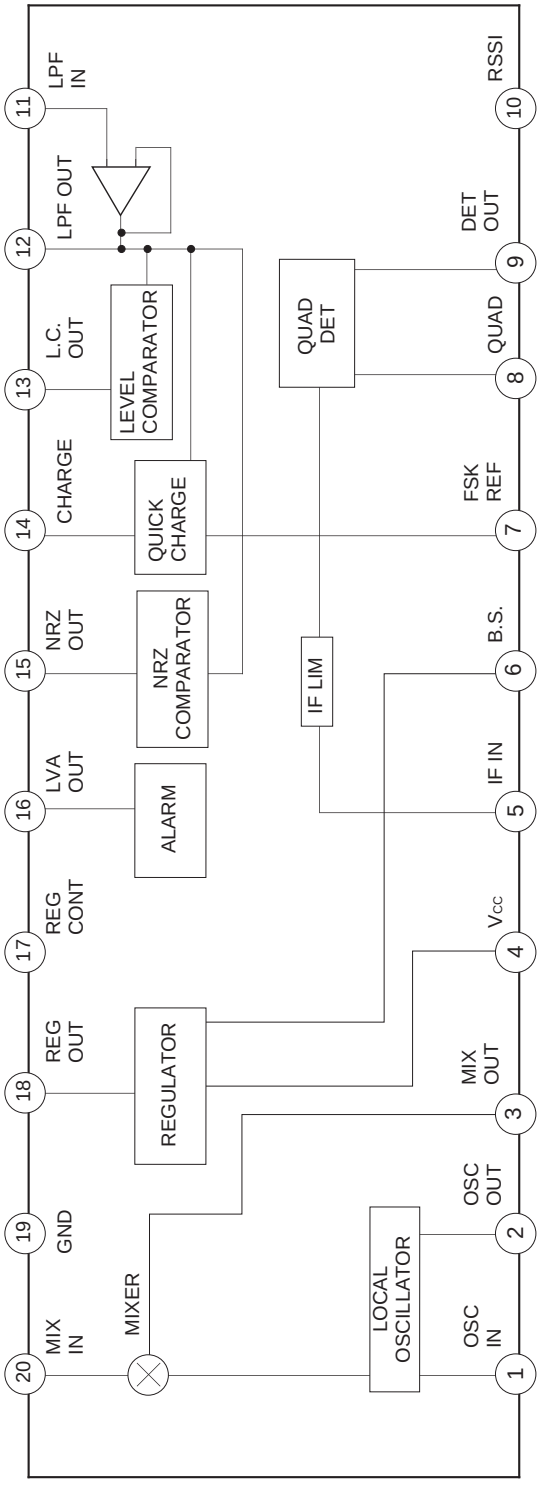
• Supply voltage	V_{CC}	7.0	V
• Operating temperature	Topr	–20 to +75	℃
• Storage temperature	Tstg	–65 to +150	℃
• Allowable power dissipation	P_D	375	mW

Operating Condition

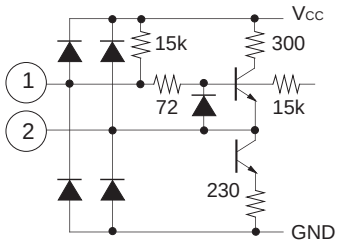
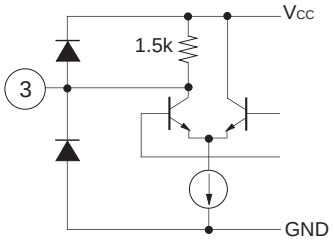
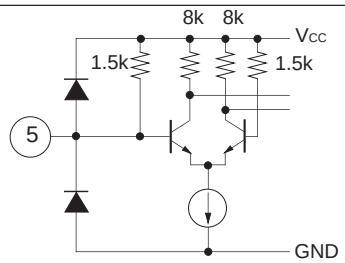
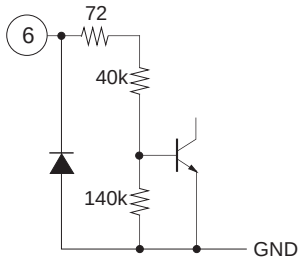
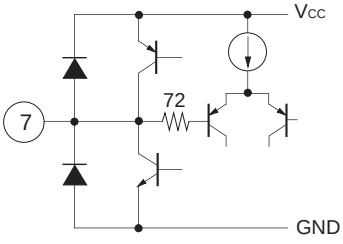
Supply voltage	$V_{CC}1$	1.1 to 4.0	V

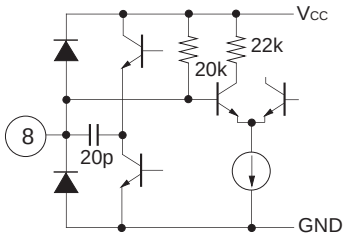
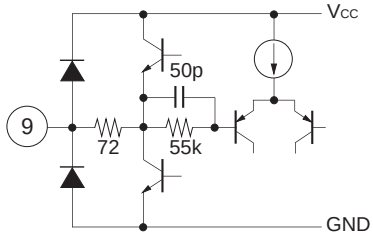
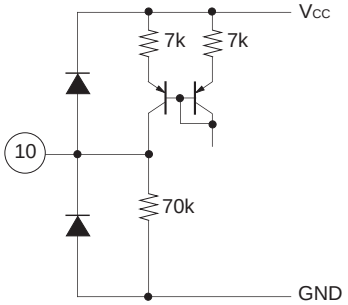
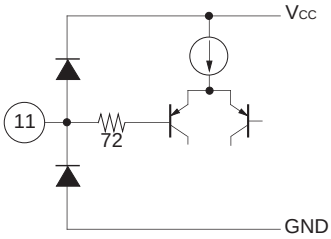
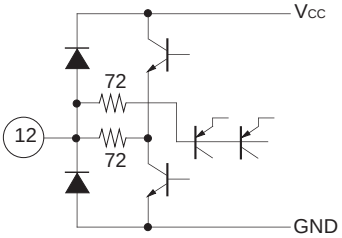
E95517C8Y

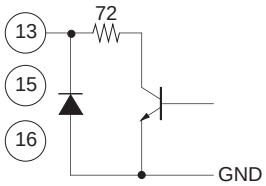
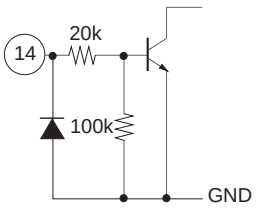
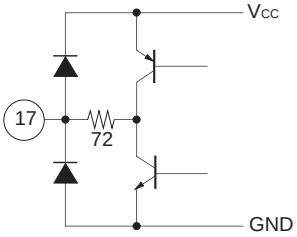
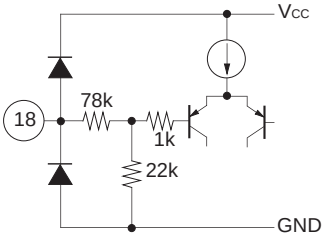
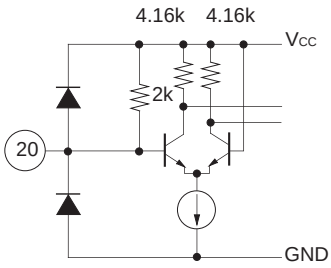
Block Diagram and Pin Configuration



Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	OSC IN	1.4 V		Connects the external parts of crystal oscillator circuit. A capacitor and crystal oscillator are connected to these pins and Vcc.
2	OSC OUT	0.7 V		
3	MIX OUT	1.2 V		Mixer output. Connect a 455 kHz ceramic filter between this pin and IF IN.
4	Vcc			Power supply.
5	IF IN	1.4 V		IF limiter amplifier input.
6	B.S.	—		Controls the battery saving. Setting this pin low suspends the operation of IC. (Applied voltage range: –0.5 V to +7.0 V)
7	FSK REF	0.2 V		Connects the capacitor that determines the low cut-off frequency for the entire system.

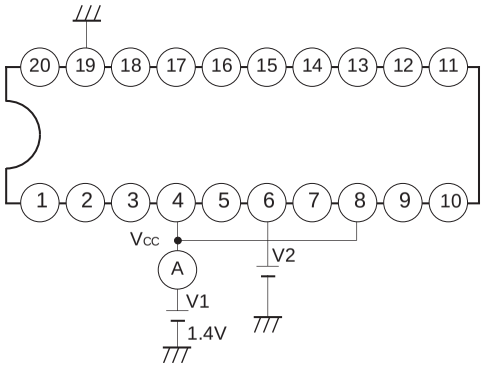
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
8	QUAD	1.4 V		Connects the phase shifter of FM detector circuit.
9	DET OUT	0.2 V		FM detector output.
10	RSSI	0 V		RSSI circuit output.
11	LPF IN	0.2 V		Operational amplifier input.
12	LPF OUT	0.2 V		Level comparator and NRZ comparator inputs. Output for operational amplifier is connected.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
13 15 16	L.C. OUT NRZ OUT LVA OUT	— — —		Level comparator, NRZ comparator and LVA comparator outputs. They are open collectors. (Applied voltage range: –0.5 V to +7.0 V)
14	CHARGE	0 V		Controls the ON/OFF operation of the quick-charge circuit. Set this pin high to execute the quick charge. (Applied voltage range: –0.5 V to +7.0 V)
17	REG CONT	—		Output for internal constant-voltage source amplifier. Connect the base of PNP transistor. (Current capacity: 100 µA)
18	REG OUT	1.0 V		Constant-voltage source output. Controlled to maintain 1.0 V.
19	GND	—		Ground
20	MIX IN	1.4 V		Mixer input.

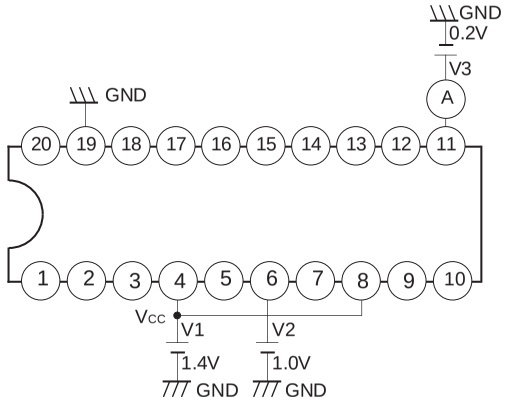
Electrical Characteristics (V_{CC} = 1.4 V, Ta = 25 °C, Fs = 21.7 MHz, F_{MOD} = 1.6 kHz, F_{DEV} = 4.8 kHz, AM_{MOD} = 30 %)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	Measurement circuit 1 V2 = 1.0 V	0.8	1.16	1.5	mA
Current consumption	I_{CCS}	Measurement circuit 1, V2 = 0 V	—	6	20	µA
AM rejection ratio	AMRR	Measurement circuit 3 30k LPF	25	—	—	dB
Op amp. input bias current	I_{BIAS}	Measurement circuit 2	—	—	100	nA
Op amp. maximum output level	V_O	Measurement circuit 4	160	—	—	mVp-p
NRZ output saturation voltage	V_{SATNRZ}	Measurement circuit 6 Vin = 0.3 V	—	—	0.4	V
NRZ output leak current	I_{LNRZ}	Measurement circuit 5 Vin = 0.1 V	—	—	5.0	µA
NRZ hysteresis width	V_{TWNRZ}	Measurement circuit 5 Vin = 0.1 to 0.3 V	—	10	20	mV
VB output current	I_{OUT}	Measurement circuit 7	100	—	—	µA
VB output saturation voltage	V_{SATVB}	Measurement circuit 7	—	—	0.4	V
REG OUT voltage	V_{REG}	Output current 0 µA	0.89	0.96	1.04	V
LVA operating voltage	V_{LVA}	Measurement circuit 8 V1 = 1.4 to 1.0 V	1.00	1.05	1.10	V
LVA output leak current	I_{LLVA}	Measurement circuit 8 V1 = 1.0 V	—	—	5.0	µA
LVA output saturation voltage	V_{SATLVA}	Measurement circuit 9	—	—	0.4	V
Detector output voltage	V_{ODET}	Measurement circuit 3	38	50	68	mVrms
Logic input voltage high level	V_{THBSV}	—	0.9	—	—	V
Logic input voltage low level	V_{TLBSV}	—	—	—	0.35	V
Limiting sensitivity	$V_{IN\ (LIM)}$	Measurement circuit 3	—	5	14	dBµ
Level comparator output saturation voltage	V_{SATLC}	Measurement circuit 11	—	—	0.4	V
Level comparator output leak current	I_{LLC}	Measurement circuit 10	—	—	5.0	µA
RSSI output offset	V_{ORSSI}	Measurement circuit 12	—	400	550	mV
Mixer input resistance	R_{INLIM}	—	1.6	2.0	2.4	kΩ
Mixer output resistance	R_{OUTMIX}	—	1.2	1.5	1.8	kΩ
IF limiter input resistance	R_{INLIM}	—	1.2	1.5	1.8	kΩ

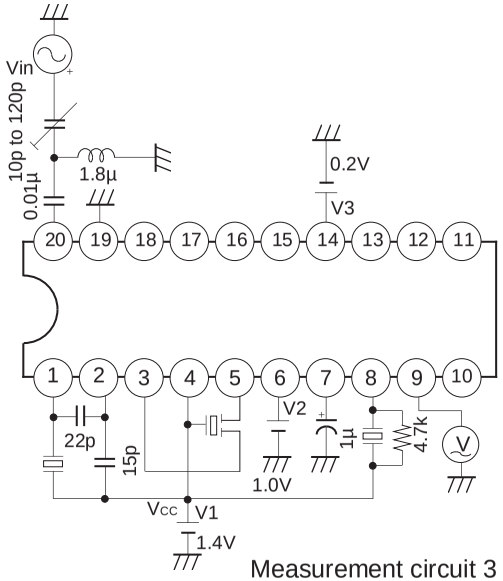
Electrical Characteristics Measurement Circuit



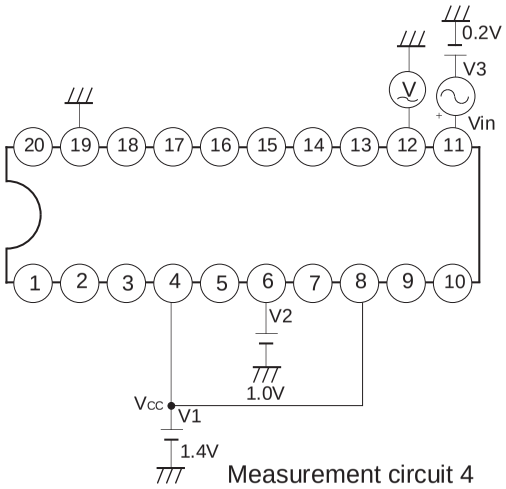
Measurement circuit 1



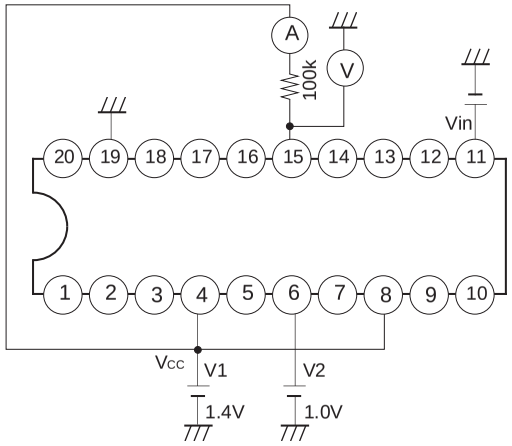
Measurement circuit 2



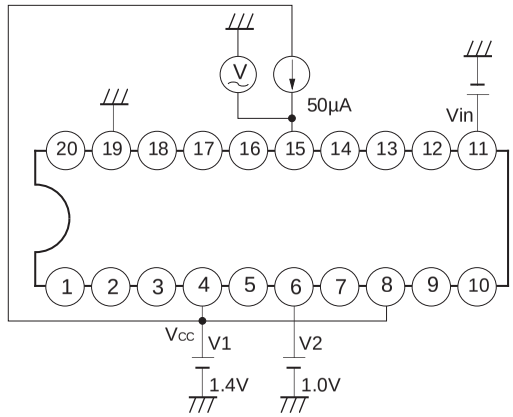
Measurement circuit 3



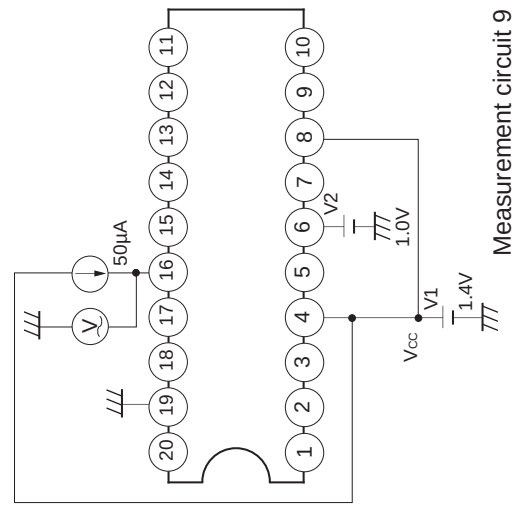
Measurement circuit 4



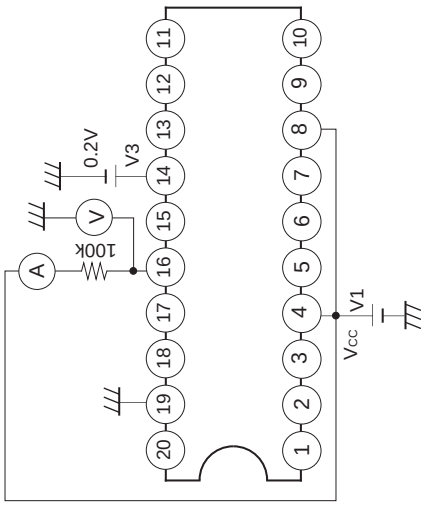
Measurement circuit 5



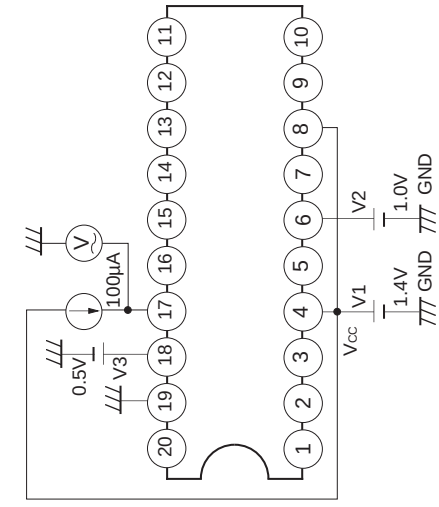
Measurement circuit 6



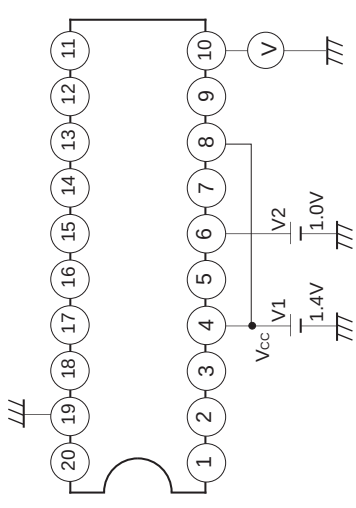
Measurement circuit 9



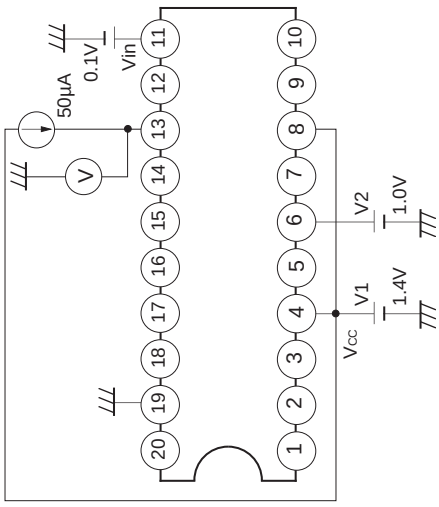
Measurement circuit 8



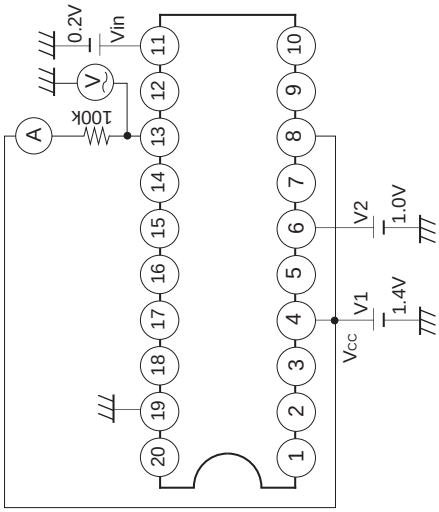
Measurement circuit 7



Measurement circuit 12

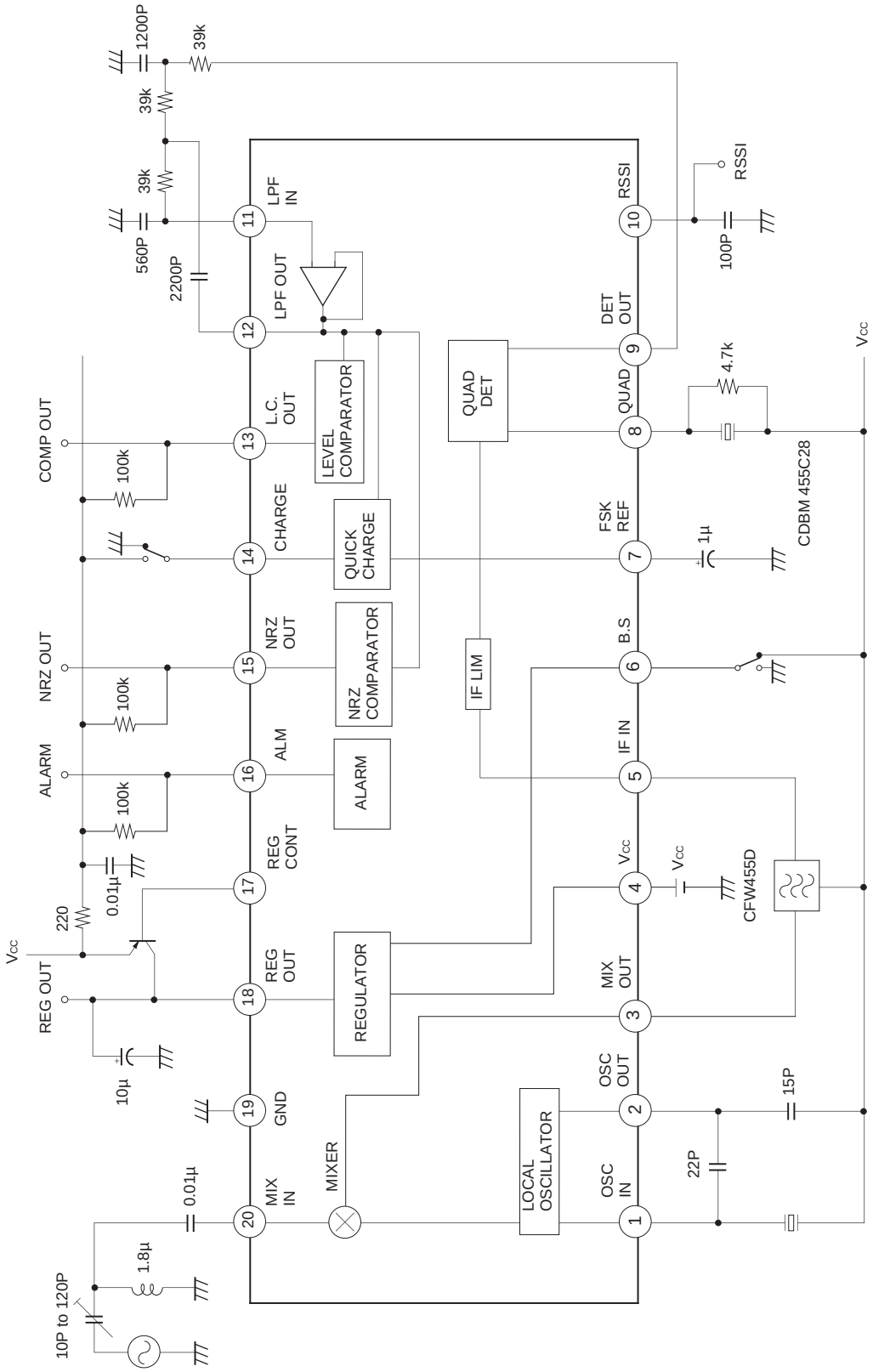


Measurement circuit 11



Measurement circuit 10

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Note

1) Power Supply

The CXA1999N, with built-in regulator, is designed to permit stable operation at wide range of supply voltage from 1.1 to 4.0 V. Decouple the wiring to VCC (Pin 4) as close to the pin as possible.

2) Oscillator Input

Oscillator input method

a) Using Pins 1 and 2, input self-excited oscillation signal through the composition of a Colpitts type crystal oscillator circuit.

b) Directly input a local oscillation signal to Pin 1.

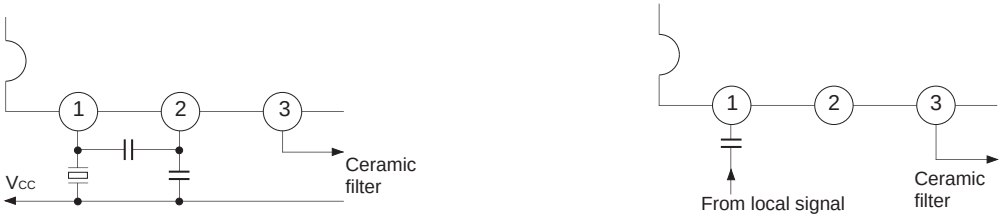


Fig. 1

3) Mixer

The mixer is of double-balance type. Pin 20 is the input pin. Input though a suitable matching circuit. The input impedance is 2.0 kΩ.

Pin 3 serves as the output pin for the mixer, and a load resistance of 1.5 kΩ is incorporated.

4) IF Filter

The filter to be connected between this mixer output and the IF limiter amplifier input should have the following specifications.

I/O impedance : 1.5 kΩ ±10 %

Band width : Changes according to applications.

5) IF Limiter Amplifier

The gain of this IF limiter amplifier is approximately 100 dB. Take notice of the following points in making connection to the IF limiter amplifier input pin (Pin 5).

a) Be sure to wire to the IF limiter amplifier input (Pin 5) is as short as possible.

b) As the IF limiter amplifier output appears at QUAD (Pin 8), be sure to wire to the ceramic discriminator connected to QUAD is as short as possible and reduce the interference with the mixer output and IF limiter amplifier input.

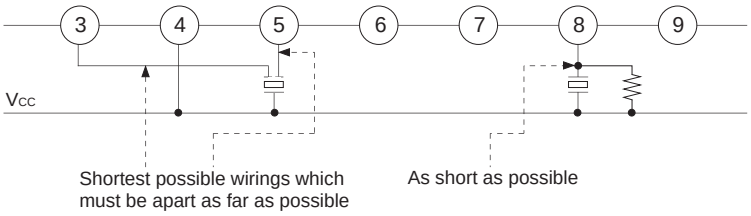


Fig. 2

6) Quick Charge

In order to hasten the rising time from when power is turned on, the CXA1999N features a quick charge circuit. Therefore, the quick charge circuit eliminates the need to insert a capacitor between the detector output and the LPF as is the case with conventional ICs, but connects a capacitor to Pin 7 to determine the average signal level during steady-state reception. The capacitance of the capacitor connected to Pin 7 should be chosen such that the voltage does not vary much due to discharge during battery saving.

Connect a signal for controlling the quick charge circuit to Pin 14. Setting this pin high enables the quick charge mode, and setting this pin low enables the steady-state reception mode. Quick charge is used when the power supply is turned on. The battery saving must be set high at the time.

Connect Pin 14 to GND when quick charge is not being used.

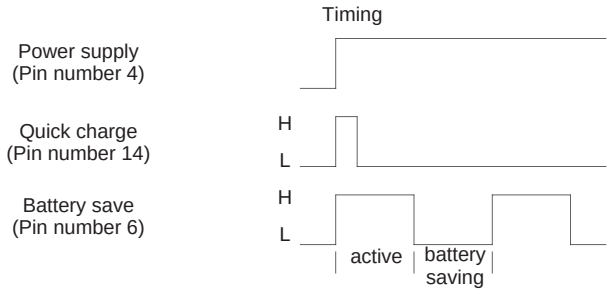


Fig. 3

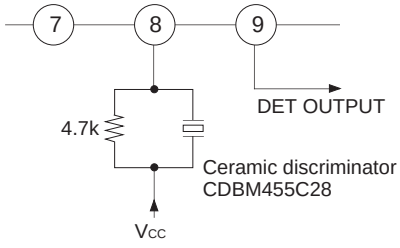
7) Detector

The detector is of quadrature type. To perform phase shift, connect a ceramic discriminator to Pin 8.

The phase shifting capacitor for the quadrature detector is incorporated. The demodulated FM (FSK) signal with the detector will be output to DET OUT (Pin 9) through the internal primary LPF.

DET OUT output impedance is 200 Ω or less. The DET OUT output is the anti-phase output to NRZ OUT.

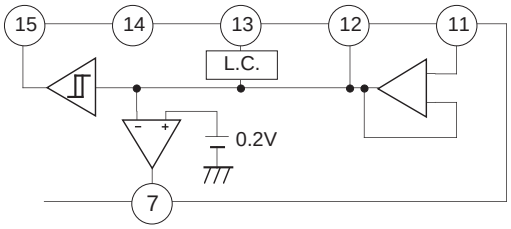
The CDBM455C28 (MURATA MFG. CO., LTD.) ceramic discriminator is recommended for the CXA1999N.



8) Filter Buffer, Level Comparator and NRZ Comparator

An operational amplifier for LPF is built in this IC.

It is connected internally to the NRZ comparator, level comparator and quick charge circuit.



Using the operational amplifier of Pins 11 and 12 to construct an LPF, remove noise from the demodulated signal and input the signal to the above three circuits.

The level comparator and the NRZ comparator shape waveform of this input signal and output it as a square wave. The comparator output stage is for open collector.

Thus, if the CPU is of CMOS type and the supply voltage is different, a direct interface as illustrated in the figure below can be implemented.

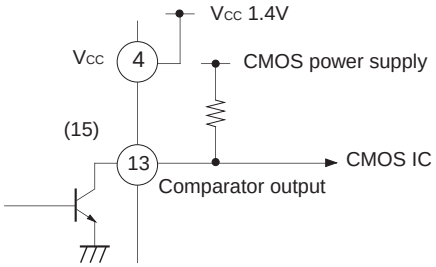


Fig. 6

9) REG CONT

Controls the base bias of the external transistors.

10) LVA OUT

This pin goes high (open) when the supply voltage becomes low. Since the output is an open collector, it can be used to directly drive CMOS device. The setting voltage of the LVA is 1.05 V (typ.), and it possesses a hysteresis with respect to the supply voltage. The hysteresis width is 50 mV (typ.).

11) B.S.

Operation of the CXA1999N can be halted by setting this pin low. This pin can be connected directly to CMOS device. The current consumption for battery saving is 20 µA or less (at 1.4 V).

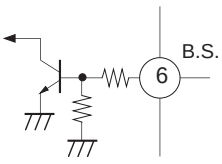
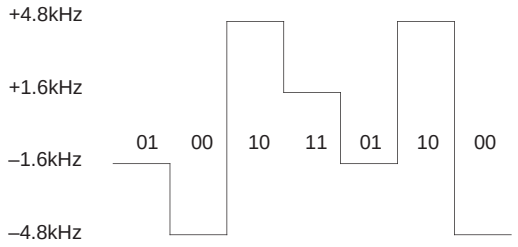


Fig. 7

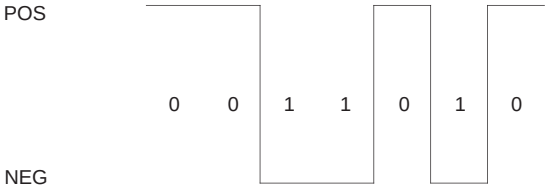
12) M-ary (M = 2- or 4-level) FSK Demodulation System

Polarity discrimination output and MSB comparator output are used to demodulate the 4-level waveform shown below.

[4-level FSK demodulating waveform]

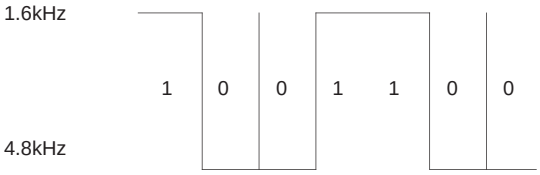


[NRZ OUT] Polarity discrimination output (When the input frequency is higher than the local frequency)



The polarity can be inverted by setting the local frequency higher than the input frequency.

[L.C. OUT] MSB comparator output



The 4-level FSK demodulating data is divided into an NRZ OUT and L.C. OUT shown above. Here, the NRZ OUT corresponds to a conventional NRZ comparator output. The L.C. OUT is made comparing the demodulated waveform amplitude to the IC internal reference voltage levels. When the threshold value of L.C. OUT is not appropriate to the detector output, the resistance value on Pin 8 should be adjusted for the detector output level adjustment.

For the 2-level FSK demodulation, it corresponds to a conventional NRZ comparator output.

13) Principle of Quick Charge Operation

BUF in Fig. 8 is the detector buffer amplifier, and AMP is an operational amplifier to construct an LPF. COMP is the level comparator or the NRZ comparator. The CXA1999N has a feedback loop from the comparator input to the input circuit of the detector output buffer. This equalizes the average value of the comparator input voltage to the reference voltage, with the quick charge circuit of CHG being set in the feedback loop. Switching the current of the quick charge circuit enables reduction of the rise time.

In this block, CHG is a comparator which compares input voltages and outputs a current based on this comparison. The current on CHG is switched between high and low at Pin 14. When the power is turned on, switch the current to high to increase the charge current at C in Fig. 8 and shorten the time constant. During steady-state reception mode, switch the current to low, lengthening the charge time constant and allowing for stable data retrieval.

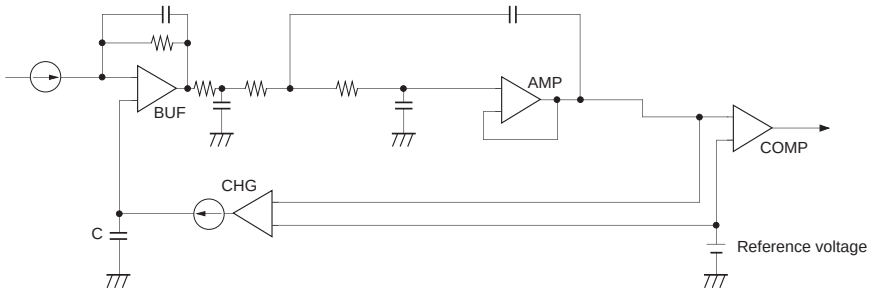


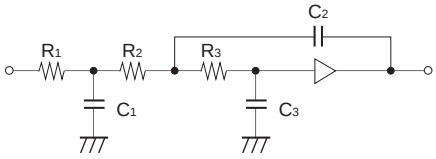
Fig. 8

14) S Curve Characteristics

Even if the IF IN input signal frequency is deviated, the feedback is applied to the DET OUT operating point so as to match it to the comparator reference voltage by the quick charge operation shown in Fig. 8. Therefore, this feedback must be halted in order to evaluate the S curve characteristics.

To execute the evaluation, measure the average voltage on Pin 12 first and input this voltage to Pin 7 from the external power supply.

15) Example of Data Filter Constants



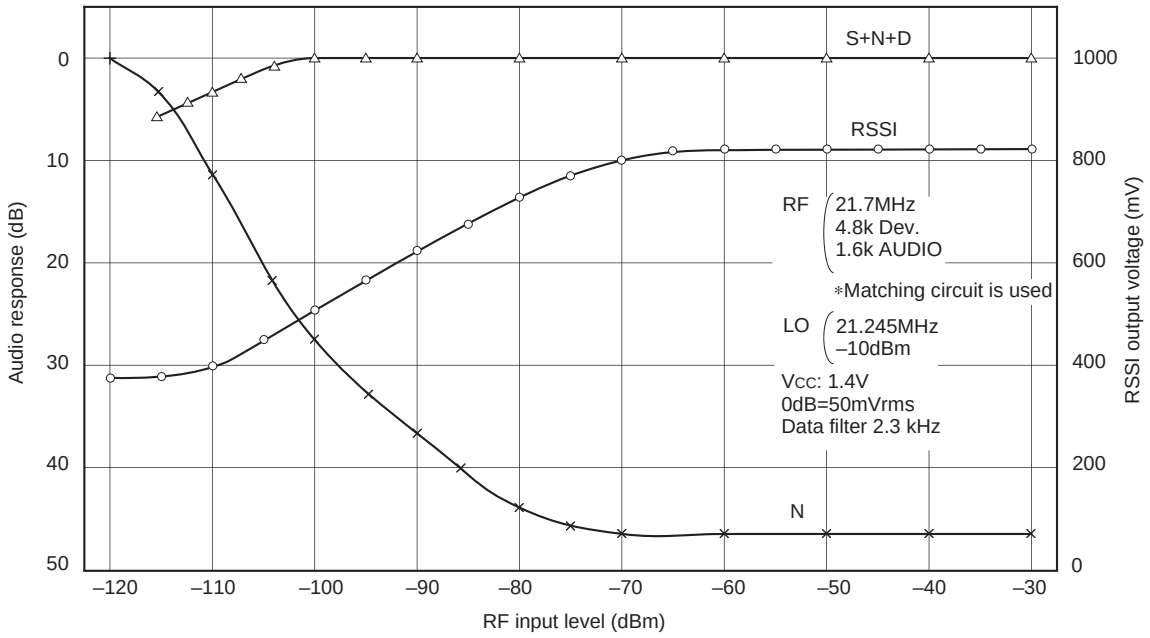
Parameter / bps	R_1	R_2	R_3	C_1	C_2	C_3	fc (Hz)
512	22 kΩ	22 kΩ	22 kΩ	0.015 µF	0.027 µF	6800 pF	350
1200	68 kΩ	68 kΩ	68 kΩ	2700 pF	4700 pF	820 pF	800
2400	39 kΩ	39 kΩ	39 kΩ	1500 pF	3300 pF	820 pF	1.7 k
3200 (6400)∗	39 kΩ	39 kΩ	39 kΩ	1200 pF	2200 pF	560 pF	2.3 k

∗ For 4 levels

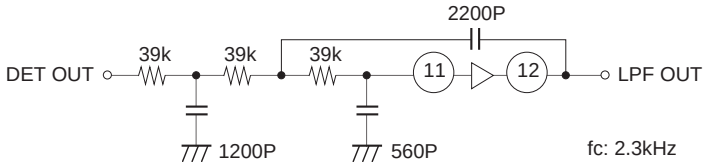
Note on operation : Measures for the prevention of electrostatic breakdown should be taken to handle this IC.

Example of Representative Characteristics

RF input level vs. Audio response, RSSI characteristics for 1.6 kHz SIN signal

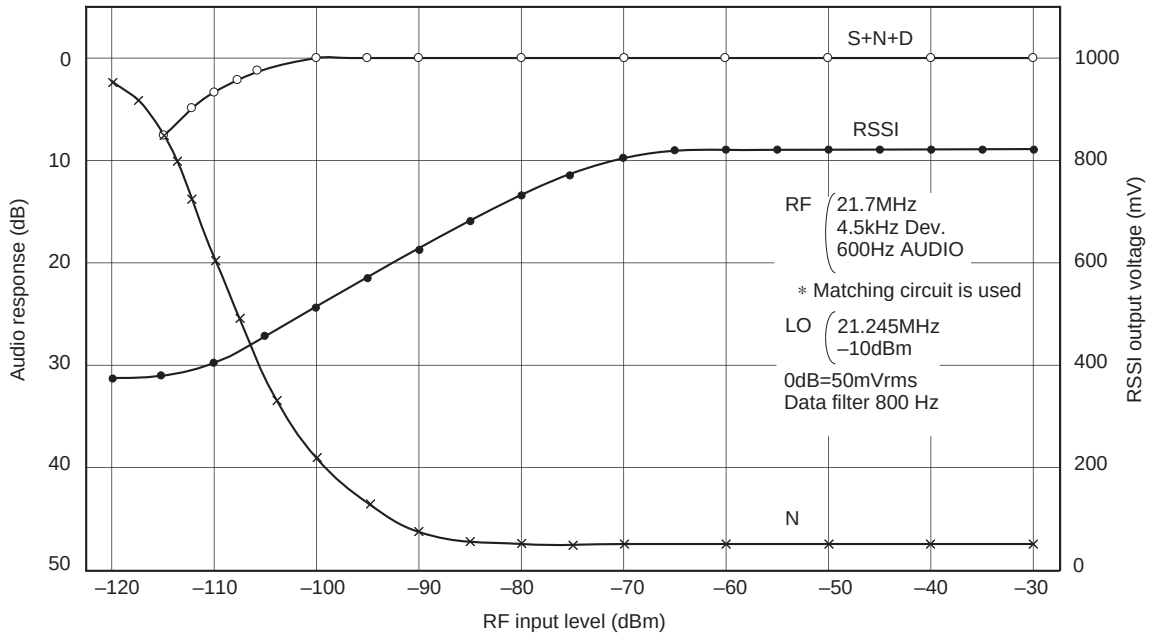


Filter constants of the graph above

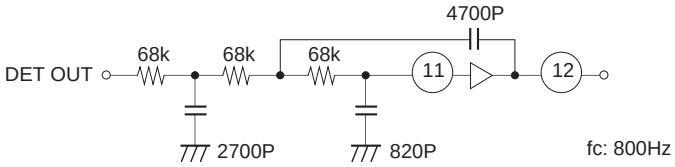


Example of Representative Characteristics

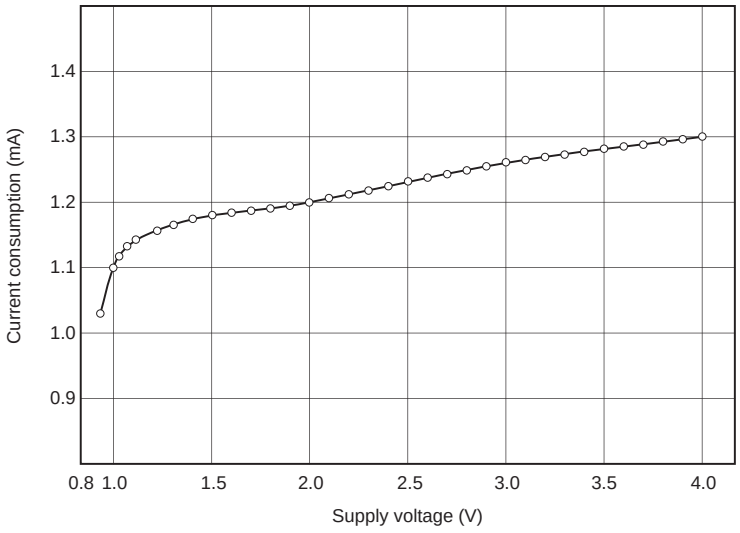
RF input level vs. Audio response, RSSI characteristics for 600 Hz SIN signal



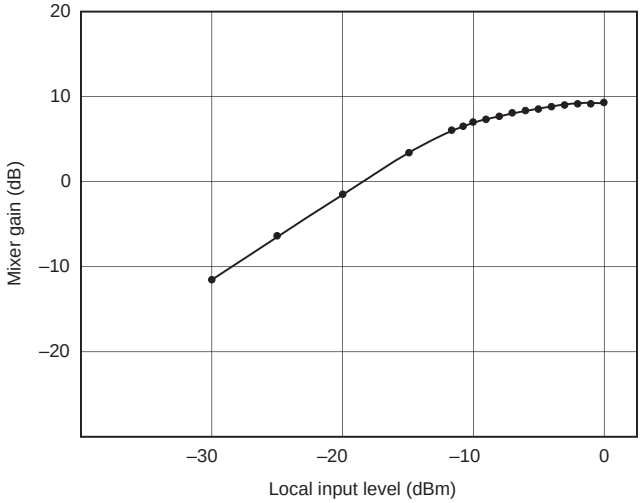
Filter constants of the graph above



Supply voltage vs. Current consumption

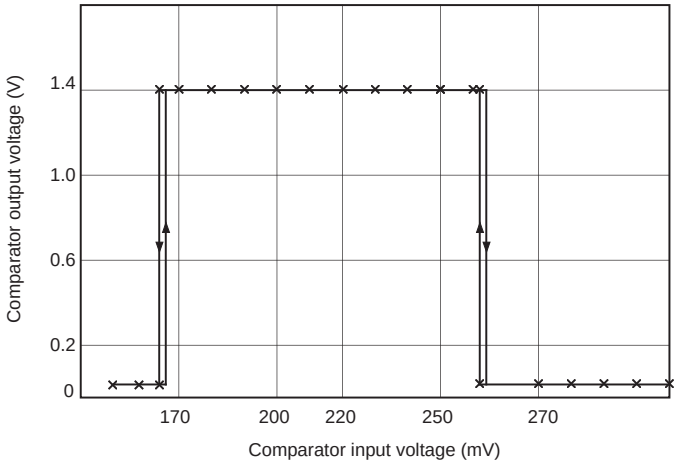


Local input level vs. Mixer gain

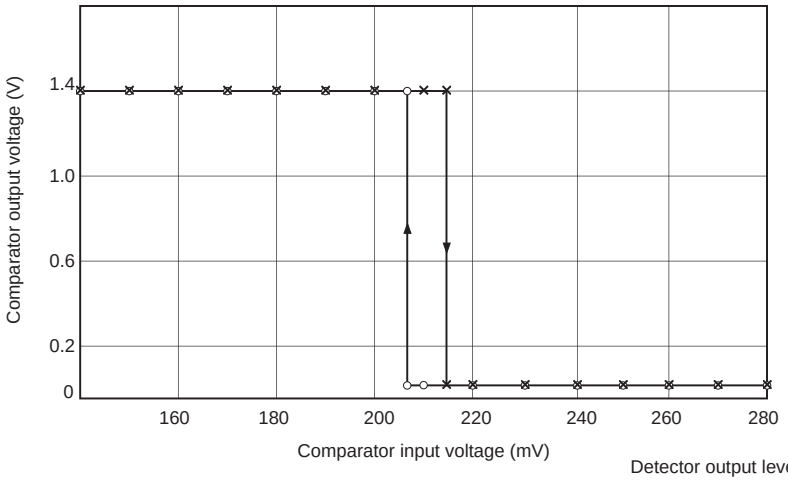


With IF filter load
RF21.7 MHz –60 dBm
Matching circuit provided
Level difference between
Pin 20 and Pin 3

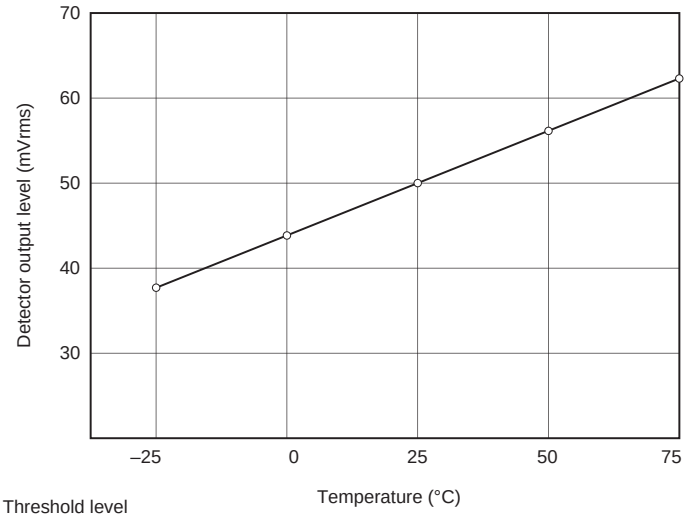
Level comparator



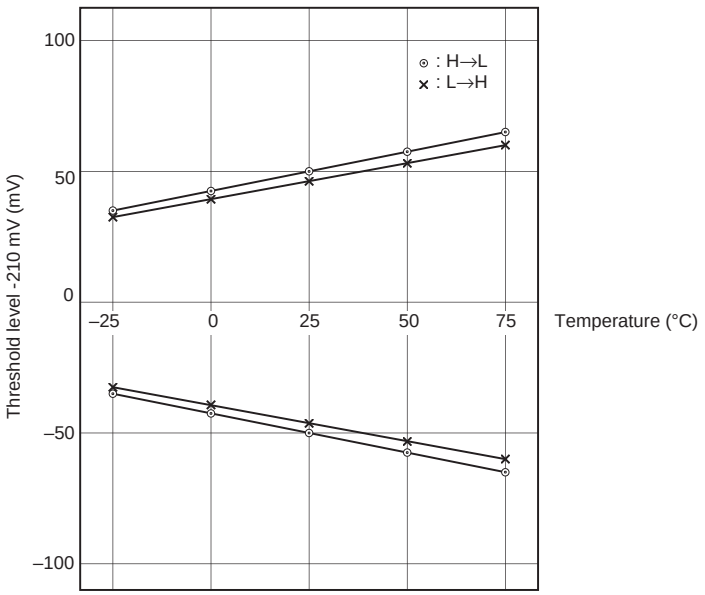
NRZ comparator



Detector output level temperature

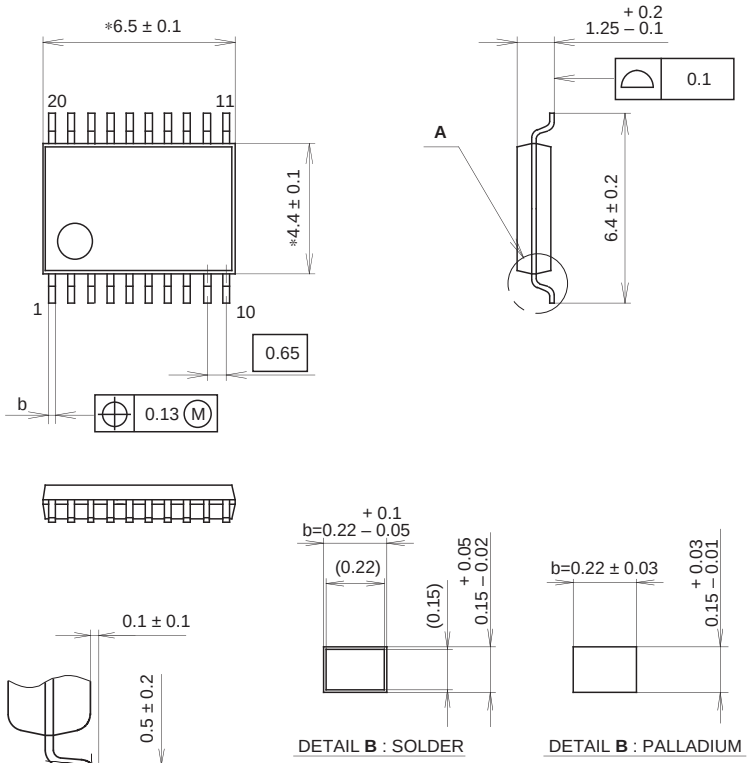


Level comparator temperature vs. Threshold level



Package Outline Unit : mm

20PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).