8 bit 30/50 MSPS Flash A/D Converter

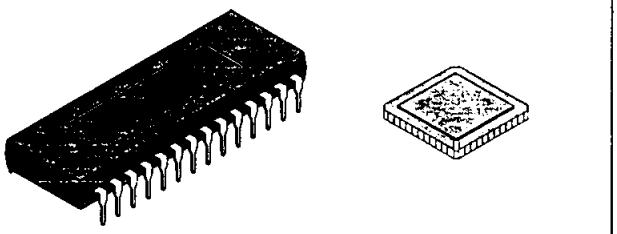
Evaluation Board Available — CXA1016PPCB/CXA1016KPCB
CXA1056PPCB/CXA1056KPCB

Description

CXA1016P/CXA1016K/CXA1056P/CXA1056K are 8 bit high-speed A/D converter ICs for various applications. They can be used widely for various purposes which require high-speed A/D conversions.

CXA1016P/CXA1056P are assembled in the plastic DIP packages and CXA1016K/CXA1056K are in the ceramic lead-less chip carriers.

28 pin DIP (Plastic) 44 pin LCC (Ceramic)



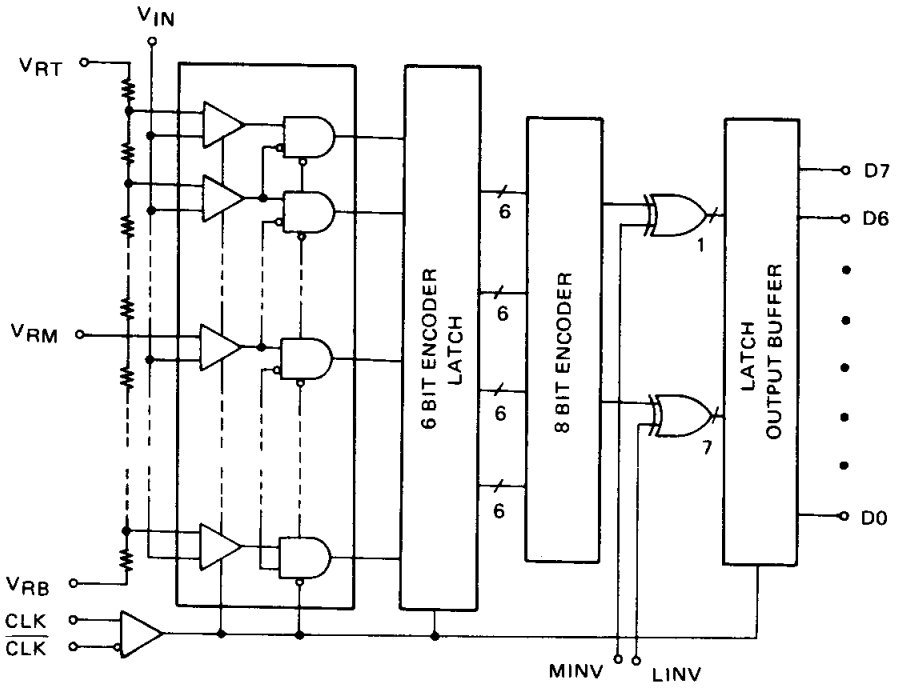
Features (CXA1016P/CXA1016K)

- Resolution — 8 bits ± 1/2 LSB
- High-speed operation — Maximum conversion Rate 30 MSPS
- Wide analog input bandwidth — 30MHz (−3dB)
- Low input capacitance — 35 pF (typ)
- Low power consumption — 420 mW (typ)

Features (CXA1056P/CXA1056K)

- Resolution — 8 bits ± 1/2 LSB
- High-speed operation — Maximum conversion Rate 50 MSPS
- Wide analog input bandwidth — 50MHz (−3dB)
- Low input capacitance — 35 pF (typ)
- Low power consumption — 550 mW (typ)

Block Diagram



E89643-ST

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}	0 to −7	V	
• Analog input voltage	V_{IN}	0.5 to V_{EE}	V	
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	0.5 to V_{EE}	V	
	$\lvert V_{RT}-V_{RB} \rvert$	2.5	V	
• Digital input voltage	CLK, $\overline{CLK}$, MINV, LINV	0.5 to −4	V	
• VRM pin input current	I_{VRM}	−3 to +3	mA	
• Digital output current	ID_0 to ID_7	0 to −10	mA	
• Operating temperature	Ta	−20 to +100	°C	(CXA1016P/CXA1056P)
	Tc	−25 to +125	°C	(CXA1016K/CXA1056K)*1
• Storage temperature	Tstg	−55 to +150	°C	
• Allowable power dissipation	P_D	1.48	W	(CXA1016P/CXA1056P)
		1.08	W	(CXA1016K/CXA1056K)

*1 Heat sinking is required above 100°C (CXA1016K)/86°C (CXA1056K).

Recommended Operating Conditions (CXA1016P/CXA1016K)

		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}-DV_{EE}	−0.05	0	0.05	V
	AGND-DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	25			ns
	Tpw0	8			ns

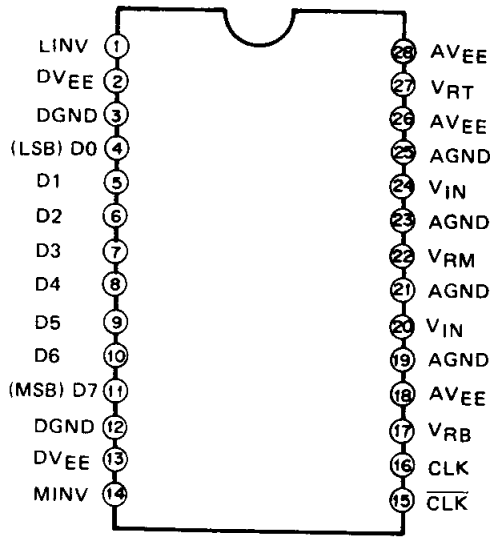
Recommended Operating Conditions (CXA1056P/CXA1056K)

		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	−5.7	−5.2	−5.0	V
	AV_{EE}—DV_{EE}	−0.05	0	0.05	V
	AGND—DGND	−0.05	0	0.05	V
• Reference input voltage	V_{RT}	−0.1	0	0.1	V
	V_{RB}	−2.2	−2	−1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Clock pulse width	Tpw1	15			ns
	Tpw0	5			ns

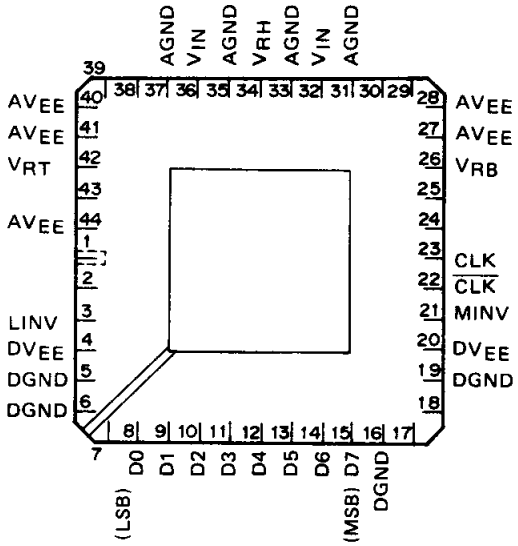
Pin Configuration (Top View)

The pin numbers without indication are empty pins. (not connected)

CXA1016P/CXA1056P



CXA1016K/CXA1056K



Pin Description

Symbol	Function
AVEE	Analog VEE, −5.2V (typ). Coupled with ~6Ω between DVEE.
LINV	Input pin for output polarity inversion of D0 (LSB)~D6. (See the code table)
DVEE	Digital VEE, −5.2V (typ).
DGND	Digital GND, which is separated from the Analog GND.
D0~D7	Digital data output pin, ECL level. D0: LSB~D7: MSB. Pull-down resistors are necessary externally.
MINV	Input pin for output polarity inversion of D7 (MSB) (See the code table). ECL level. "0" level is held when it is released.
$\overline{CLK}$	Inverse clock input pin, ECL level.
CLK	Clock input pin, ECL level.
VRB	Reference voltage (bottom), −2V (typ).
AGND	Analog GND
VIN	Analog input, input range is VRT~VRB
VRM	Middle point of the reference voltage, it can be used as a linearity correction pin.
VRT	Reference voltage (top), 0V (typ).
	Empty pins (not connected), 2 and 19 are used to be grounded to DGND, the others are used to be grounded to AGND.

Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111 . . . 11	100 . . . 00	011 . . . 11	000 . . . 00
.	111 . . . 10	100 . . . 01	011 . . . 10	000 . . . 01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
VIN .	100 . . . 00	111 . . . 11	000 . . . 00	011 . . . 11
.	011 . . . 11	000 . . . 00	111 . . . 11	100 . . . 00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000 . . . 01	011 . . . 10	100 . . . 01	111 . . . 10
−2V	000 . . . 00	011 . . . 11	100 . . . 00	111 . . . 11

1: VIH, VOH
0: VIL, VOL

Electrical Characteristics (CXA1016P/CXA1016K)

(T_a=25°C, V_{EE}=−5.2V, V_{RT}=0V, V_{RB}=−2V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Conversion Rate		Fc	V_{IN}=0 to −2V, fin=1 kHz, ramp	30			MSPS
Supply Current		I_{EE}			−75	−100	mA
Analog Input Capacitance		C_{IN}	V_{IN}=−1V+0.07 Vrms		35	40	pF
Analog Input Bias Current		I_{IN}	V_{IN}=−1V		60	90	μA
Reference Resistor		Rr (V_{RT}~V_{RB})		70	80	100	Ω
Offset Voltage	V_{RT}			7	9	11	mV
	V_{RB}			15	17	19	mV
Digital Input Voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital Input Current		I_{IH}	V_{IH}=−0.9V	0		0.4	mA
		I_{IL}	V_{IL}=−1.75V	−0.05		0.35	mA
Digital Output Voltage		V_{OH}	Rℓ=620Ω ~ V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output Data Delay		Td	Rℓ=620Ω ~ V_{EE}		4.0	5.0	ns
Non-linearity Error			Fc = 30 MSPS, V_{IN}=0 to −2V, fin=1 kHz, ramp			±½	LSB
Differential Non-linearity Error			Fc = 30 MSPS			±½	LSB
Differential Gain		DG	NTSC 40 IRE mod. ramp, Fc = 30 MSPS			1.5.	%
Differential Phase		DP				0.5	deg.
Aperture Jitter		Taj			45		ps
Sampling Delay		Tsd		6.3	6.8	7.3	ns
Full scale input BW (−3dB)		BW_F	*1		30		MHz

*1 Source impedance = 50 Ω
Without a buffer amplifier driving A/D input

Electrical Characteristics (CXA1056P/CXA1056K)

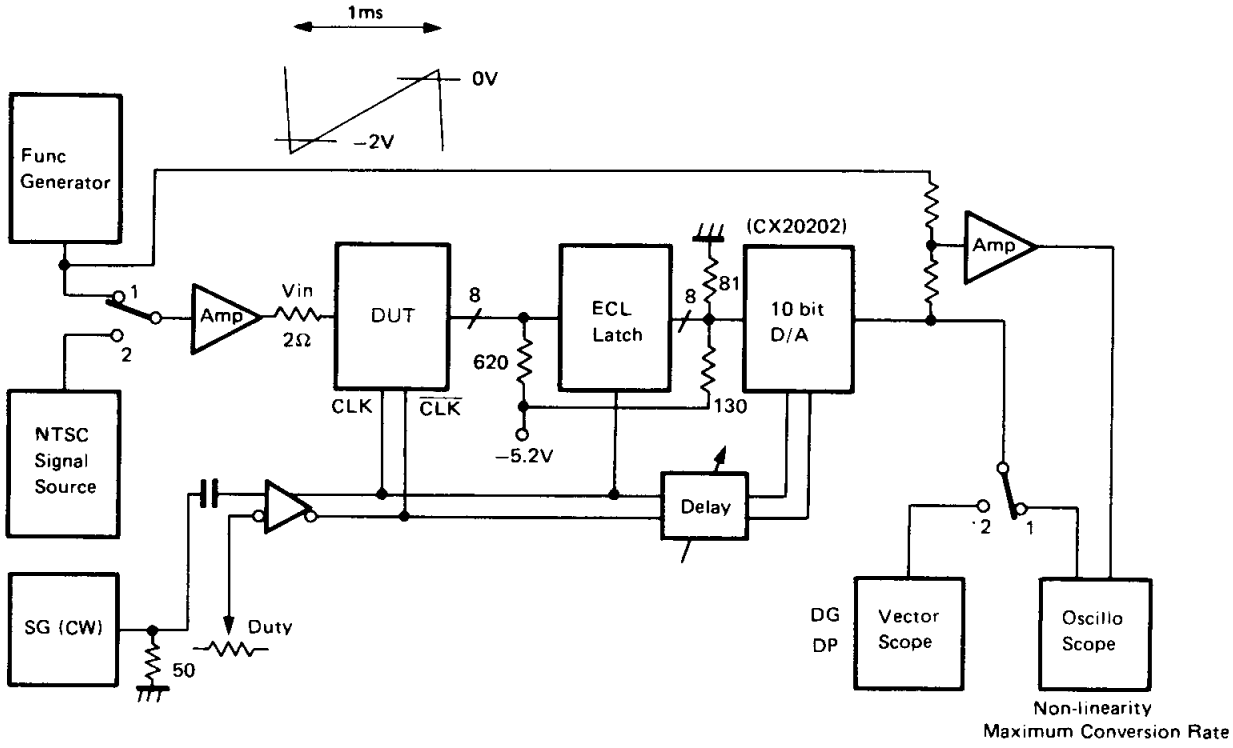
(Ta=25°C, V_{EE}=−5.2V, V_{RT}=0V, V_{RB}=−2V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Conversion Rate		Fc	V_{IN}=0 to −2V, fin=1 kHz, ramp	50			MSPS
Supply Current		I_{EE}			−95	−120	mA
Analog Input Capacitance		C_{IN}	V_{IN}=−1V+0.07 Vrms		35	40	pF
Analog Input Bias Current		I_{IN}	V_{IN}=−1V		75	115	μA
Reference Resistor		Rr (V_{RT}~V_{RB})		70	80	100	Ω
Offset Voltage	V_{RT}			7	9	11	mV
	V_{RB}			15	17	19	mV
Digital Input Voltage		V_{IH}		−1.0	−0.9	−0.7	V
		V_{IL}		−1.9	−1.75	−1.6	V
Digital Input Current		I_{IH}	V_{IH}=−0.9V	0		0.4	mA
		I_{IL}	V_{IL}=−1.75V	−0.05		0.35	mA
Digital Output Voltage		V_{OH}	Rℓ=620Ω ~ V_{EE}	−1.0			V
		V_{OL}				−1.6	V
Output Data Delay		Td	Rℓ=620Ω ~ V_{EE}		4.0	5.0	ns
Non-linearity Error			Fc = 50 MSPS, V_{IN}=0 to −2V, fin=1 kHz, ramp			±½	LSB
Differential Non-linearity Error			Fc = 50 MSPS			±½	LSB
Differential Gain		DG	NTSC 40 IRE mod. ramp, Fc = 50 MSPS			1.5	%
Differential Phase		DP				0.5	deg.
Aperture Jitter		Taj			30		ps
Sampling Delay		Tsd		5.4	5.7	6.0	ns
Full scale input BW (−3dB)		BW_F	*1		50		MHz

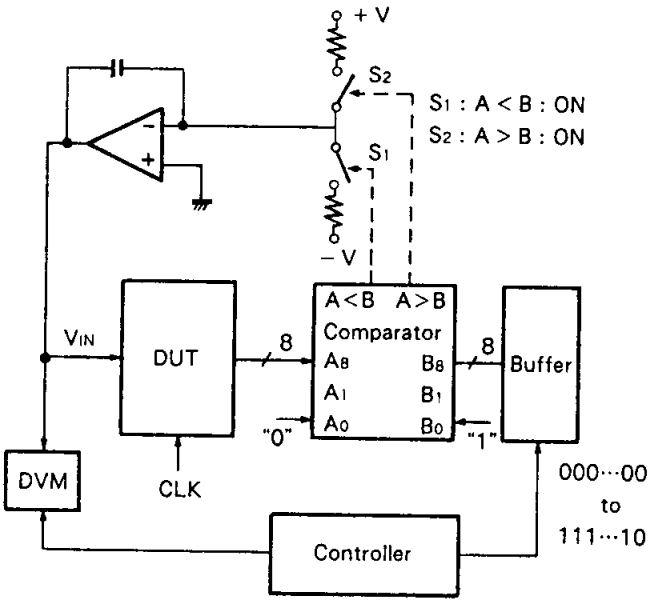
*1 Source impedance = 50 Ω
Without a buffer amplifier driving A/D input

Electrical Characteristics Test Circuit

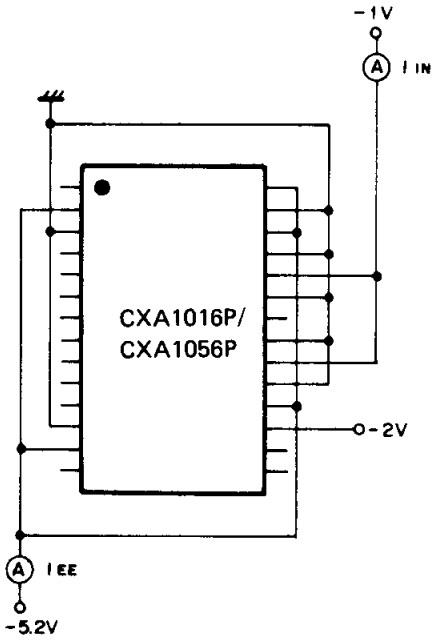
Maximum Conversion Frequency Test Circuit
Differential Gain Error Test Circuit
Differential Phase Error Test Circuit

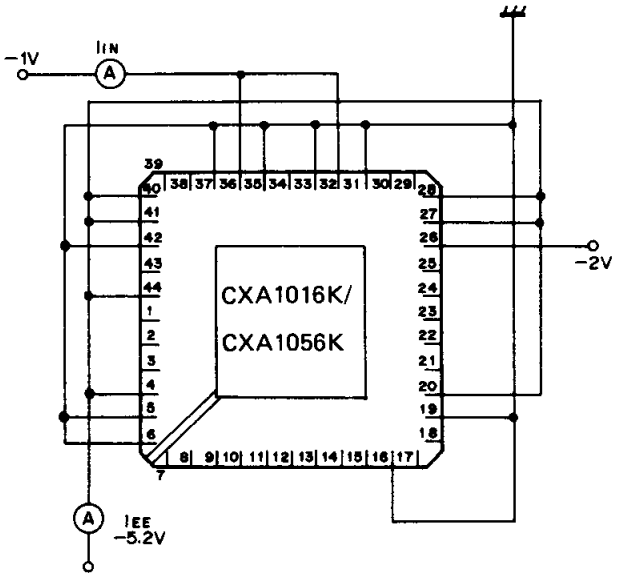


Differential Non-linearity Test Circuit
Integral Non-linearity Test Circuit

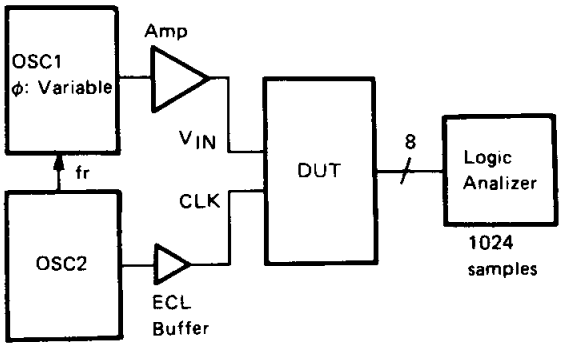


Power Supply Current Test Circuit
Analog Input Bias Current Test Circuit





Aperture Jitter Test Circuit



Description of Function (See the block diagram and timing chart.)

1. The reference voltage, which is obtained by dividing equally the voltage across V_{RT} to V_{RB} into 256 by the reference resistor ledder, is applied to the respective ⊕ (positive) input sides of 256 clocked comparators. An analog input is applied to the ⊖ (negative) input sides of all the 256 clocked comparators from the V_{IN} pin.

2. When the state of CLK is in Low, the master (front stage) of the comparator compares the respective reference voltage and the analog input voltage which is ever-changing.

3. When the CLK moves from Low into Hi, each master latches the state immediately prior to the above simultaneously, and as a result, it provides conditions of "11 .... 1100 .. 0" in sequence from the V_{RT} side to the V_{RB} side.

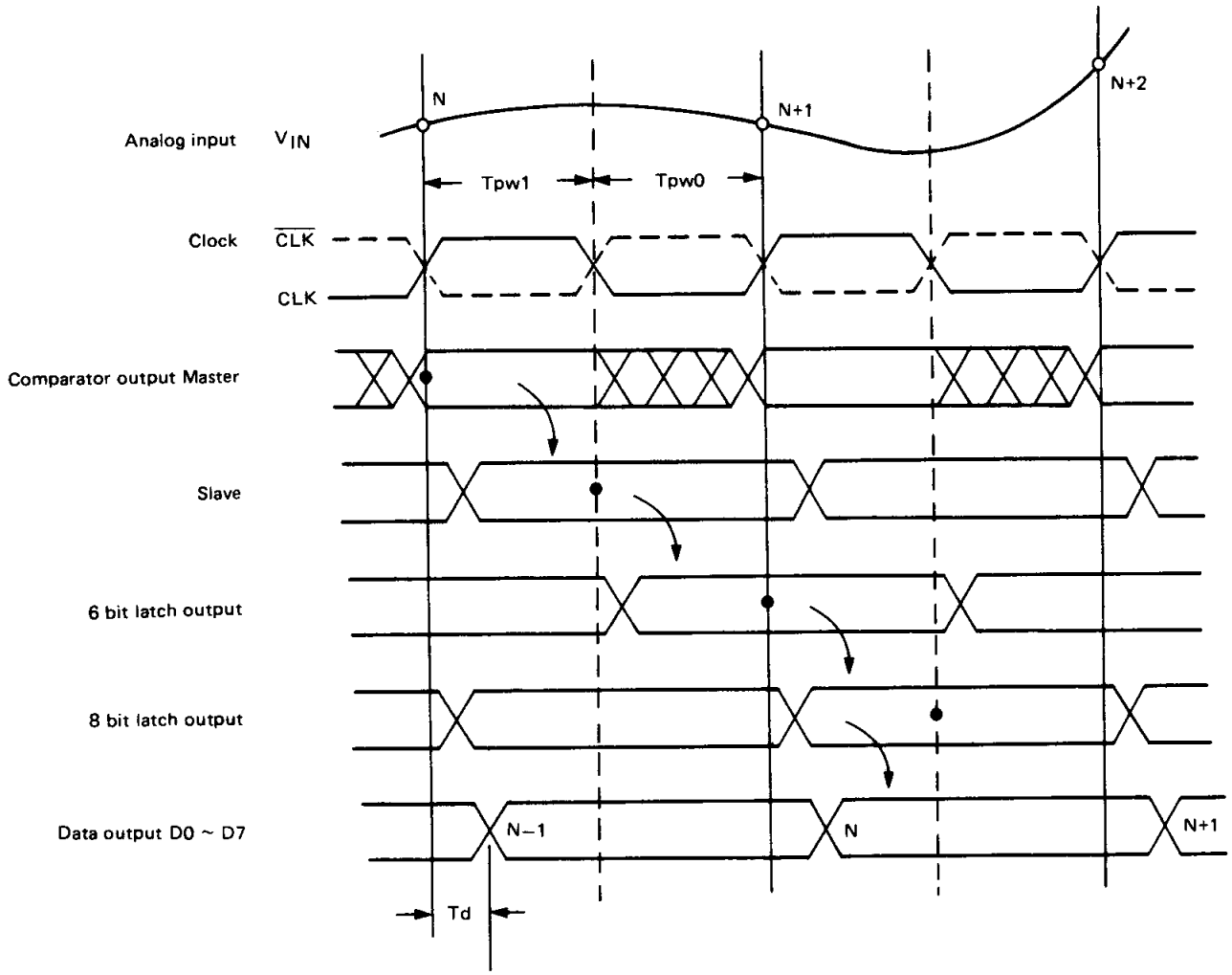
4. The output of the master is ANDed between the respective adjacent outputs, and "1" stands only when neighboring 2 outputs become "10", and the all other outputs become "0".

5. The result of the AND is latched when CLK moves from Hi into Low. Output of the slave is divided into 4 blocks and each block has 32 clocked comparators, and they are coded into binary codes of 6 bits respectively by the transistor matrix circuit.

6. The 6 bit codes are further coded into 8 bit codes by the transistor matrix circuit after they are respectively latched, and they are then output into the ECL level by the output buffer after being 8 bit latched. The output data is delayed 1 clock from the data sampling point and appears at the output pin.

7. Two polarity inversion inputs such as MINV and LINV are fed externally to the output buffer, and each of them selects output polarity of MSB and other polarity than MSB respectively.

Timing Chart

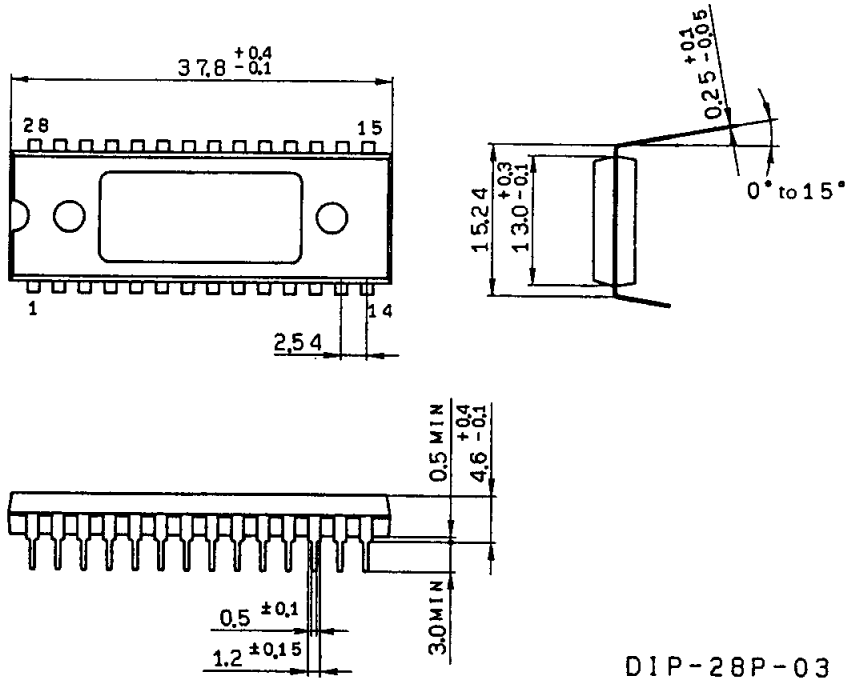


Dots (•) in the chart demote respective latch timings.

*See page 54 for Tpwl and Tpw0.

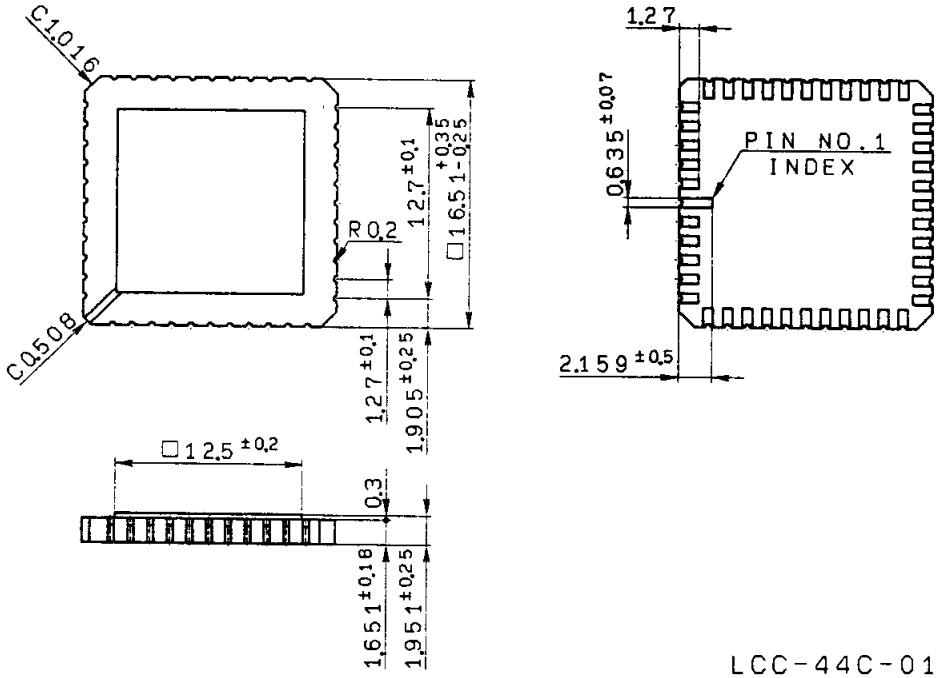
Package Outline Unit: mm

CXA1016P/CXA1056P 28 pin DIP (Plastic)



DIP-28P-03

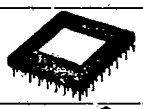
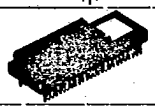
CXA1016K/CXA1056K 44 pin LCC (Ceramic)



LCC-44C-01

T-90-20

Sony Package Product Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction

*P……Plastic, C……Ceramic