SONY CXA1260Q-Z

8 bit 35 MSPS RGB 3-Channel D/A Converter

Description

CXA1260Q-Z is an 8-bit high-speed D/A converter for video band use. It has an output/input equivalent to 3 channels of R, G and B. It is suitable for use of digital TV, graphic display, etc.

48 pin QFP (Plastic)

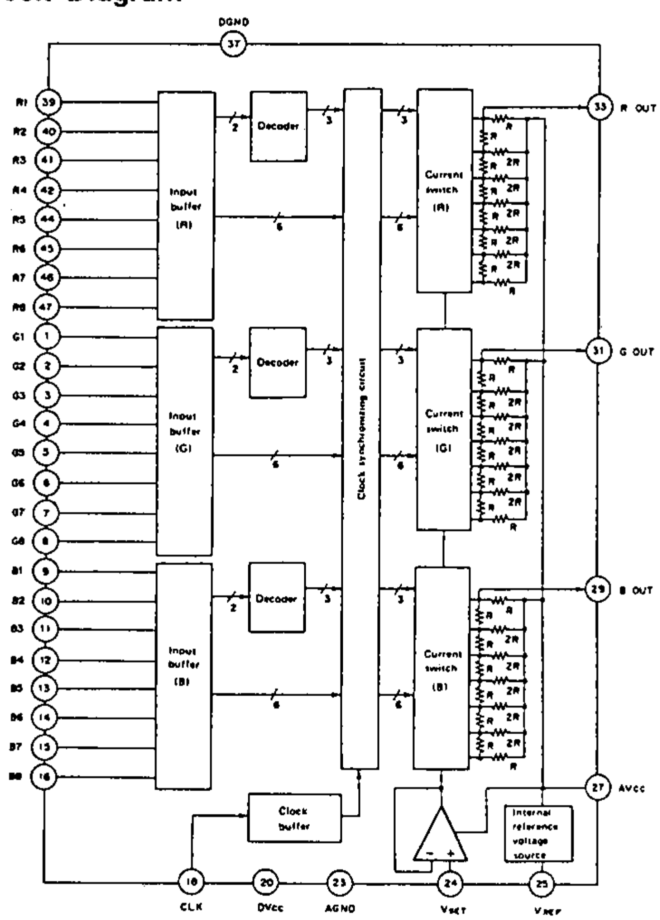
Features

- Resolution: 8-bits
- Maximum conversion speed: 35MSPS
- RGB 3-channel input/output
- Differential linearity error: ±1/2LSB
- Digital input voltage: TTL level
- Output voltage full-scale: 1 Vp-p (typ)
- Low power consumption: 360 mW (typ)
- +5V single power supply

Structure

Bipolar silicon monolithic IC

Block Diagram



E89648-ST

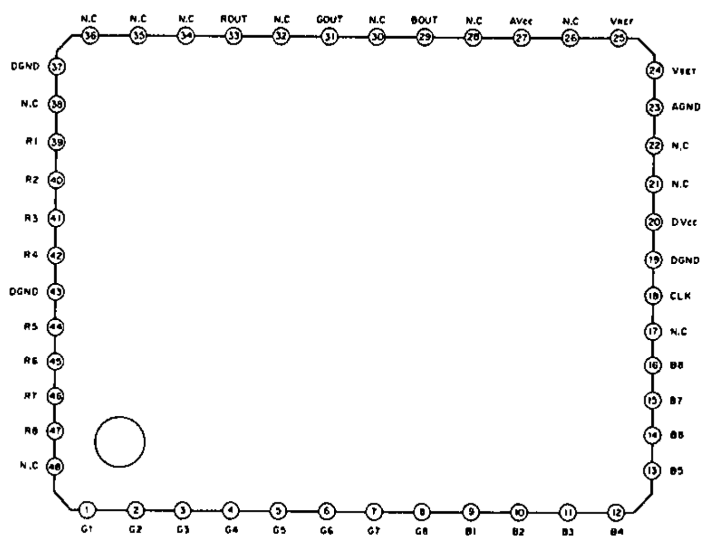
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	0 to 7	V
• Input voltage (digital)	VI	−0.3 to Vcc	V
	VCLK	−0.3 to Vcc	V
• Input voltage (VSET pin)	VSET	−0.3 to Vcc	V
• Output voltage (analog)	VOUT	Vcc−2.1 to Vcc	V
• Output current (analog)	IOUT	−3 to +10	mA
(VREF pin)	IREF	−5 to 0	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	0.7	W

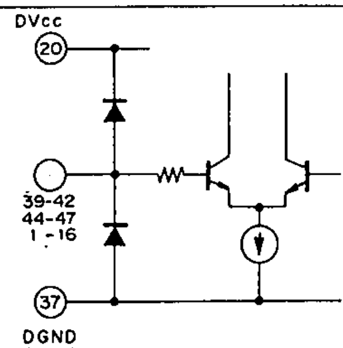
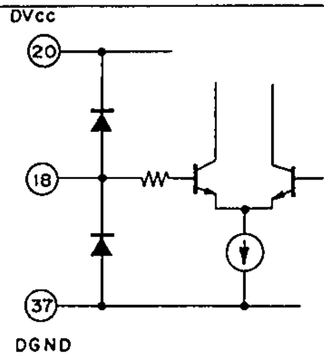
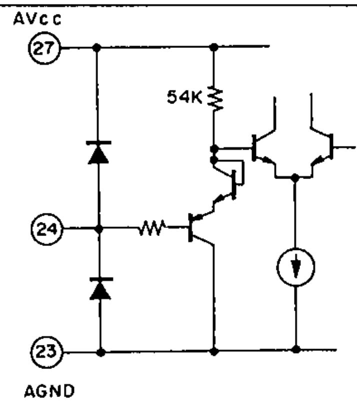
Recommended Operating Conditions

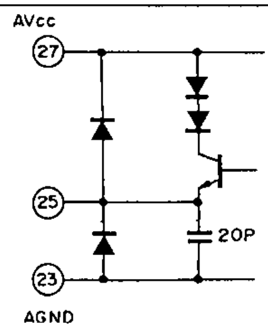
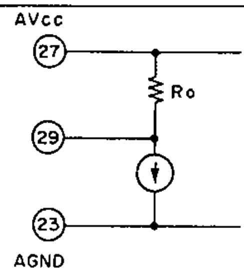
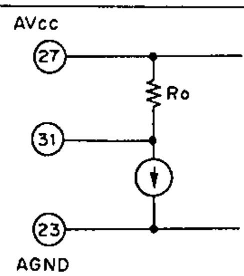
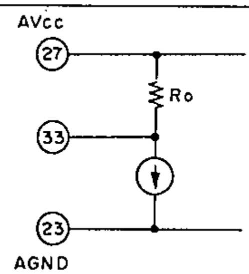
• Supply voltage	AVcc, DVcc	4.5 to 5.5	V
	AVcc–DVcc	−0.2 to +0.2	V
	AGND–DGND	−0.05 to +0.05	V
• Digital input voltage H level	VIH, VCLKH	2.0 to DVcc	V
L level	VIL, VCLKL	DGND to 0.8	V
• VSET input voltage	VSET	0.7 to 1.0	V
• VREF pin current	IREF	−3 to −0.4	mA
• Clock pulse width	Tpw1	15	ns
	Tpw0	10	ns

Pin Configuration (Top View)



Pin Description

No.	Symbol	Equivalent circuit	Description
39 to 42 44 to 47 1 to 16	R1 to R8 G1 to G8 B1 to B8		Digital input pin. From pins 39 to 42 and from 44 to 47 are for RED. R1 is MSB and R8 is LSB. From pins 1 to 8 are for GREEN. G1 is MSB and G8 is LSB. From pins 9 to 16 are for BLUE. B1 is MSB and B8 is LSB.
18	CLK		Clock input pin.
20	DVcc		Digital Vcc.
17 21 to 22	NC		Vacant pin (non-connection)
23	AGND		Analog GND.
24	VSET		Bias input pin. Normally, apply 0.87V. See "Note on use".

No.	Symbol	Equivalent circuit	Description
25	VREF		Internal reference voltage out-put pin 1.2V (typ) A pull-down resistance is necessary externally. See "Note on use".
26	NC		Vacant pin (non-connection)
27	AVcc		Analog Vcc
28	NC		Vacant pin but connect to AVcc*
29	BOUT		Analog output pin for BLUE.
30	NC		Vacant pin but connect to AVcc*
31	GOUT		Analog output pin for GREEN.
32	NC		Vacant pin but connect to AVcc*
33	ROUT		Analog output pin for RED.
34 to 36	NC		Vacant pin but connect to AVcc*
19 37 43	DGND		Digital GND
48	NC		Vacant pin (non-connection)

***Note)** Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AVcc.

Electrical Characteristics

Ta=25°C, $AV_{CC}=DV_{CC}=5.0V$, AGND=DGND=0.0V

Item			Symbol	Test condition	Min.	Typ.	Max.	Unit
Resolution			RSL			8		bit
Monotony			MNT			Guara-ntee		
Differential linearity error			DLE	$V_{SET}-AGND=0.87V$ $R_L>10k\Omega$ F.S.=Full-scale	−0.5		+0.5	LSB
Integral linearity error			ILE		−0.4		+0.4	% of F.S.
Maximum conversion speed			f_{MAX}	$V_{SET}-AGND=0.87V$ $R_L>10k\Omega$ $C_L<20pF$	35			MSPS
Full-scale output voltage*1			V_{OFS}		0.85	1.0	1.15	Vp-p
RGB output voltage full-scale ratio*2			FSR		0	4	8	%
Output zero offset voltage			Voffset		−40	−6	0	mV
Output resistance			Ro		270	340	420	Ω
Consumption current			I_D	$V_{SET}-AGND=0.87V$ $R_L>10k\Omega$ $I_{REF}=-400\mu A$	54	72	90	mA
Digital data input current	H level	Upper 2 bits	$I_{IH(U)}$	$V_I=DV_{CC}$		1.2	20	μA
		Lower 6 bits	$I_{IH(L)}$			0.6	10	μA
	L level	Upper 2 bits	$I_{IL(U)}$	$V_I=DGND$	−10	0	10	μA
		Lower 6 bits	$I_{IL(L)}$		−10	0	10	μA
Clock input current	H level		I_{CLKH}	$V_{CLK}=DV_{CC}$		3	30	μA
	L level		I_{CLKL}	$V_{CLK}=DGND$	−10	0	10	μA
V_{SET} input current			I_{SET}	$V_{SET}-AGND=0.87V$	−5	−0.3	0	μA
Internal reference voltage			V_{REF}	$I_{REF}=-400\mu A$	1.08	1.20	1.32	V
Set-up time			ts		12			ns
Hold time			th		3			ns

Note) *1. $AV_{CC}-V_O$

*2. Maximum value among

$$100\times\left|\frac{V_{OFS(R)}}{V_{OFS(G)}}-1\right|,\ 100\times\left|\frac{V_{OFS(G)}}{V_{OFS(B)}}-1\right|,\ \text{or}\ 100\times\left|\frac{V_{OFS(B)}}{V_{OFS(R)}}-1\right|$$

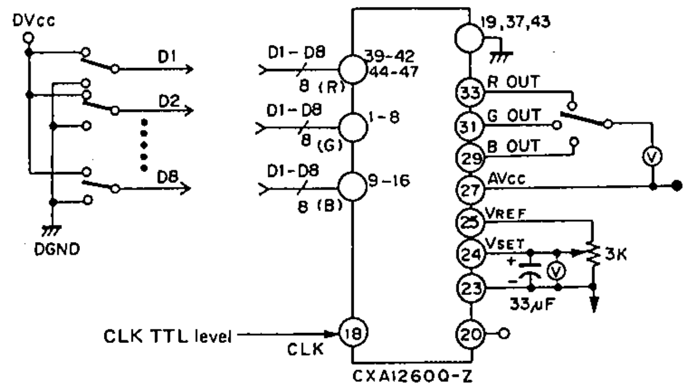
Input corresponding table

Input code	Output voltage
MSB LSB 1 1 1 1 1 1 1 1	Vcc+Voffset
· · ·	· · ·
1 0 0 0 0 0 0 0	Vcc+Voffset−0.5V
· · ·	· · ·
0 0 0 0 0 0 0 0	Vcc+Voffset−1.0V

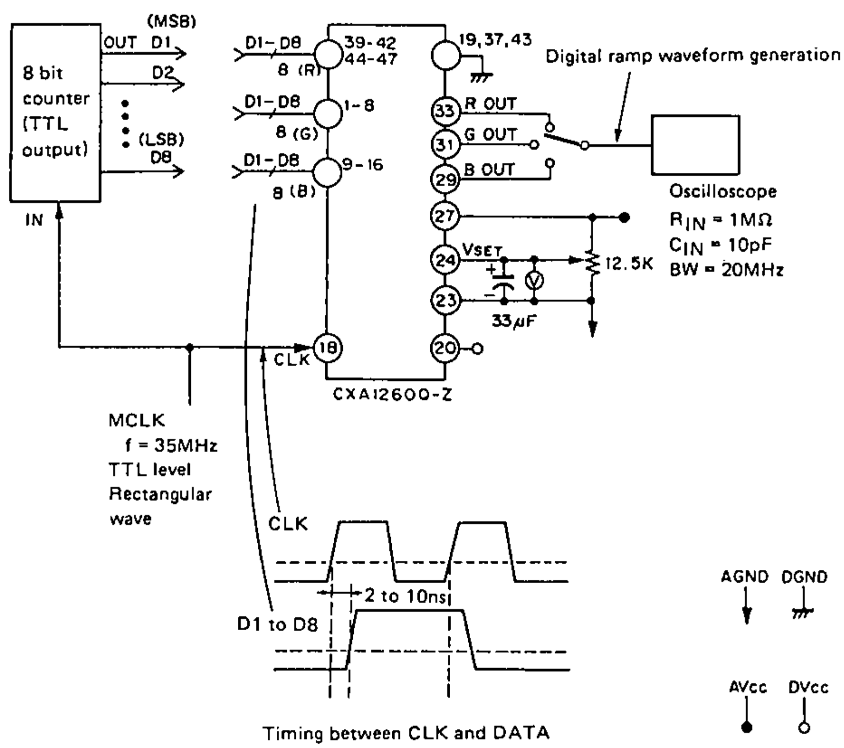
In case the output voltage full-scale is 1.00V. (1 LSB=3.92 mV)

Electrical Characteristics Test Circuit

Differential linearity and integral linearity test circuits



Maximum conversion speed test circuit



Output voltage full-scale precision, RGB output voltage full-scale ratio, and output zero offset voltage test circuits

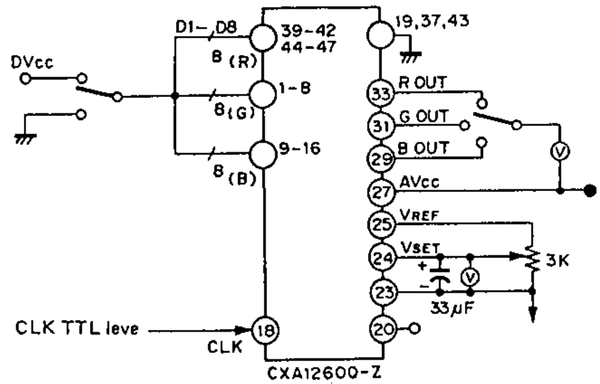
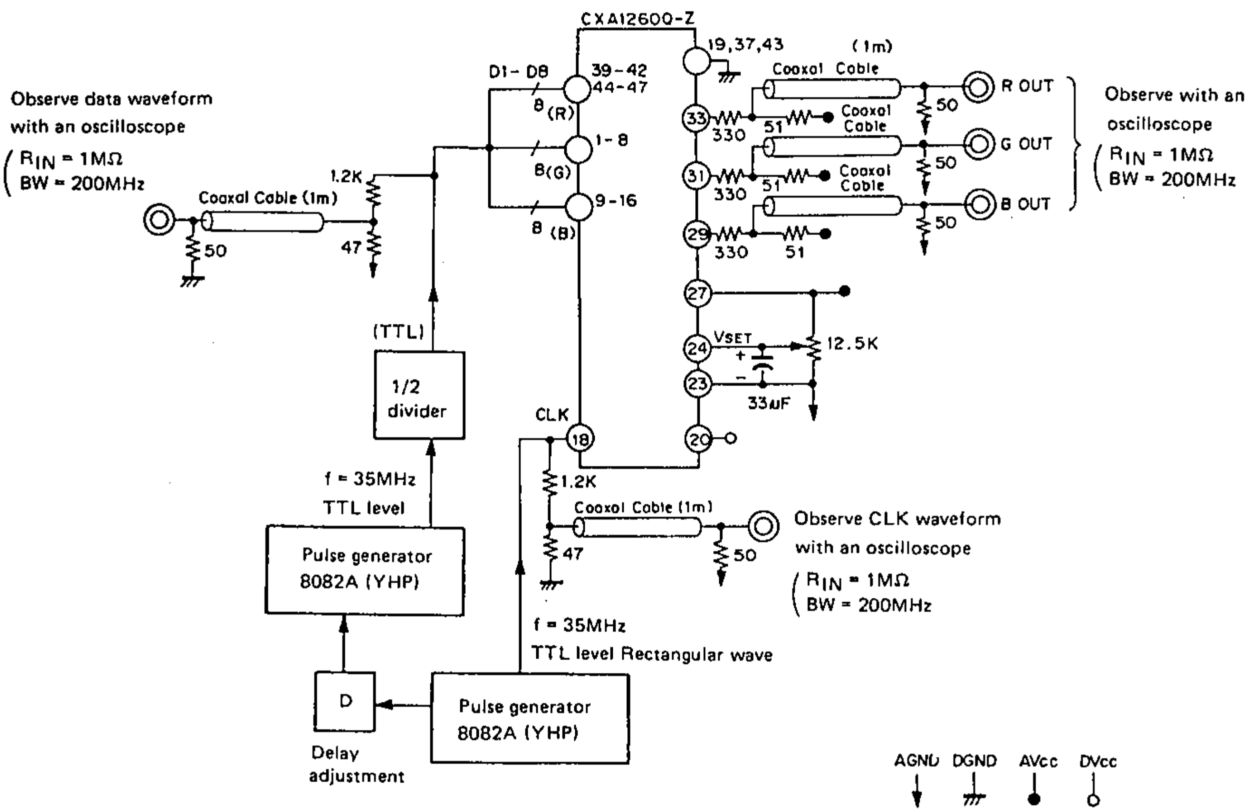


Fig. 1

Set-up time, hold time, and rise and fall time test circuits



Standard Circuit Design Data Ta=25°C, AV_{CC}=DV_{CC}=5.0V, AGND=DGND=0.0V

Item	Symbol	Measuring condition	Min.	Typ.	Max.	Unit
Crosstalk among R, G and B	CT	D/A OUT: 1Vp-p R_L>10kΩ C_L<20pF f_{DATA}=7MHz f_{CLK}=14MHz See Fig.2		−40	−35	dB
Glitch energy	GE	V_{SET}−AGND=0.87V R_L>10kΩ f_{CLK}=1MHz Digital ramp output See Fig.3*1		30		pV-s
Rise time*2	tr	V_{SET}−AGND=0.87V See Fig. 1.		5.5		ns
Fall time*2	tf			5.0		ns
Settling time	tset			16		ns

Note) *1. Observe the glitch which is generated when the digital input varies as follows:

0 0 1 1 1 1 1 1 — 0 1 0 0 0 0 0 0
0 1 1 1 1 1 1 1 — 1 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 — 1 1 0 0 0 0 0 0

*2. The time required for the D/A OUT to arrive at 90% of its final value from 10%.

Standard Circuit Design Data Test Circuit

Crosstalk among R, G and B test circuit

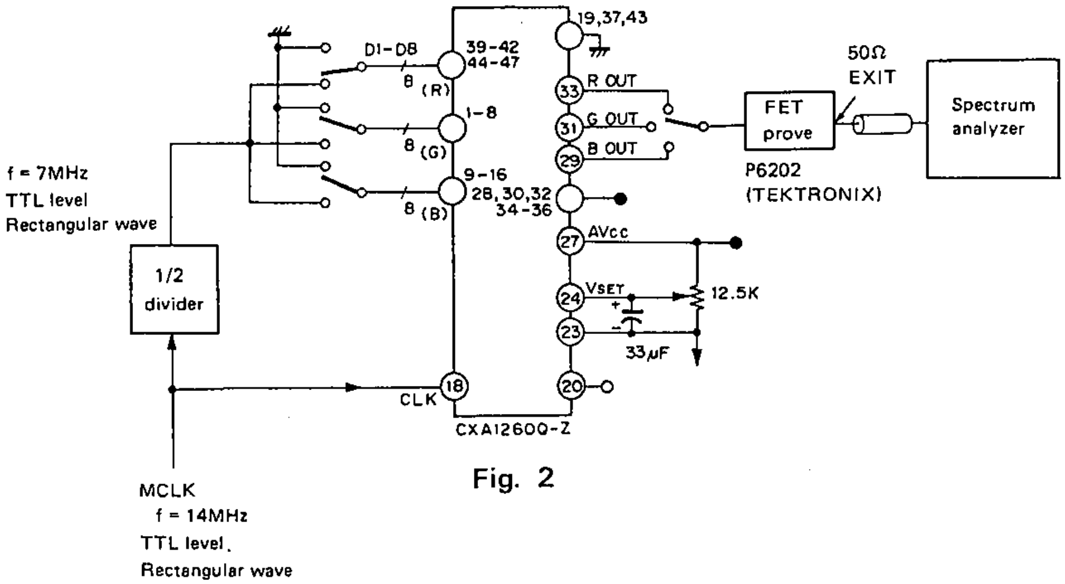


Fig. 2

[Measuring method]

In case the measuring crosstalk of G → R

1 Apply the data to G only and measure the power of the frequency component of the data at R OUT.

2 Apply the data to R only and measure the power of the frequency component of the data at R OUT.

3 Take the difference of the above two powers. The unit is in dB.

Glitch energy test circuit

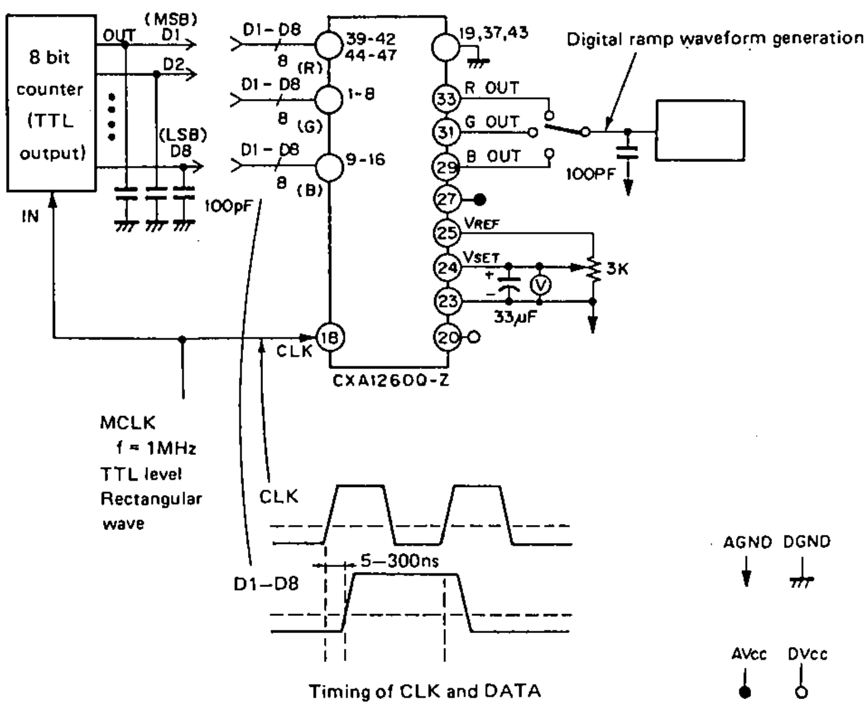
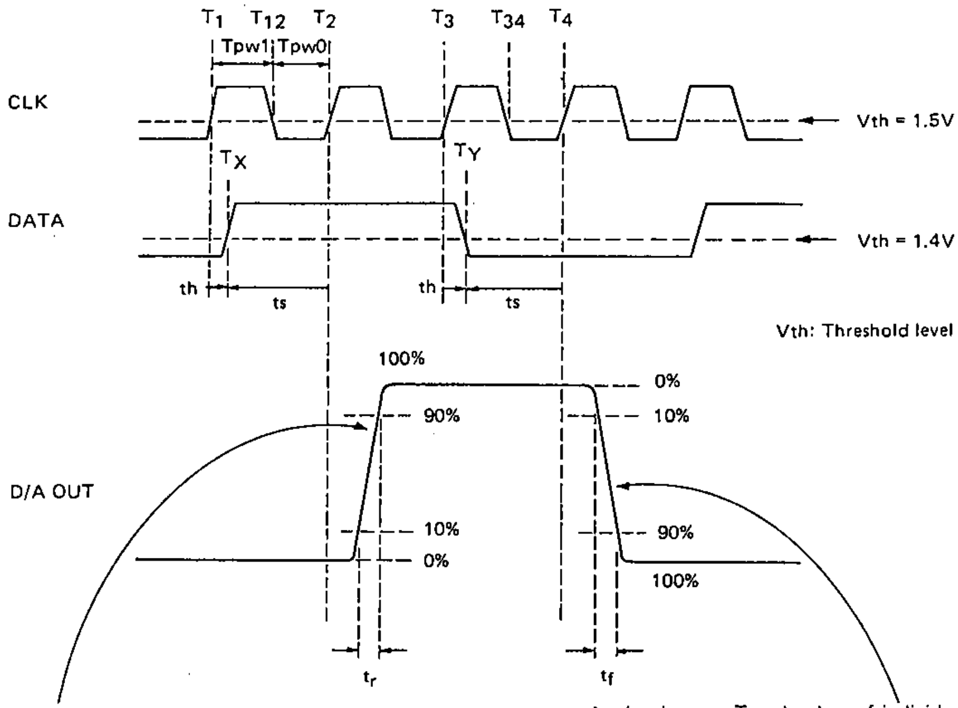


Fig. 3

Operation Description

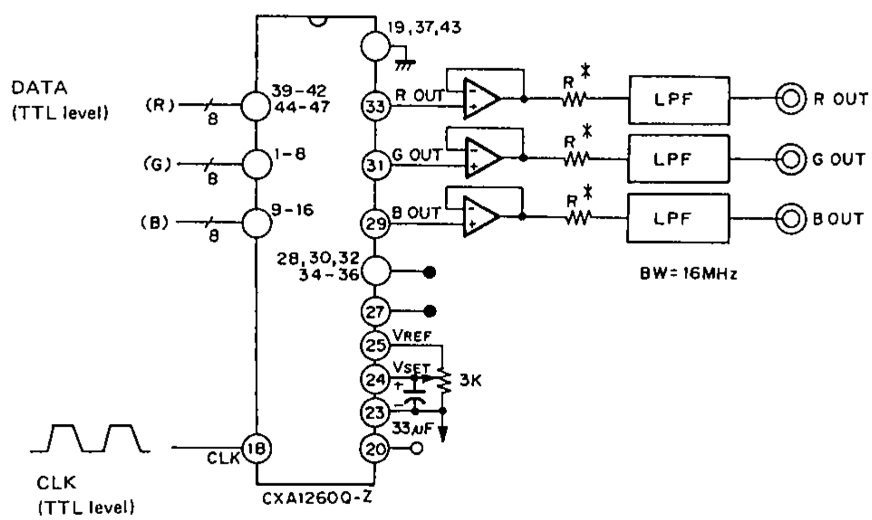
Timing chart



At the time t = T_X, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_2, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t = T_{12})).

At the time t = T_Y, the data of individual bits are switched and thereafter when the CLK becomes L → H at t = T_4, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK.
(In this case, fetching of the data is carried out at the fall of the CLK (at the time when t=T_4)).

Application Circuit



R* is matching resistance for LPF

AGND DGND AVcc DVcc

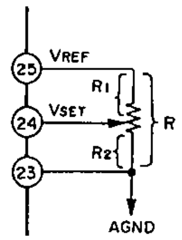
Note on Use

1. Setting of pin 24 (V_{SET})

   The full-scale of the D/A output voltage changes by applying voltage to pin 24 (V_{SET}). When load is connected to pin 25 (V_{REF}), DC volatage of 1.2V is issued and the said voltage is dropped to 0.87V by resistance division.

   When the 0.87V is applied to pin 24 (V_{SET}), the D/A output of 1 Vp-p can be obtained.

   (Example of use)



   Adjustment method

   1) The resistance R is determined in accordance with the recommended operating condition of I_{REF} (Current flowing through resistance R).
      See R vs. I_{REF} of Fig. 4. The calculation expression is as follows:
      $R = V_{REF}/I_{REF}$
   2) Adjust the volume so that the RGB output voltage full-scale becomes 1.0V.
      (At this point, it becomes R1:R2=2:5)

Resistance vs. V_{REF} pin current

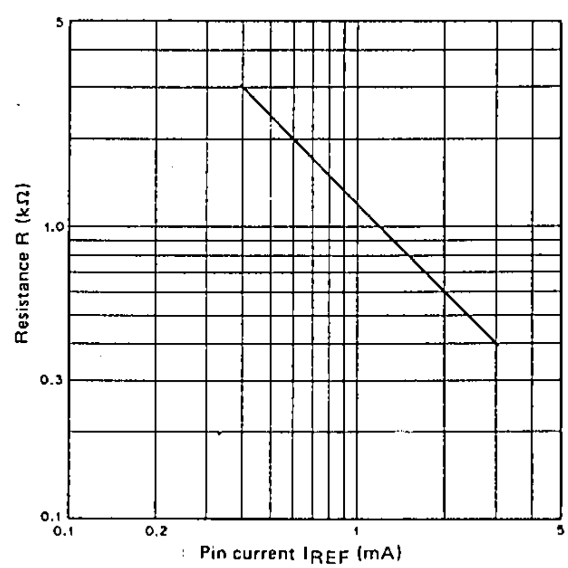


Fig. 4

2. Phase relationship between data and clock

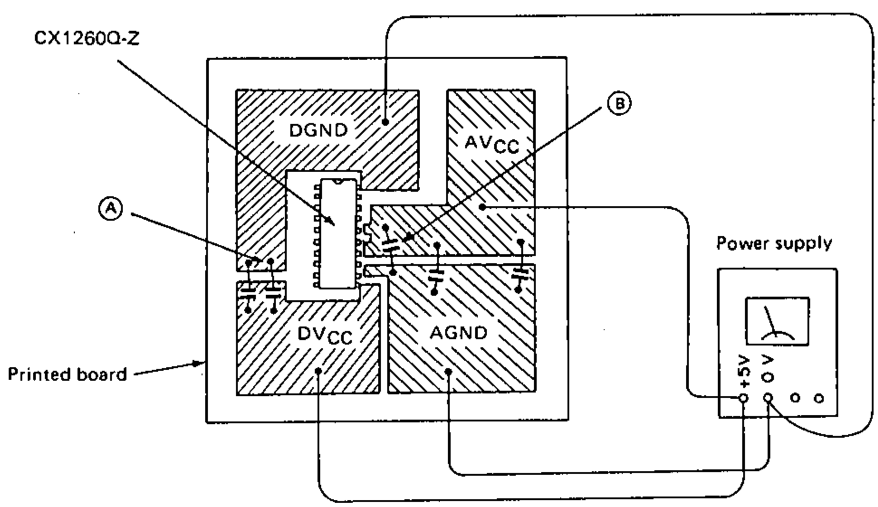
   In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.

   Satisfy the standard of the set-up time (ts) and hold time (th) indicated in the electrical characteristics. As to the meaning of ts and th, see the timing chart.

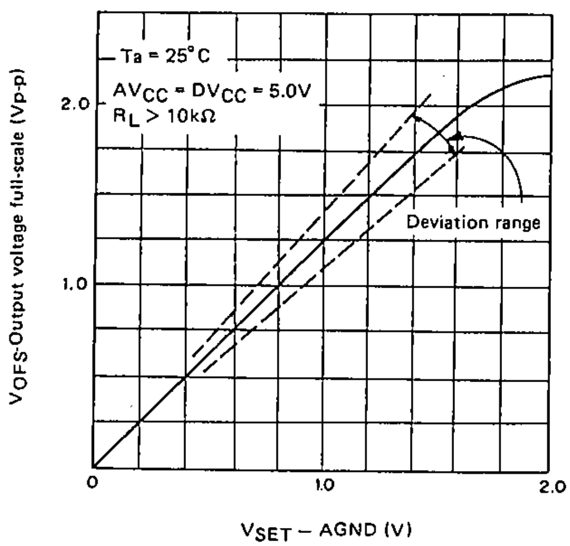
   Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

3. Regarding the load of D/A output pin
Receive the D/A output of the next stage with high impedance. In other words, perform so that it becomes as follows:
$R_L > 10\ k\Omega$
$C_L < 20\ pF$
The temperature characteristics indicated in the characteristics diagram has been measured under this condition.
However, when it is made to $R_L \leqq 10\ k\Omega$ the temperature characteristics may change considerably. In addition, when it is made to $C_L \geqq 20\ pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

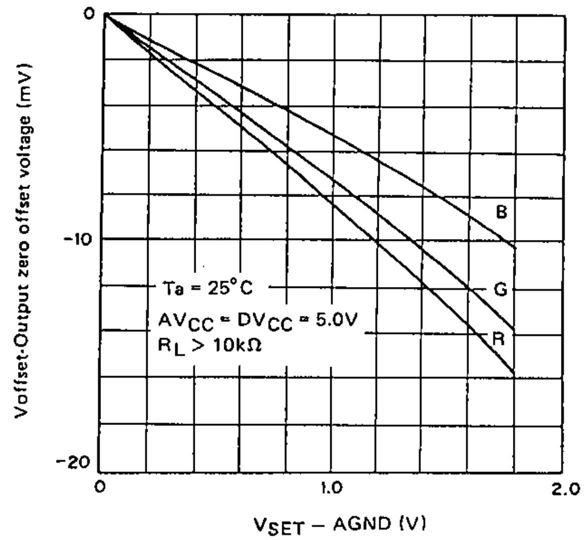
4. Noise reduction measures
As the D/A output voltage is a minute voltage of approximately 4 mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore use the items given below as reference.
- When mounting onto the printed board, allow as much space as possible to the ground surface and the Vcc surface on the board and reduce the parasitic inductance and resistance.
- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AVcc and DVcc. As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AVcc and DVcc be conducted separately, and then making AGND and DGND as also AVcc and DVcc in common right near the power supply respectively.
- Insert in parallel a 47 μF tantalum capacitor and a 1000 pF ceramic capacitor between the Vcc surface on the printed board and the nearmost ground surface. (A of diagram below). It is also desirable to insert the above between the Vcc surface near the pin of the IC and the ground surface. (B of diagram below). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.
- It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1 μF between pin 23 (AGND) and pin 24 (V_{SET}).



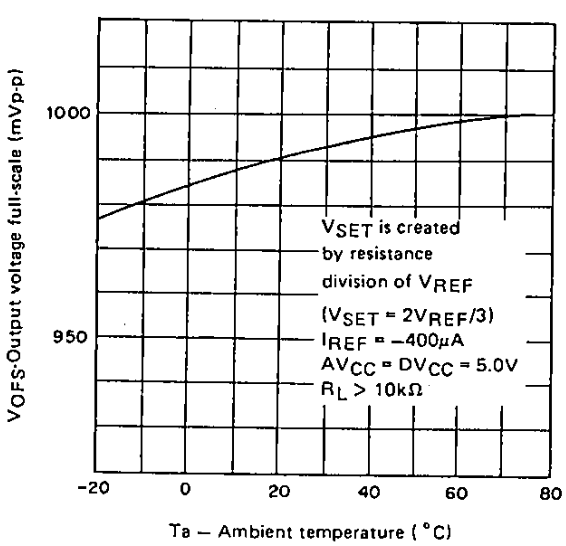
Output voltage full-scale vs. VSET—AGND



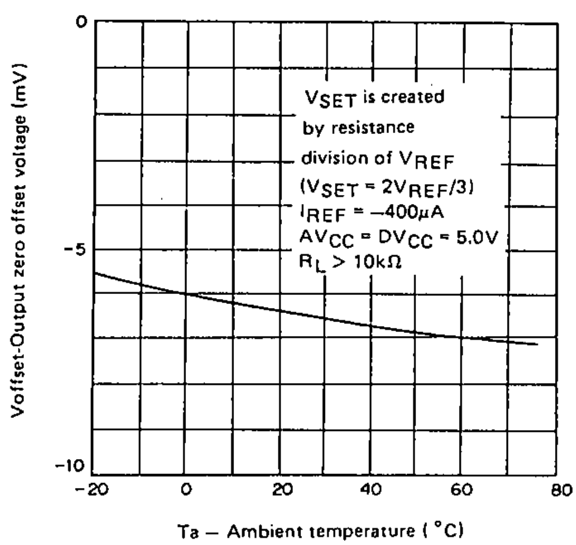
Output zero offset voltage vs. VSET—AGND



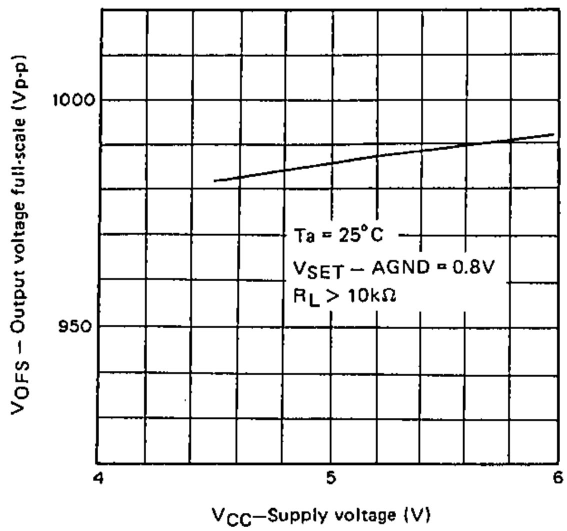
Output voltage full-scale vs. Ambient temperature



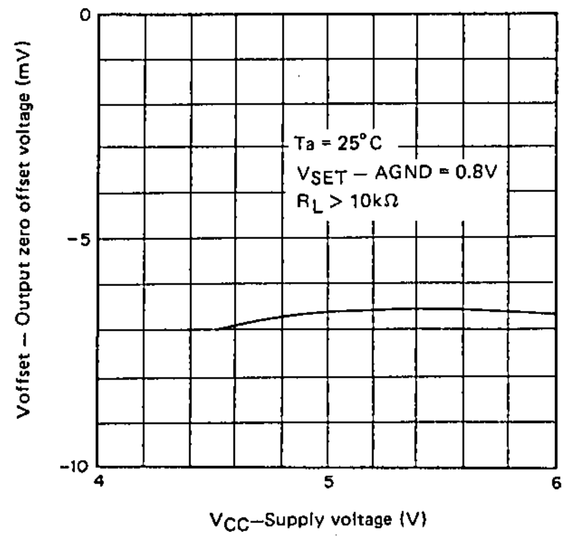
Output zero offset voltage vs. Ambient temperature



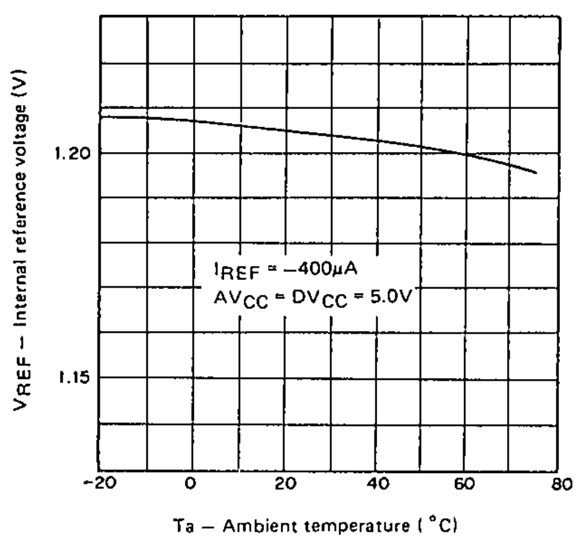
Output voltage full-scale vs. Supply voltage



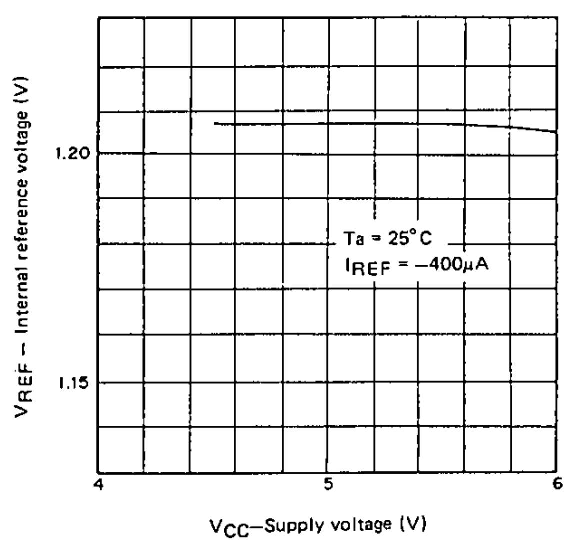
Output zero offset voltage vs. Supply voltage



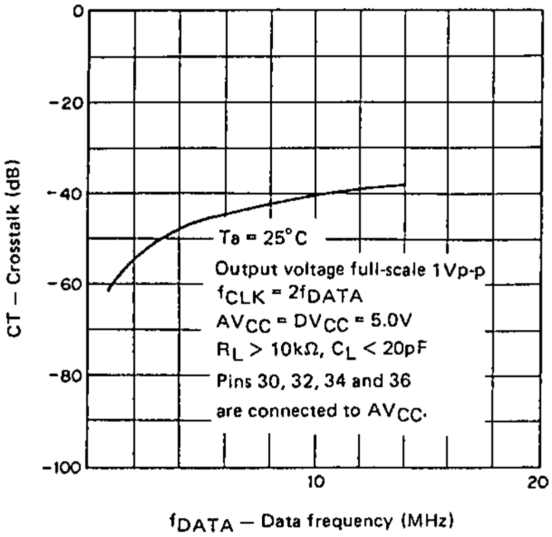
Internal reference voltage vs. Ambient temperature



Internal reference voltage vs. Supply voltage

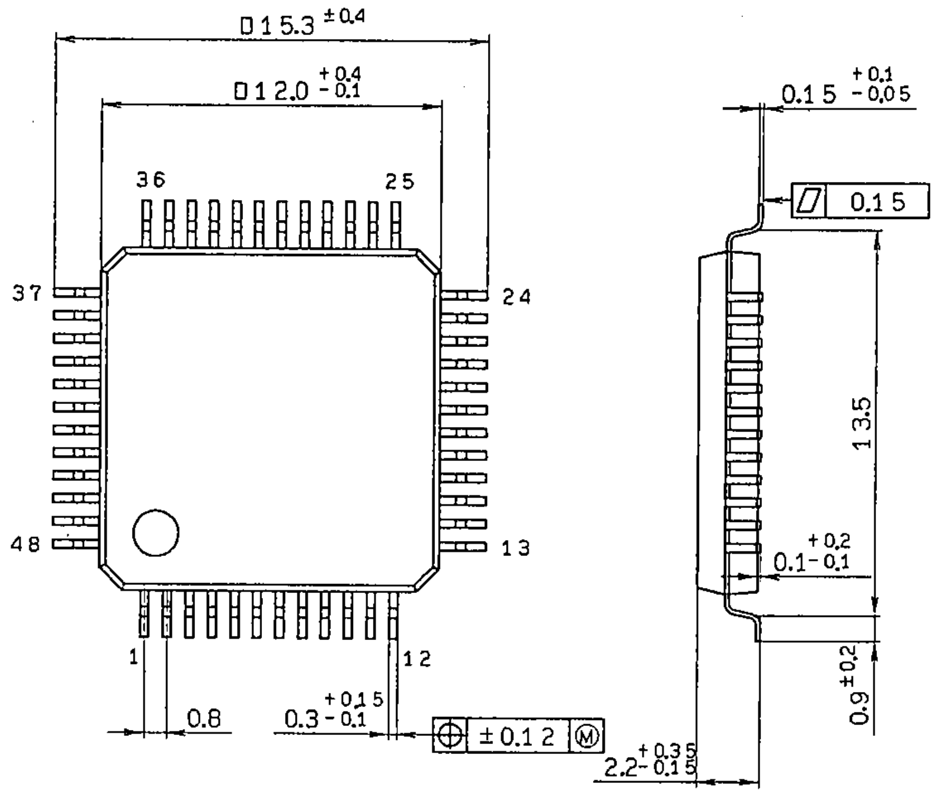


Crosstalk among R, G and B vs. Data frequency



Package Outline Unit: mm

48 pin QFP (Plastic) 0.6g



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