SONY CXA1218S/CXA1228S

NTSC/PAL Decoder

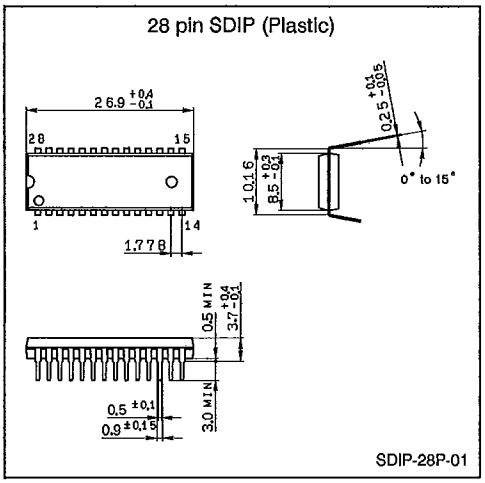
Description

CXA1218S and CXA1228S are decoder ICs used to convert composite video signals into color difference signals. They have signal outputs, such as composite sync, burst flag, subcarrier, and alternate signal outputs, necessary, for image processing. CXA1228S operates in both NTSC and PAL modes.

Ratio is R–Y : B–Y = 1.4 : 1.0 for CXA1218S
R–Y : B–Y = 1 : 1.27 for CXA1228S

Package Outline

Unit: mm



Features

- Single supply operation 5V
- Low power consumption (85 mW Typ.)
- Compatible with both NTSC and PAL modes
- Provides composite sync, burst flag, subcarrier, and line alternate signal output

Function

Synchronous separation, compostie sync output, burst flag output, ACC, ACK, APC, demodulator, DL amplifier, PAL ID, HUE control.

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

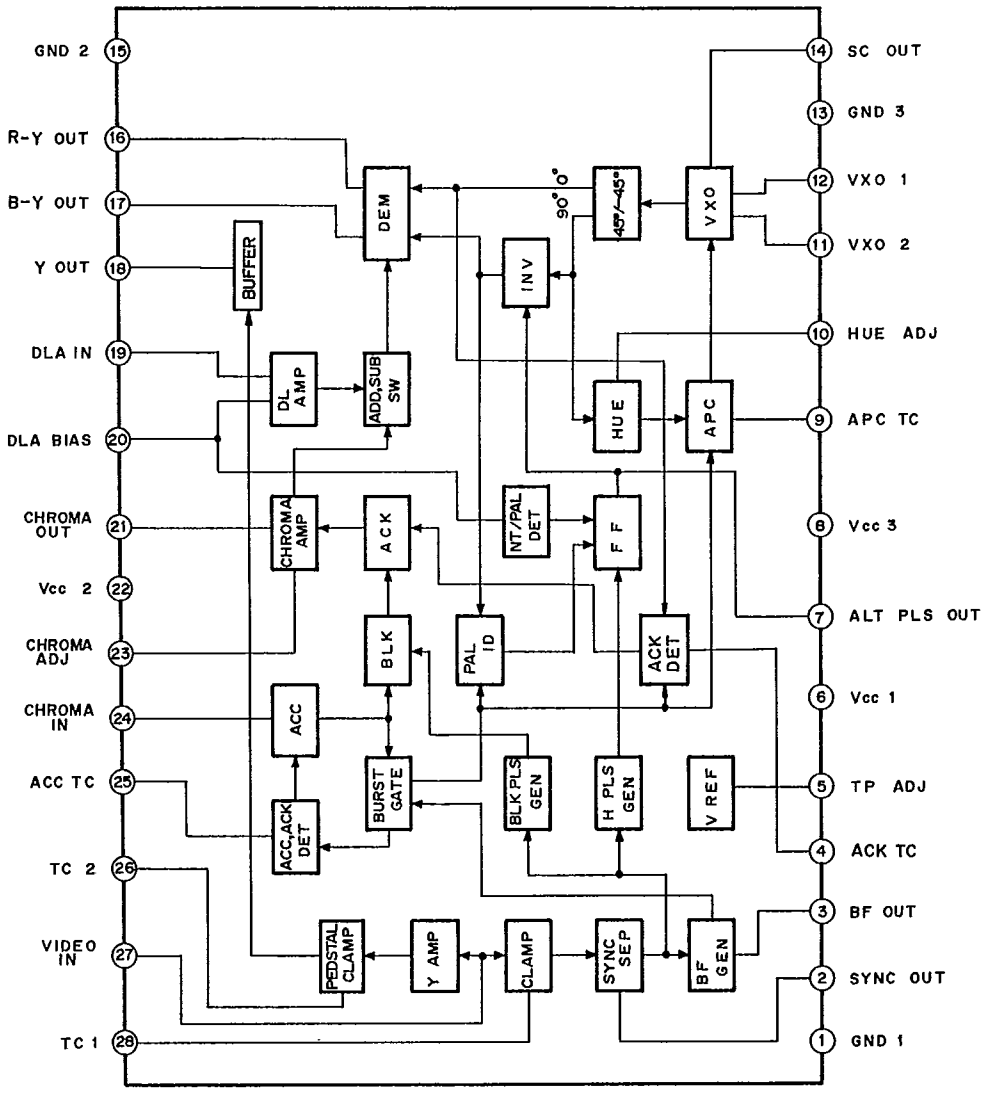
• Supply voltage	Vcc		10		V
• Operating temperature	Topr	–20	to	+75	°C
• Storage temperature	Tstg	–55	to	+150	°C
• Allowable power dissipation	PD		250		mW

Recommended Operating Condition

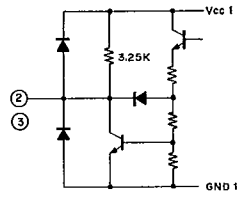
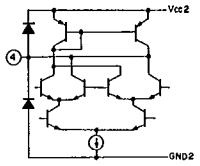
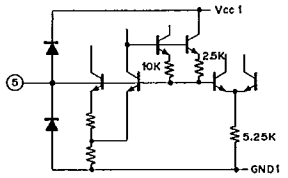
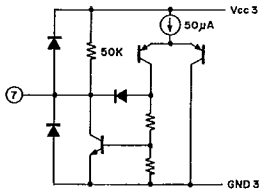
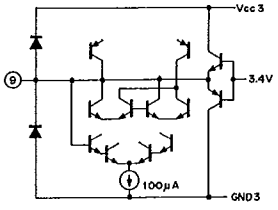
• Supply voltage	Vcc	5	±	0.25	V

80444-YA

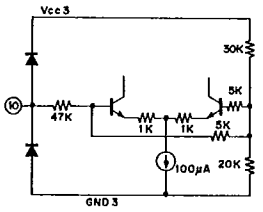
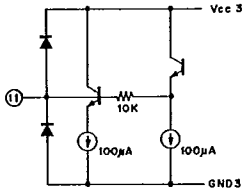
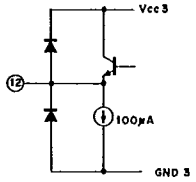
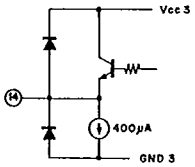
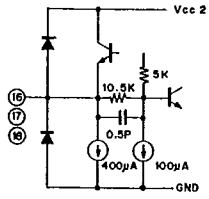
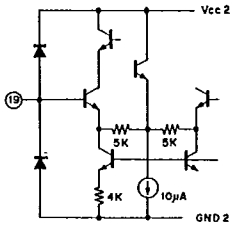
Block Diagram and Pin Configuration



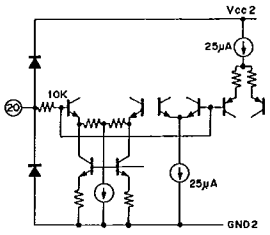
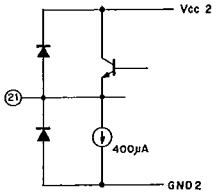
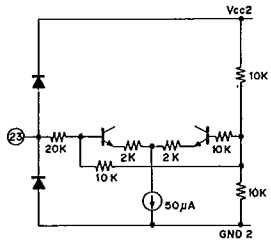
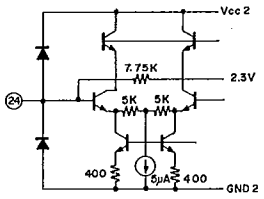
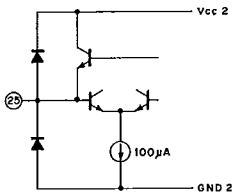
Pin Description

No.	Symbol	Voltage	Equivalent circuit	Description
1	GND 1	0V		GND pin of Y AMP and SYNC SEP.
2	SYNC OUT	H; 2.4V Min. L; 0.4V Max.		Composite Sync output pin (TTL level)
3	BF OUT			Burst flag output pin (TTL level)
4	ACK TC	3.1V Typ.		ACK (Auto Color killer) time constant pin
5	TP ADJ	1.23V Typ.		Burst flag positional adjusting pin By changing the current from this pin burst flag position adjustment to to (BF) = 5.6 μs can be performed.
6	Vcc 1	*5V		Supply pin of Y AMP and SYNC SEP.
7	ALT PLS OUT	H; 2.4V Min. L; 0.4V Max.		Line alternate pulse output pin NTSC mode; L PAL mode ; Alternate H and L every IH.
8	Vcc 3	*5V		Supply pin of APC, HUE, VXO and SYNC SEP.
9	APC TC	*3.4V		APC (Auto Phase Control) time constant and fo adjusting pin By varying the DC voltage to be applied to this pin, free running frequency of VXO adjustment can be performed.

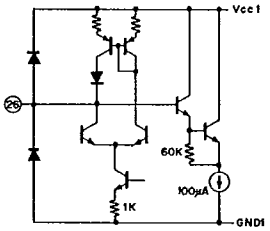
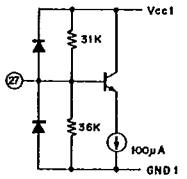
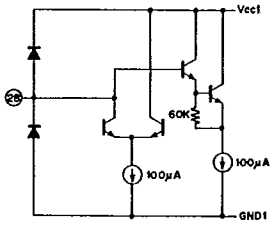
***Note)** External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
10	HUE ADJ	*2.0V		HUE adjusting pin By applying voltage 0 to 5V to this pin, HUE adjustment at over ±30° can be performed. Ground with a capacitor at PAL mode.
11	VXO 2	3.1V Typ.		X' tal oscillation pin
12	VXO 1	3.3V Typ.		X' tal oscillation pin
13	GND 3	0V		GND pin of APC, HUE and VXO.
14	SC OUT	1.8V Typ.		Sub carrier output pin
15	GND 2	0V		GND pin of demodulator and Y/C mixer.
16	R-Y OUT	2.0V Typ.		R-Y output pin
17	B-Y OUT			B-Y output pin
18	Y OUT	2.0V Typ.		Y output pin
19	DLA IN	*2.3V (PAL) *0V (NTSC)		DL amplifier input pin Ground at NTSC mode. Connect with IHDL output during PAL mode.

***Note)** External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
20	DLA BIAS	*2.3V (PAL) *0V (NTSC)		NTSC/PAL mode switching and DL amplifier gain adjusting pin. NTSC/PAL mode selection and DL amplifier gain adjustment in PAL mode are effected through application of voltage to this pin. $V_{20} \leq 0.8V$; NTSC mode $2.0V \leq V_{20} \leq 2.8V$; PAL mode Variable range over ±3dB
21	CHROMA OUT	3.7V Typ.		Chroma output pin Connect to Vcc 2 at NTSC mode. Connect to IHDL input at PAL mode.
22	Vcc 2	*5V		Supply pin of demodulator and Y/C mixer.
23	CHROMA ADJ	2.5V Typ.		Chroma amplifier gain adjusting pin Chroma amplifier adjustment can be performed by applying volage to this pin. $V_{23} \leq 0.8V$; B/W (Free run) mode $2.0V \leq V_{23} \leq 3.2V$; Color mode. Variable range –20 to 0dB.
24	CHROMA IN	2.3V Typ.		Chroma signal input pin Typical input level is burst amplitude 143mVp-p.
25	ACC TC			ACC (Auto Color Control) time constant pin

***Note)** External apply voltage.

No.	Symbol	Voltage	Equivalent circuit	Description
26	TC 2			Pedestal clamp time constant pin
27	VIDEO IN	2.7V Typ.		Video signal (luminance + sync signal) input pin Standard input level is 0.36 Vp-p.
28	TC 1			Feed back clamp time constant pin for SYNC SEP.

Electrical Characteristics

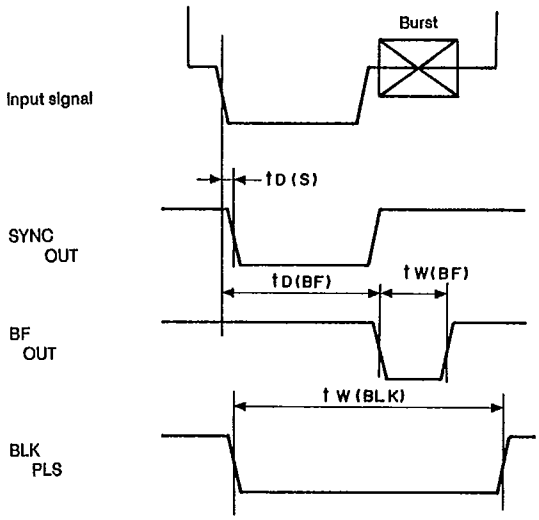
(See the Electrical Characteristics Test Circuit.)
Ta = 25°C, Vcc = 5V

Test item		Symbol	Condition	Input signal V	Input signal C	Test point	Min.	Typ.	Max.	Unit
Consumption current 1		Icc1	Chroma input no signal PAL mode	2	–	6	3.45	4.55	6.70	mA
Consumption current 2		Icc2				22	5.48	7.24	10.65	mA
Consumption current 3		Icc3				8	3.13	4.13	6.07	mA
Video amplifier voltage gain		$V_{O(Y)}$	V_{AC}=0.1Vp-p f=100kHz V_{DC}=0.125V Refer to test method detail-1	1	–	18	9 (11.5)	10 (12.5)	11 (13.5)	dB
Video amplifier frequency characteristics		$f_{O(Y)}$	Input frequency of –3dB with 100kHz output taken as 0dB	1	–	18	5.0			MHz
Video amplifier maximum output		$V_{OM(Y)}$	V_{AC}=0.32Vp-p f=100kHz V_{DC}=0.16V	1	–	18	0.7 (1.0)			Vp-p
Demodulation output DC voltage		$E_{O(R-Y)}$	Chroma input no signal	2	–	16	1.4	2.0	2.7	V
		$E_{O(B-Y)}$				17	1.4	2.0	2.7	
Video output pedestal voltage		$E_{O(Y)}$				18	1.6	2.0	2.3	
Color difference demodulation output voltage		$E_{O(R-Y)}$	Refer to test method detail-2	3	5/7	16	1.4 (1.0)			Vp-p
		$E_{O(B-Y)}$				17	1.0 (1.27)			
Demodulating output residual carrier		$CL_{(R-Y)}$	Chroma input no signal 3.58MHz component	2	–	16			40	mVp-p
		$CL_{(B-Y)}$				17				
ACC characteristics 1		ACC1	$ACC1 = \frac{Voc\ (Vin=-20dB)}{Voc\ (Vin=0dB)}$	3	5/7	21	–5.0	–2.0		dB
ACC characteristics 2		ACC2	$ACC2 = \frac{Voc(Vin=+6dB)}{Voc(Vin=0dB)}$	3	5/7	21		+1.0	+3.0	dB
Color killer level		ek	Chroma input level during color killer operation	3	5/7	24	–44	–38	–32	dB
APC pulling range		fp		2	6/8	14	±300			Hz
Synchronizing output	H level	$V_{OH(S)}$		2	–	2	2.4			V
	L level	$V_{OL(S)}$							0.4	
	Delay time	$t_{D(S)}$					0.4	0.5	0.6	μs
Burst flag output	H level	$V_{OH(BF)}$		2	–	3	2.4			V
	L level	$V_{OL(BF)}$		2	–	3			0.4	V
	Pulse width	$t_{W(BF)}$	when adjust to $t_{D(bf)}$=5.6μs	2	–	3	2.2	2.4	2.6	μs
Blanking pulse width		$t_{W(BLK)}$		2	4	18	9.0	10.0	11.0	μs
Sub carrier output voltage		$V_{O(SC)}$		3	5/7	14	400	500		mVp-p
Alternate pulse output	H level	$V_{OH(ALT)}$	PAL mode	3	5/7	7	2.4			V
	L level	$V_{OL(ALT)}$							0.4	

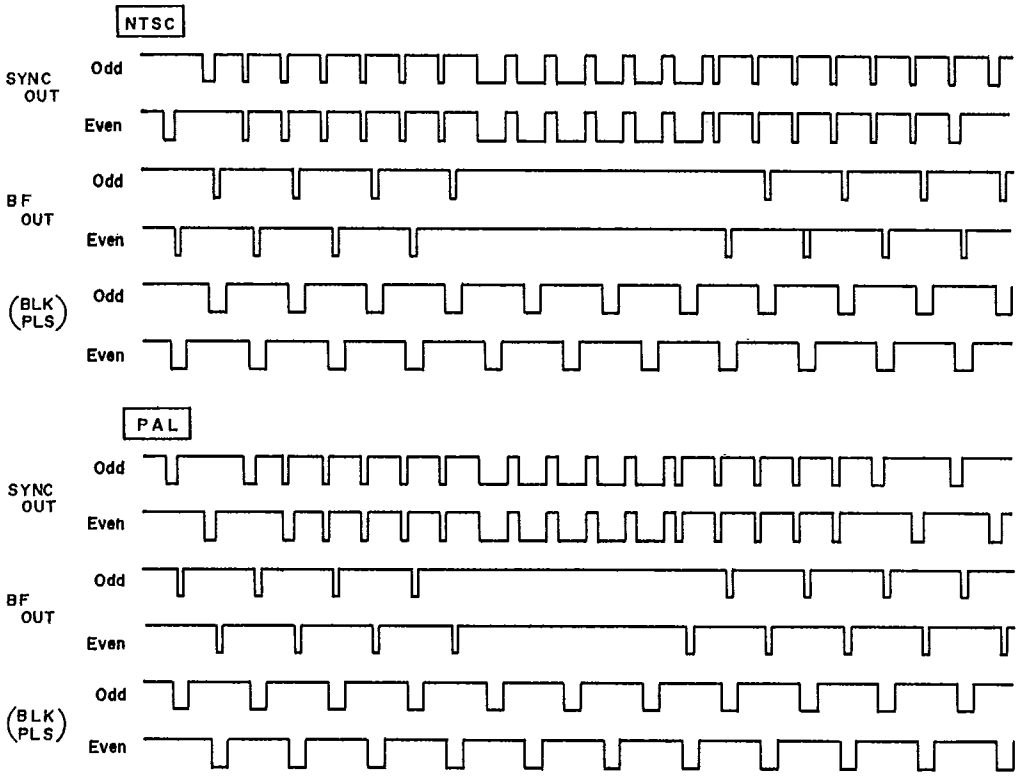
Note) The values in the parentheses are for CXA1228S.

Synchronous Timing Chart

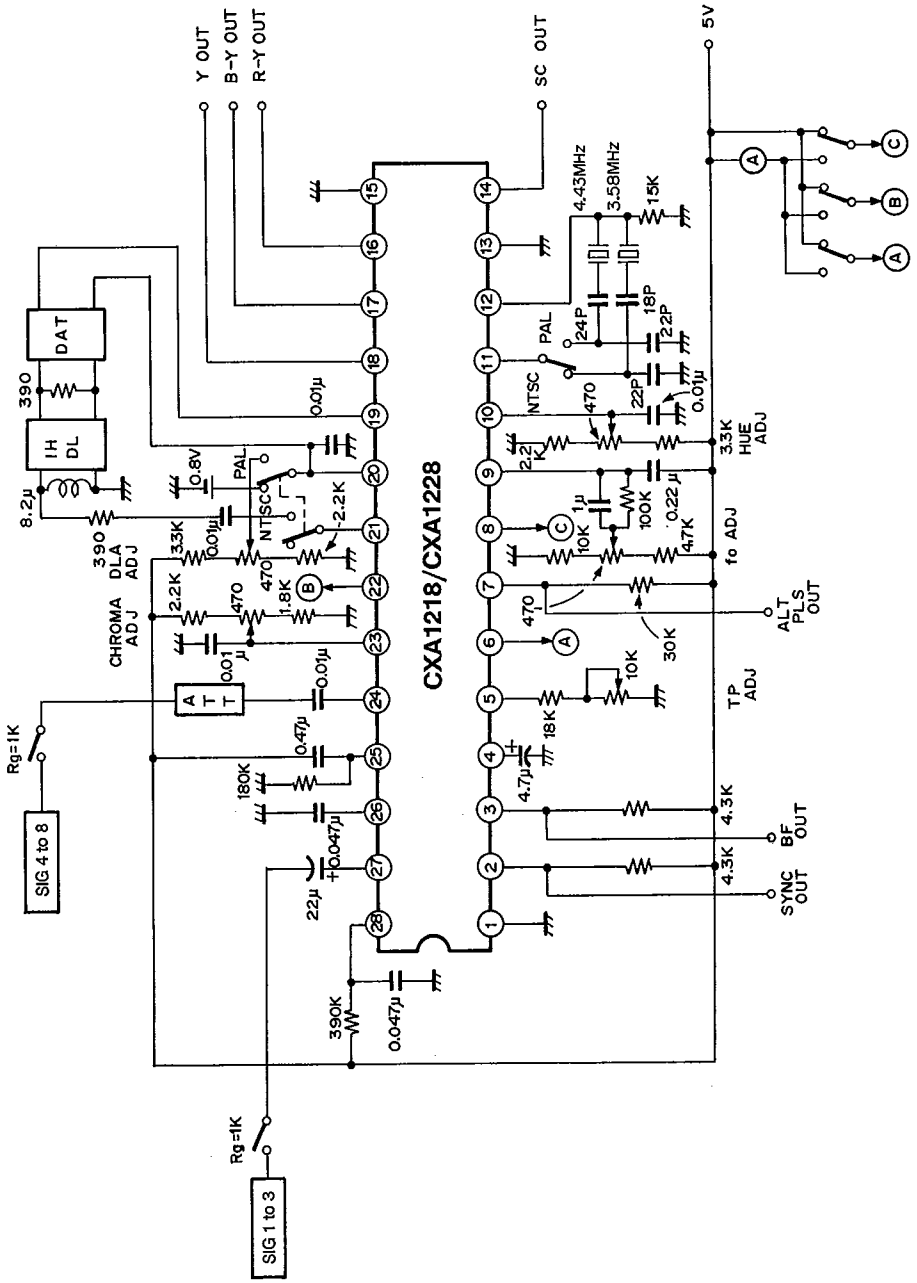
H Synchronizing



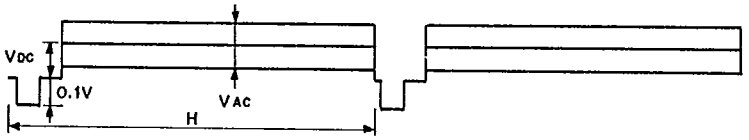
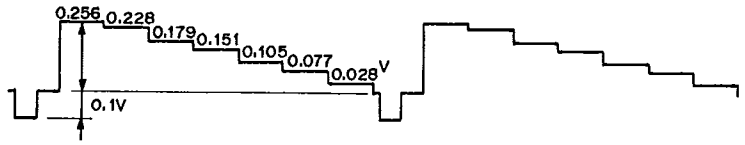
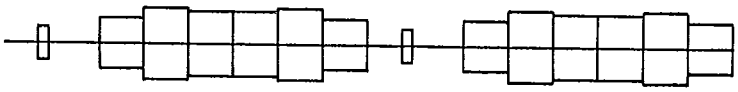
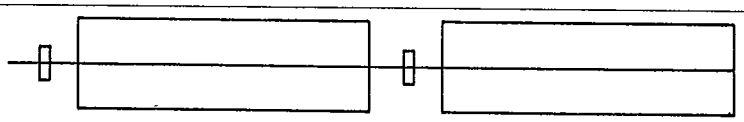
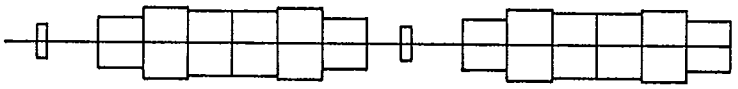
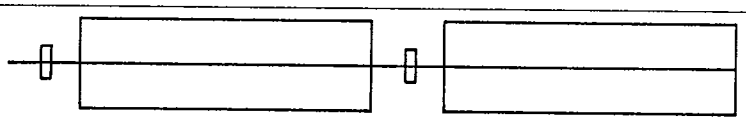
V Synchronizing



Electrical Characteristics Test Circuit

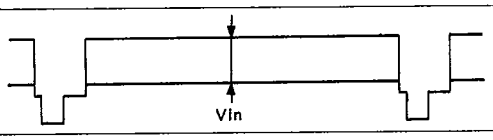
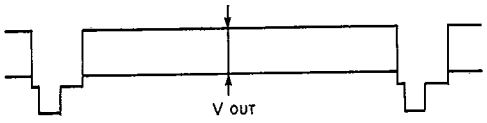


Input signal

V	SIG 1	
	SIG 2	
	SIG 3	
C	SIG 4	Sine wave Frequency 3.579545 MHz Amplitude 143 mVp-p
	SIG 5	 Amplitude 143 320 451 422 422 451 320 mVp-p Phase 180 168 284 241 61 104 348 deg Frequency 3.579545 MHz
	SIG 6	 Amplitude 143 436 mVp-p Phase 180 0 deg Frequency 3.579545 MHz ±300 Hz
	SIG 7	 Amplitude 143 320 451 422 422 451 320 143 320 451 422 422 451 320 mVp-p Phase 135 168 284 241 61 104 348 225 192 76 119 299 256 12 deg Frequency 4.433619 MHz
	SIG 8	 Amplitude 143 436 143 436 mVp-p Phase 135 0 225 0 deg Frequency 4.433619 MHz ±300 Hz

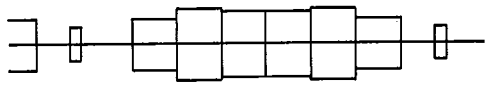
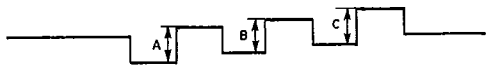
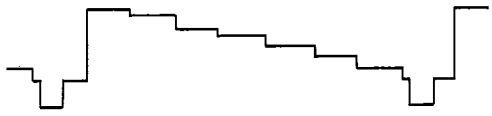
Details of Test Method

1. Video amplifier voltage gain

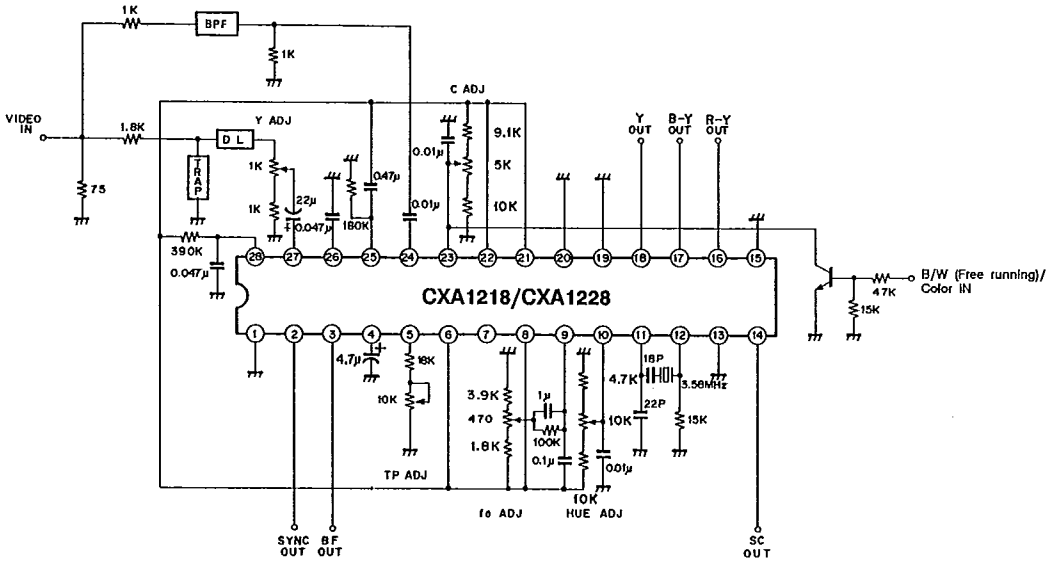
Input waveform	VIDEO IN	
	CHROMA IN	No signal input
Output waveform	Y OUT	

$$Gv = 20 \log \frac{Vout}{Vin} \quad (dB)$$

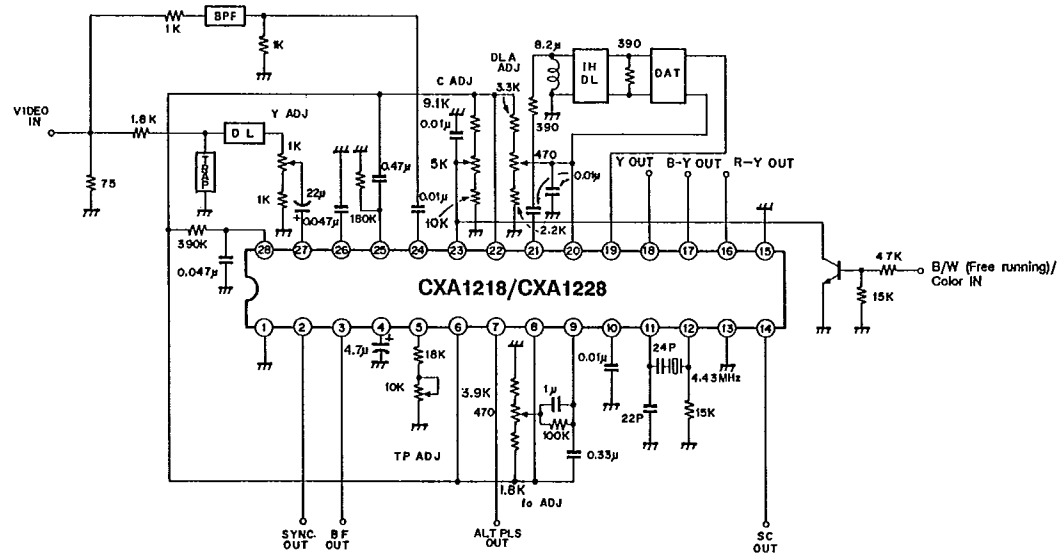
2. Primitive output voltage

Input waveform	VIDEO IN	
	CHROMA IN	
Output waveform	R-Y OUT	
	B-Y OUT	
	Y OUT	

Application Circuit (NTSC mode)



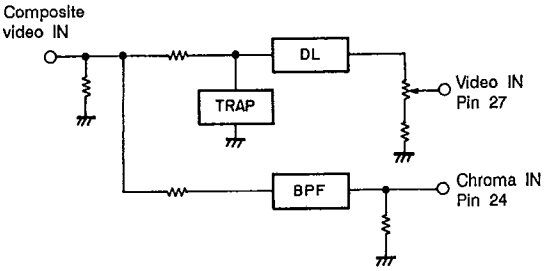
Application Circuit (PAL mode)



Applications

1. Input signals

Composite video signal input is separated into video signal (Y) and chroma signal (C) by band-pass filter, trap and delay line, Y is input to Pin 27 and C to Pin 24. While composite video signal is input at 1 Vp-p, the typical levels of the input signals are as shown in the table below.



		CXA1218S	CXA1228S
Composite video input (Synchronous negative polarity)		1.0Vp-p	1.0Vp-p
Video input	Luminance	0.256Vp-p	0.189Vp-p
	Sync	0.103Vp-p	0.076Vp-p
Chroma input	Burst	0.143Vp-p	0.143Vp-p

2. Time pulse adjustment

BF (Burst Flag) pulse positional adjustment can be performed by changing the current to be taken out from Pin 5. Setting t_D (BF) at 5.6 μs by this adjustment results in that BF pulse width is set at approx. 2.4 μs and BLK (blanking) pulse width at 10 μs.

3. Monochrome (free-running)/color mode switching

If Pin 23 (CHROMA ADJ) is set to H ($\geq$2.0 V), the color mode is established. Input chroma signal will be decoded and output in the form of color difference signal. If Pin 23 is set to L ($\leq$0.8V), the monochrome (free-running) mode is established and the APC circuit is made to stop. As a result, VXO oscillates in the free-running mode.

4. NTSC/PAL mode switching

Setting Pin 20 (DL A BIAS) to H ($\geq$2.0V), establishes the PAL mode, and setting the pin to L ($\leq$0.8V).

5. Chroma output

Chroma signal subjected to ACC and blanking is output at Pin 21 (CHROMA OUT). Output amplitude is approx. 160mVp-p with typical input (75% color bar).
In the PAL mode, this output is to be input to 1 H DL. In the NTSC mode, connect Pin 21 to the power supply (Vcc).

6. DL (Delay Line) AMP

An amplifier for insertion of 1 H DL and matching loss compensation when in the PAL mode. Its gain is variable within 14 $\pm$ 4 dB to absorb DL dispersion.
Its input pin is Pin 19 (DL A IN); apply to this pin a bias voltage of the same potential as with Pin 20 (DL A BIAS). The signal having passed through 1 H DL is to be input to Pin 19 after adjusted at the delay adjusting transformer (DAT) so that the delay time is 1 H (64 μs).

In the NTSC mode, this amplifier is not used; set the levels of Pins 19 and 20 at L ($\leq$0.8V).

7. VXO and APC
Pin 9 (APC TC) a time constant pin for APC. In the monochrome (free-running) mode in which the APC circuit does not operate, the free-running frequency depends on the DC voltage across this pin. VXO can operate either for NTSC or PAL by changing the quartz oscillator and series capacity.

8. Adjustment procedure
Input signal : 100% color bar

[NTSC mode]

1) BF positional adjustment
Adjust the resistance between Pin 5 and GND so that BF position to = 5.6 μs.
2) Video amplifier level adjustment
Adjust Y ADJ so that Y output white peak (100% white) is of 0.714 Vp-p.
3) fo adjustment
Establish the monochrome (free-running) mode, and adjust fo ADJ so that oscillation frequency (output subcarrier) frequency is fsc.
4) Hue adjustment
Establish the color mode, and adjust HUE ADJ so that output amplitudes A, B and C are all equal.
5) Chroma level adjustment
CXA1218S: Adjust C ADJ so that the maximum amplitude of output B-Y is 1.0 Vp-p.
CXA1228S: Adjust C ADJ so that the maximum amplitude of output B-Y is 1.27 Vp-p.

[PAL mode]

1) BF positional adjustment ..... Same as with NTSC mode.
2) Video amplifier level adjustment .. Same as with NTSC mode.
3) fo adjustment ..... Same as with NTSC mode.
4) DL amplifier adjustment
Establish the color mode, and adjust DLA ADJ so that the R output amplitude is the same for any adjacent two H intervals.
5) Chroma level adjustment
CXA1218S: Adjust C ADJ so that the maximum amplitude of output B-Y is 1.0 Vp-p.
CXA1228S: Adjust C ADJ so that the maximum amplitude of output B-Y is 1.27 Vp-p.

Description of Operation

1. Sync separation system
   The sync separation system clamps the sync tip of the video signal having been input from Pin 27 to separate the sync signal from the input video signal. Sync pulses are then processed to form BF, H, and BLK pulses, which are supplied to subsequent circuits. Of these pulses, sync and BF pulses are output at Pins 2 and 3, respectively, after transformed to TTL level via buffer.

2. Luminance signal regeneration system
   Video signal input from Pin 27 has its pedestal clamped, and amplified by the Y amplifier.

3. ACC system
   The burst component of the chroma signal having been input from Pin 24 is detected at ACC DET. Feedback to ACC AMP occurs depending on the detected output so that the burst level is kept constant.

4. APC system
   After the signal level is brought to the fixed value at ACC AMP, the burst component alone goes into the APC circuit via the BURST GATE circuit. Meanwhile, a 0° carrier and a 90° carrier are formed from VXO output, and the 90° carrier goes into APC via the HUE circuit. At APC, phase comparison is carried out between the 90° carrier and the input burst, and feedback to VXO is performed so that the phase difference is 90°. The 0° and 90° carriers thus formed are supplied to B-Y DEM and R-Y DEM, respectively. Therefore, demodulation axis can be changed by rotating the phase of the 90° carrier at the HUE circuit.

5. Color signal regeneration system
   1) NTSC system
      The chroma signal amplified at ACC AMP is amplified again at CHROMA AMP, then demodulated at B-Y DEM and R-Y DEM, and output at Pins 16 and 17 in the form of color difference signal.

   2) PAL system
      Processing is the same as with the NTSC system up to CHROMA AMP.
      The chroma signal output at Pin 21 goes into DL AMP at Pin 19 via 1 H DL and DAT, and then input to the ADD/SUB circuit after level-controlled. At the ADD/SUB circuit, the signal is subjected to addition and subtraction with respect to the original signal. The signals obtained by addition and subtraction are input to B-Y DEM and R-Y DEM, and demodulated by the 0° carrier and the 90° carrier inverted every H. After that, the signal is output in the form of color difference signal as with the NTSC system.

6. PAL ID
   The PAL signal is transmitted with its R-Y component inverted every H. It is therefore necessary to inverse the demodulation axis every H. In this IC, the 90° carrier is inverted in synchronization with H BLK pulses, and checking for correspondence with the input burst is performed by synchronous detection. If an error is detected, feedback to FF (Flip Flop) is performed for correction.