

Quadrature Modulator for 900 MHz-Band Mobile Communications

For the availability of this product, please contact the sales office.

Description

The CXA1852N is an IC package that combines a $\pi/2$ phase shifter with a quadrature modulator. This is suitable for 900 MHz digital cordless telephone (CT2) and digital cellular.

Features

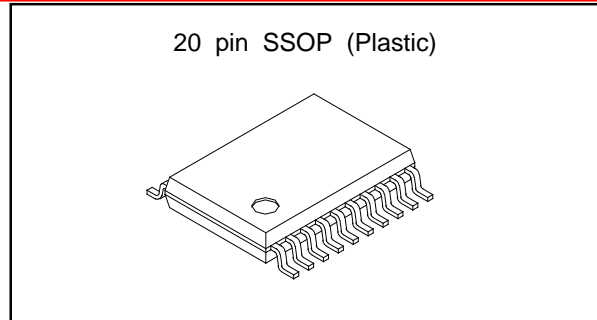
- Quadrature modulator IC has a built-in $\pi/2$ phase shifter.
- Local frequency = 300.1 MHz (max.); I&Q = 36 kHz (max.)
- Small phase error
- Operating voltage range: 2.7 to 5 V
- Power saving function
- 20-pin SSOP package used for set size reduction

Applications

- CT2 digital cordless telephone
- Digital cellular

Structure

Bipolar silicon monolithic IC



Absolute Maximum Ratings (Ta=25 °C)

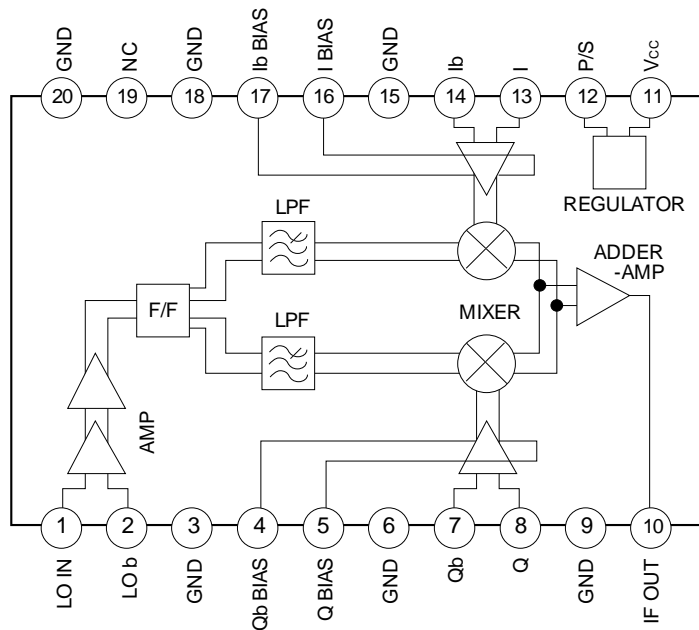
• Supply voltage	V _{cc}	6	V
• Operating temperature	T _{opr}	-20 to +70	°C
• Storage temperature	T _{stg}	-65 to +150	°C
• Allowable power dissipation	P _d	530*	mW

*When mounted on a 50 × 50 × 1.6 mm copper-foiled glass epoxy board

Recommended Operating Conditions

• Supply voltage	V _{cc}	2.7±5.0	V
------------------	-----------------	---------	---

Block Diagram and Pin Configuration



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Pin Description

Pin No.	Symbol	Typical pin voltage (V)	Equivalent circuit	Description
1	LOCAL IN	0		Local input pin. The internal resistor provides 50 Ω matching.
2	$\overline{\text{LOCAL IN}}$	*2.0		Bias pin for the local input amplifier. Ground this pin via a capacitor.
3	GND	0		
4	$\overline{\text{Q-BIAS}}$	*0.175		Local leak level adjustment pins. Normally ground these pins via 1 kΩ resistors.
5	Q-BIAS	*0.175		
6	GND	0		
7	$\overline{\text{Q-INPU}}$	*1.85 V to 0.85 V		Q signal input pin. The input impedance is 500 kΩ or more. (Only DC signals can be normally input at the $V_{cc}/2$ DC Bias.)
8	Q-INPUT	*1.85 V to 0.85 V		Q signal input pin. The input impedance is 500kΩ or more. (Signals of up to 1 Vp-p can be input at the $V_{cc}/2$ DC Bias.)
9	GND	0		
10	IF OUTPUT	*1.4		IF output pin. (An output impedance of 50 Ω is provided by the emitter follower.)

Pin No.	Symbol	Typical pin voltage (V)	Equivalent circuit	Description
11	Vcc	5.5 to 2.7		Power supply pin.
12	POWER SAVE	0 to 5.5		Power saving control pin. OFF when $V_{P/S} \leq 1.0$ V; ON when $V_{P/S} \geq 1.8$ V
13	I-INPUT	*0.85 to 1.85		I signal input pin. The input impedance is 500 k Ω or more. (Signals of up to 1 V _{p-p} can be input at the V _{cc} /2 DC Bias.)
14	I-INPUT	*0.85 to 1.85		I signal input pin. The input impedance is 500 k Ω or more (Only DC signals can be normally input at the V _{cc} /2 DC Bias.)
15	GND	0		
16	I-BIAS	*0.175		Local leak level adjustment pin. Normally ground this pin via a 1 k Ω resistor.
17	I-BIAS	*0.175		
18	GND	0		
19	N.C	—		
20	GND	0		

Electrical Characteristics

(Ta=25 °C, V_{CC}=2.7 V, Z_L=Z_S=50 Ω)*

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I _{CC}	For no signal input	10	15.0	22	mA
Standby current consumption	I _{CC} (PS)	PS		330	480	μA
IF output power	P _{out}	50 Ω load, f=f _{LO} /2+f _{I/Q}	-15	-11	-7.0	dBm
Lo carrier leak	ISO (Lo)	f _{I/Q} =36 kHz, 1 V _{p-p} , f _{out} =f _{LO} /2	26	35.0		dBc
Lo leak level	P _{LO}	I/Q=V _{CC} /2, f _{out} =f _{LO} /2		-49.0	-37	dBm
Image rejection (side-band leak)	ImR	f _{out} =f _{LO} /2-f _{I/Q}	28.5	37.5		dBc
I/Q input impedance	Z _{I/Q}		500			kΩ
Power saving response time	Rise	T _{P/S} (RISE)		1.0	5.0	μs
	Fall	T _{P/S} (DOWN)		1.0	3.0	μs
Power saving control voltage		V _{P/S} (ON)	1.8		5.5	V
		V _{P/S} (OFF)			1.0	V
Lo input level	L _{oin}		-17		-7	dBm

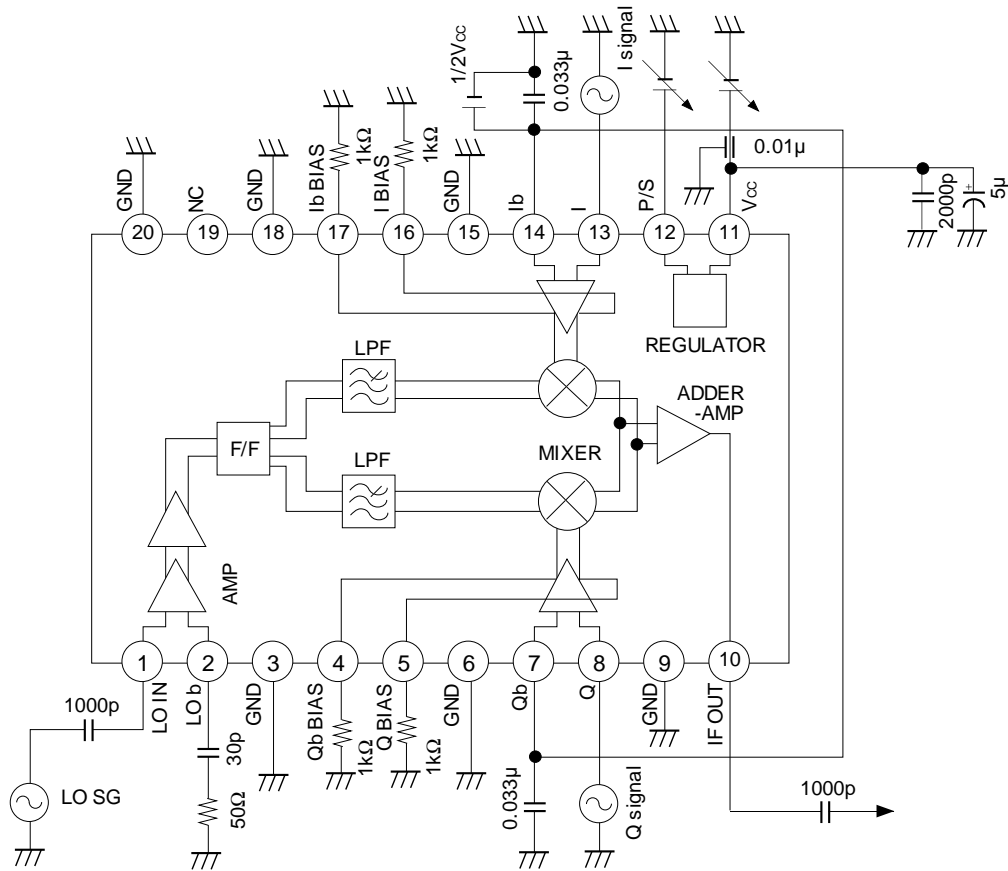
Design Reference Values

(Ta=25 °C, V_{CC}=2.7 V, Z_L=Z_S=50 Ω)*

Item	Symbol	Conditions	Typ.	Unit
I/Q third-order intermodulation distortion	IM _{3I/Q}	f _{out} =f _{LO} /2-3f _{I/Q}	37.3	dBc
Lo input VSWR			1.1	X:1
IF output VSWR			1.2	X:1

* f_{LO}=300.1 MHz Pin=-10 dBm
 f_{I/Q}=36 kHz 1 V_{p-p} DC=V_{CC}/2

Electrical Characteristics Test Circuit

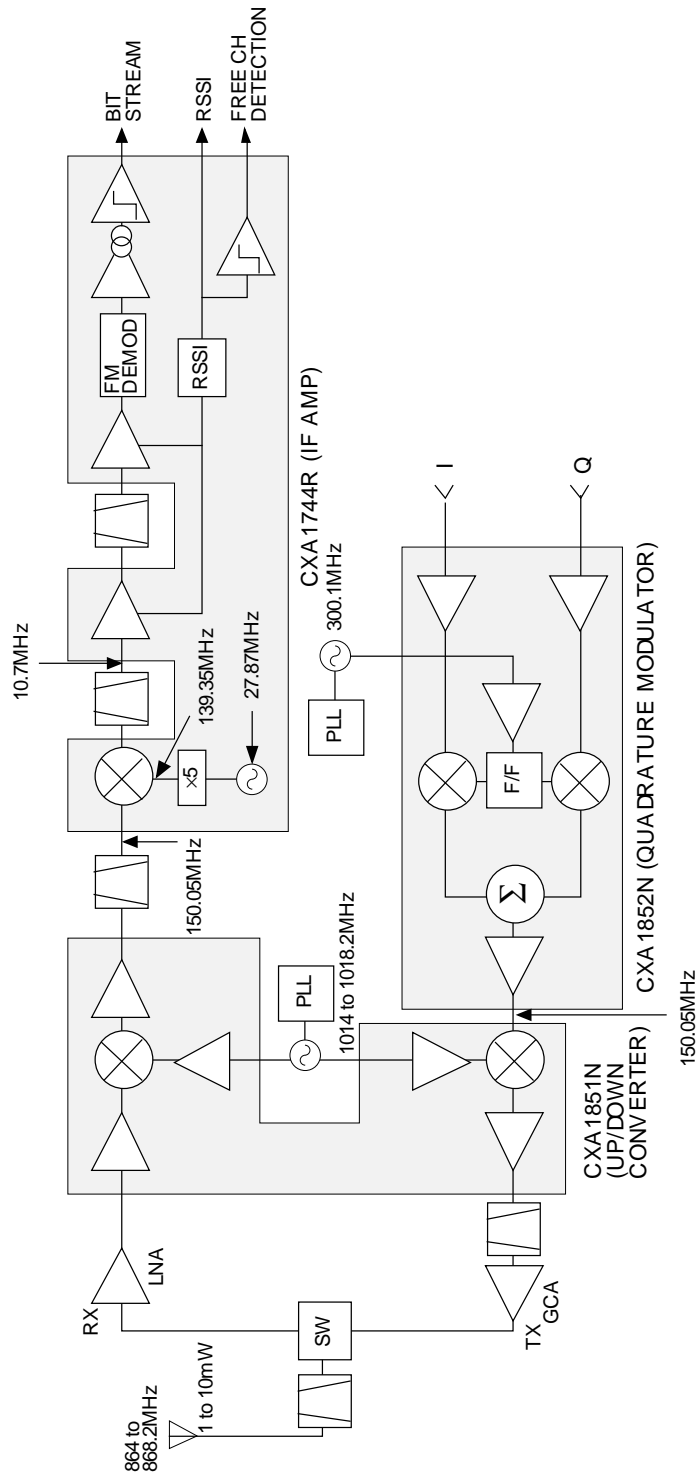


Signal	Frequency	Input level	Remarks
Lo	300.1 MHz	-10 dBm	
I signal	36 kHz	1 Vp-p	I/O phase difference = 90 °C
Q signal	35 kHz	1 Vp-p	DC for measuring the local leak

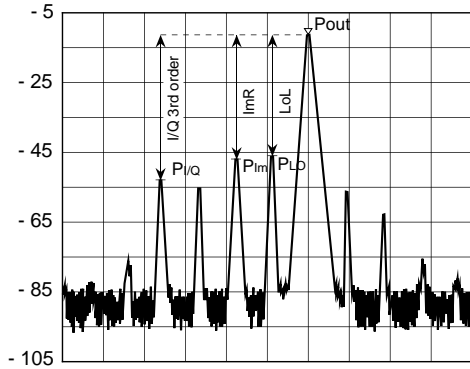
$V_{CC}=V_{P/S}$	2.7 to 5.5 V
$V_I=V_{Ib}=V_Q=V_{Qb}$	$0.5 \times V_{CC}$

Block Diagram

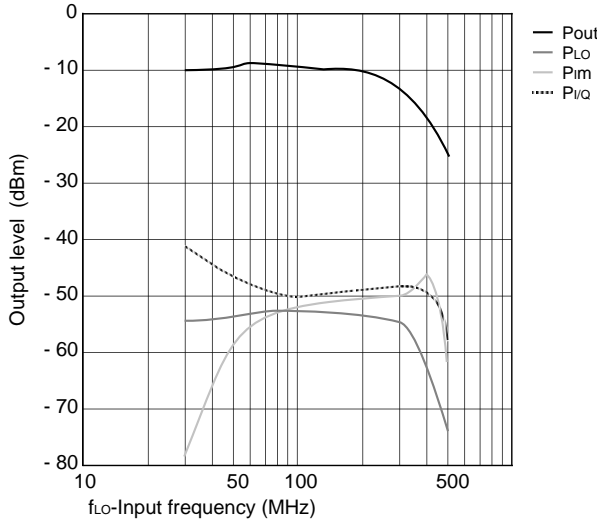
Digital cordless telephone chip set (CXA1744R/CXA1851N/CXA1852N)



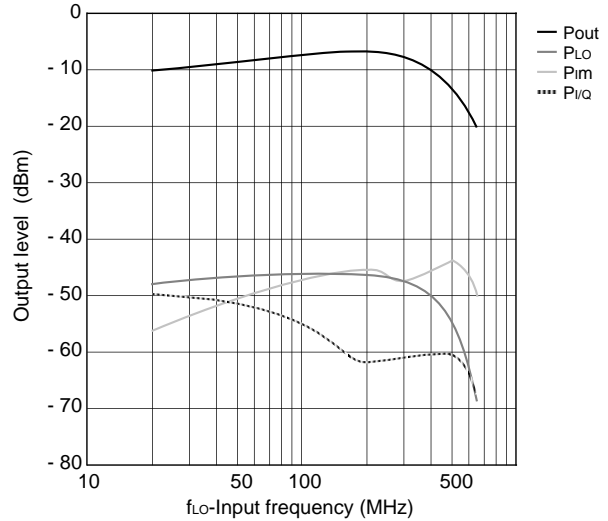
Modulation spectrum ($V_{CC}=2.7V$, S.P.A. measurement)



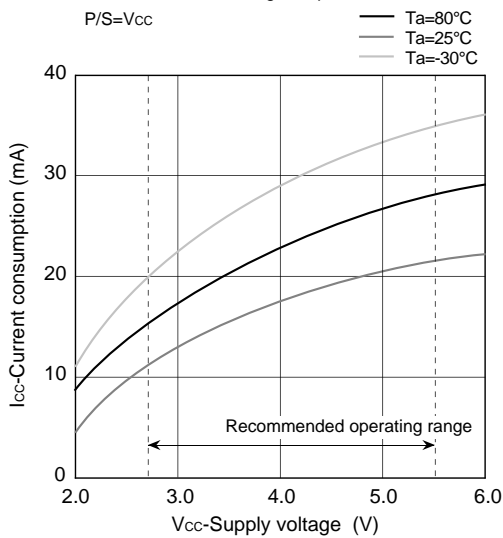
f_{LO} vs. P_{out} , P_{Lo} , P_{Im} , $P_{I/Q}$ characteristics ($V_{CC}=2.7V$)



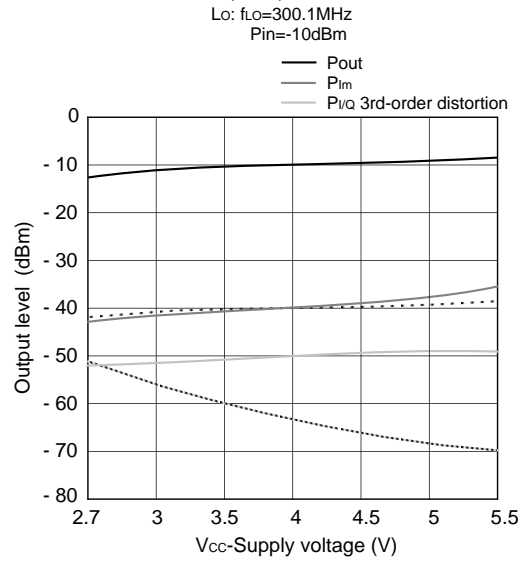
f_{LO} vs. P_{out} , P_{Lo} , P_{Im} , $P_{I/Q}$ characteristics ($V_{CC}=5.5V$)



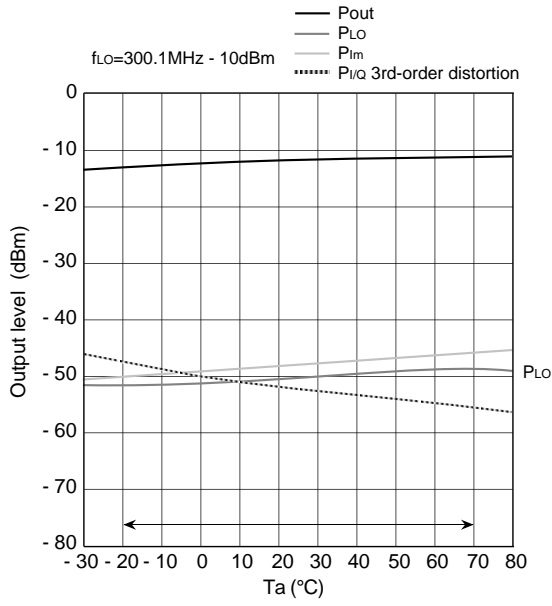
V_{CC} vs. I_{CC} characteristics
No signal input



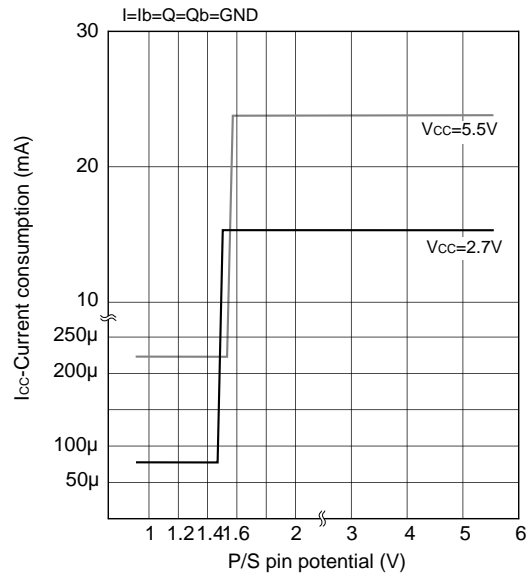
V_{CC} vs. P_{out} , P_{Im} , $P_{I/Q}$ characteristics



Ta vs. Pout, PLo, PIm, P_{I/O} characteristics (V_{CC}=2.7V)



V_{P/S} vs. I_{CC} characteristics

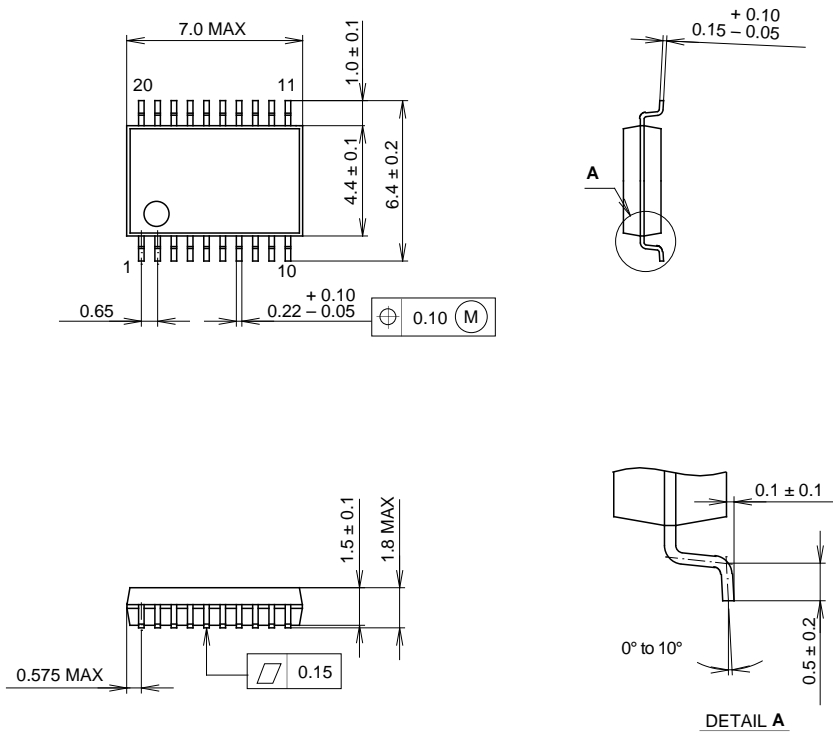


Notes on Operation

- (1) Electrostatic sensitive devices because of the high-frequency process .
- (2) Earth pattern should be as wide as possible, and do not increase ground impedance to prevent from the parasitic oscillation.
- (3) Wire the GND pin as short as possible.
- (4) Connect a by-pass capacitor to the Vcc pin.

Package Outline Unit : mm

20PIN SSOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SSOP-20P-L072
EIAJ CODE	SSOP020-P-0225-BN
JEDEC CODE	—

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.1g