SONY

CXA1851N

Up/Down Converter for 900 MHz-Band Mobile Communications

For the availability of this product, please contact the sales office.

Description

The CXA1851N is an up/down converter IC for 900 MHz-band mobile communications.

This is suitable for 900 MHz-band digital cordless telephone (CT2) and digital cellular.

Features

- Transmission/reception converter on a single chip
- Operating frequency: 800 to 900 MHz
- Supply voltage: 2.7 to 4.5 V
- Power saving function
- 20-pin SSOP package used for set size reduction

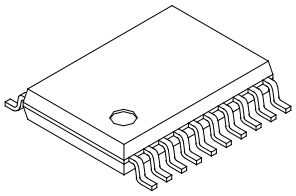
Applications

- CT2 digital cordless telephone
- Digital cellular

Structure

Bipolar silicon monolithic IC

20 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25°C)

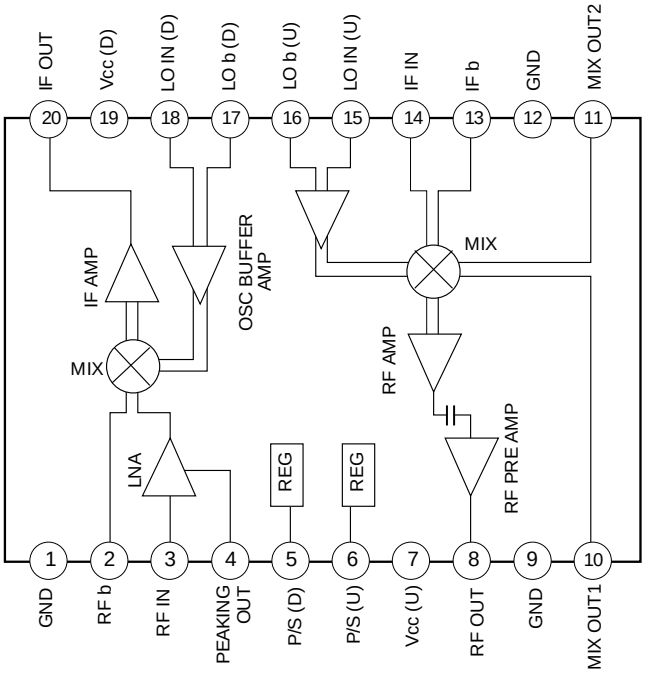
• Supply voltage	Vcc	5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	530∗	mW

∗ When mounted on a 505×0×1.6 mm copper-foiled glass epoxy board

Recommended Operating Conditions

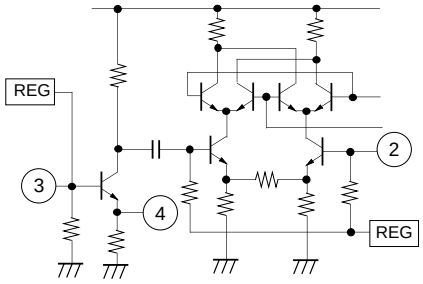
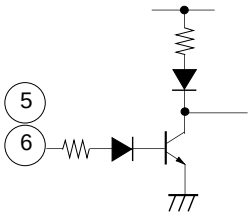
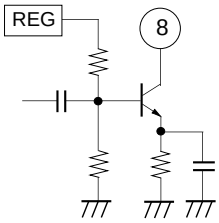
Supply voltage	Vcc	2.7 to 4.5	V

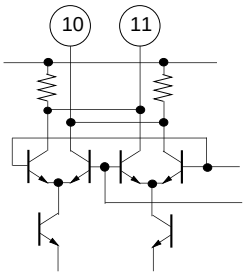
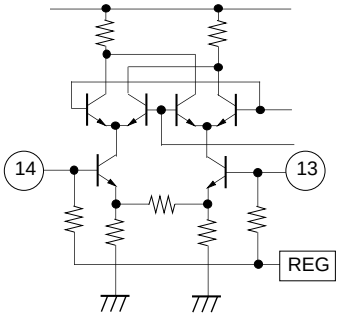
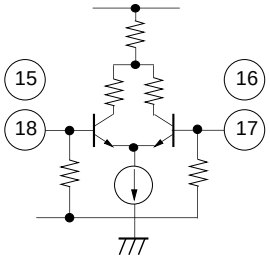
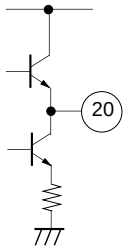
Block Diagram and Pin Configuration



E93505-TE

Pin Description

Pin No.	Symbol	Typical pin voltage (V)	Equivalent circuit	Description
1	GND	0.0		GND pin for the down converter.
2	RF BYPASS	1.1		MIX input by-pass pin for the down converter.
3	RF INPUT	0.9		RF input pin for the down converter. Because of high impedance, a 4.7 nH external chip inductor should be used for impedance matching.
4	PEAKING OUT	0.12		Emitter pin for the low-noise amplifier. Connect an approximately 3 pF chip capacitor and an approximately 22Ω chip resistor in series to the GND.
5	P/S (for DOWN CONV.)	0 to 4.5		Power saving control pin for the down converter. OFF when Vp/s≤1.0 V; ON when Vp/s≥1.8 V
6	P/S (for UP CONV.)	0 to 4.5		Power saving control pin for the up converter. OFF when Vp/s≤1.0 V; ON when Vp/s≥1.8 V
7	V_{CC} (for Up CONV.)	2.7 to 4.5		Power supply for the up converter.
8	RF OUTPUT	2.7 (Vcc=2.7V)		RF output pin for the up converter. Connect this pin to the Pin 7 power supply via the 15 nH chip inductor.
9	GND	0.0		GND pin for the up converter RF amplifier.

Pin No.	Symbol	Typical pin voltage (V)	Equivalent circuit	Description
10	MIX OUT1	2.3		MIX output pin for the up converter.
11	MIX OUT2	2.3		MIX output pin for the up converter. Connect an approximately 4.7 nH chip inductor and an approximately 3.5 pF chip capacitor between this pin and Pin 10 to form a tank circuit.
12	GND	0.0		GND pin for the oscillator buffer amplifier and mixer blocks of the up converter.
13	IF BYPASS	1.03		IF input by-pass pin for the up converter.
14	IF INPUT	1.03		IF input pin for the up converter. Because of high impedance, an external matching circuit is necessary which consists of a 220 nH chip inductor and an approximately 1.5 pF chip capacitor.
15	OSC INPUT (for UP CONV.)	1.8		Oscillator input pin for the up converter. A matching circuit consisting of a 51Ω resistor is necessary.
16	OSC BYPASS (for UP CONV.)	1.8		Oscillator input by-pass pin for the up converter.
17	OSC BYPASS (for DOWN CONV.)	1.85		Oscillator input by-pass pin for the down converter.
18	OSC BYPASS (for DOWN CONV.)	1.85		Oscillator input pin for the down converter. A matching circuit consisting of a 51Ω resistor is necessary.
19	Vcc (for DOWN CONV.)	2.7 to 4.5		Power supply for the down converter.
20	IF OUTPUT	1.45		IF output pin for the down converter.

Electrical Characteristics

(Ta=25°C, V_{CC}=2.7V, Z_L=Z_S=50Ω)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Up Converter Block ∗1						
Current consumption	I_{CC}	For no signal input	18.0	25.0	35.0	mA
Conversion gain	CG	Pin= - 40dBm	17.5	20.5	25.5	dB
RF output power	Pout	Pin= -10dBm, 50Ω load	0	3		dBm
Noise figure	NF	DSB mode		13	18	dB
Lo leak	ISO (Lo)	Pin= - 10dBm		- 25.0	- 10	dBm
IF leak	ISO (IF)	Pin= - 10dBm		- 12.0	- 5	dBm
Standby current consumption	I_{CC} (PD)	6pin (P/S)<1.0V		220 ∗2	350 ∗2	µA
Power saving control voltage	Vp/s (ON)		1.8		4.5	V
	Vp/s (OFF)				1.0	V
Rise time	Tup			2.5	5.0	µs
Down Converter Block ∗3						
Current consumption	I_{CC}	For no signal input	8.0	15.0	22.0	mA
Conversion gain	CG	Pin= - 40dBm, 50Ω load	15.0	18.0	23.0	dB
IF output power	Pout (IF)	Pin= - 10dBm, 50Ω load	- 4.5	- 2.0		dBm
Third-order intermodulation distortion	IM3	f_{RF}1=866.4MHz, Pin1= - 40dBm	45	49.0		dBc
		f_{RF}2=866.8MHz, Pin2= - 40dBm				
Noise figure	NF	DSB mode		7.5	10	dB
Standby current consumption	I_{CC} (PD)	5pin (P/S)≤1.0V		220 ∗2	350 ∗2	µA
Power saving control voltage	Vp/s (ON)		1.8		4.5	V
	Vp/s (OFF)				1.0	V
Rise time	Tup			2.5	5.0	µs

∗1: f_{IF}in=150.05MHz, f_{RF}out=864.05 to 868.05MHz
f_{LO}in=1014.10 to 1018.1MHz (- 9dBm)

∗2: These are the total values for the up and down converters.

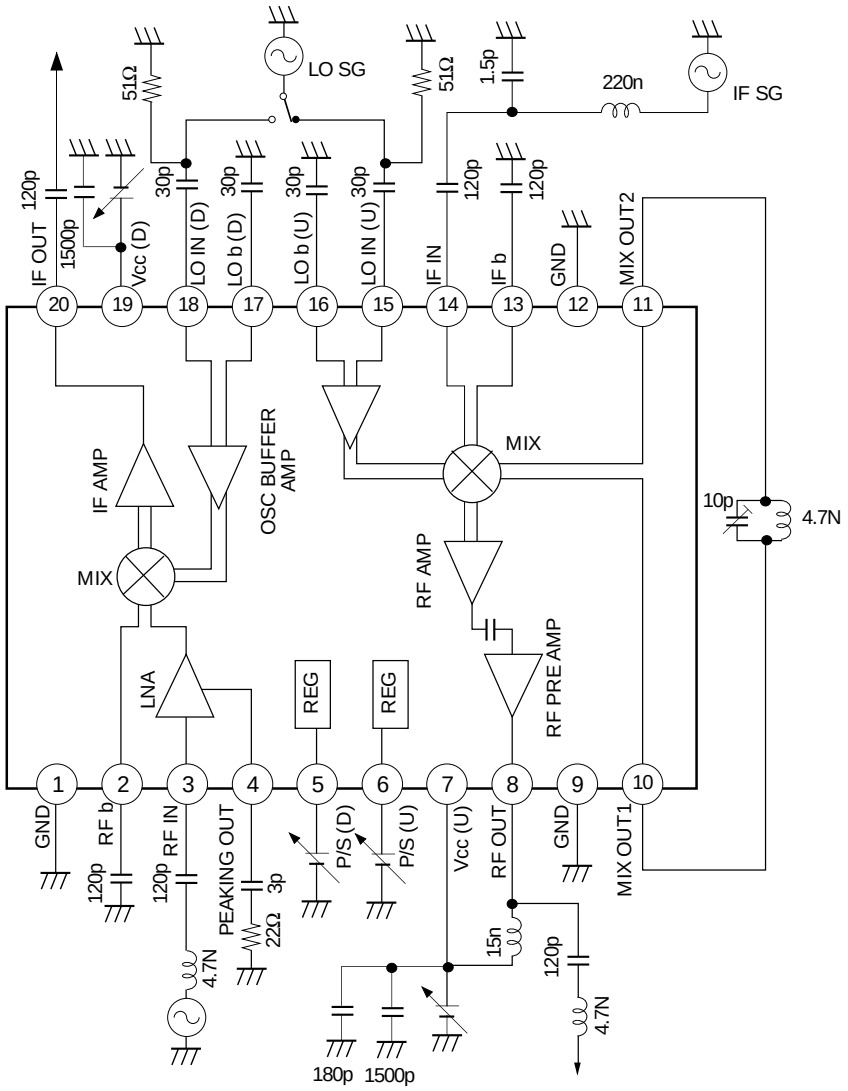
∗3: f_{RF}in=864.05 to 868.05MHz
f_{LO}in=1014.10 to 1018.1MHz (- 9dBm)

Typical Reference characteristics

(Ta=25°C, V_{CC}=2.7V, Z_L=Z_S=50Ω)

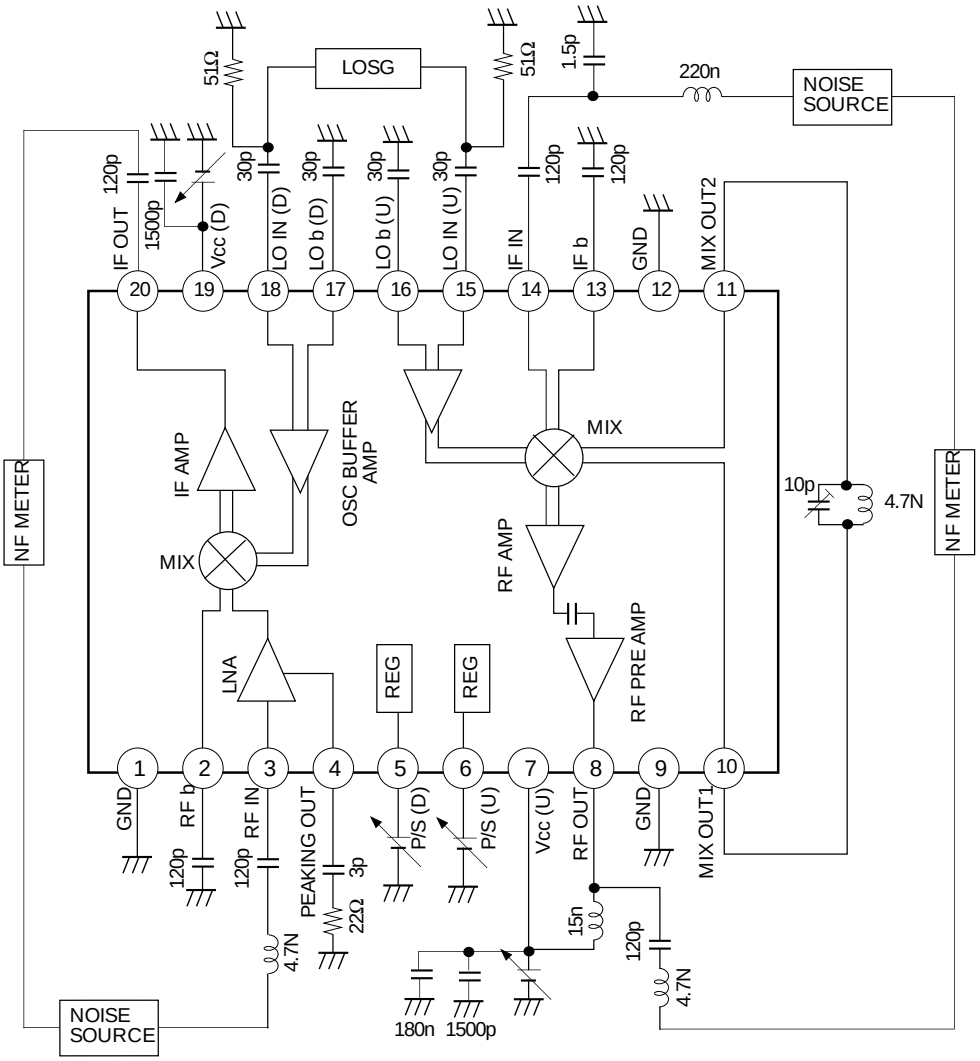
Item	Symbol	Conditions	Typ.	Unit
Up Converter Block				
Third-order intermodulation distortion	IM3	fIF1=150.4MHz, P_{IF}1= - 30dBm	39.0	dBc
		fIF2=150.8MHz, P_{IF}2= - 30dBm		
Down Converter Block				
1 dB compression	P- 1dB	Output conversion, 50Ω load	- 7.0	dBm
Lo leak	ISO (Lo)	Pin= - 40dBm	- 29.0	dB
RF leak	ISO (RF)	Pin= - 40dBm	- 44.0	dB

Electrical Characteristics Test Circuit 1



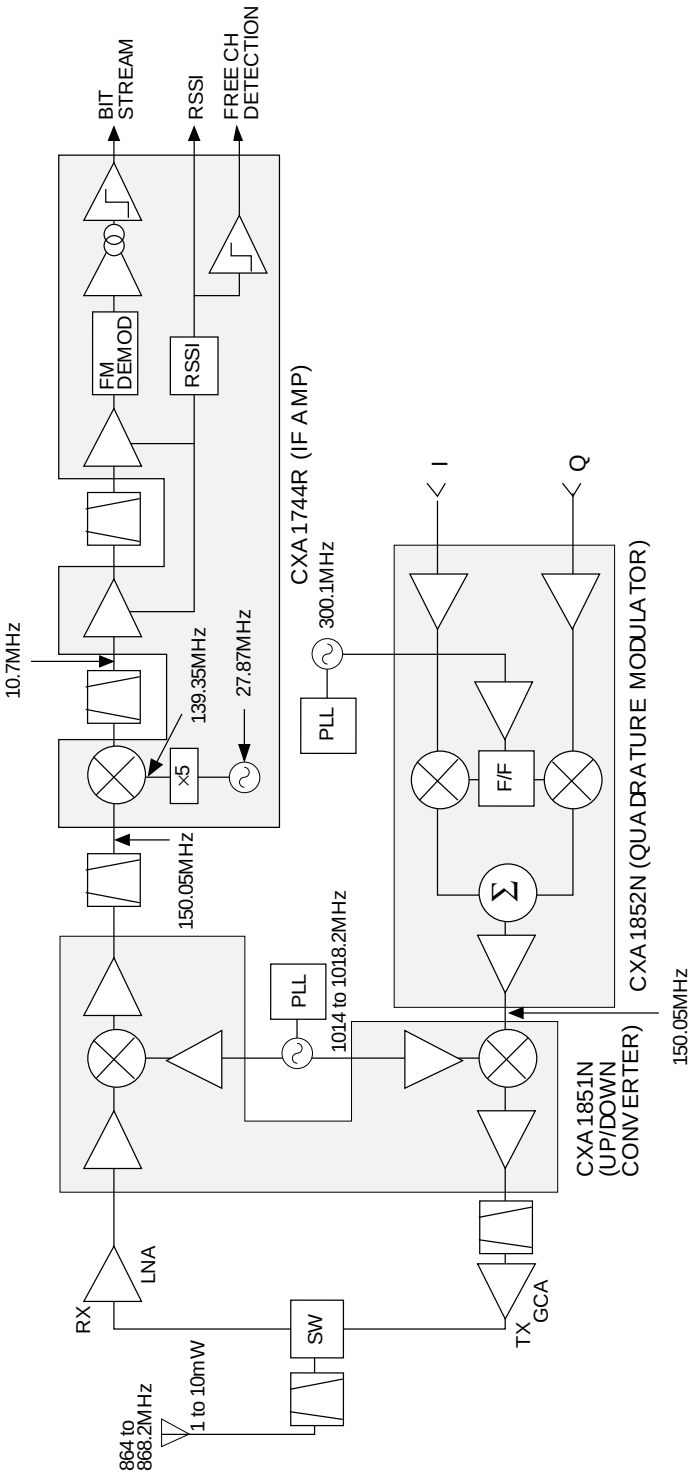
Electrical Characteristics Test Circuit 2

Items: NF (D), NF (U)

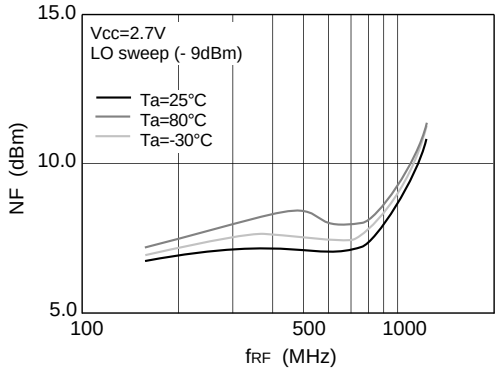


Block diagram

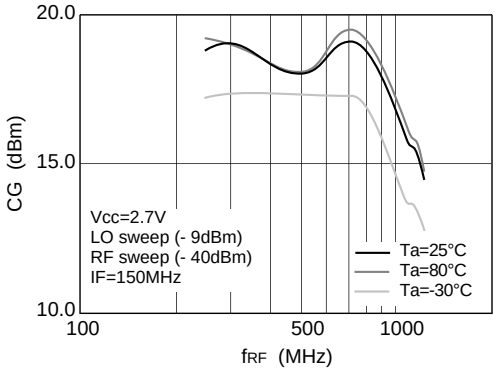
Digital cordless telephone chip set (CXA1744R/CXA1851N/CXA1852N)



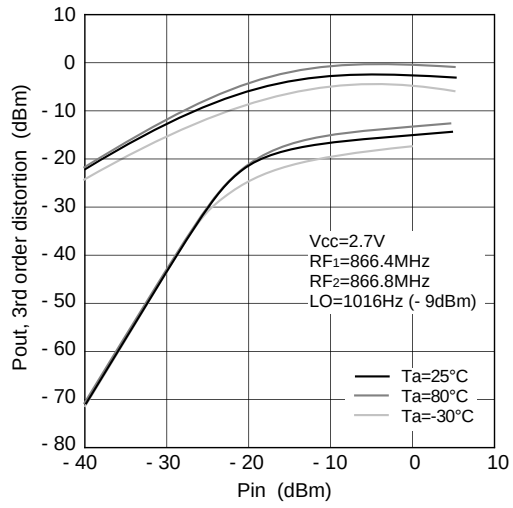
(Down-Con) f_{RF} vs. NF characteristics



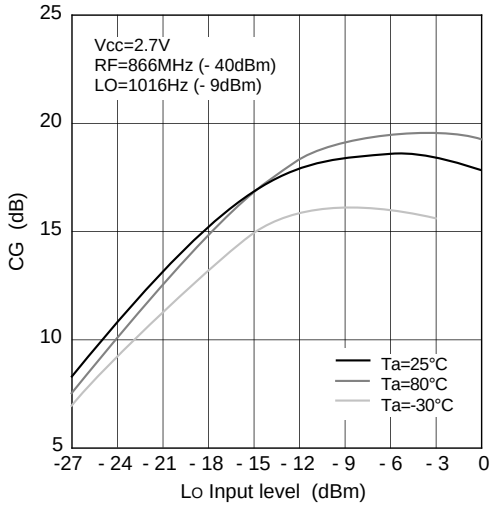
(Down-Con) f_{RF} vs. CG characteristics



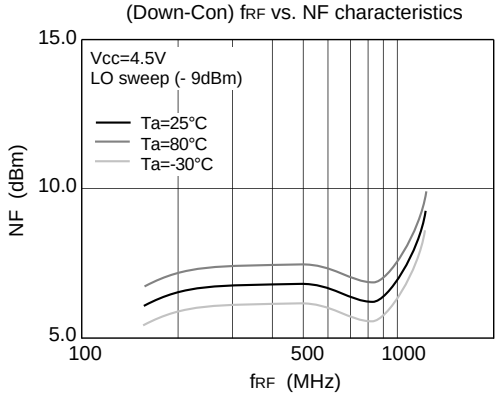
(Down-Con) Pin vs. Pout and IM3 characteristics



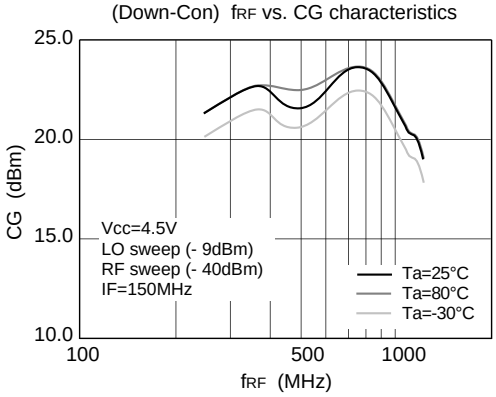
DS3 (Down-Con) LO input level vs. CG characteristics



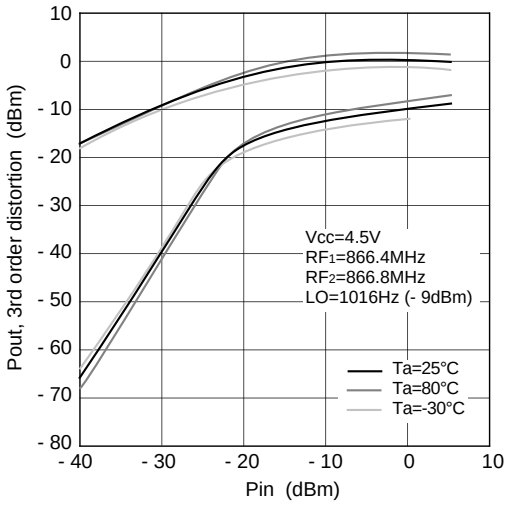
(Down-Con) f_{RF} vs. NF characteristics



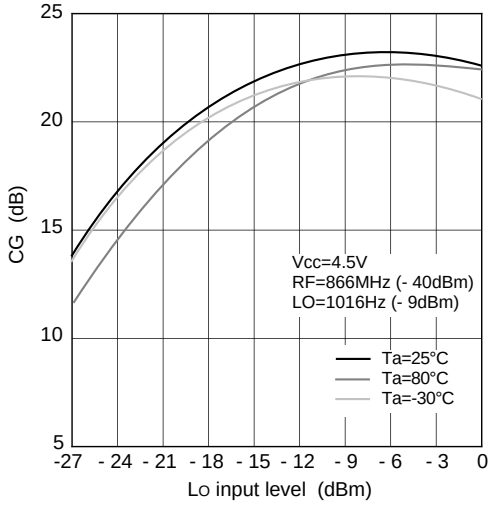
(Down-Con) f_{RF} vs. CG characteristics



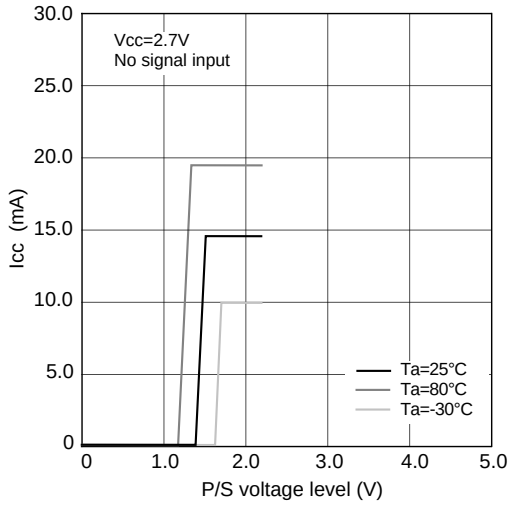
(Down-Con) Pin vs. Pout and IM3 characteristics



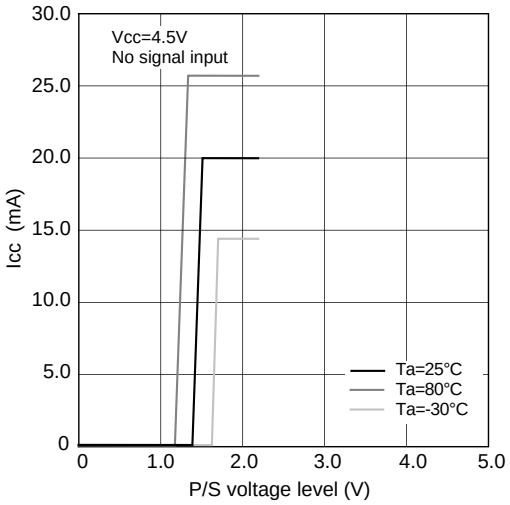
(Down-Con) LO input level vs. CG characteristics



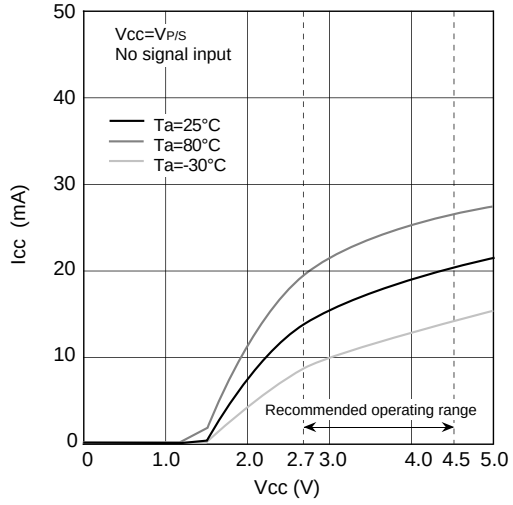
(Down-Con) P/S voltage level vs. ICC characteristics



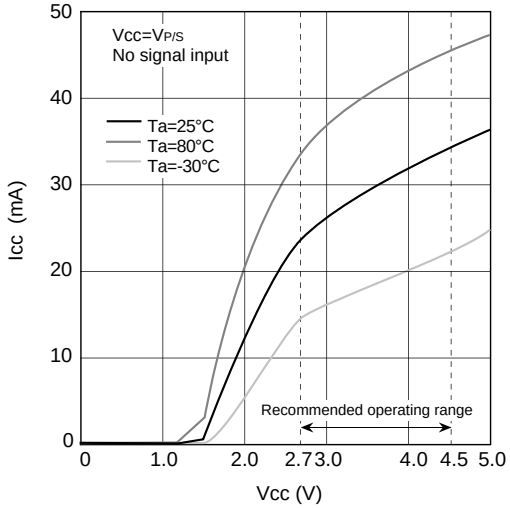
(Down-Con) P/S voltage level vs ICC characteristics



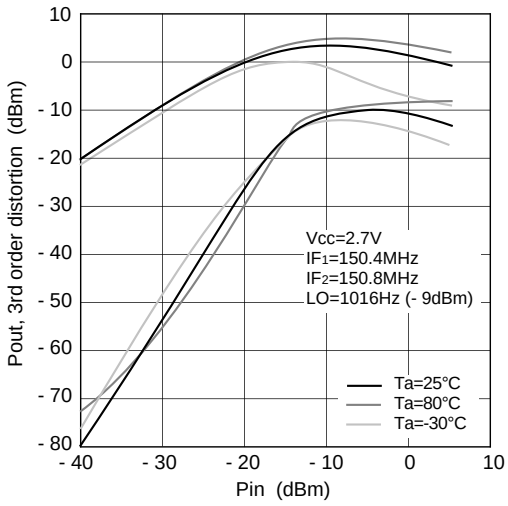
(Down-Con) Vcc vs. ICC characteristics



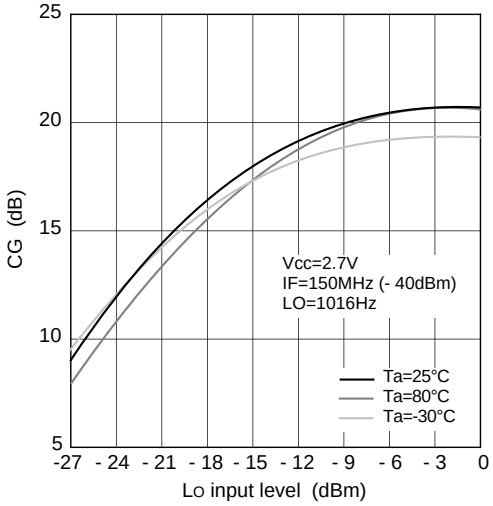
(Up-Con) Vcc vs. ICC characteristics



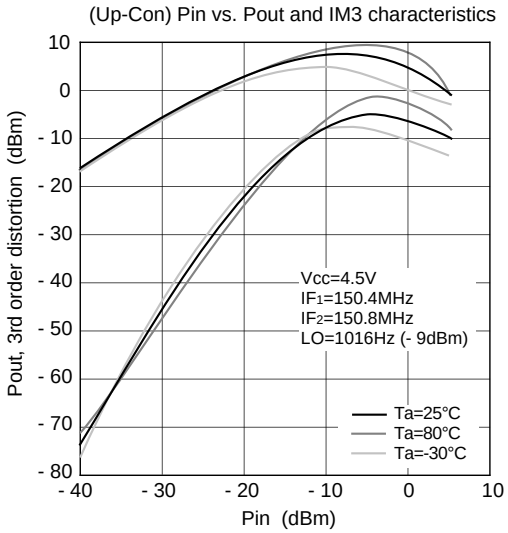
(Up-Con) Pin vs. Pout and IM3 characteristics



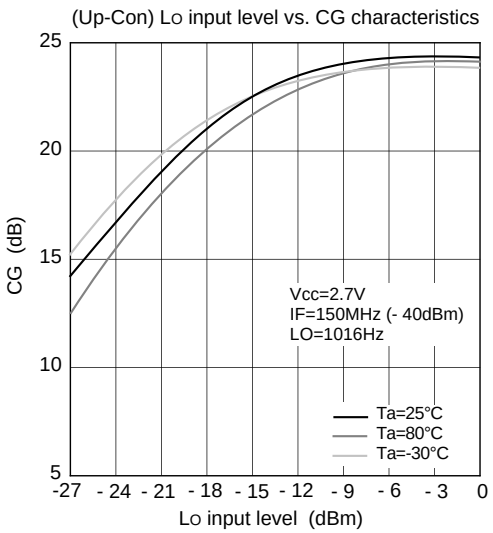
(Up-Con) Lo input level vs. CG characteristics



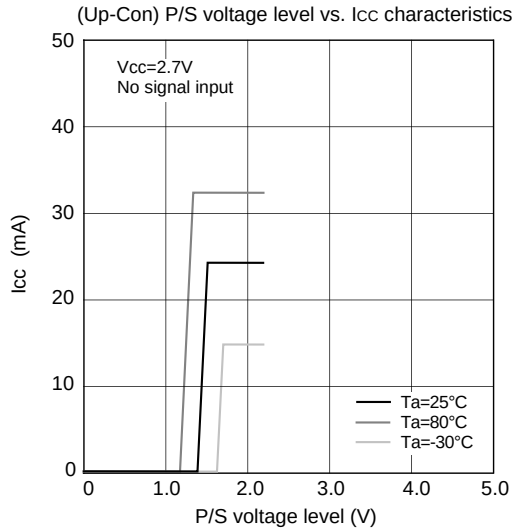
(Up-Con) Pin vs. Pout and IM3 characteristics



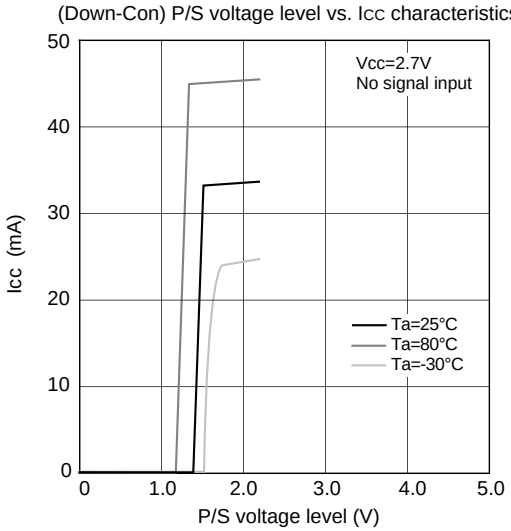
(Up-Con) Lo input level vs. CG characteristics



(Up-Con) P/S voltage level vs. Icc characteristics



(Down-Con) P/S voltage level vs. Icc characteristics

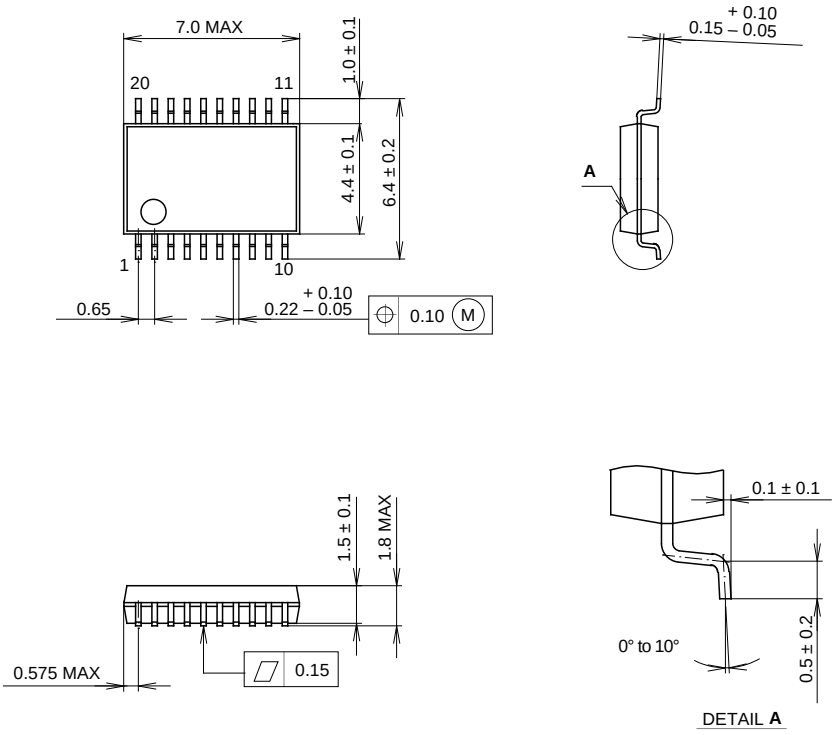


Notes on Operation

(1) Electrostatic sensitive diveces because of the high-frequency process.
(2) Earth pattern should be as wide as possible and do not increase ground impedanse to prevent from the parasitic osellation.
(3) Wire the GND pin as short as possible.
(4) Connect a by-pass capacitor to the V_{CC} pin.

Package Outline Unit : mm

20PIN SSOP (PLASTIC)



SONY CODE	SSOP-20P-L072
EIAJ CODE	SSOP020-P-0225-BN
JEDEC CODE	

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.1g