SONY

CXA1184M/N

Low-voltage FM IF Amplifier

Description

CXA1184M and CXA1184N are designed for FM communication devices. They incorporate a paging system, mixer, IF limiter, FM detector, operational amplifier, comparator, and others.

Features

- Low operating voltage 1.0 to 4.0 V
- Low power consumption 2 mA at 1.5 V
- Built-in power source voltage monitor.

Applications

IF Amplifier for Paging System Receiver

Structure

Bipolar silicon monolithic IC

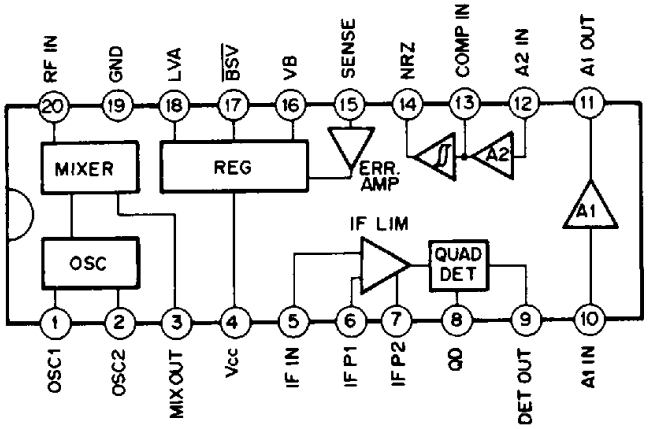
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	10	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C

Recommended Operating Conditions

• Supply voltage	Vcc	1.0 to 4.0	V

Block Diagram and Pin Configuration



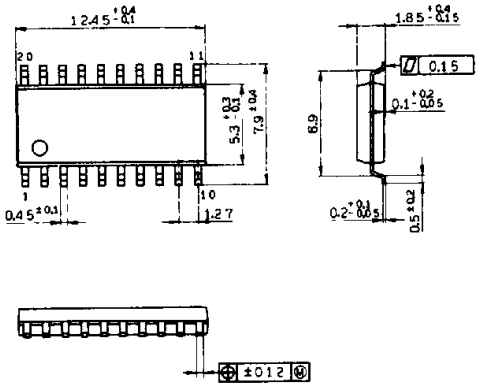
Note) DET. : DETECTOR
LIM : LIMITTER
REG : REGURATOR
ERR : ERROR CORRECTION

Package Outline

Unit: mm

CXA1184M

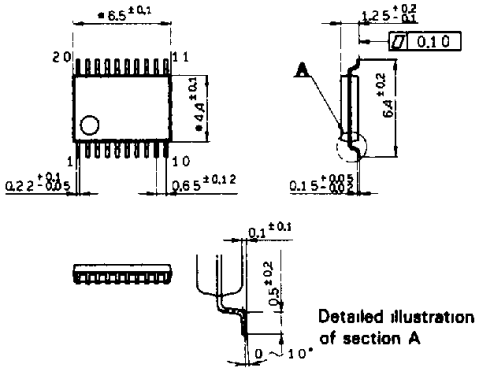
20 pin SOP (Plastic)



SOP-20P-L01

CXA1184N

20 pin VSOP (Plastic)

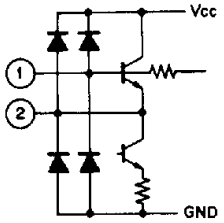
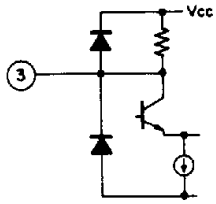
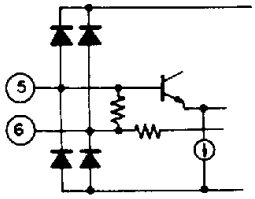
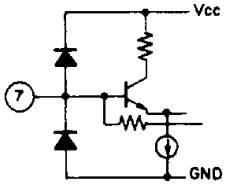
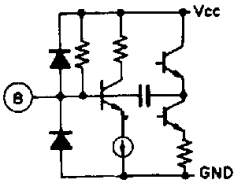


VSOP-20P-L01

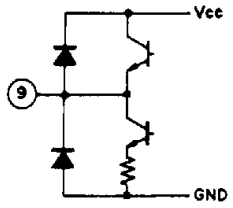
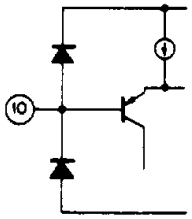
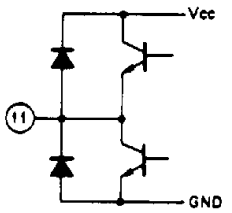
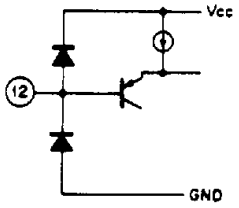
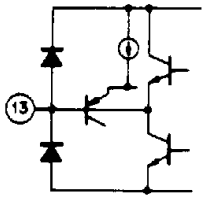
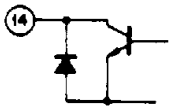
Note: *The dimension with an asterisk does not include residual resin.

E88Z43-TO

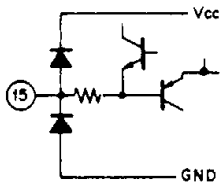
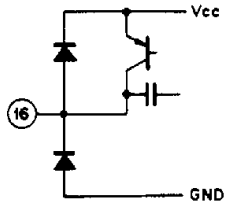
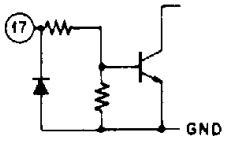
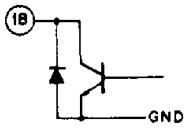
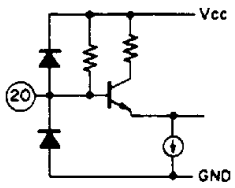
Pin Description

No.	Symbol	Equivalent circuit	Description
1	OSC1		Those pins are connected to the external parts of an oscillating circuit. The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Vcc, pins 1 and 2 respectively.
2	OSC2		
3	MIX OUT		Mixer output pin. Connect a 455 kHz ceramic filter between this pin and the IF IN pin.
4	Vcc		Vcc pin.
5	IF IN		Input pin for the IF limiter amplifier.
6	IF P1		Connection pin of the bypass capacitor for the IF limiter amplifier. Connect a capacitor of about 0.047 μF between this pin and ground (or Vcc).
7	IF P2		Connection pin of the bypass capacitor for the IF limiter amplifier. Connect a capacitor of about 0.047μF between this pin and ground (or Vcc).
8	QD		Connected to a quadrature detector phase shifter.

Pin Description

No.	Symbol	Equivalent circuit	Description
9	DET OUT		Recovered signal output.
10	A1 IN		Input pin of inverting OP amplifier A1.
11	A1 OUT		Output pin of OP amplifier A1.
12	A2 IN		Input pin of OP amplifier A2.
13	COMP IN		Input pin of the comparator. This pin is internally connected to the output of OP amplifier A2.
14	NRZ		NRZ (Non Return Zero) output pin

Pin Description

No.	Symbol	Equivalent circuit	Description
15	SENSE		Voltage control pin for external bias supply.
16	VB OUT		Supplies bias voltage to external circuit transistors and others
17	BSV		Reduces IC power consumption. Lowering pin voltage below 0 35 V stops IC operation.
18	LVA		Output pin for Low Voltage Alarm (LVA). The pin turns to high impedance when power voltage drops below 1.05 V.
19	GND		Ground pin
20	RF IN		Mixer input pin

3

Electrical Characteristics

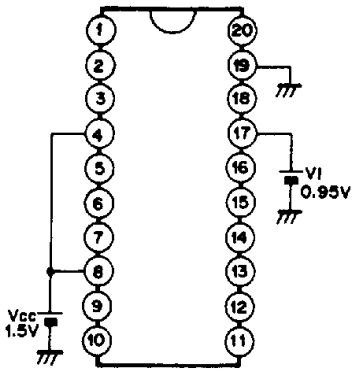
V_{CC} = 1.5 V, Ta = 25°C, f_S = 21.7 MHz,
f_{MOD} = 256 Hz, f_{DIV} = 2.3 kHz, AM$_{MOD}$30%

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption (during operation)	I_{CC}	Test circuit 1	1.2	2.0	2.5	mA
Power consumption (during battery saving)	I_{CCS}	Test circuit 1 V_I = 0.3 V	–	–	20	μA
Input for −3 dB Limiting	V_{IN} (LIM)	Test circuit 3	–	7	–	dBμ
AM rejection ratio	AMRR	Vin = 60dBμ Test circuit 3	25	–	–	dB
OP amplifier input bias current	I_{BIAS}	Test circuit 2	–	30	100	nA
OP amplifier open loop gain	A_V	Test circuit 4	45	60	–	dB
OP amplifier output voltage amplitude	V_O	Test circuit 5	0.25	–	–	Vp-p
Comparator hysteresis width	V_{TW}	Test circuit 6	30	40	5.0	mV
NRZ* output leak current	I_{LNRZ}	Test circuit 7	–	–	5.0	μA
NRZ* saturation voltage	V_{SATNRZ}	I_{SINK} = 200μA Test circuit 8	–	–	0.4	V
VB output current	I_{OUT}	V_B = 0.9V	0.1	–	–	mA
VB output voltage	V_{BOUT}	Test circuit 9	0.95	–	–	V
Sense voltage	V_{SEN}	Test circuit 9	85	100	115	mV
LVA threshold voltage	V_{PML}	Test circuit 10	1.05	1.10	1.15	V
LVA hysteresis width	V_{PMTH}	$V_{PMH} - V_{PML}$	40	50	70	mV
LVA output leak current	I_{LLVA}	Test circuit 7	–	–	5.0	μA
LVA saturation voltage	V_{SATLVA}	Test circuit 8	–	–	0.4	V
Recovered signal voltage	V_{DET}	Test circuit 3	10	–	–	mVrms
BSV high level	V_{THBSV}		0.95	–	–	V
BSV low level	V_{TLBSV}		–	–	0.35	V

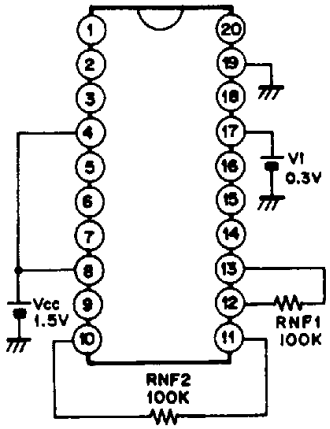
*NRZ: Non Return Zero

Electrical Characteristics Test Circuit

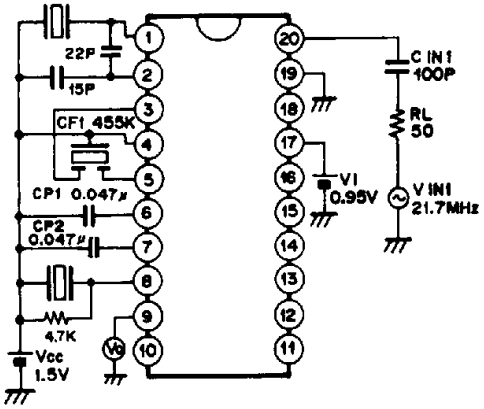
1)



2)



3)



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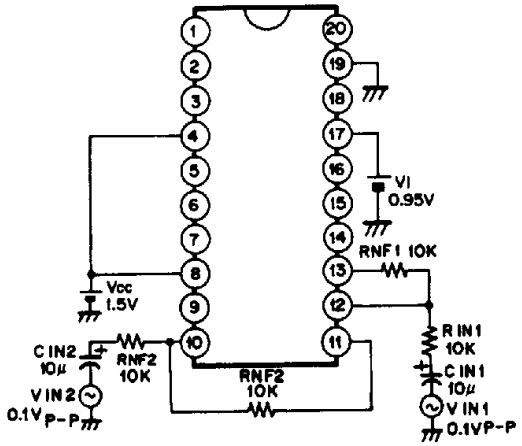
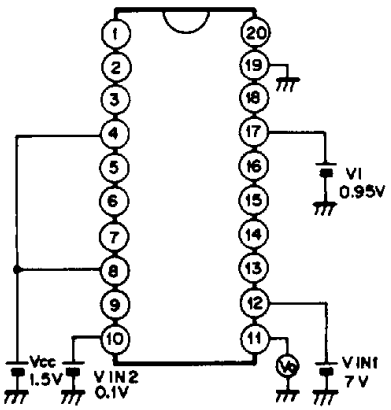
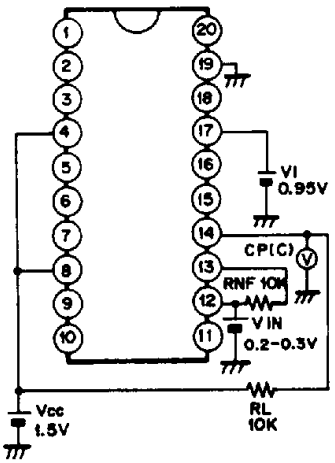


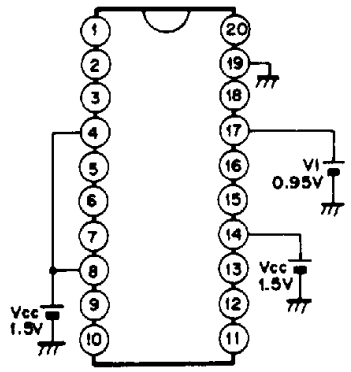
5)



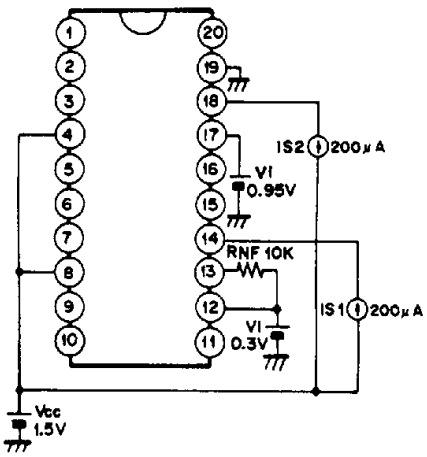
6)



7)



8)



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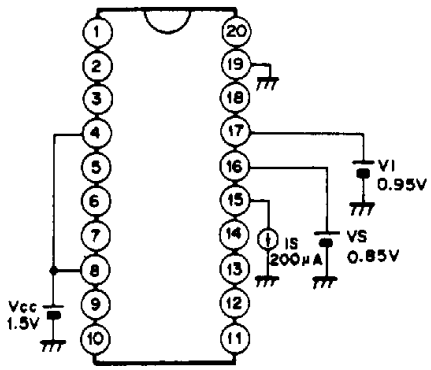
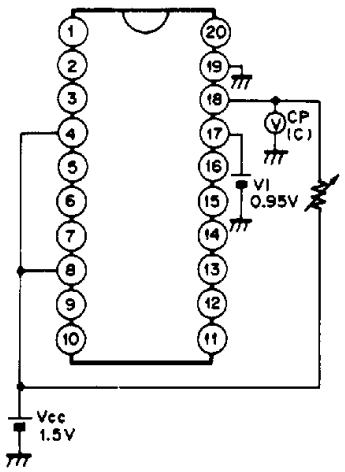


10)



Test Method

Input for −3 dB Limiting V_{IN} (LIM)

Use test circuit 3. Apply a signal with the following characteristics to SIG IN.

Signal frequency:	fs = 21.7 MHz
Modulation frequency:	f_{MOD} = 256 Hz
Frequency deviation:	f_{DIV} = 2.3 kHz
Signal level:	V_L = 40 dBμ

Here, the value of V_{AC} is specified as V_{AC1}. Next, the signal level V_L is changed to 19dBμ and V_{AC} value is hence specified as V_{AC2}.

$$20 \log \frac{V_{AC1}}{V_{AC2}} < 3 \text{ dB}$$

AM rejection ratio (AMRR)

Use test circuit 3. Apply a signal with the following characteristics to SIG IN.

Signal frequency:	fs = 21.7 MHz
Modulation frequency:	f_{MOD} = 256 Hz
Frequency deviation:	f_{DIV} = 2.3 kHz
Signal level:	V_L = 40 dBμ

Here, the value of V_{AC} is specified as V_{AC1}. Next, AM is modified to:

Modulation ratio:	AM_{MOD} = 30%
Modulation frequency:	f_{MOD} = 256 Hz

and the V_{AC} value is hence specified as V_{AC2}.

$$AMRR = 20 \log \frac{V_{AC1}}{V_{AC2}} > 25 \text{ dB}$$

Recovered signal voltage V_{DET}

Use test circuit 3. Apply a signal with the following characteristics to SIG IN.

Signal frequency:	fs = 21.7 MHz
Modulation frequency:	f_{MOD} = 256 Hz
Frequency deviation:	f_{DIV} = 2.3 kHz
Signal level:	V_L = 50 dBμ

Here, the value of the pin-9 output voltage is expressed as V_{DET}.

OP amplifier output voltage amplitude V_O (OP)

Use test circuit 5. If output voltage V is expressed as V_1 when V_{IN} is 0.1 V, and as V_2 when V_{IN} is 0.3 V, it follows that:

$$V_O = V_1 - V_2$$

3

Comparator hysteresis width V_{TW}
Use test circuit 6.
Vary V_{IN} between 0.1 to 0.3 V.
Specify V_{IN} voltage, as V_1 when (C) voltage changes from low to high.
Similarly, specify V_{IN} voltage as V_2, when (C) voltage changes from high to low.

Therefore: VHY $V_{TW} = V_1 - V_2$

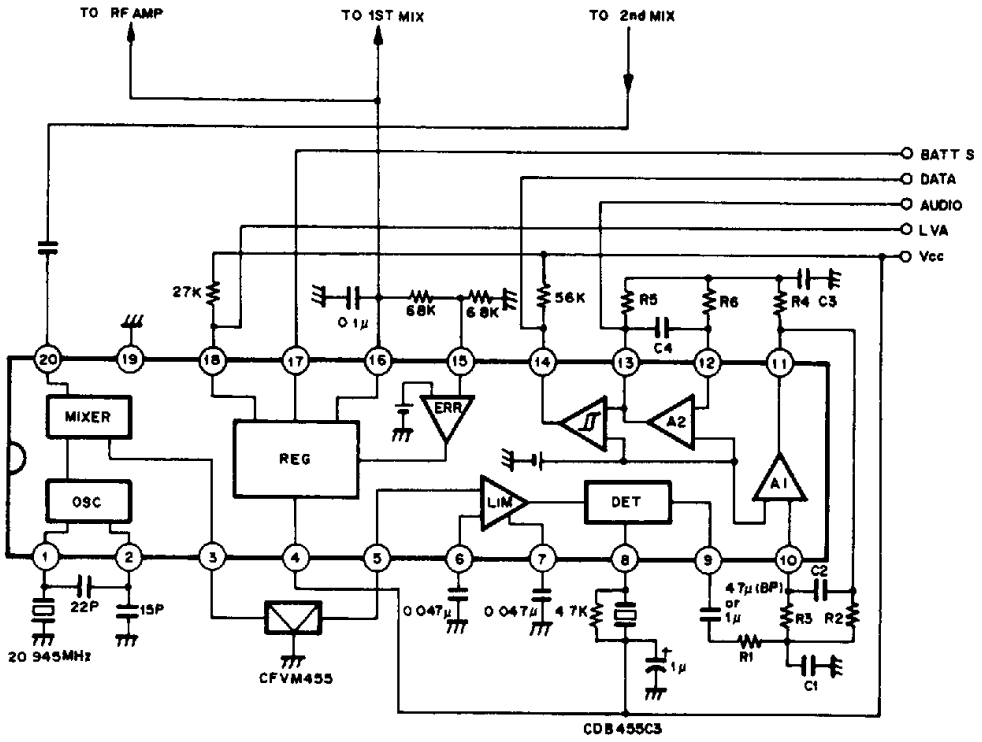
LVA threshold voltage V_{PML} and recovery voltage V_{PMH}
Use test circuit 10.
Vary power voltage V_{CC} from 1.3 to 0.95 V.
Specify V_{CC} as V_{PML}, when (C) voltage changes from low to high.
Similarly, specify V_{CC} as V_{PMH}, when (C) voltage changes from high to low.

Design Reference Values

Ta = 25°C, Vcc = 1.4V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Mixer input resistance	$R_{IN\ (MIX)}$		1.3	1.6	1.9	kΩ
Mixer input capacity	$C_{IN\ (MIX)}$		–	4.0	–	pF
Mixer output resistance	$R_{OUT\ (MIX)}$		1.44	1.8	2.16	kΩ
IF input resistance	$R_{IN\ (IF)}$		1.44	1.8	2.16	kΩ
IF gain stability	$G_{S\ (IF)}$	Ta = −20 to +60°C	–	±6	–	dB
Detector output resistance	$R_{OUT\ (QD)}$		1.28	1.6	2.0	kΩ
OP amplifier max. input voltage	V_{INMAX}		–	–	0.39	V
OP amplifier min. input voltage	V_{INMIN}		0.05	–	–	V
Comparator max. input voltage	$V_{INMAXCOMP}$		–	–	0.39	V
Comparator min. input voltage	$V_{INMINCOMP}$		0.05	–	–	V
OP amplifier off-set voltage	V_{OFS}		–	–	3	mV

Application Circuit



3

1) Supply

This IC incorporates a regulation and is designed to operate steadily on a wide range of supply voltage from 1.0 to 4.0 V.

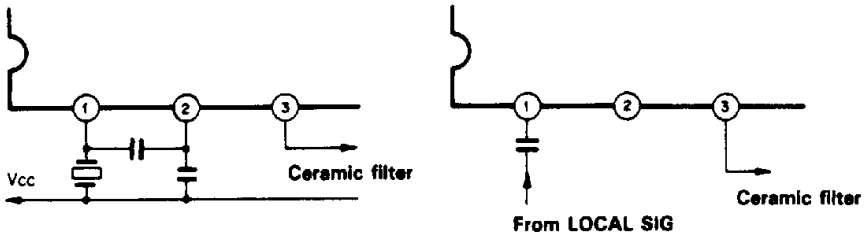
Decoupling on the wiring to the supply pin (pin 4) should be done as close to the pin as possible.

2) Oscillation input

Oscillation input method

a) Using pins 1 and 2, input self-excited oscillation signals through the composition of a Colpitts type crystal oscillating circuit.

b) Input local oscillation signals to pin 1 directly.



a b

Fig. 1

3) Mixer

This IC's mixer is of the double balance type. Pin 24 is the input pin. Input through a suitable alignment circuit. Input impedance is at 1.6kΩ. The mixer output features a built-in 1.6kΩ load resistance at pin 3.

4) IF filter

The filter to be connected between this IC's mixer and the IF limiter should have the following specifications.

I/O impedance : 1.6kΩ ±10%
Band width : Use according to application

5) IF limiter

The IF limiter of this IC features a gain of about 100 dB. To this effect, the following points should be considered for the wiring connecting IF limiter input pin (pin 5) and decoupling capacitor pins (pins 6 and 7).

a) Wiring to mixer output (pin 3) and IF limiter input (pin 5) should be as short and as far apart as possible to avoid neutral interference.
b) Connect a decoupling capacitor to IF limiter IF P1 (pin 6) and IF P2 (pin 7).
Here the decoupling capacitor should be positioned as close as possible to each pin and the wiring be as short as can be.
c) As IF limiter output shows at QD (pin 8), keep the wiring connected to QD pin,R, L, C and the ceramic discriminator as short as possible. Interference to the mixer output, IF limiter input and others must be kept to a minimum.

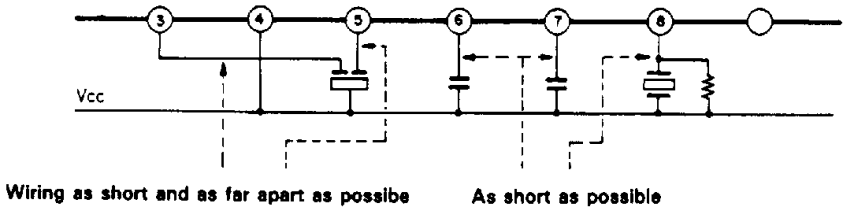


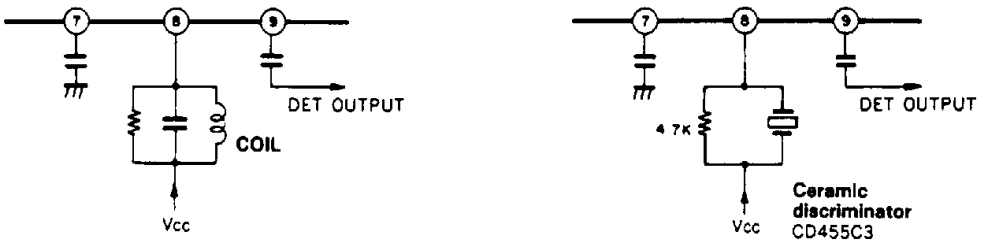
Fig. 2

6) Detector

The detector is of the quadrature type. To phase shift, either R, L, C resonance circuit or the ceramic discriminator is connected to pin 8.

The phase capacitor of the quadrature detector is built-in. FM (FSK) signals demodulated by this detector have their high frequency components dropped by the LPF formed inside from CRs, to be output at DET OUT (pin 9). DET OUT output impedance is about 3kΩ.

For the CXA1184M ceramic discriminator, CDB455C3 (Murata Production) is recommended.



a) Coil

b) Ceramic discriminator

Fig. 3

7) OP AMP, NRZ OUT

This IC has 2 built-in operation amplifiers.
One of these operation amplifiers is connected inside the IC to NRZ comparator.

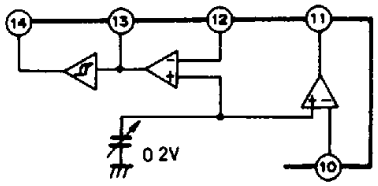


Fig. 4

Making use of these operation amplifiers an LPF or the sort is made up to eliminate noise during signal demodulation and input to the following NRZ comparator.

NRZ comparator molds the waveform of input signals to output them as square waves. NRZ comparator output is an open collector.

Accordingly as CPU is a CMOS, in case the supply voltage differs, by following the method indicated in Fig. 5 direct interfacing becomes possible.

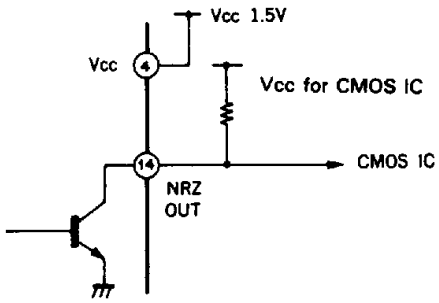


Fig. 5

8) VB SENSE, VB OUT

This controls the base bias of the external transistor. Pin 16 VB OUT can be used as the previous amplifier 1st mixer bias.

9) LVA OUT

When supply voltage turns low this pin turns to High (Open). Output is an open collector and, similarly as NRX OUT, can directly drive CMOS.

This LVA setting voltage is at 1.1V ±50 mV with hysterisis versus supply voltage.
Hysterisis width is at 50mV ±10 mV.

10) $\overline{\text{BSV}}$

By turning this pin to low, this IC's operation can be stopped.
This pin can also be directly connected to CMOS.
Consumption current with $\overline{\text{BSV}}$ is 20 μA (at 1.5 V) and below.

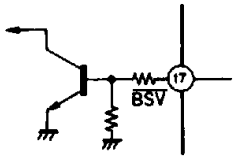
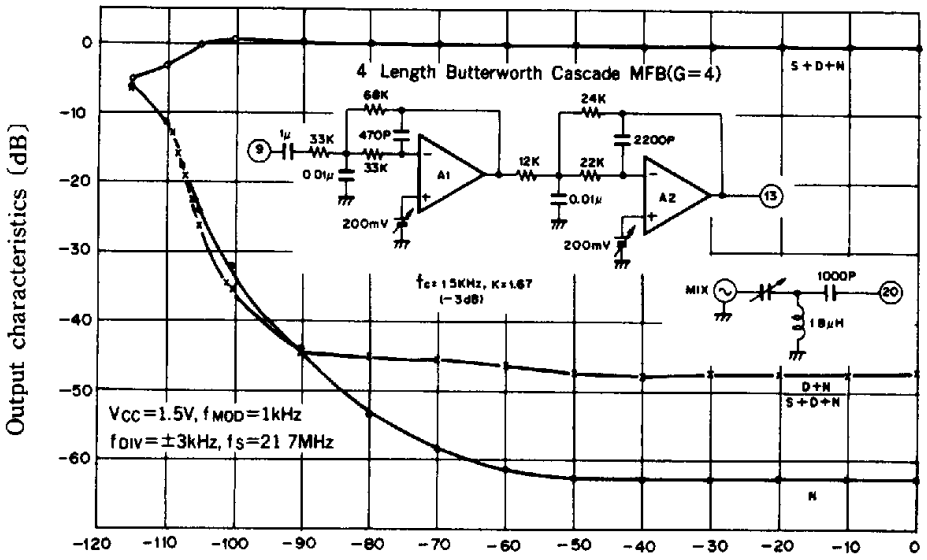


Fig. 6

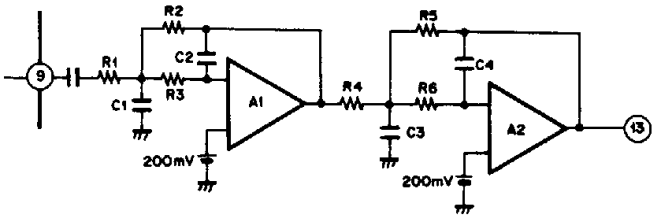
Mixer input signal vs Output characteristics

Input sensitivity



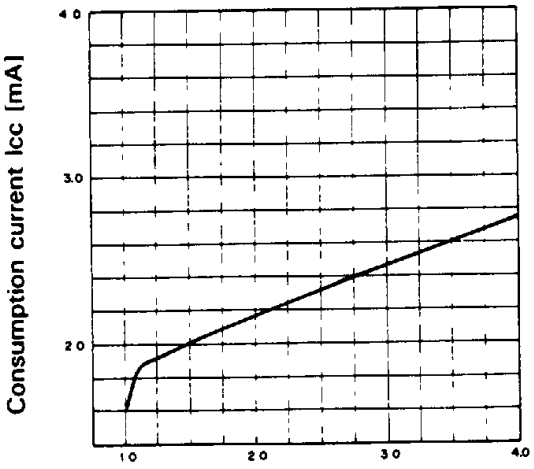
3

4th LP Butterworth cascade MFB constant using OP1 and OP2 inside CXA1184M.

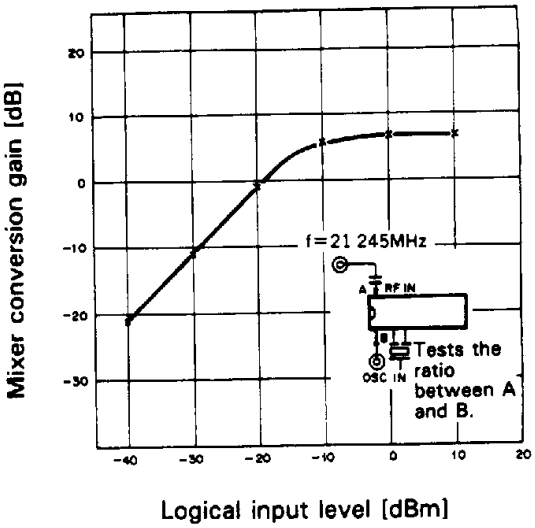


f_{MOD}	256Hz
f_c (−3dB)	400Hz
A1Gain	1
A2Gain	4
R1	47KΩ
R2	47KΩ
R3	22KΩ
R4	47KΩ
R5	180KΩ
R6	33KΩ
C1	0.012μF
C2	680pF
C3	0.015μF
C4	1200pF

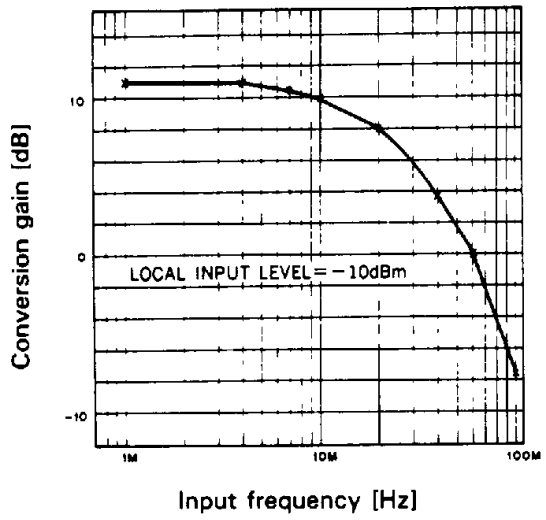
Supply voltage vs. Consumption Current



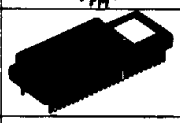
Logical input level vs. Mixer conversion



Input frequency vs. Conversion gain



Package Name

Type		Package name		Package	Features			
		Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN LINE PACKAGE		P	2 54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	ZIG ZAG IN-LINE PACKAGE		P	2 54mm (100MIL) Zig·Zag in-line	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	Package under side
		PIGGY BACK	PIGGY BACK		C	2 54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE		P	1 778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK ZIG-ZAG IN-LINE PACKAGE		P	1 778mm (70MIL) Zig·Zag in-line	Through Hole Lead	1-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT L LEADED PACKAGE		P C	1.0mm 0.8mm 0 65mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE L-LEADED PACKAGE		P	1 27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE		P	1 27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0 5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull-Wing	2-direction
		TSOP	THIN SMALL OUTLINE PACKAGE		P	0.5mm (0 55mm)	Gull-Wing	2-direction
	Standard chip carrier	Q F J	QUAD FLAT J-LEADED PACKAGE		P	1 27mm (50MIL)	J-Lead	4-direction
		Q F N	QUAD FLAT NON-LEADED PACKAGE		C	1.27mm (50MIL)	Leadless	Package under side

*P ·····Plastic, C ····Ceramic

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