SONY

CXA1166K

8-bit 250 MSPS Flash A/D Converter

Description

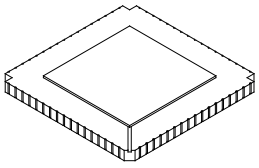
The CXA1166K is an 8-bit ultrahigh-speed flash A/D converter IC capable of digitizing analog signals at a maximum rate of 250 MSPS. The digital I/O level of this A/D converter is compatible with the ECL 100K/10KH/10K.

This IC is pin-compatible with the conventional CXA1076AK/CXA1176K/CXA1176AK, and can replace the conventional models easily. Compared with the conventional models, the CXA1166K has a greatly improved performance because of the new circuit design and carefully considered layout.

Features

- Differential linearity error: ±0.5 LSB or less
- Integral linearity error: ±0.5 LSB or less
- Built-in integral linearity compensation circuit
- Ultrahigh-speed operation with maximum conversion rate of 250 MSPS
- Low input capacitance: 18pF
- Wide analog input bandwidth: 250MHz (full-scale input, standard)
- Single power supply: –5.2V
- Low power consumption: 1.4W (Typ.)
- Low error rate
- Good temperature characteristics
- Capable of driving 50Ω loads

68 pin LCC (Ceramic)



Structure

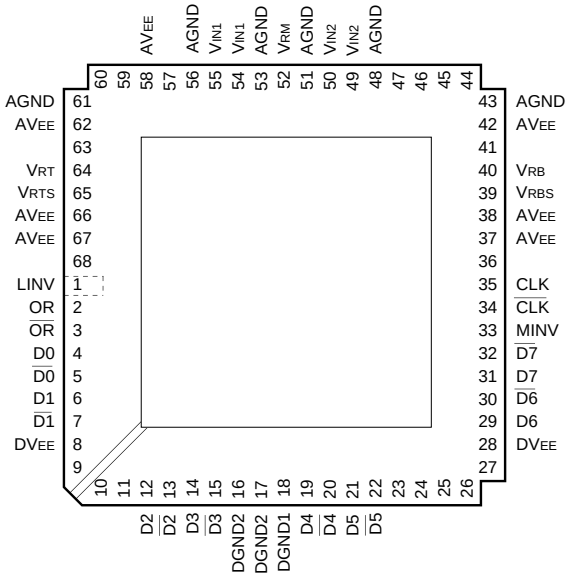
Bipolar silicon monolithic IC

Applications

- Digital oscilloscopes
- Other apparatus requiring ultrahigh-speed A/D conversion

Pin Configuration (Top View)

Pins without name are NC pins (not connected internally).



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E90406-ST

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Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	–7 to +0.5	V
• Analog input voltage	V_{IN}	–2.7 to +0.5	V
• Reference input voltage	V_{RT}, V_{RB}, V_{RM}	–2.7 to +0.5	V
	$\lvert V_{RT} - V_{RB} \rvert$	2.5	V
• Digital input voltage	MINV, LINV, CLK, $\overline{CLK}$	–4 to +0.5	V
	$\lvert CLK - \overline{CLK} \rvert$	2.7	V
• V_{RM} pin input current	I_{VRM}	–3 to +3	mA
• Digital output current	ID_0 to ID_7, IOR, $\overline{ID_0}$ to $\overline{ID_7}$, $\overline{IOR}$	–30 to 0	mA
• Storage temperature	Tstg	–65 to +150	℃

Operating Conditions		Min.	Typ.	Max.	Unit
• Supply voltage	AV_{EE}, DV_{EE}	–5.5	–5.2	–4.95	V
	$AV_{EE} - DV_{EE}$	–0.05	0	0.05	V
	AGND – DGND	–0.05	0	0.05	V
• Reference input voltage	V_{RT}	–0.1	0	0.1	V
	V_{RB}	–2.2	–2.0	–1.8	V
• Analog input voltage	V_{IN}	V_{RB}		V_{RT}	
• Operating temperature	Tc	–20		100	℃

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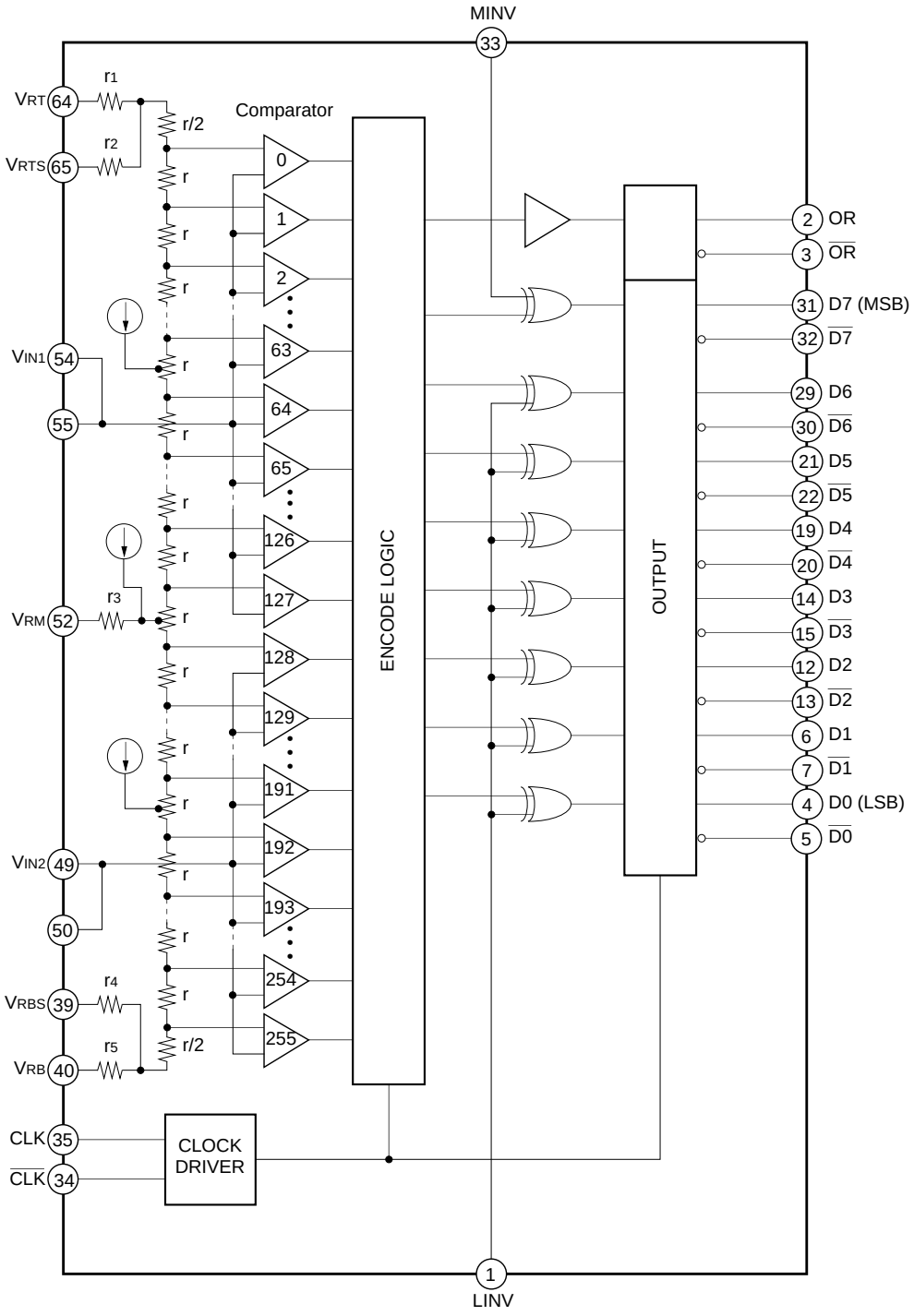
Block Diagram



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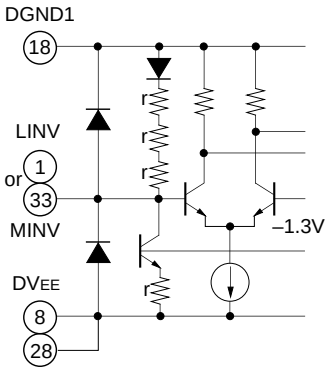
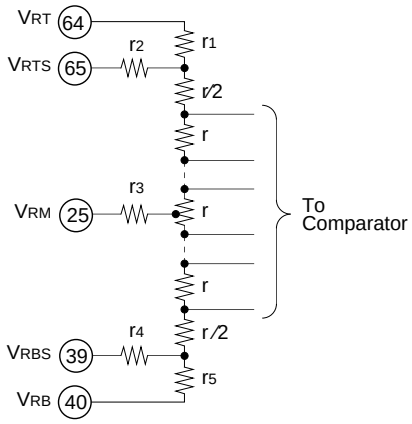
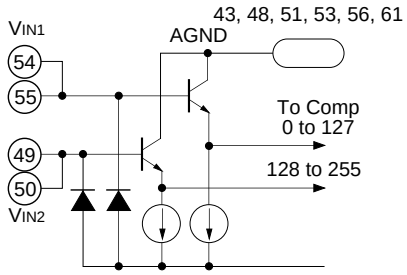
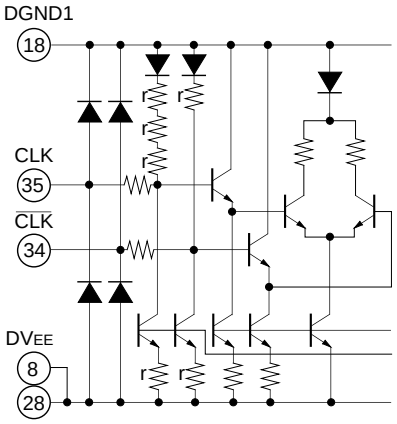
Pin Description

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
1	LINV	I	ECL		Polarity selection other than MSB and overrange. (Refer to the table of input voltage vs. Digital output) Low level is maintained with left open.
33	MINV	I	ECL		Polarity selection for MSB (Refer to the table of input voltage vs. Digital output) Low level is maintained with left open.
64	V_{RT}	I	0V		Reference voltage (Top) (0V typ.)
65	V_{RTS}	O	0V		Reference voltage sense (Top)
52	V_{RM}	I	V_{RB}/2		Reference voltage mid-point. Can be used for linearity compensation.
39	V_{RBS}	O	–2V		Reference voltage sense (Bottom)
40	V_{RB}	I	–2V		Reference voltage (Bottom)
54 55	V_{IN1}	I	V_{RTS} to V_{RBS}		Analog input. Pins 49, 50 and Pins 54, 55 should be connected externally.
49 50	V_{IN2}				
35	CLK	I	ECL		CLK input
34	$\overline{CLK}$	I	ECL		Complementary CLK input. ECL threshold potential (–1.3V) is maintained with left open. The complementary input is recommended for stable operation at high speed though the operation only with the CLK input is possible when the $\overline{CLK}$ input is left open.

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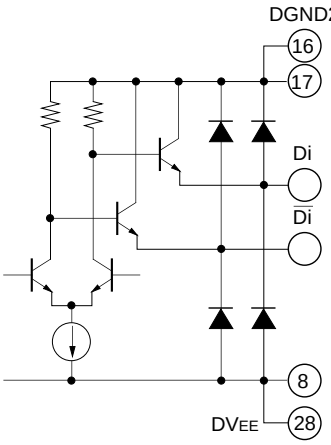
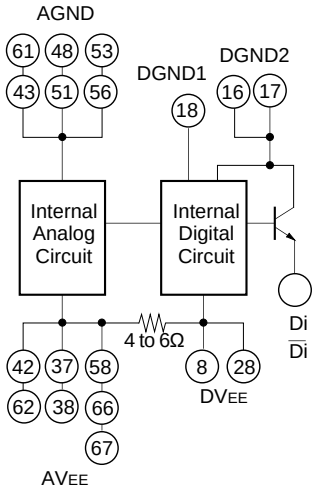
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
31 32	$\overline{D_7}$ D_7	O	ECL		MSB and complementary MSB output
29 30	$\overline{D_6}$ D_6	O			D_1 to D_6: Output $\overline{D_1}$ to $\overline{D_6}$: Complementary output
21 22	$\overline{D_5}$ D_5	O			
19 20	$\overline{D_4}$ D_4	O			
14 15	$\overline{D_3}$ D_3	O			
12 13	$\overline{D_2}$ D_2	O			
6 7	$\overline{D_1}$ D_1	O			
4 5	$\overline{D_0}$ D_0	O			LSB and complementary LSB output
2 3	$\overline{OR}$ OR	O			Overrange output; Low level for overrange. Overrange complementary output; High level for overrange.
37, 38, 42, 58, 62, 66, 67	AVEE*		–5.2V		Analog supply. Internally connected with DVEE (resistance: 4 to 6Ω).
43, 48, 51, 53, 56, 61	AGND*		0V		Analog ground. Separated from DGND.
8 28	DVEE*		–5.2V		Digital supply. Internally connected with AVEE (resistance: 4 to 6Ω).
18	DGND1		0V		Digital ground
16 17	DGND2*		0V		Digital ground for output drive
41, 44, 45, 46, 47, 57, 59, 60, 63	NC		—		No connected. It is recommended to connect these pins to AGND.
9, 10, 11, 23, 24, 25, 26, 27, 36, 68	NC		—		No connected. It is recommended to connect these pins to DGND.

* For stable operation, all of these pins must be connected on the corresponding PCB pattern.

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Electrical Characteristics (AV_{EE} = DV_{EE} = –5.2V, V_{RT}, V_{RTS} = 0V, V_{RB}, V_{RBS} = –2V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution				8		bits
DC characteristics						
Integral linearity error	E_{IL}				±0.5	LSB
Differential linearity error	E_{DL}				±0.5	LSB
Analog input						
Analog input capacitance	C_{IN}	V_{IN} = –1V + 0.07Vrms		18		pF
Analog input resistance	R_{IN}	V_{IN} = –1V	50	120		kΩ
Input bias current	I_{IN}	V_{IN} = –1V	20		450	µA
Reference inputs						
Reference resistance	R_{REF}		83	125	182	Ω
Residual resistance∗1 r_1	r_1		0.1	0.6	2.0	Ω
r_2	r_2		300	500	700	Ω
r_3	r_3		0.5	2.0	5.0	Ω
r_4	r_4		300	500	700	Ω
r_5	r_5		0.1	0.6	2.0	Ω
Digital inputs						
Logic High level	V_{IH}		–1.13			V
Logic Low level	V_{IL}				–1.50	V
Logic High current	I_{IH}	V_{IH} = –0.8V	0		70	µA
Logic Low current	I_{IL}	V_{IL} = –1.6V	–50		50	µA
Input capacitance				4		pF
Switching characteristics						
Maximum conversion rate	Fc		250			MSPS
Aperture jitter	Taj			9		ps
Sampling delay	Tds		0.4	1.4	2.4	ns
Output delay	Tdo	R_L = 50Ω to –2V	1.8	2.5	3.2	ns
Clock High pulse width	T_{PW1}	T_{PW1} + T_{PW0} = 4.0ns	1.8			ns
Clock Low pulse width	T_{PW0}	T_{PW1} + T_{PW0} = 4.0ns	1.8			ns
Digital output						
Logic High level	V_{OH}	R_L = 50Ω to –2V	–1.00			V
Logic Low level	V_{OL}	R_L = 50Ω to –2V			–1.60	V
Output rise time	Tr	R_L = 50Ω to –2V		0.6	1.5	ns
Output fall time	Tf	R_L = 50Ω to –2V		0.6	1.5	ns
Dynamic characteristics						
Input bandwidth		V_{IN}=2Vp-p	200			MHz
SNR	SNR	Input = 1kHz, FS, Clock = 250MHz	44	46		dB
		Input = 62.499MHz, FS, Clock = 250MHz	30	35		dB
Error rate		Input = 49.999MHz, FS, Error > 16LSB, Clock = 200MHz			10^{-9}	TPS∗2
		Input = 62.499MHz, FS, Error > 16LSB, Clock = 250MHz		10^{-8}	10^{-6}	TPS∗2
Differential gain error	DG	NTSC 40IRE mod. ramp, Fc = 250MSPS		1.0		%
Differential phase error	DP	NTSC 40IRE mod. ramp, Fc = 250MSPS		0.5		deg
Power supply						
Supply current	I_{EE}		–360	–270		mA
Power consumption∗3	Pd			1.4	1.9	W

∗1 See Block Diagram.

∗2 TPS: Times Per Sample

∗3 $Pd = I_{EE} \bullet V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$

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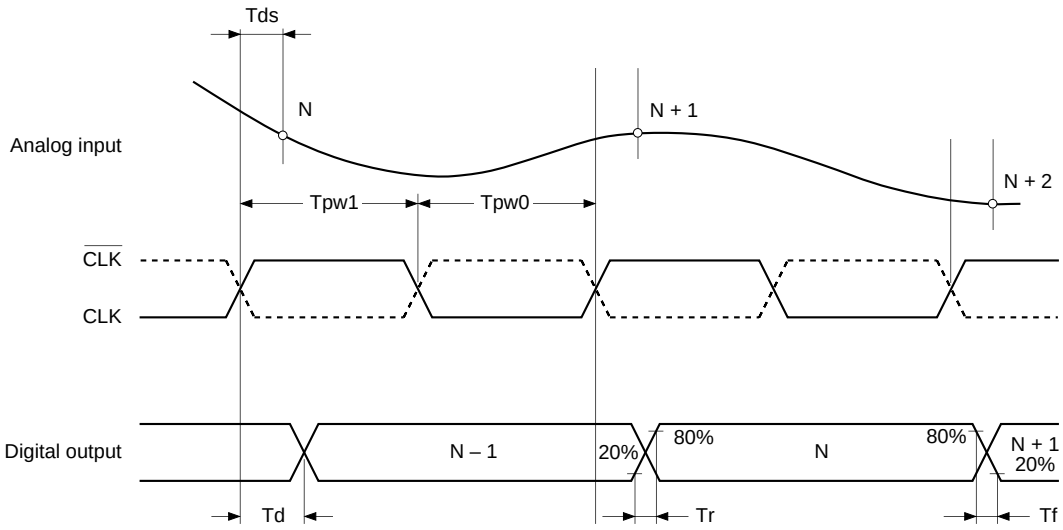
Input Voltage vs. Digital Output

V_{IN}*	Step	MINV 1 LINV 1		0 1		1 0		0 0	
		OR	D7 D0	OR	D7 D0	OR	D7 D0	OR	D7 D0
0V		0	0 0 0 ..... 0 0	0	1 0 0 ..... 0 0	0	0 1 1 ..... 1 1	0	1 1 1 ..... 1 1
	0	1	0 0 0 ..... 0 0	1	1 0 0 ..... 0 0	1	0 1 1 ..... 1 1	1	1 1 1 ..... 1 1
	1	1	0 0 0 ..... 0 1	1	1 0 0 ..... 0 1	1	0 1 1 ..... 1 0	1	1 1 1 ..... 1 0
			:		:		:		:
			:		:		:		:
–1V	127	1	0 1 1 ..... 1 1	1	1 1 1 ..... 1 1	1	0 0 0 ..... 0 0	1	1 0 0 ..... 0 0
	128	1	1 0 0 ..... 0 0	1	0 0 0 ..... 0 0	1	1 1 1 ..... 1 1	1	0 1 1 ..... 1 1
		:	:	:	:	:	:	:	:
		:	:	:	:	:	:	:	:
	254	1	1 1 1 ..... 1 0	1	0 1 1 ..... 1 0	1	1 0 0 ..... 0 1	1	0 0 0 ..... 0 1
	255	1	1 1 1 ..... 1 1	1	0 1 1 ..... 1 1	1	1 0 0 ..... 0 0	1	0 0 0 ..... 0 0
–2V		1	1 1 1 ..... 1 1	1	0 1 1 ..... 1 1	1	1 0 0 ..... 0 0	1	0 0 0 ..... 0 0

* $V_{RT} = V_{RTS} = 0V$, $V_{RM} = -1V$ or Open, $V_{RB} = V_{RBS} = -2V$

Timing Diagram



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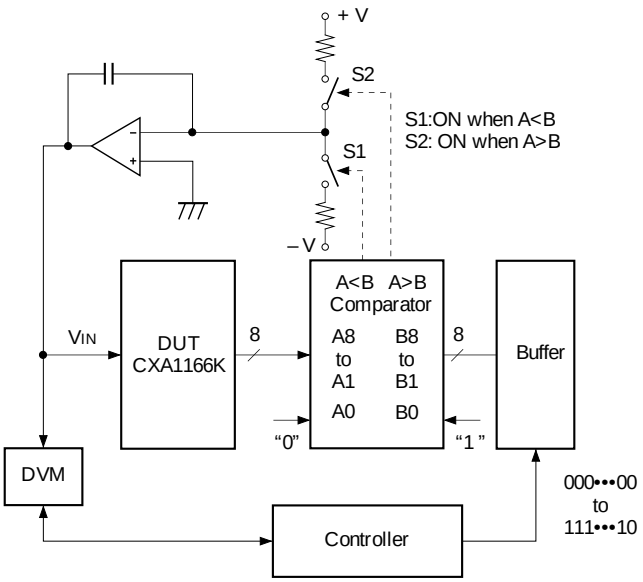
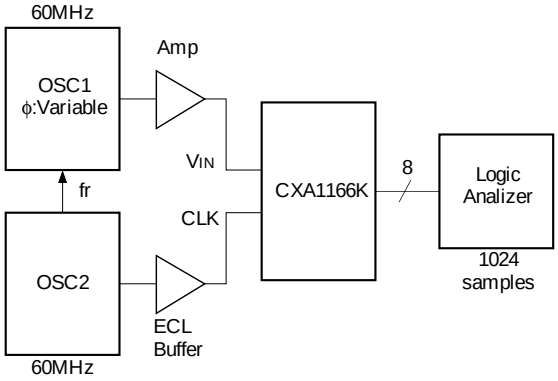
Electrical Characteristics Measurement Circuit

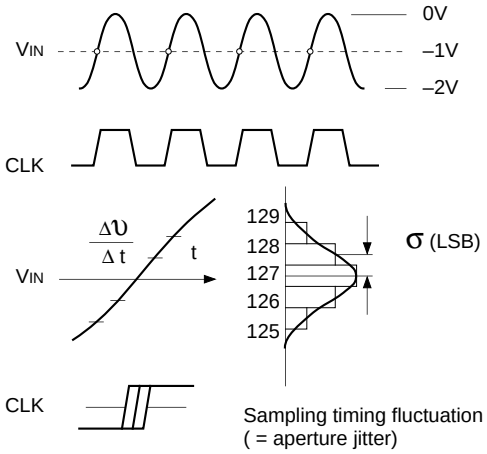
Integral Linearity Error Measurement Circuit
Differential Linearity Error Measurement Circuit



Sampling Delay Measurement circuit
Aperture Jitter Measurement circuit



Aperture Jitter Measurement Method



When the distribution of the output codes is σ (unit: LSB) If the maximum slew rate point is sampled with the clock signal having the same frequency as that of the analog input signal, Aperture jitter (Taj) is defined as follows:

$$Taj = \sigma / \frac{\Delta \upsilon}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f \right)$$

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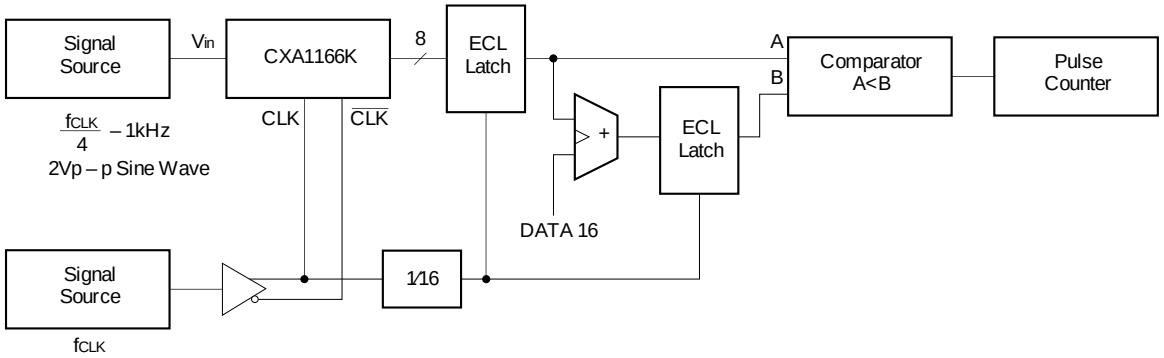
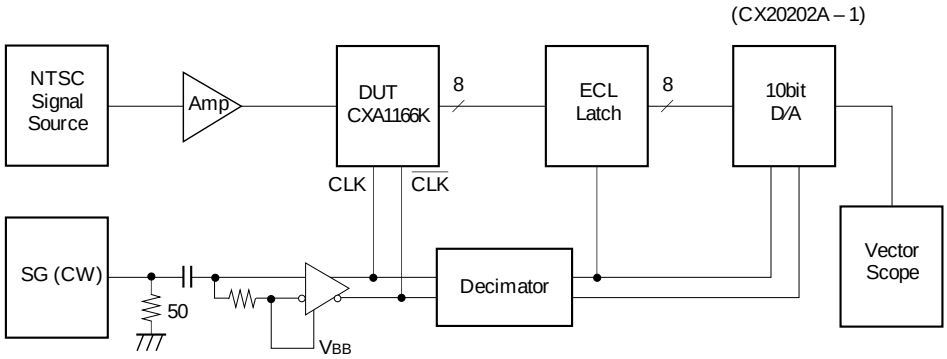
Error Rate Measurement Circuit



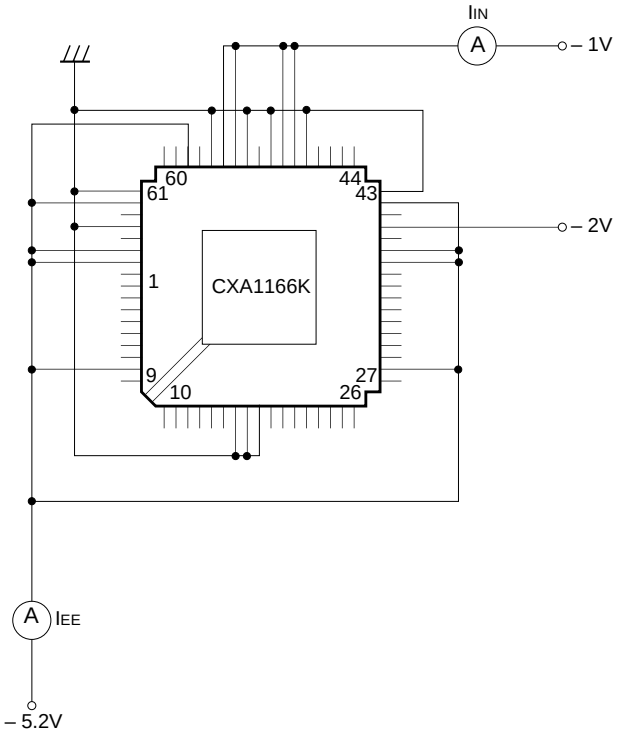
Differential Gain Error Measurement Circuit

Differential Phase Error Measurement Circuit



Power Supply Current Measurement Circuit

Analog Input Bias Current Measurement Circuit



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Notes on Operation

- The CXA1166K is an ultra-high speed A/D converter featuring ECL level of input/output for the logic block. In order to derive the most from its high-speed performance, the characteristic impedance should be matched properly.

- The outputs are designed to drive a load terminated to –2V at 50Ω. An excellent transmission characteristic can be yielded by designing the printed circuit board with a 50Ω characteristic impedance.
  Yielding its top performance is difficult on the printed circuit board with a characteristic impedance of 100Ω or more.

- The power supply and ground pattern greatly affect the characteristics of the converter. The higher the frequency, the more important these connections become. The general precautions are as follows.
  – Make the pattern of the power supply and ground as wide as possible. Using a ground plane inner layer by using a multilayer printed circuit board is recommended.
  – Isolate the AGND, DGND pins and the AV_{EE}, DV_{EE} from one another on the pattern in order to safeguard against interaction. Connect the AGND and DGND pins at one place using a ferrite-bead filter to prevent DC offset. The same processing is requited for the AV_{EE} and DV_{EE} pins.

- When mounting the A/D converter on the socket, use the one of shortest leads. The QFP socket, the type name IC61-0684-048, manufactured by YAMAICHI ELECTRONICS CO., LTD. is recommended.

- The V_{IN} analog input pins have somewhat large input capacitance (approximately 18pF) for high-frequency circuits. In order to drive them with an excellent frequency response, it is necessary to safeguard against any deterioration in performance resulting from parasitic capacitance and parasitic inductance by using a high-capacity drive circuit, keeping the wiring as short as possible, and using chip parts as resistors and capacitors, for instance. The drive circuit shown in the Application Circuit has a virtually flat frequency response up to approximately 170MHz. C89, R11 and C15 have been inserted mainly to expand the bandwidth, while R10 has been inserted mainly to suppress operational amplifier oscillation and block peaking of the frequency response. Since the optimal values of these elements differ depending on the printed circuit board pattern and mounting condition of the A/D converter socket used, they must be determined on the basis of experimentation.

- Connect all four V_{IN} pins directly and as short as possible. Unlike the CXA1176, it is not necessary to insert resistance of several ohms for each pin.

- The voltage at the V_{RT} and V_{RB} reference voltage pins and the reference voltage inside these pins differ slightly due to residual resistance. V_{RTS} and V_{RBS} are provided to detect the reference voltage inside the pins. The overrange reference voltage is 1/2 LSB down from V_{RTS}; the lowest input voltage at which the output code changes is 1/2 LSB up from V_{RBS}.

- Provide adequate by-pass capacitors for V_{RT} and V_{RB} to protect them from high-frequency noise. Normally, V_{RT} is connected to AGND of an inner layer of the printed circuit board. Using a chip capacitor (approximately 0.1µF), make the by-pass from V_{RB} to AGND as short as possible. C22 (1µF), in the Application Circuit is for suppressing the oscillation of the reference voltage generation circuit.

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- Unlike the CXA1176, V_{RTS} and V_{RBS} are connected to the reference resistors via resistors of approximately 500Ω. Since these resistors may be eliminated in the future improved versions of this converter, use a reference voltage generation circuit which is adaptable to their elimination. The reference voltage generation circuit (the section composed of IC12_2, etc.) in the Application Circuit is recommended.

- Although V_{RM} is provided to compensate for the integral linearity error, there is no need for such compensation. It is recommended that it is kept open.

- OR and $\overline{OR}$ are output pins for indicating that the input is over range. They are not inverted by MINV or LINV.

- Noise in MINV and LINV results in misoperation, the cause of which is extremely difficult to track down. Keep these pins open in cases where low level setting voltage alone is sufficient. When high level voltage input is required, provide the shortest possible by-pass from them to DGND using chip capacitors (approximately 0.1µF). Input voltages of –0.5V to –1.0V for high level and –1.6V to –2.5V for low level are recommend. Do not make the direct connection to DGND when high level voltage is input.

- Inputting differential signals is recommended for the CLK and $\overline{CLK}$ clock input pins. Although operation is possible by driving only the CLK pin, doing so involves the risk that the characteristics may become unstable near the maximum speed. This is because the internal operation of the A/D converter depends on both clock rise and fall.

- When the $\overline{CLK}$ pin is not used, by-pass it to DGND using a capacitor (approximately 0.1µF). At this time, approximately –1.3V voltage will be generated at this pin. However, the driving capacity is too weak for this to be used as the V_{BB} threshold voltage. It cannot drive even one ECL input load.

- This converter is designed to be used at the clock duty cycle of 50%. The deviation from this condition will subtly affect the performance of the A/D converter but the degree of the affection is not so great as to require adjustment. The “Error rate vs. Clock duty cycle characteristics” graph shows an example of these changes in the converter’s performance.

- Increasing chip temperature will cause the supply current and also the error rate to rise. Adding to these reasons, in order to prolong the converter’s service life, provide an adequate means of cooling. See the “Maximum conversion frequency vs. Temperature characteristics” and “Supply current vs. Temperature characteristics” graphs. The reference data for thermal resistance is shown in the “Thermal resistance of the converter mounted on a board” graph. Note that the actual thermal resistance will differ greatly depending on the mounting conditions.

- Since the CXA1166K is a high-speed IC, take adequate measures to prevent electrostatic breakdown. For further details on these measures, refer to “Precautions for IC Application” in Sony’s Data book.

- Sony’s SPECL series is used as the logic ICs in the Application Circuit to investigate the maximum performance of the CXA1166K. For normal applications, lower speed logic ICs can be used according to the applied frequency.

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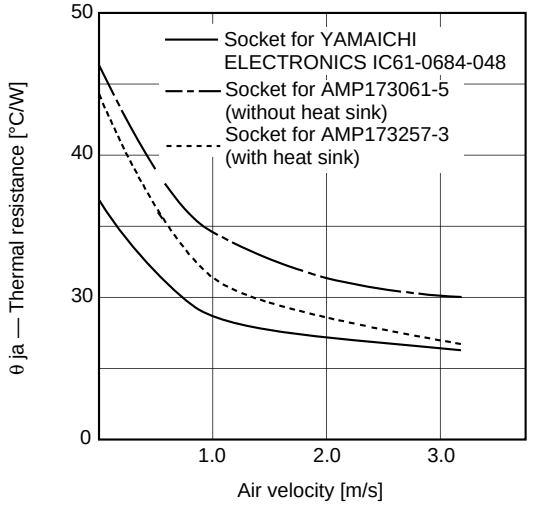
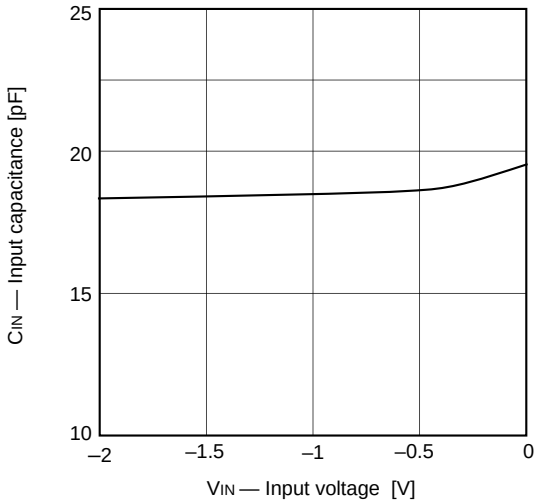
Example of Representative Characteristics

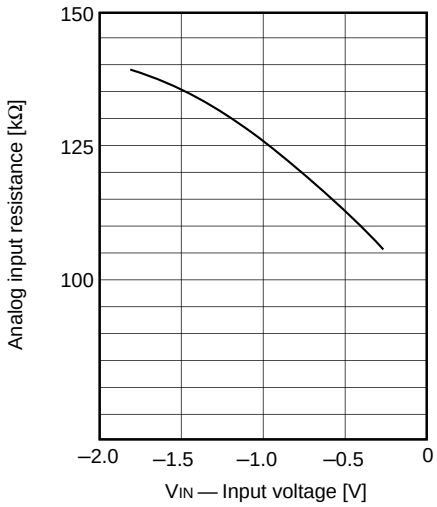
Thermal resistance at on-board condition



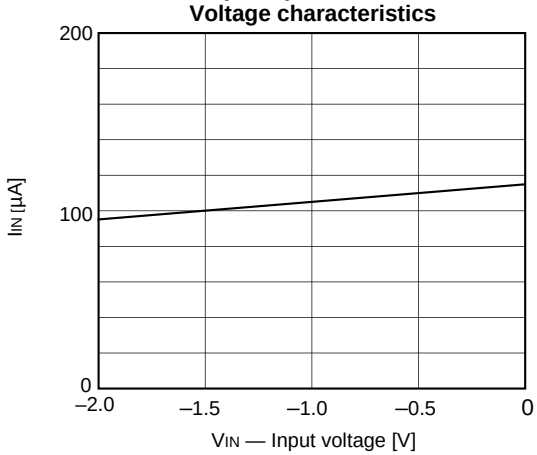
VIN pin input capacitance vs. Voltage characteristics



VIN pin input resistance vs. Voltage characteristics



VIN pin input current vs. Voltage characteristics



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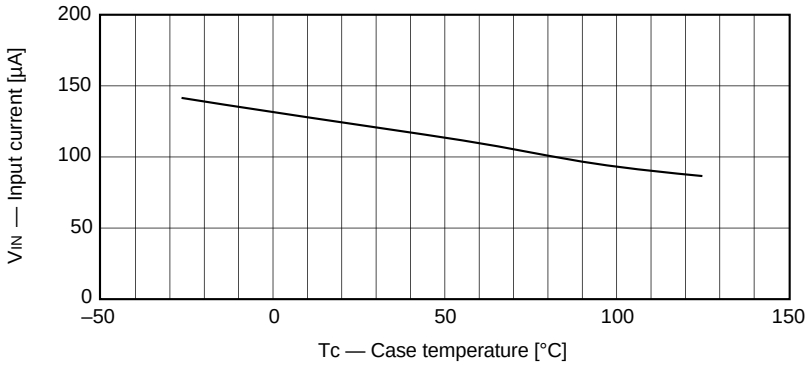
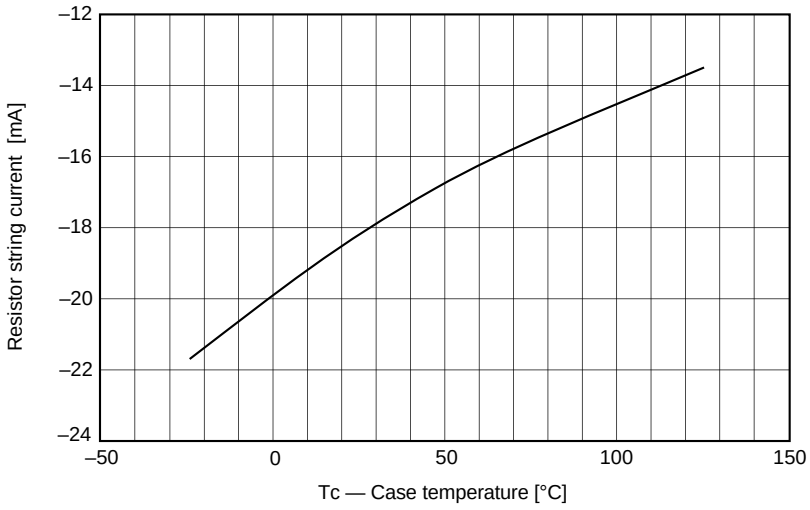
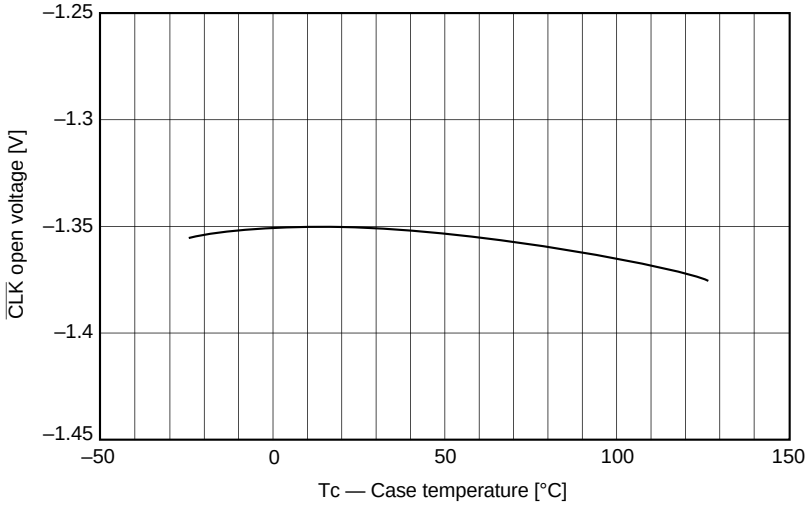
V_{IN} pin input current vs. Temperature characteristics



Resistor string current vs. Temperature characteristics



$\overline{CLK}$ open voltage vs. Temperature characteristics



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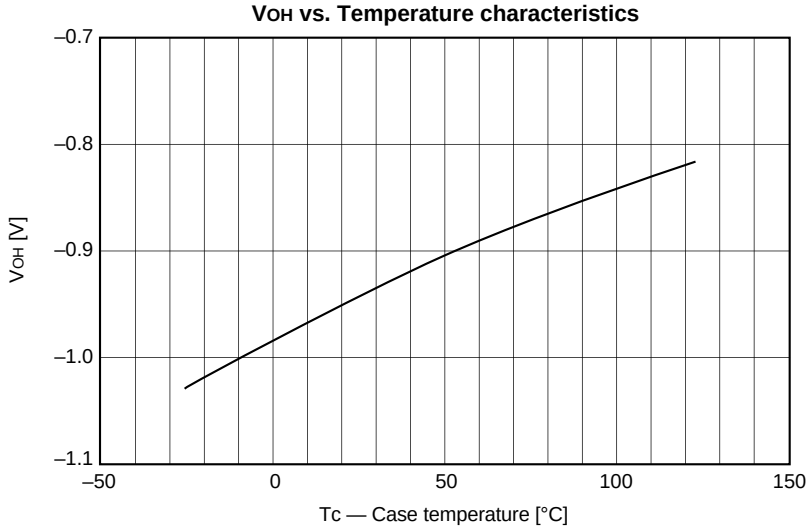
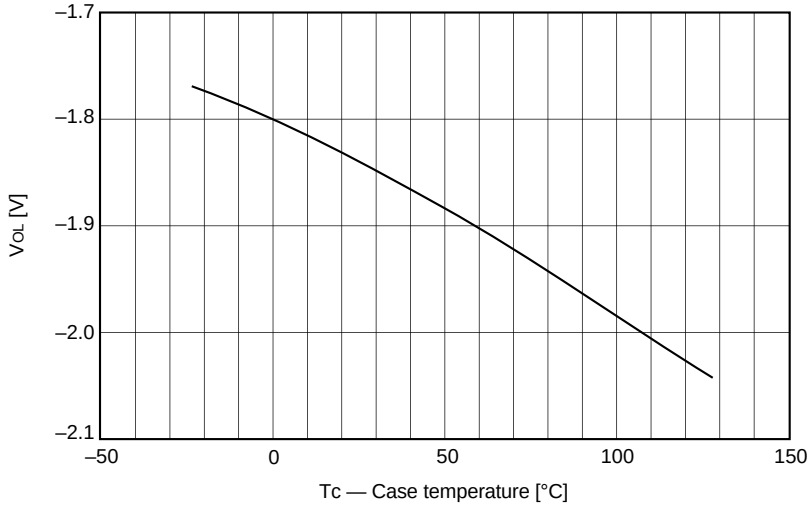
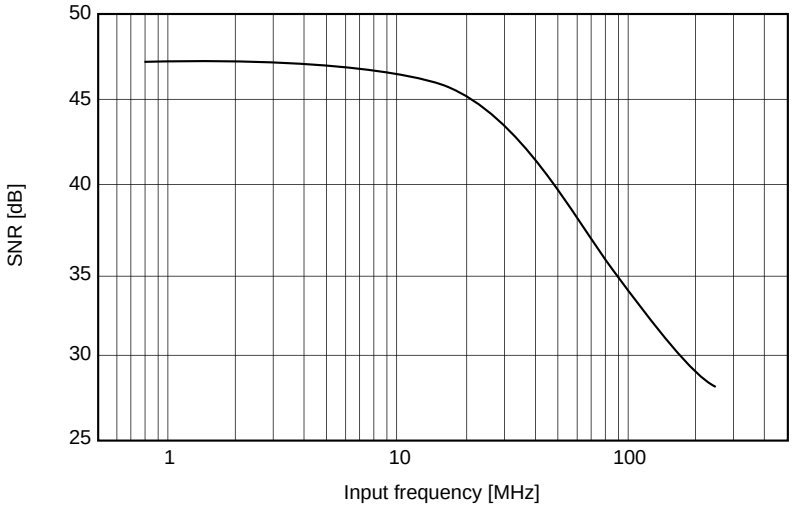
V_{OH} vs. Temperature characteristics



V_{OL} vs. Temperature characteristics



SNR vs. Input frequency response characteristics



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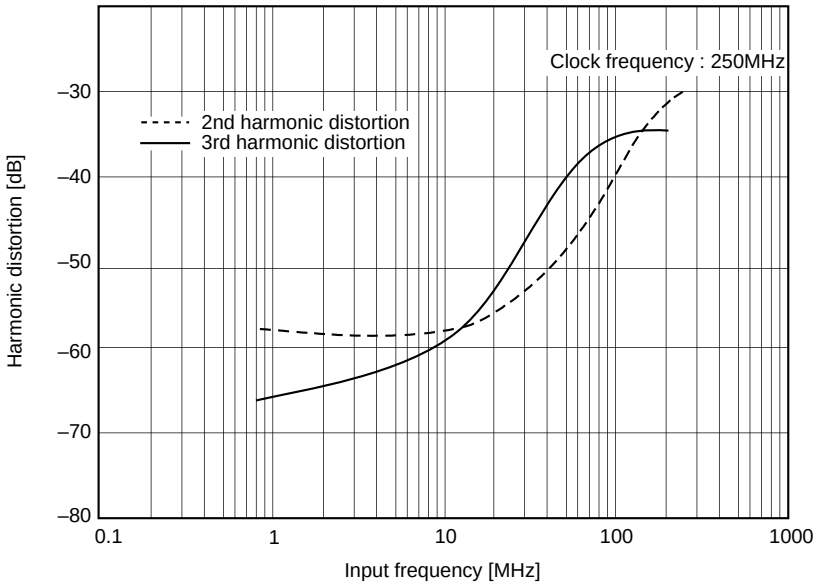
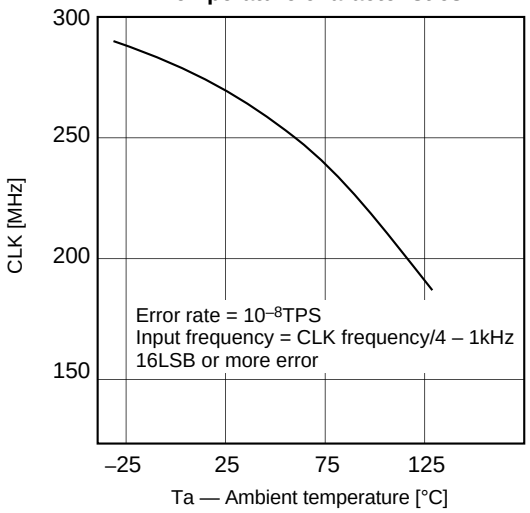
Harmonic distortion vs. Input frequency response characteristics



Maximum conversion rate vs. Temperature characteristics



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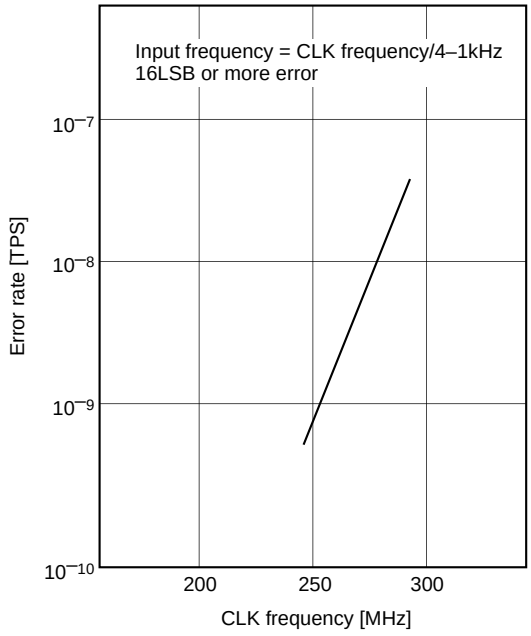
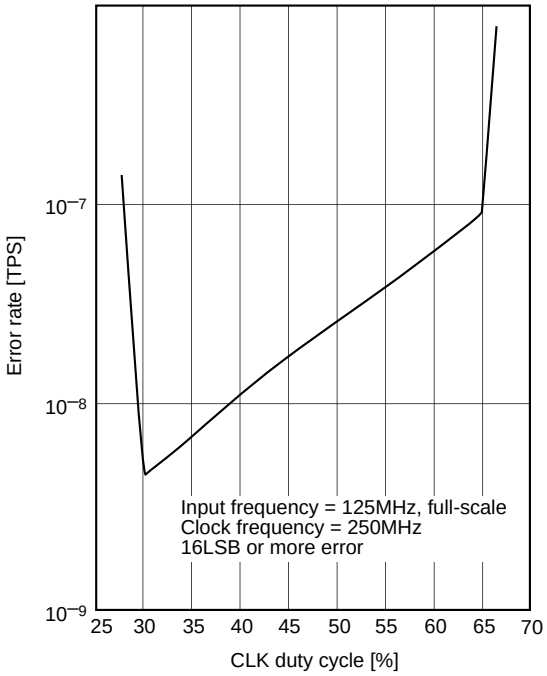
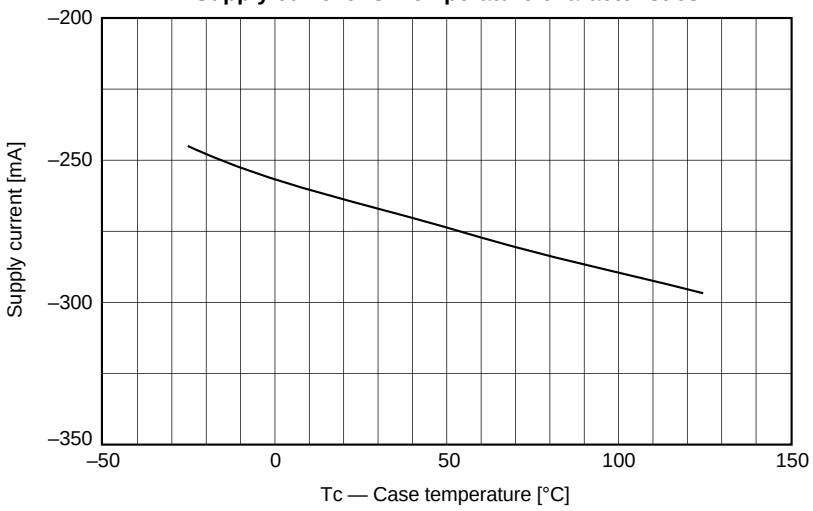
Error rate vs. Conversion rate



Error rate vs. Clock duty cycle



Supply current vs. Temperature characteristics



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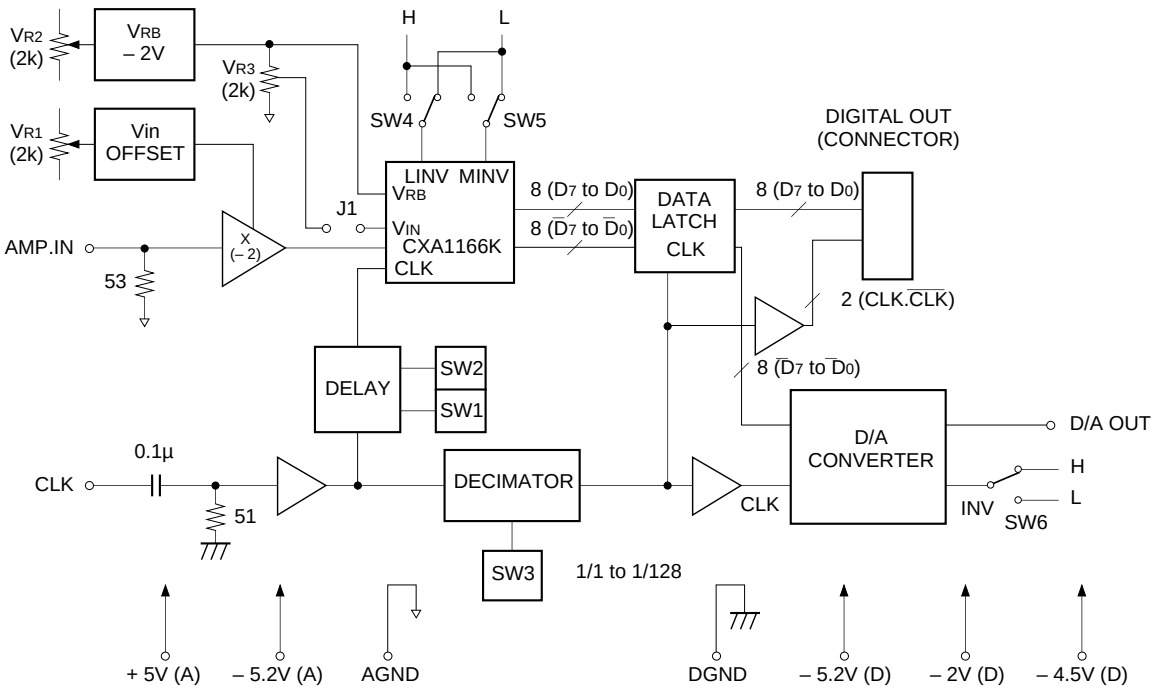
8-bit, 250 MSPS ADC Evaluation Board

The CXA1166K PCB is a tool for customers to evaluate the performance of the CXA1166K (8-bit, 250MHz, high-speed A/D converter). In addition to indispensable features such as the reference voltage generator, this tool equips the input voltage offset generator, clock decimator, output date latches, 10-bit high-speed DAC, and 20-pin cable connector for digital outputs. This evaluation board is designed to facilitate evaluation.

Features

- Resolution: 8 bits
- Maximum conversion rate: 250 MSPS
- Supply voltage: –5.2V, –4.5V, –2.0V, +5.0V
- Clock level converter: Sine wave to ECL level signal
- Reference voltage adjustment circuit for A/D converter
- Built-in clock frequency decimation circuit: 1/1 to 1/128

Fig. 1. Block Diagram



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Supply Current

Item	Min.	Typ.	Max.	Unit
–5.2V		0.65	0.9	A
+5.0V		17	40	mA
–4.5V		0.9	1.1	A
–2.0		0.7	0.9	A

Analog Input (AMP. IN)

Item	Min.	Typ.	Max.	Unit
Input voltage (AMP.IN) ∗	–2.0		0	V
Input impedance		50		Ω

(∗ Adjustable with VR1)

Clock input (CLK)

Item	Min.	Typ.	Max.	Unit
Input voltage (Peak to Peak)		2.0		Vp-p
Input impedance		50		Ω

Digital output (Digital OUT)

ECL level

Output Code Table

1: ECL High level, 0: ECL Low level

	MINV (SW5) / LINV (SW4)	0 / 0	0 / 1	1 / 0	1 / 1
V_{IN}	0V	1 1 1 ..... 1 1	1 0 0 ..... 0 0	0 1 1 ..... 1 1	0 0 0 ..... 0 0
	:	1 1 1 ..... 1 0	1 0 0 ..... 0 1	0 1 1 ..... 1 0	0 0 0 ..... 0 1
	:	:	:	:	:
	:	:	:	:	:
	:	1 0 0 ..... 0 0	1 1 1 ..... 1 1	0 0 0 ..... 0 0	0 1 1 ..... 1 1
	:	0 1 1 ..... 1 1	0 0 0 ..... 0 0	1 1 1 ..... 1 1	1 0 0 ..... 0 0
	:	:	:	:	:
	:	:	:	:	:
	:	0 0 0 ..... 0 1	0 1 1 ..... 1 0	1 0 0 ..... 0 1	1 1 1 ..... 1 0
	–2V	0 0 0 ..... 0 0	0 1 1 ..... 1 1	1 0 0 ..... 0 0	1 1 1 ..... 1 1

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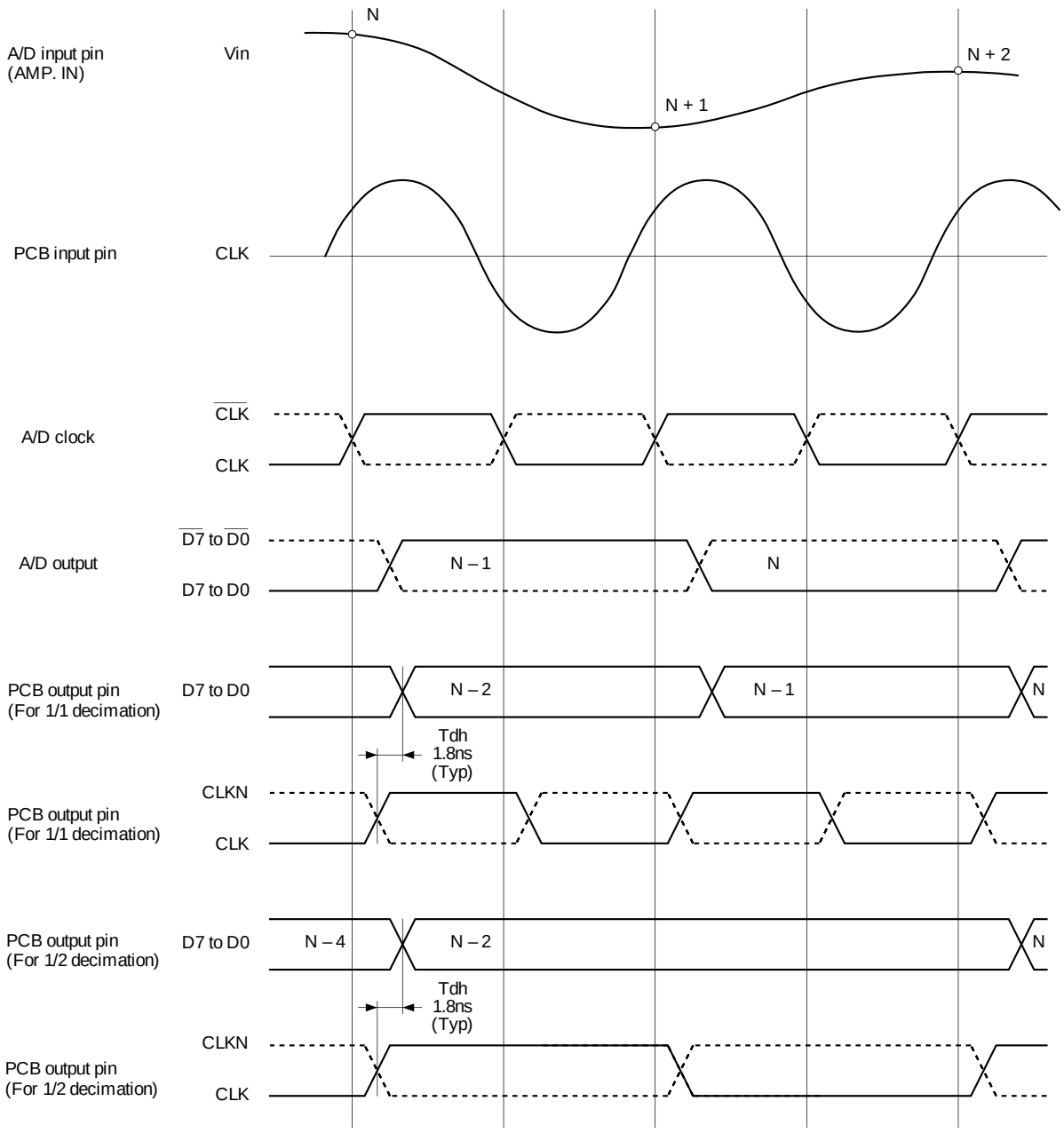
Fig. 2. Timing Diagram



Adjustment Methods and Notes on Operation

1) V_{IN} Offset (VR1)

The volume to adjust the AMP. IN signal range (0V center assumed) with the A/D converter input range.

2) A/D Full Scale (VR2)

The volume to adjust A/D converter V_{RB} voltage (–2V typ.).

3) Linearity (VR3)

The volume to adjust the VRM (linearity) voltage by shorting the J1.

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4) D/A Full Scale (VR4)
The volume to adjust the bottom of D/A output full scale voltage (–1V typ.)

5) SW1 and SW2
Selection switches to adjust the clock delay. These switches enable clock delay to be stepped to any one of 128 settings (binary code of “0000000” to “1111111”) through binary input. Approximately 163ps is delayed per one step. Normal evaluation requires the binary code of “0000000” (all of OFF), so that these switches are not mounted for shipment.

6) SW3 (Decimation)
The switch to select clock frequency decimation. Selection settings are as follows.

SW3			Decimation ratio
3	2	1	
L	L	L	1/1
L	L	H	1/2
L	H	L	1/4
L	H	H	1/8
H	L	L	1/16
H	L	H	1/32
H	H	L	1/64
H	H	H	1/128

∗ H = ECL High level ; L = ECL Low level

7) SW4
The switch for LINV High/Low.

8) SW5
The switch for MINV High/Low.

9) SW6 (D/A INV)
The switch for D/A converter output inversion.

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10) The waveform monitoring pins P6 through P39 are designed to make connection to GND easily in order to reduce distortion when monitoring the waveform with an oscilloscope. As shown in the diagram below, the distance between the measuring point and GND is 300mil, and each is equipped with a through hole of 1.2mm. When a Tektronix ground chip (part No. 013-1185-00) is mounted on the tip of a probe, the signal – GND positions match.

Fig. 3.

11) D/A converter (IC9) input data (waveform monitoring pins P28 to P35) are the negative logic signals of the decimated A/D converter outputs. Those are inverted again in the D/A converter so that the direction (rise/fall) of reproduced waveform can agree with the A/D input signal's.

12) In order to maintain the accuracy of the reproduced waveform (waveform from A/D to D/A), set the decimator such that the clock frequency of the D/A converter (IC9: CX20201A-1) is less than 100MHz.

13) The input bandwidth weighs with the design of this PCB analog input circuit. Therefore, the SNR (signal-to-noise ratio) should be less significant. The input circuit example to improve the SNR is shown in Fig.4. See the measured data in Fig.s 6 to 8 for the SNR and the input circuit characteristics.

14) The part number of the digital output connector mounted on the PCB is KEL 8830E-020-170S. A corresponding connector and cable assembly is JUNKOSHA KB0020MCG50B1.

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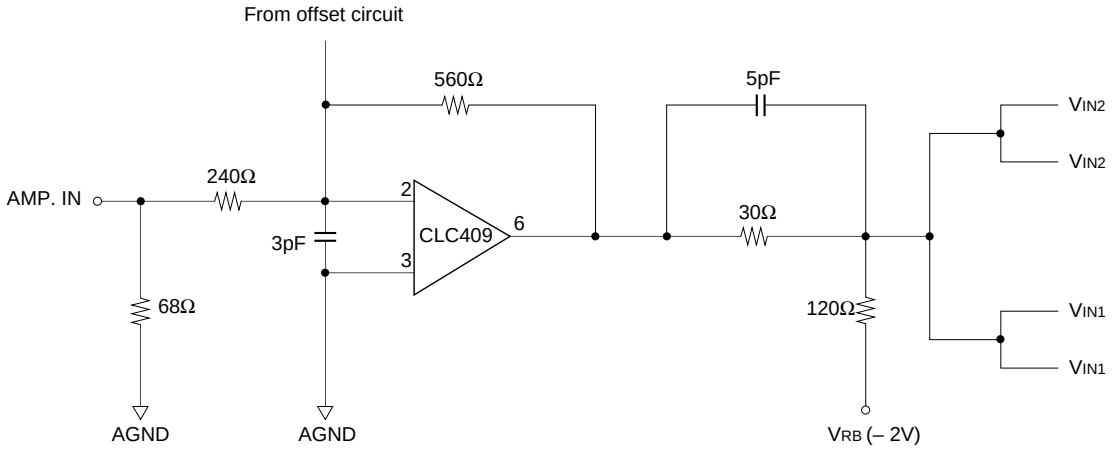

Fig. 4. Example of SNR Improvement Circuit

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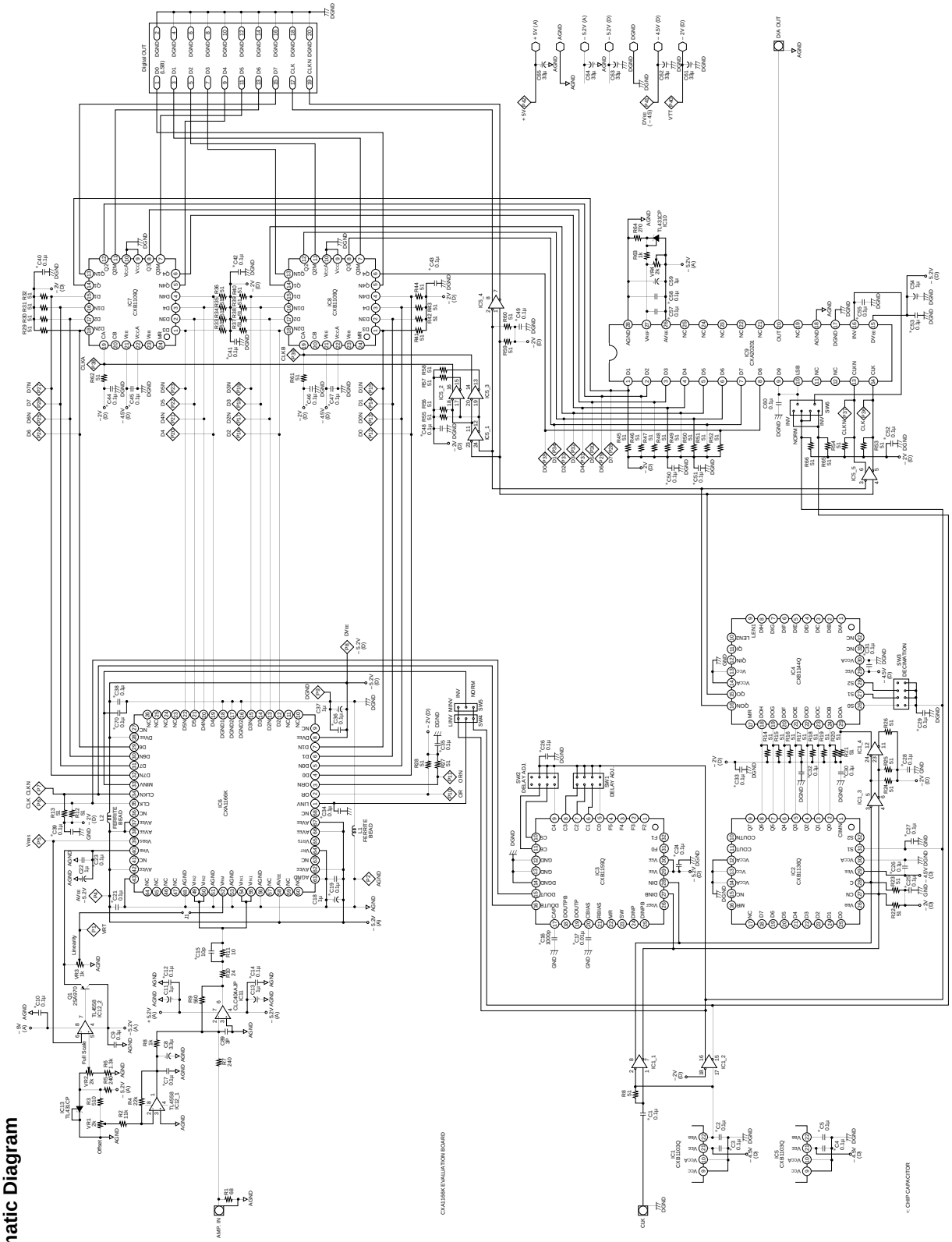

Fig. 5. Schematic Diagram

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Characteristics

Fig.6. Gain vs. Input frequency

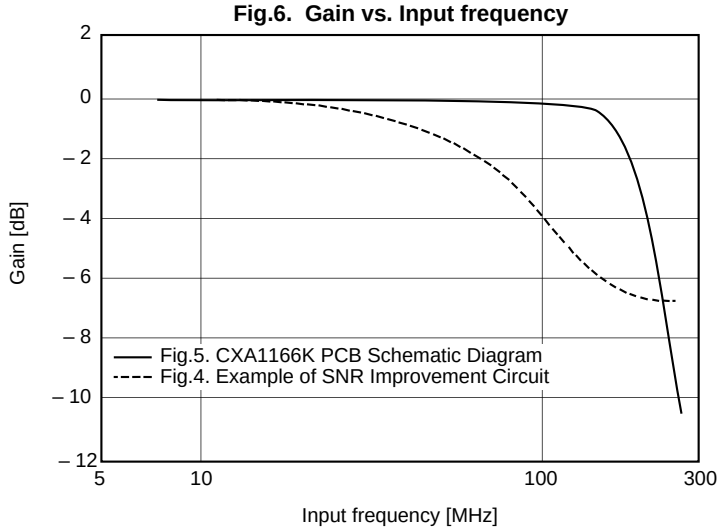


Fig.7. SNR vs. Input frequency

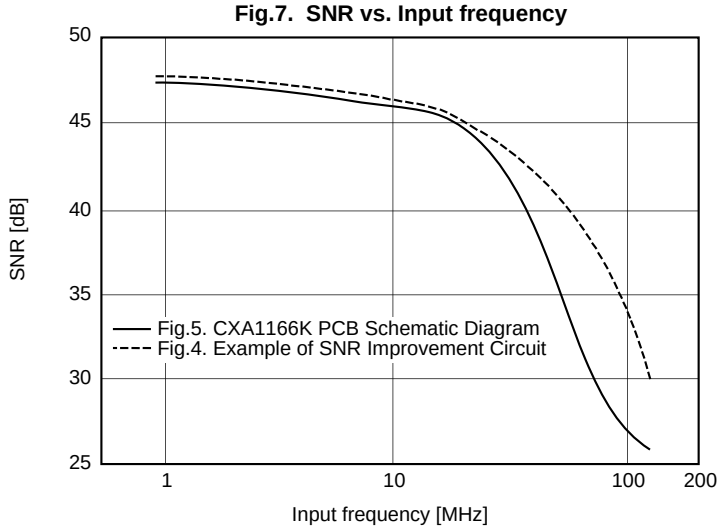
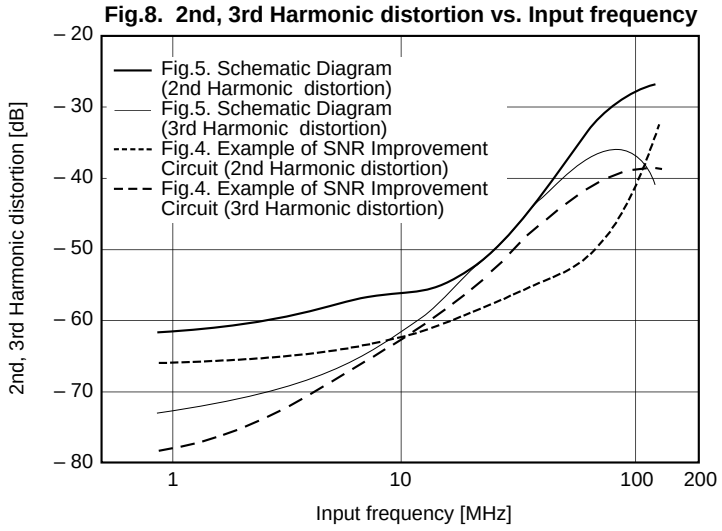


Fig.8. 2nd, 3rd Harmonic distortion vs. Input frequency



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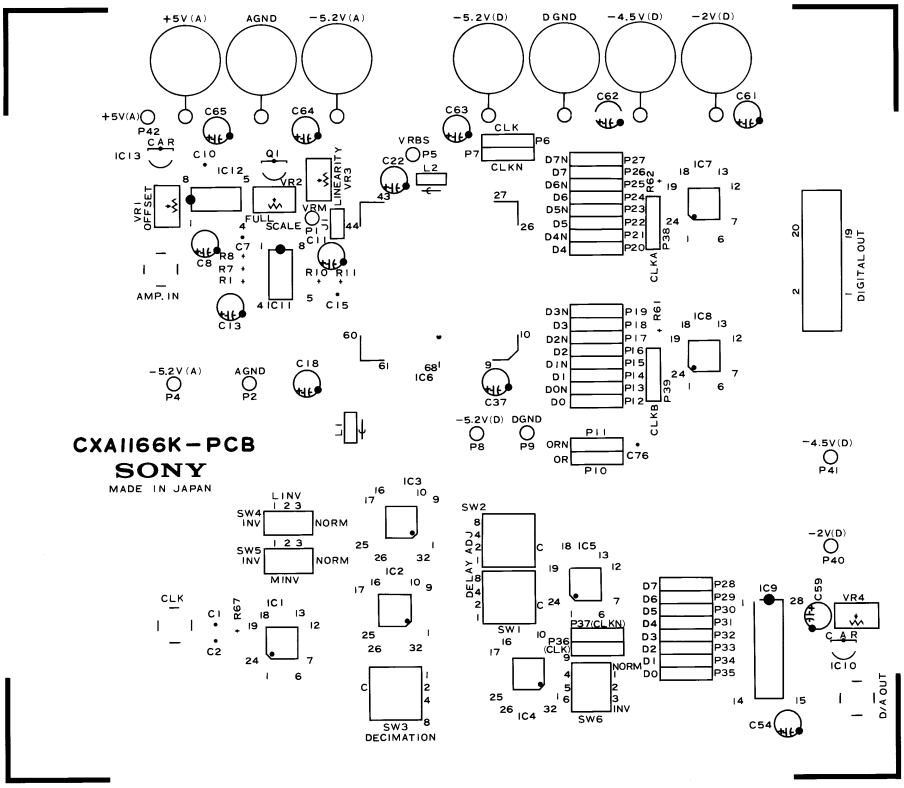
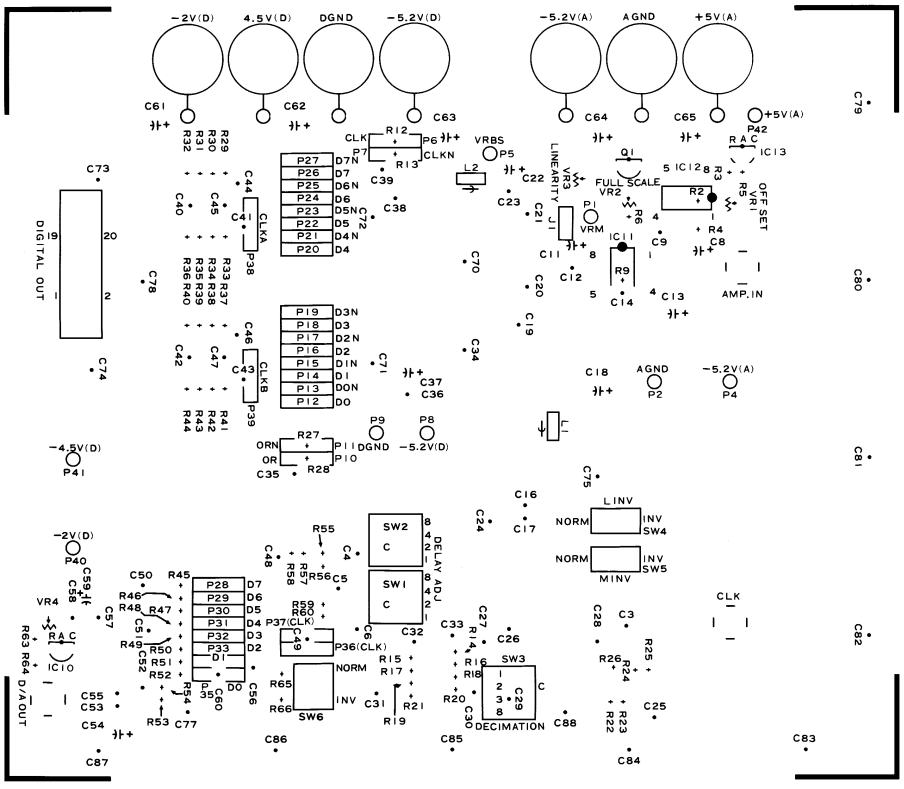
Parts Layout



Component side



Soldering side

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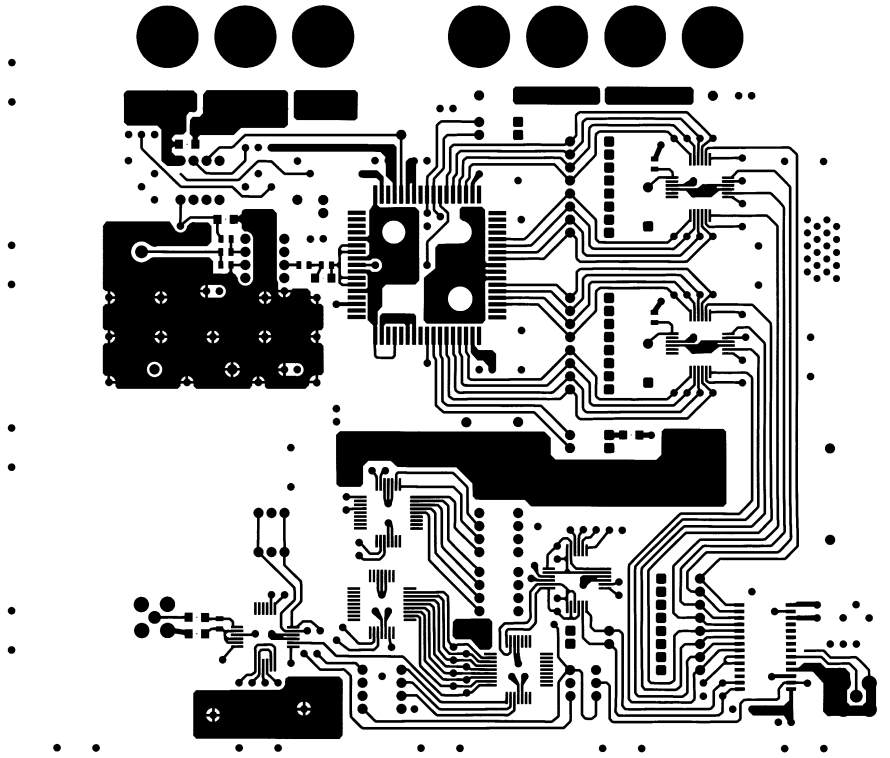
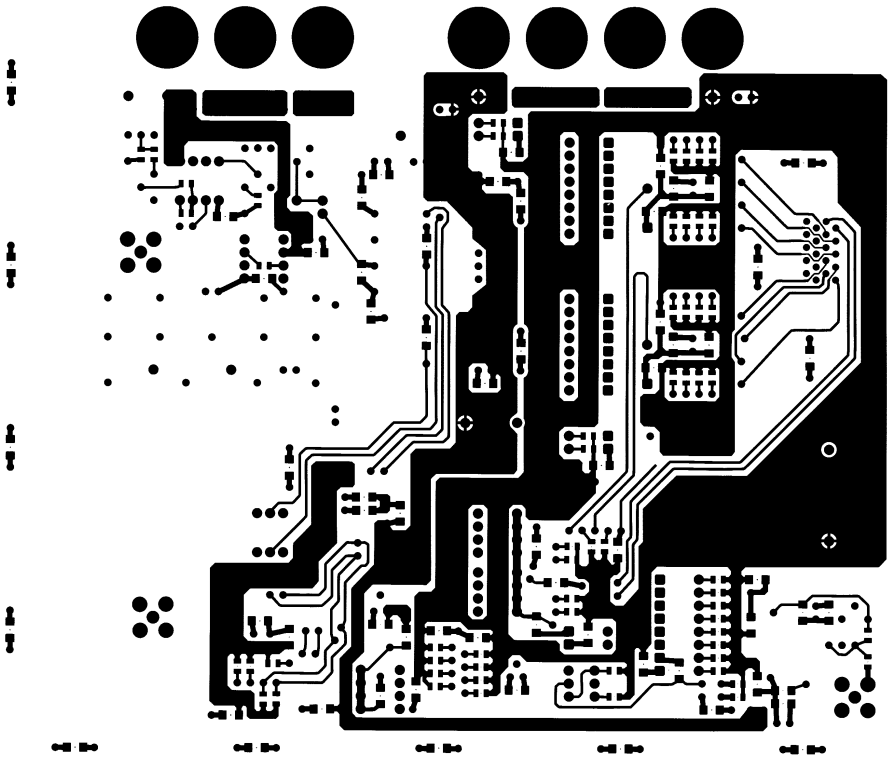
Printed Pattern



Component side



Soldering side

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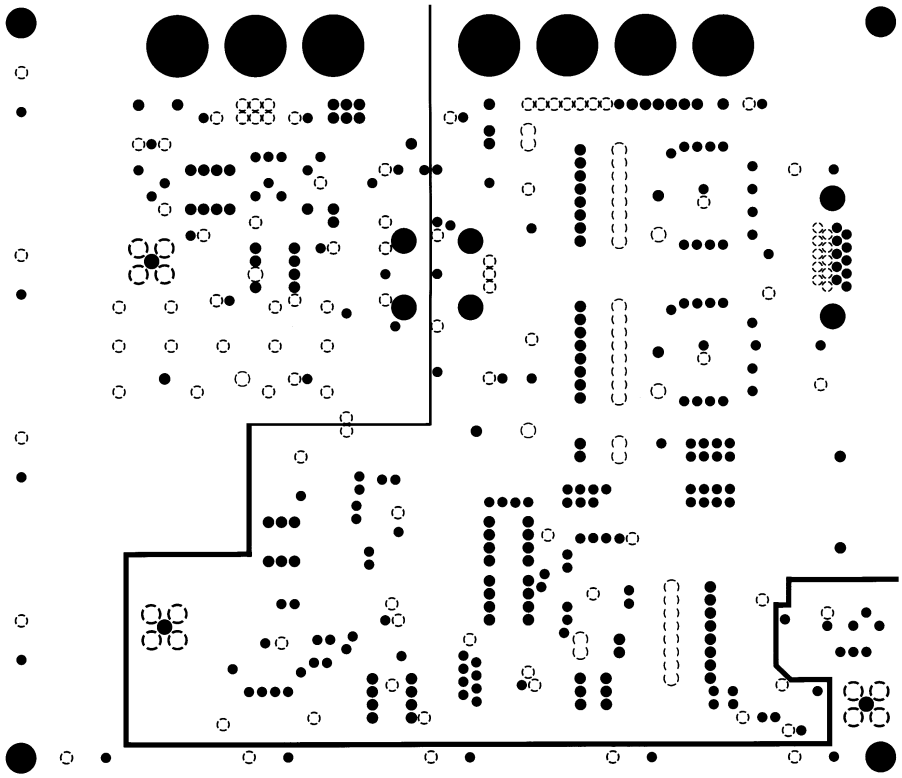
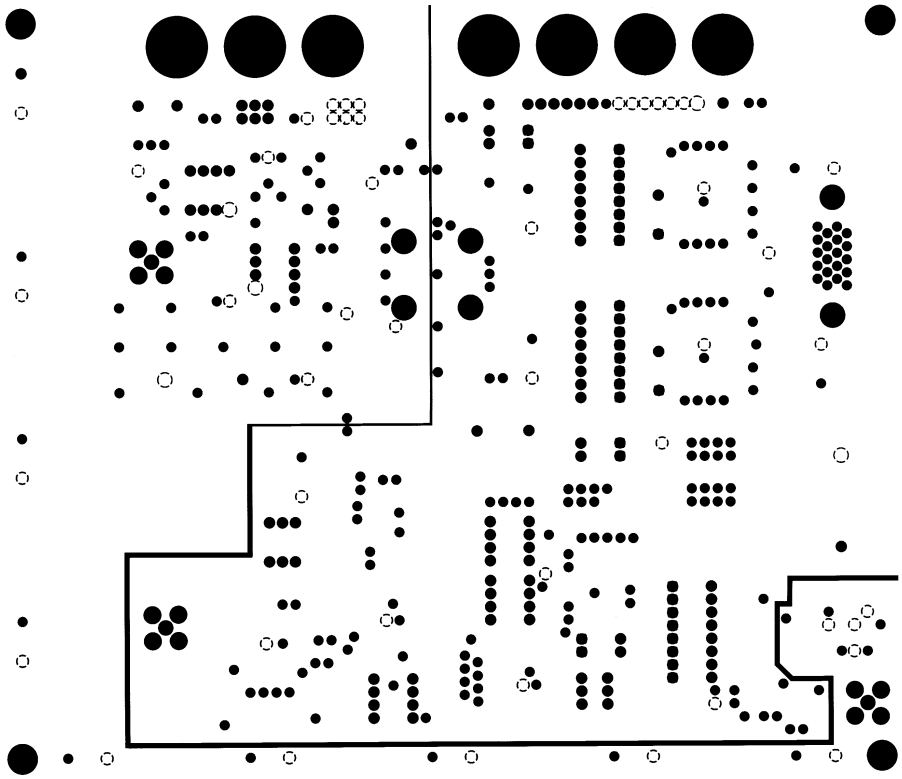


GND layer (inner layer)



V_{EE} layer (inner layer)

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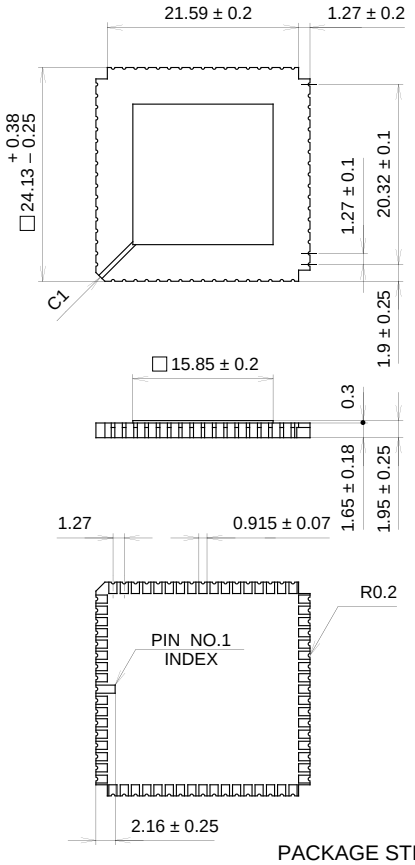
Package Outline Unit: mm

68PIN LCC (CERAMIC)



SONY CODE	LCC-68C-01
EIAJ CODE	∗QFN068-C-S950-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	————
PACKAGE WEIGHT	3.7g

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