SONY

CXA1720Q

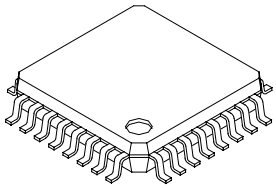
Read/Write Amplifier (with Built-in Filters) for FDDs

For the availability of this product, please contact the sales office.

Description

The CXA1720Q is an IC for use with floppy disk drives, and contains a Read circuit (with built-in filters), Write circuit, Erase circuit, and supply voltage detection circuit, all into a single chip.

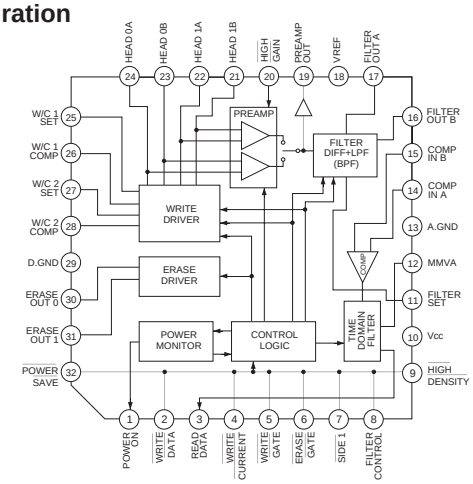
32 pin QFP (Plastic)



Features

- Single 5 V power supply.
- Filter system can be switched among four modes: 1M/2M, and inner track/outer track. This allows for a significant reduction in the number of external parts such as differentiator constants, low-pass filters, and switches. (Compared with conventional Sony products, the number of parts has been reduced by one-half.)
- Filter characteristics can be customized.
- Low pre-amplifier input conversion noise voltage of 2.0 nV/ $\sqrt{\text{Hz}}$ (typ.) keeps Read data output jitter to a minimum. The pre-amplifier voltage gain can be selected as either 100× or 200×.
- The monostable multivibrator No. 1 pulse width switching function for the time domain filter permits switching between 1M and 2M mode.
- Write current switching function permits switching of the Write current among four modes: 1M/2M and inner track/outer track. (Filter inner track/outer track switching is separate.)
- Supply voltage detection circuit prohibits error writing during power ON/OFF or abnormal voltage.
- Power consumption is kept down to 115 mW (typ.) and this IC is suitable for use with battery-driven FDDs.
- Built in Time constant capacitors for monostable multivibrator Nos. 1 and 2. (The pulse width for monostable multivibrator No. 2 is fixed.)
- Power saving function reduces power consumption when the IC is not in use. When in power saving mode (5 mW typ.), only the power supply ON/OFF detector functions.
- The Write driver has a built-in reset circuit. When the mode is switched from Read mode to Write mode, the Write current flows from head 0A if head side 0 is selected and from head 1A if head side 1 is selected.

Block Diagram and Pin Configuration



E93717-TE

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	7	V
• Digital signal input pin (note) input voltage		–0.5 to V_{CC}+0.3	V
• Power ON output applied voltage		V_{CC}+0.3	V
• Erase output applied voltage		V_{CC}+0.3	V
• Head 0A, 0B, 1A, 1B applied voltage		15	V
• Power ON output sink current		7	mA
• Erase output sink current		30	mA
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	500	mW

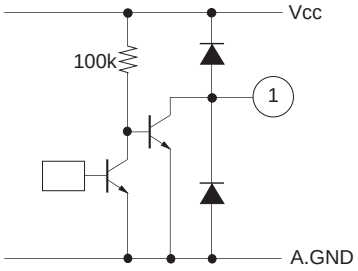
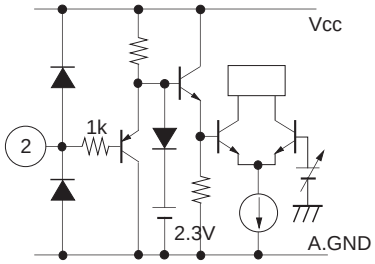
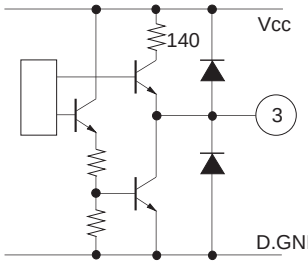
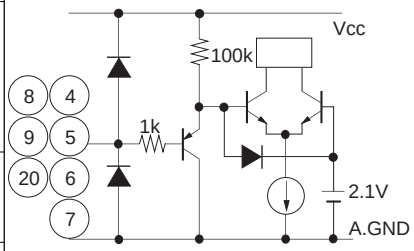
Supply Voltage Range

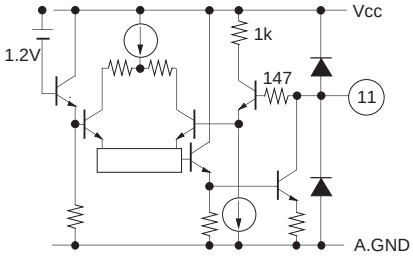
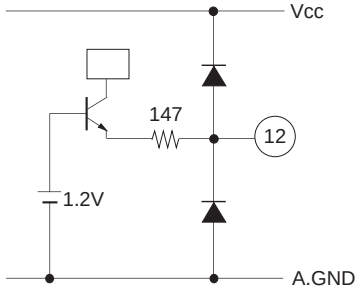
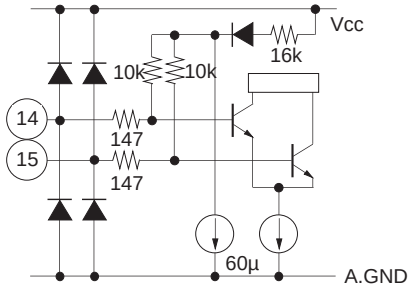
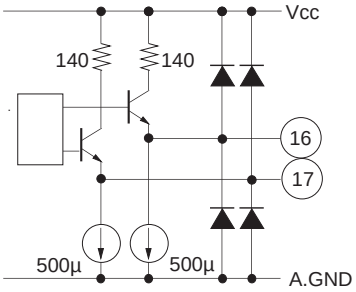
	V_{CC}	4.4 to 6.0	V

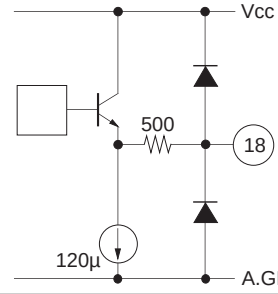
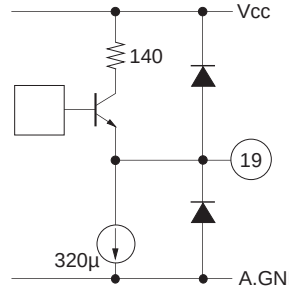
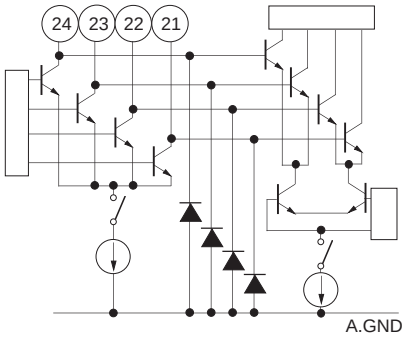
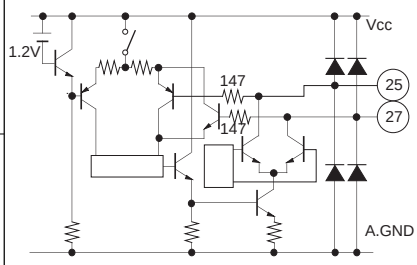
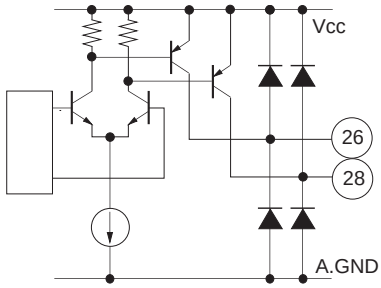
Note) $\overline{\text{WRITE DATA}}$, $\overline{\text{WRITE CURRENT}}$, $\overline{\text{WRITE GATE}}$, $\overline{\text{ERASE GATE}}$
$\overline{\text{SIDE1}}$, FILTER CONTROL, $\overline{\text{HIGH DENSITY}}$, $\overline{\text{HIGH GAIN}}$, $\overline{\text{POWER SAVE}}$

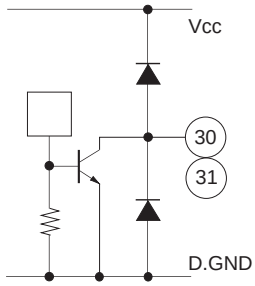
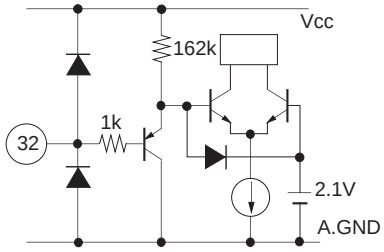
Pin Description

(Ta=25 °C, Vcc=5 V)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	POWER ON	—		Reduced voltage detection output. This is an open collector that outputs a low signal when Vcc is below the specified value.
2	$\overline{\text{WRITE}}$ $\overline{\text{DATA}}$	—		Write data input. This pin is a Schmitt-type input and is triggered when the logical voltage goes from high to low.
3	READ DATA	—		Read data output. This pin is active when the logical voltage of the Write gate signal and the Erase gate signal is high.
4	$\overline{\text{WRITE}}$ $\overline{\text{CURRENT}}$	—		Write current control. The Write current is increased when the logical voltage is low.
5	$\overline{\text{WRITE}}$ $\overline{\text{GATE}}$	—		Write gate signal input. The Write system is active when the logical voltage is low.
6	$\overline{\text{ERASE}}$ $\overline{\text{GATE}}$	—		Erase gate signal input. The Erase system is active when the logical voltage is low.
7	$\overline{\text{SIDE1}}$	—		Head side switching signal input. The HEAD1 system is active when the logical voltage is low, and the HEAD0 system is active when the logical voltage is high, but only when the logical voltage for the Write gate and the Erase gate is high.
8	FILTER CONTROL	—		Filter inner track/outer track mode control. Inner track mode is selected when the logical voltage is low.
9	$\overline{\text{HIGH}}$ $\overline{\text{DENSITY}}$	—		Filter, time domain filter and Write current 1M/2M mode control. 2M mode is selected when the logical voltage is low.
20	$\overline{\text{HIGH}}$ $\overline{\text{GAIN}}$	—		Pre-amplifier voltage gain selection. Gain of 100x is selected when the logical voltage is high; gain of 200x is selected when the logical voltage is low.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
10	V_{CC}	—		Power supply (5 V) connection.
11	FILTER SET	3.8 V		Connection for filter cut-off frequency setting resistor. Connect the filter cut-off frequency setting resistor R_F between this pin and V_{CC} to set the cut-off frequency.
12	MMVA	0.5 V		Time domain filter monostable multivibrator No. 1 pulse width setting pin. Connect the monostable multivibrator No. 1 pulse width setting resistor R_A between this pin and A.GND.
13	A. GND	—		Analog system GND connection.
14	COMP IN A	3.3 V		Comparator differential inputs.
15	COMP IN B	3.3 V		
16	FILTER OUT B	3.3 V		Filter differential outputs.
17	FILTER OUT A	3.3 V		

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
18	VREF	2.8 V		Connection for internal reference voltage decoupling capacitor. Connect the decoupling capacitor CREF between this pin and A.GND.
19	PREAMP OUT	2.8 V		Pre-amplifier output.
21	HEAD 1B	—		Connection for magnetic head input/output. Connect the recording/playback magnetic head to these pins, and connect the center tap to Vcc. When the logical voltage for Pin 7 ($\overline{\text{SIDE1}}$) is low, the HEAD1 system is active; when the logical voltage is high, the HEAD0 system is active.
22	HEAD 1A	—		
23	HEAD 0B	—		
24	HEAD 0A	—		
25	W/C1SET			Connection for 1M write current setting resistor. Connect the Write current setting resistor R_{W1} between this pin and Vcc to set the Write current.
27	W/C2SET			Connection for 2M Write current setting resistor. Connect the Write current setting resistor R_{W2} between this pin and Vcc to set the Write current.
26	W/C1 COMP	—		Connection for 1M Write current compensation resistor. Connect the Write current compensation resistor R_{WC1} between this pin and Pin 25 (W/C1SET) to set the amount of increase in the Write current.
28	W/C2 COMP	—		Connection for 2M Write current compensation resistor. Connect the Write current compensation resistor R_{WC2} between this pin and Pin 27 (W/C2SET) to set the amount of increase in the Write current.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
29	D. GND	—		Digital system GND connection.
30	ERASE OUT0	—		Erase current output for the HEAD0 system.
31	ERASE OUT1	—		Erase current output for the HEAD1 system.
32	$\overline{\text{POWER}}$ $\overline{\text{SAVE}}$	—		Power saving signal input. When the logical voltage is low, the IC is in power saving mode. In power saving mode, only the power supply ON/OFF detection function operates.

Electrical Characteristics

Current Consumption (Ta=25 °C, V_{CC}=V)

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Current consumption for Read	ICCR	V_{CC}=5 V $\overline{WG}$="H"	—	—	13.0	23.0	33.0	mA
Current consumption for Write/Erase	ICCWE	V_{CC}=5 V $\overline{WG}$="L", EG="L"	—	—	8.0	14.0	20.0	
Current consumption for Power saving	ICCPS	V_{CC}=5 V $\overline{PS}$="L"	—	—		0.9	1.8	

Power Supply Monitoring System (Ta=25 °C)

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Power supply ON/OFF detector threshold voltage	VTH		—	—	3.5	3.9	4.3	V
Power ON output saturation voltage	VSP	V_{CC}=3.5 V I=1 mA	—	—			0.5	

Read System

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Pre-amplifier voltage gain SIDE0*	GV0	f=100 kHz SW4=a, b	1	G	38.1/44.1	40/46	41.6/47.6	dB
Pre-amplifier voltage gain SIDE1*	GV1	f=100 kHz SW4=a, b SW1, 5=b						
Pre-amplifier frequency response SIDE0*	BW0	A_V/A_{V0}=–3 dB SW4=a, b	1	G	5			MHz
Pre-amplifier frequency response SIDE1*	BW1	A_V/A_{V1}=–3 dB SW4=a, b SW1, 5=b						
Pre-amplifier input conversion noise voltage SIDE0	EN0	Bandwidth=400 Hz to 1 MHz Vi=0, SW4=b	1	G		2.0	2.9	μVrms
Pre-amplifier input conversion noise voltage SIDE1	EN1	Bandwidth=400 Hz to 1 MHz SW4=b Vi=0, SW1, 5=b						

* When SW4 = a: Vi = 10 mVp-p
When SW4 = b: Vi = 5 mVp-p

Read System (Ta=25 °C, V_{CC}=5 V)

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Pre-amplifier output offset voltage (vs. VREF)	VOFSP	Vi=0 SW4=a, b, SW1, 5=a, b	1	F, G	–500		+500	mV
Pre-amplifier output voltage amplitude**	VOP	f=100 kHz SW4=a, b, SW1, 5=a, b	1	G	1.8			Vp-p
Filter differential output offset voltage	VOFSF	Vi=0	1	D, E	–100		+100	mV
Filter differential output voltage amplitude	VOF	f=100 kHz Vi=60 mVp-p	1	D, E	2.8			Vp-p
Time domain filter monostable multivibrator No. 1 pulse width precision	ETM1 ETM1'	R_A=27 kΩ Refer to Fig. 1	1	B, C A	–10		+10	%
Time domain filter monostable multivibrator No. 2 pulse width (fixed)	T2	R_A=27 kΩ Refer to Fig. 1	1	A	260	400	540	ns
Read data output low voltage	VOL	I_{OL}=2 mA	1	A			0.5	V
Read data output high voltage	VOH	I_{OH}=–0.4 mA	1	A	2.8			V
Read data output*** rise time	TR	R_L=2 kΩ C_L=20 pF	1	A			100	ns
Read data output*** fall time	TF	R_L=2 kΩ C_L=20 pF	1	A			100	ns
Peak shift****	PS	Vi=0.25 mVp-p to 10 mVp-p f=62.5 kHz Refer to Fig. 1	1	A			1	%

** When SW4 = a: Vi = 60 mVp-p
When SW4 = b: Vi = 30 mVp-p

*** Read data output between 0.5 V to 2.4 V

**** For Vi = 0.25 mVp-p to 5m Vp-p: SW4 = b (pre-amplifier voltage gain: 46 dB)
For Vi = 0.5 mVp-p to 10 mVp-p: SW4 = a (pre-amplifier voltage gain: 40 dB)

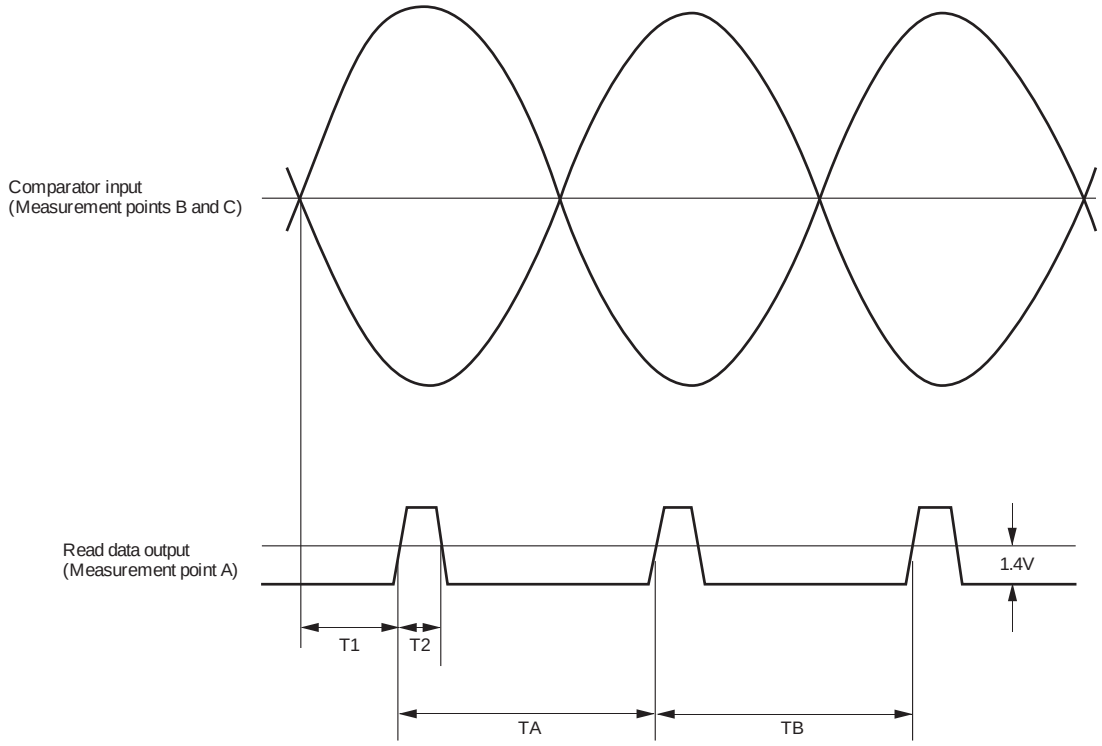


Fig. 1 Monostable multivibrator Nos. 1 and 2 pulse width precision and peak shift measurement conditions

- Monostable multivibrator No. 1 pulse width precision
  When $\overline{HD}$ = high:

$$ETM1 = \left(\frac{T_1}{2.45\ \mu S} - 1 \right) \times 100\ (\%)$$

When $\overline{HD}$ is low:

$$ETM1' = \left(\frac{T_1}{1.25\ \mu S} - 1 \right) \times 100\ (\%)$$

- Monostable multivibrator No. 2 pulse width = T_2
- Peak shift

$$PS = \frac{1}{2} \left| \frac{T_A - T_B}{T_A + T_B} \right| \times 100\ (\%)$$

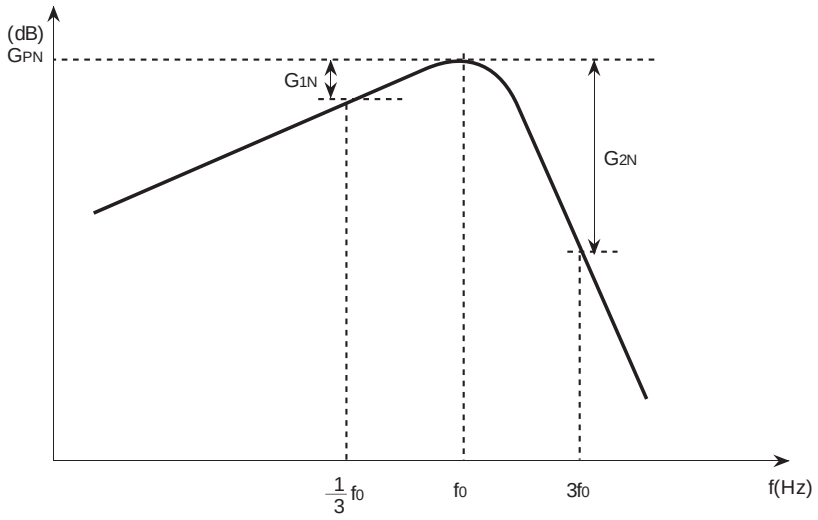
Read System (Filters) (Ta=25 °C, V_{CC}=5 V)

Item		Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
1M/ outer track	Peak frequency	F_{O1}	Vi=3mVp-p $\overline{HG}$="L" $\overline{HD}$="H" FC="H"	1	D, E	153.0	170.0	187.0	kHz
	Peak voltage gain*****	G_{P1}	Refer to Fig. 2 at f_{O1}	1	G D, E	3.6	5.5	7.1	dB
	Frequency response (1)	G_{11}	Refer to Fig. 2 at $\frac{1}{3}$ f_{O1}	1	D, E	–7.6	–7.1	–6.6	
	Frequency response (2)	G_{12}	Refer to Fig. 2 at 3f_{O1}	1	D, E	–25.0	–23.1	–21.5	
1M/ inner track	Peak frequency	f_{O2}	Vi=3mVp-p $\overline{HG}$=":L" $\overline{HD}$="H" FC="L"	1	D, E	163.8	182.0	200.2	kHz
	Peak voltage gain*****	G_{P2}	Refer to Fig. 2 at f_{O2}	1	G D, E	3.6	5.5	7.1	dB
	Frequency response (1)	G_{21}	Refer to Fig. 2 at $\frac{1}{3}$ f_{O2}	1	D, E	–7.6	–7.1	–6.6	
	Frequency response (2)	G_{22}	Refer to Fig. 2 at 3f_{O2}	1	D, E	–25.0	–23.1	–21.5	
2M/ outer track	Peak frequency	f_{O3}	Vi=3mVp-p $\overline{HG}$="L" $\overline{HD}$="L" FC="H"	1	D, E	288.0	320.0	352.0	kHz
	Peak voltage gain*****	G_{P3}	Refer to Fig. 2 at f_{O3}	1	G D, E	3.6	5.5	7.1	dB
	Frequency response (1)	G_{31}	Refer to Fig. 2 at $\frac{1}{3}$ f_{O3}	1	D, E	–7.6	–7.1	–6.6	
	Frequency response (2)	G_{32}	Refer to Fig. 2 at 3f_{O3}	1	D, E	–25.0	–23.1	–21.5	
2M inner track	Peak frequency	f_{O4}	Vi=3mVp-p $\overline{HG}$="L" $\overline{HD}$="L" FC="L"	1	D, E	310.5	345.0	379.5	kHz
	Peak voltage gain*****	G_{P4}	Refer to Fig. 2 at f_{O4}	1	G D, E	5.3	7.2	8.8	dB
	Frequency response (1)	G_{41}	Refer to Fig. 2 at $\frac{1}{3}$ f_{O4}	1	D, E	–8.6	–8.1	–7.6	
	Frequency response (2)	G_{42}	Refer to Fig. 2 at 3f_{O4}	1	D, E	–36.2	–34.3	–32.7	

***** $G_{PN} = 20\text{Log}_{10} (V_{Filterout}/V_{Preout})$

$V_{Filterout}$: Filter differential output voltage

(N=1 to 4)



(N=1 to 4)

Fig. 2 Filter frequency response measurement conditions

Write/Erase System (Ta=25 °C, V_{CC}=5 V)

Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Write current output precision∗	EW	$\overline{WG}$="L" R_W=4.3 kΩ	2	LKJI	–7		+7	%
Write current output unbalance	DW	$\overline{WG}$="L" R_W=4.3 kΩ	2	LKJI	–1		+1	
Write current compensation current precision∗∗	EWC	$\overline{WG}$="L" R_W=4.3 kΩ R_{WC}=12 kΩ	2	LKJI	–10		+10	
Head I/O pin leak current for Write	ILKW	$\overline{WG}$="L"	2	LKJI			10	µA
Head I/O pin saturation voltage for Write	VSW	$\overline{WG}$="L" SW1=6	2	L'K'J'I'			1	V
Leak current for Erase current switch	ILKE	$\overline{EG}$="L"	2	MN			10	µA
Output saturation voltage for Erase current switch	VSE	$\overline{EG}$="L" I=30 mA SW2=b	2	M'N'			500	mV

∗ Write current output precision $E_W = \left(\frac{I_W}{2.70\ mA} - 1 \right) \times 100\ (\%)$

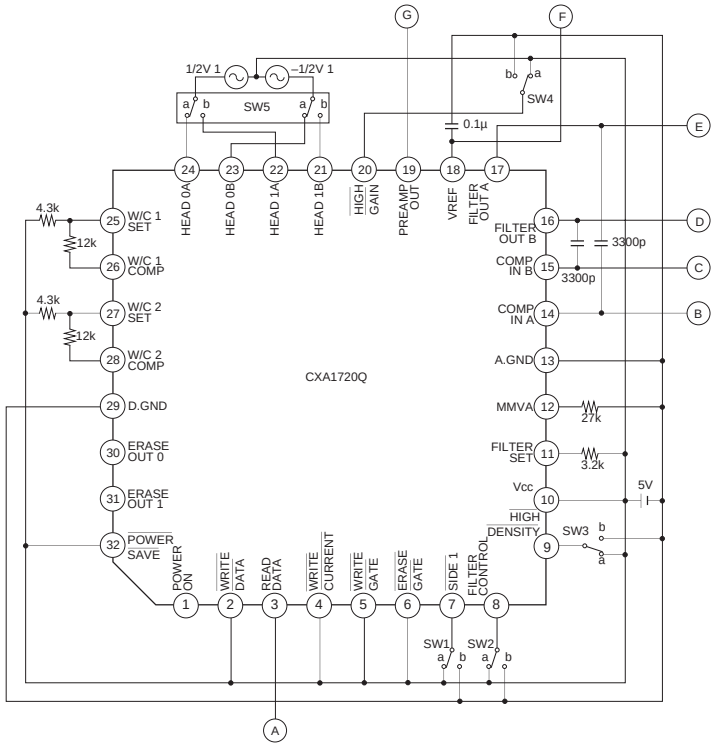
∗∗ Write current compensation current precision $E_{WC} = \left(\frac{I_W' - I_W}{0.90\ mA} - 1 \right) \times 100\ (\%)$

I_W: $\overline{\text{WRITE CURRENT}}$ = "H" I_W': $\overline{\text{WRITE CURRENT}}$ = "L"

Logic Input Block

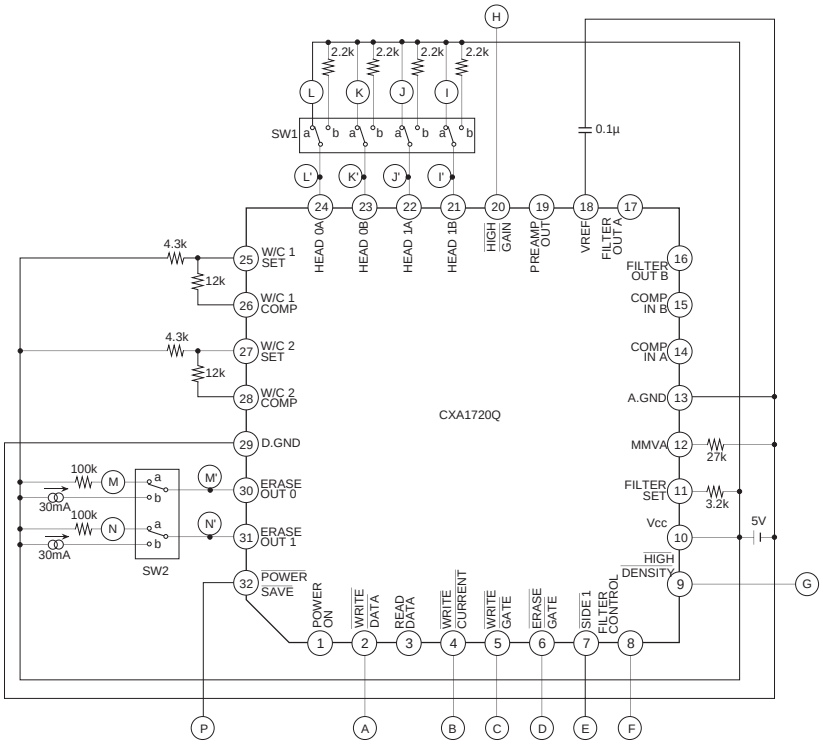
Item	Symbol	Conditions	Measure-ment circuit	Measure-ment point	Min.	Typ.	Max.	Unit
Digital low input voltage	VLD		2	BCDE FGHP			0.8	V
Digital high input voltage	VHD		2	BCDE FGHP	2.0			
Schmitt-type digital low input voltage	VLSD		2	A			0.8	
Schmitt-type digital high input voltage	VHSD		2	A	2.0			
Digital low input current	ILD	V_L=0 V	2	ABCD EFGHP	–20			µA
Digital high input current	IHD	V_H=5 V	2	ABCD EFGHP			10	

Electrical Characteristics Measurement Circuit 1



Note) Unless otherwise specified, switches are assumed to be set to “a”.

Electrical Characteristics Measurement Circuit 2



Note) Unless otherwise specified, switches are assumed to be set to “a”.

Description of Operation

(1) Read system

Pre-amplifier

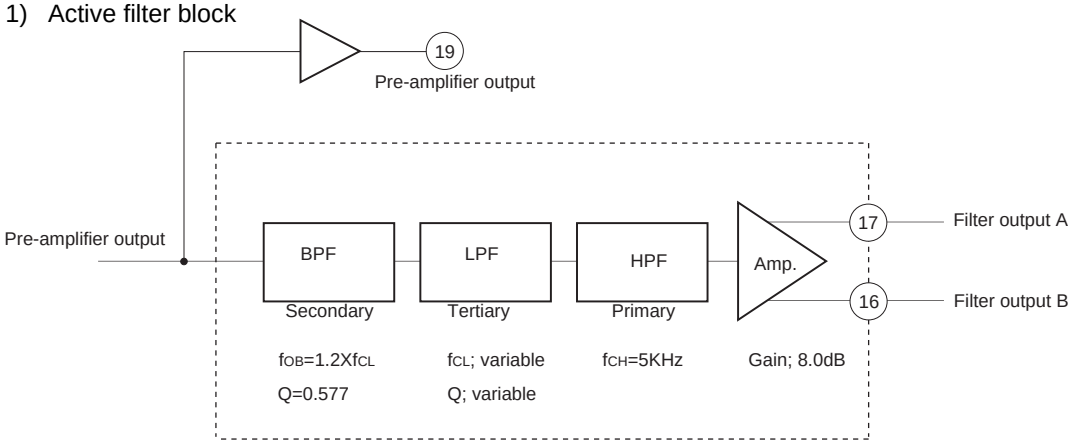
The pre-amplifier amplifies input signals. The voltage gain can be switched between 40 dB and 46 dB, using Pin 20.

Filters

The filters differentiate the signals amplified by the pre-amplifier. The high-band noise components are attenuated by the low-pass filter. The filters can be switched among four modes, depending on the settings of Pins 8 and 9. In 1M/outer track mode, the peak frequency f_{O1} is set by external resistor R_F. f_O for the other three modes is switched by the internal settings of the IC, with f_{O1} used as a reference (1.00).

The filters are explained below.

1) Active filter block



Filter Characteristics

Table 1

Pin 8	Pin 9	LPF characteristics	f_O ratio
H	H	1M/outer track mode: Butterworth	1.00
L	H	1M/inner track mode: Butterworth	1.07
H	L	2M/outer track mode: Butterworth	1.88
L	L	2M/inner track mode: Chebyshev 1 dB ripple	2.03

The formula for the peak frequency f_{01} for 1M/outer track mode is shown below:

$f_{01} = 527/R_F + 5.8$ (kHz) f_{01}: peak frequency in 1M/outer track mode

R_F: filter setting resistance (kΩ)

The relationship between f01 and f0 in the four modes is as follows:

1M/outer track: $f_{01} = 1.0 \times f_{01}$

1M/inner track: $f_{02} = 1.07 \times f_{01}$

2M/outer track: $f_{03} = 1.88 \times f_{01}$

2M/inner track: $f_{04} = 2.03 \times f_{01}$

Note that these filters can be customized.

Customization is explained on pages 17 and 18.

Comparator

The comparator detects the crosspoint of the filter differential output.

Time domain filter

The time domain filter converts the comparator output to Read data.

This filter is equipped with two monostable multivibrators. Monostable multivibrator No. 1 eliminates unnecessary pulses, and monostable multivibrator No. 2 determines the pulse width of Read data.

The monostable multivibrator No. 1 pulse width T_A is determined by the resistor R_A between Pin 12 and A.GND. T_A can be switched as follows by the setting of Pin 9:

$\overline{\text{HIGH DENSITY}}$ = "H" $T_{A\,LOW} = 84R_A + 180$ (nS) R_A (kΩ)

$\overline{\text{HIGH DENSITY}}$ = "L" $T_{A\,HIGH} = 42R_A + 110$ (nS)

The pulse width for monostable multivibrator No. 2 is fixed at 400 ns.

(2) Write System

Write data input through Pin 2 is frequency-divided by the T flip-flop and generates the head recording current. The recording current can be switched by the setting of Pin 9.

The Write current Iw is set by the resistor R_W connected between Pin 25 and V_{CC} and between Pin 27 and V_{CC}.

$I_W = 11.6/R_W$ (mA) R_W (kΩ)

Furthermore, the Write current compensation I_{WC} is set by the resistor R_{WC} connected between Pin 25 and Pin 26, and between Pin 27 and Pin 28.

$I_{WC} = 10.8/R_{WC}$ (mA) R_{WC} (kΩ)

(3) Erase System

Pins 30 and 31 are open collector outputs; the Erase current is set by the resistance between these pins and the Erase head.

(4) Power ON/OFF Detection System

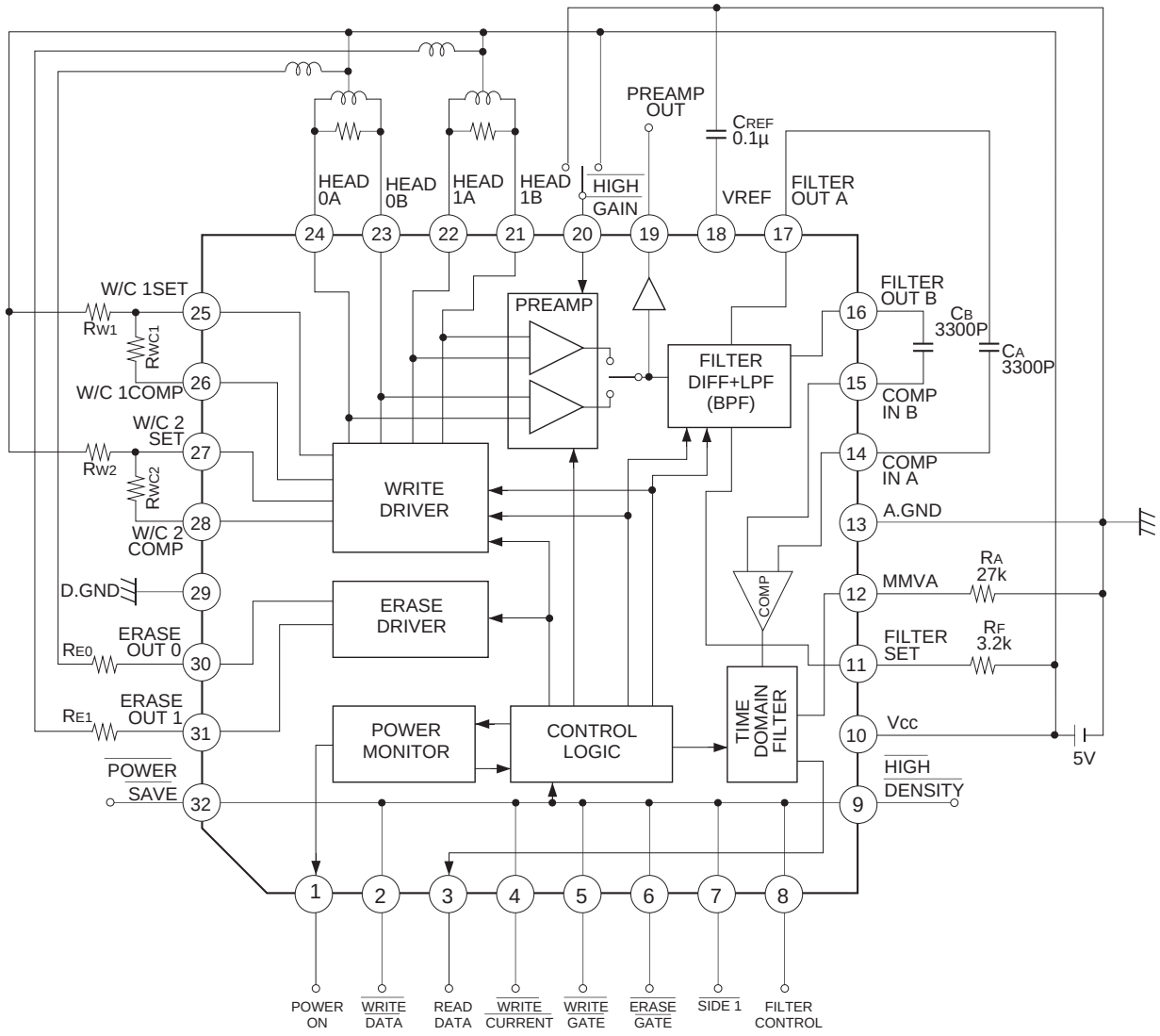
The power ON/OFF detection system detects a reduced voltage.

When V_{CC} is below the stipulated voltage, the Write system and Erase system cease operation, disabling the Write and Erase functions

Notes on Operation

- Select the voltage gain so that the pre-amplifier output amplitude is 1 Vp-p or less.
  If the pre-amplifier output amplitude exceeds 1 Vp-p, the filter output waveform becomes distorted.
- Observe the following points when mounting this IC.
- Connect a V_{CC} decoupling capacitor of approximately 0.1 µF close to the IC.
- The ground should be as large as possible.

Application Circuit (for 1M/2M devices)

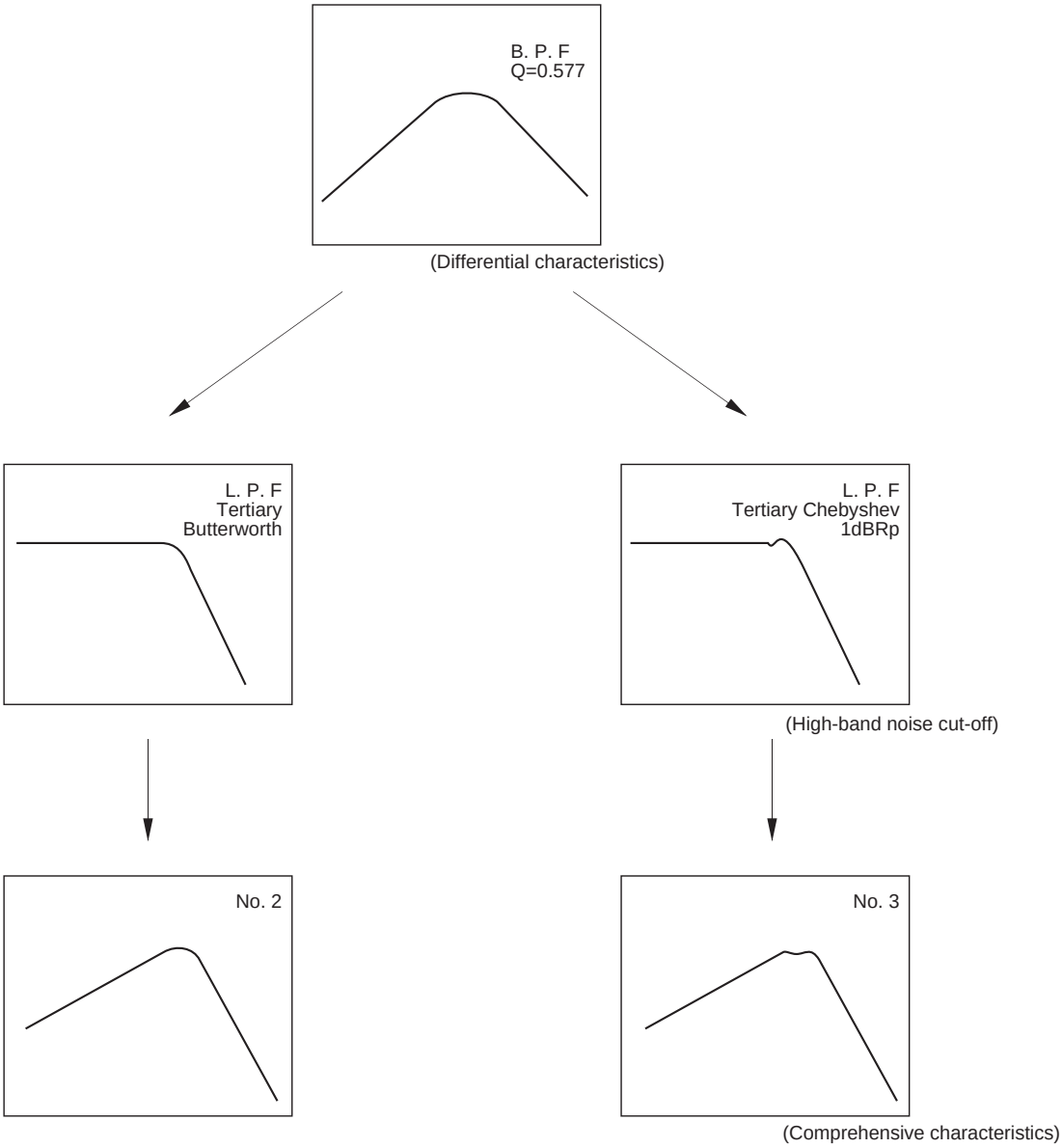


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Customization

Filter frequency response

In 2M/inner track mode, the filter frequency response can be changed as shown below.



Filter Customization Selections/Combinations

In filter settings, use the LPF cut-off frequency f_{C1} in 1M/outer track mode as 1.00 as shown in Table 1 to select fc ratios and LPF types for the other three modes. The 1M/outer track to 2M/outer track modes for the LPF are fixed to Butterworth, while either Butterworth or Chebyshev 1 dB ripple can be selected in 2M/inner track mode.

Note that the BPF center frequency f_{oB} is fixed at 1.2 times the LPF cut-off frequency fc. In addition, the relationship between the peak frequencies fo and fc in regards to the comprehensive characteristics is as follows, depending on differences in LPFs.

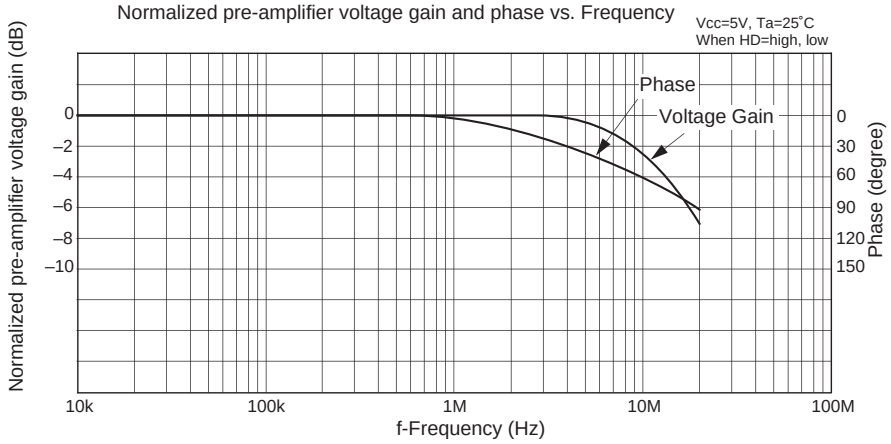
Butterworth characteristics: $f_C = 1.28fo$
Chebyshev 1 dB ripple characteristics: $f_C = 1.12fo$

Table 1 LPF fc Ratios and Types

Mode	LPF type	f_c ratio when f_{c1} is assumed as 1.00				
1M/outer track	Butterworth	[1.00]				
1M/inner track	Butterworth	[1.07]	1.14	1.23	1.33	1.45
		1.60	2.00			
2M/outer track	Butterworth	1.33	1.39	1.45	1.52	1.60
		1.68	1.78	[1.88]	2.00	2.13
		2.29	2.46	2.67		
2M/inner track	Butterworth	1.33	1.39	1.45	1.52	1.60
	[Chebyshev (1 dB ripple)]	1.68	[1.78]	1.88	2.00	2.13
		2.29	2.46	2.67		

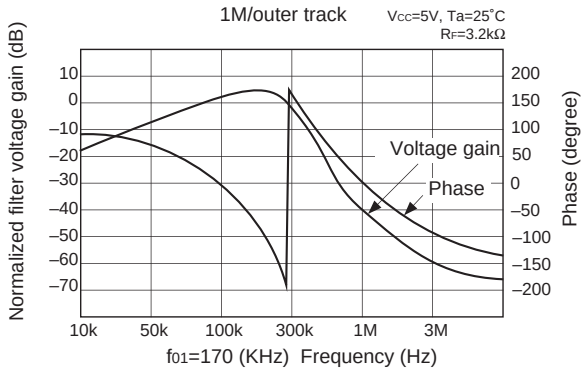
Note) The boxed item indicates the setting for the CXA1720Q.

Normalized pre-amplifier voltage gain and phase vs. Frequency

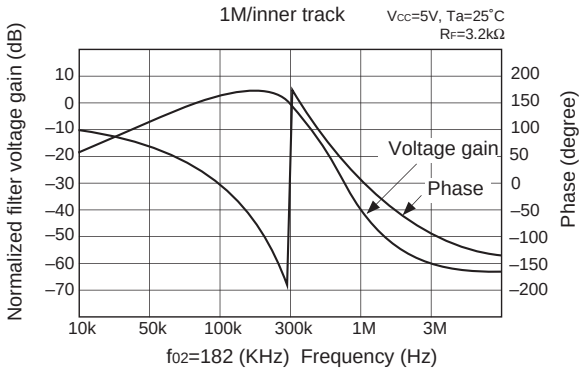


Filter characteristics in the four modes
(These characteristics are based on pre-amplifier output. 0dB=pre-amplifier output level)

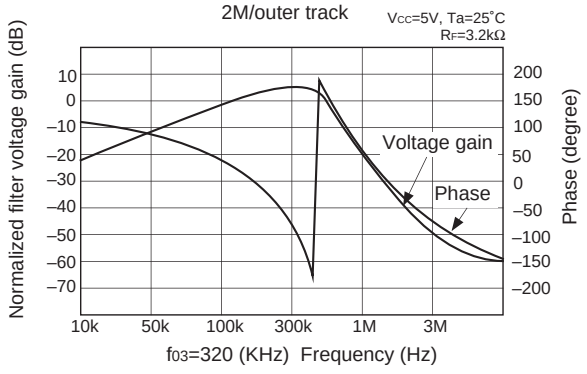
1M/outer track



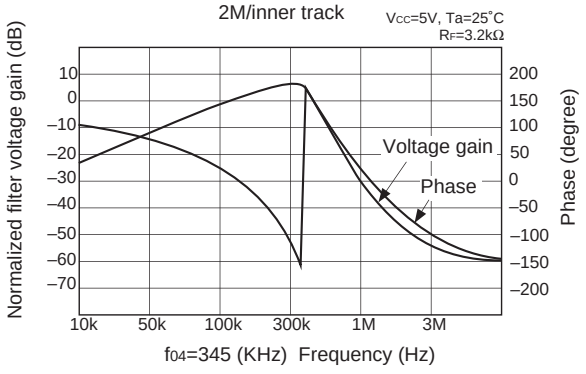
1M/inner track



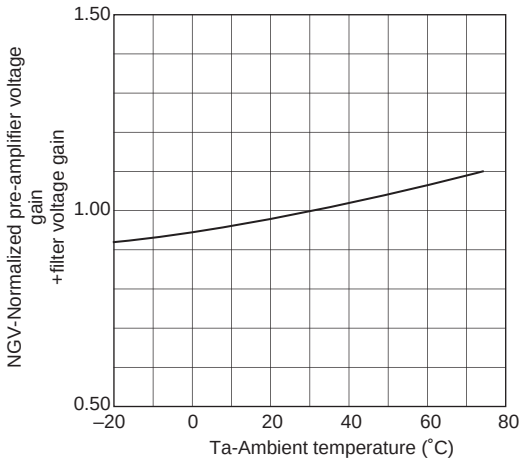
2M/outer track



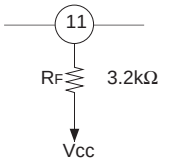
2M/inner track



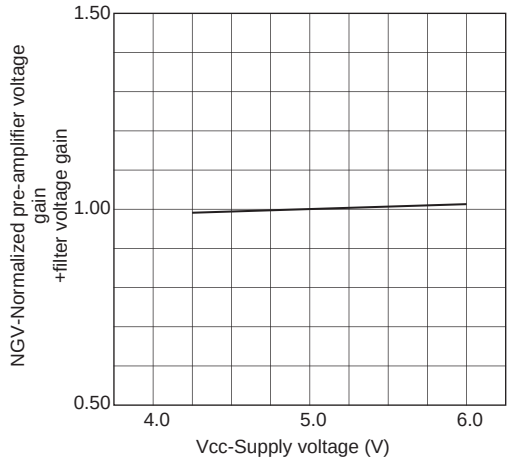
Normalized pre-amplifier voltage gain+filter voltage gain
vs. Ambient temperature



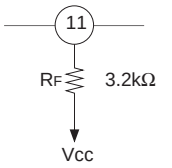
f=100KHz Vcc=5V
Vin=10mVp-p (HG="H")
Vin=5mVp-p (HG="L")
NGV=GV/GV (Ta=25˚C)



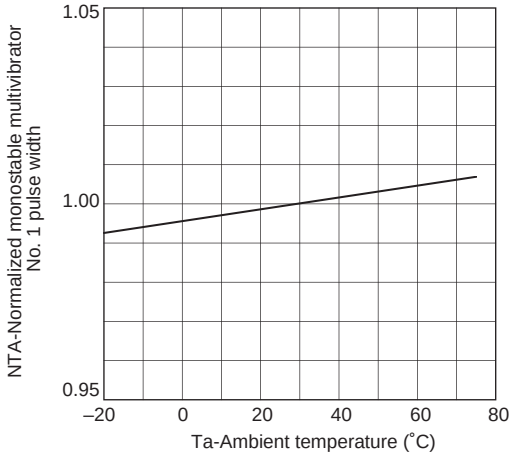
Normalized pre-amplifier voltage gain+filter voltage gain
vs. Supply voltage



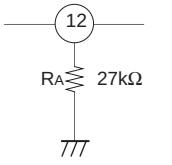
Ta=25˚C
f=100KHz
Vin=10mVp-p (HG="H")
Vin=5mVp-p (HG="L")
NGV=GV/GV (Vcc=5V)



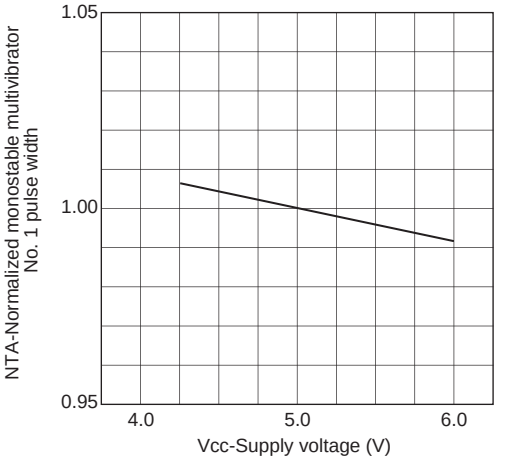
Normalized monostable multivibrator No. 1 pulse width
vs. Ambient temperature



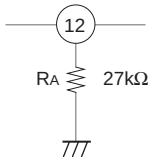
Vcc=5V
NTA=TA/TA (Ta=25˚C)
When HD=high, low



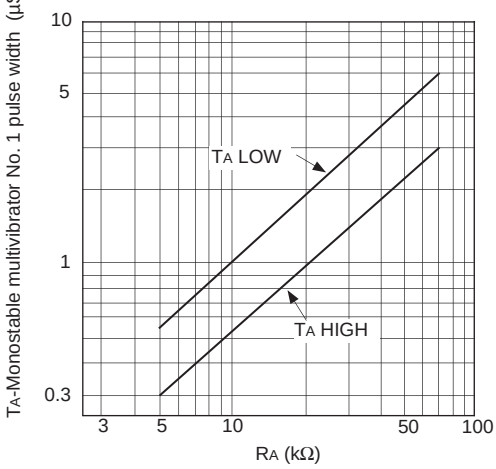
Normalized monostable multivibrator No. 1 pulse width
vs. Supply voltage



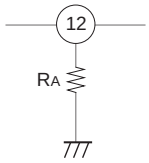
Ta=25˚C
NTA=TA/TA (Ta=25˚C)
When $\overline{HD}$=high, low



Monostable multivibrator No. 1 pulse width vs. RA

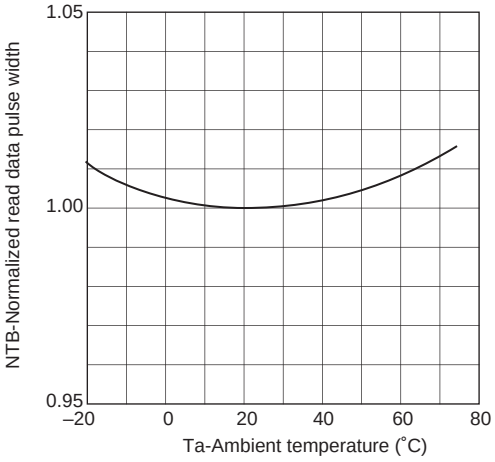


Vcc=5V
Ta=25˚C



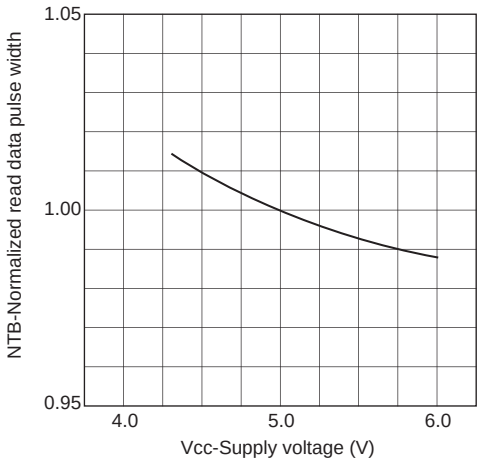
TA LOW=84RA+180 (ns)
TA HIGH=42RA+110 (ns)
RA (kΩ)

Normalized read data pulse width
vs. Ambient temperature



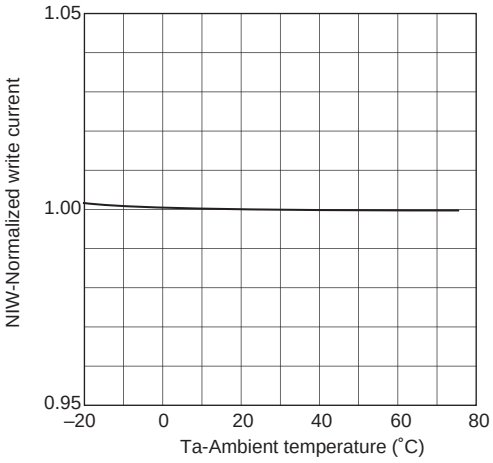
Vcc=5V
NTB=TB/TB (Ta=25˚C)

Normalized read data pulse width
vs. Supply voltage

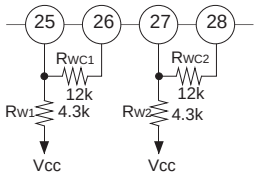


Ta=25˚C
NTB=TB/TB (Vcc=5V)

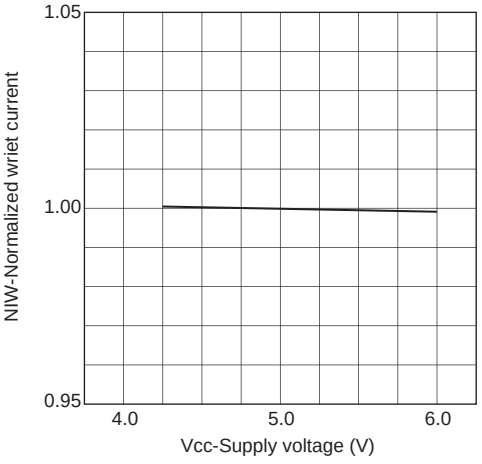
Normalized write current vs. Ambient temperature



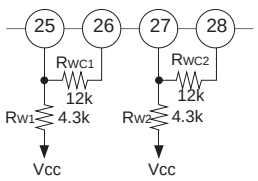
Vcc=5V
NIW=IW/IW (Ta=25˚C)



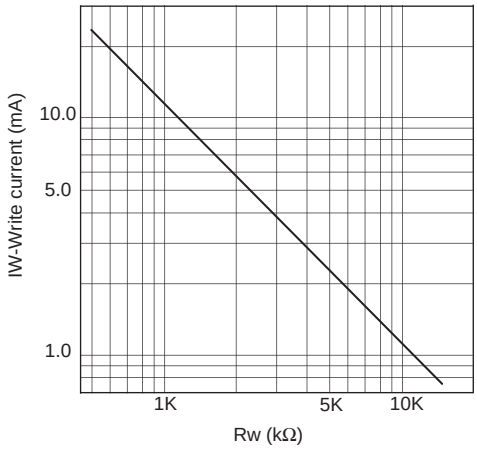
Normalized write current vs. Supply voltage



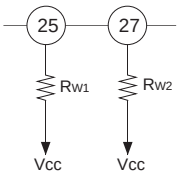
Ta=25˚C
NIW=IW/IW (Vcc=5V)



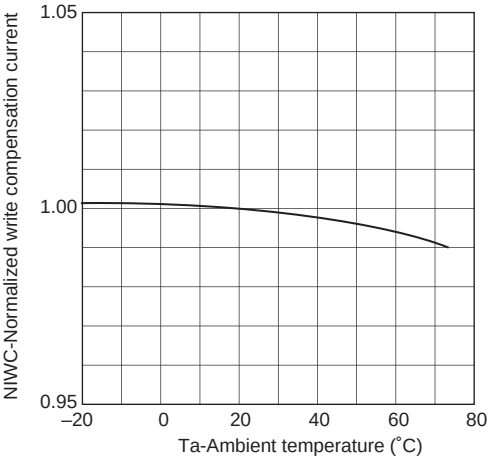
Write current vs. RW



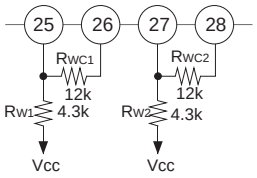
Vcc=5V
Ta=25˚C
IW=11.6/Rw (mA)
Rw (kΩ)



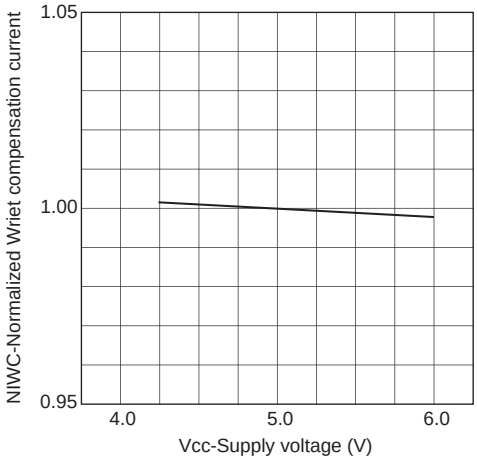
Normalized write compensation current vs.
Ambient temperature



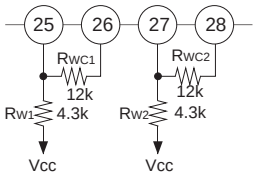
Vcc=5V
NIWC=IWC/IWC (Ta=25˚C)



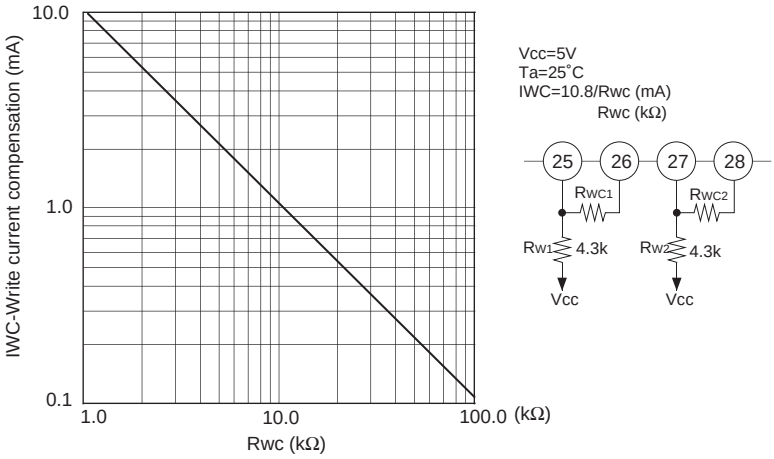
Normalized Write compensation current vs.
Supply voltage



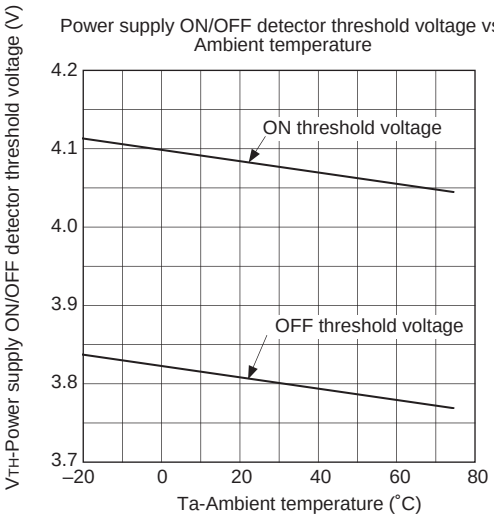
Ta=25˚C
NIWC=IWC/IWC (Vcc=5V)



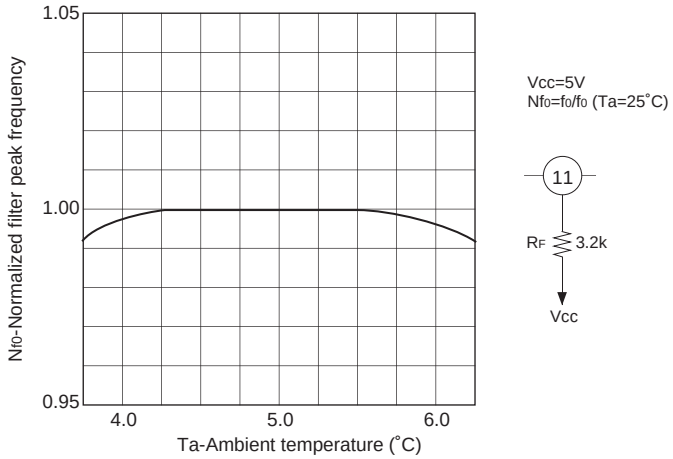
Write current compensation vs. Rwc



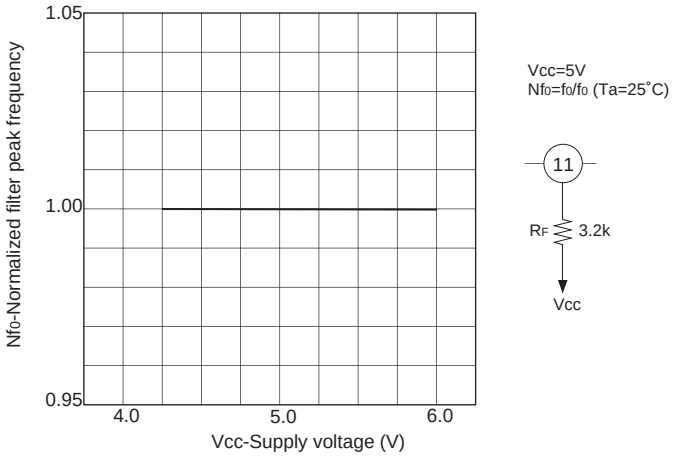
Power supply ON/OFF detector threshold voltage vs. Ambient temperature



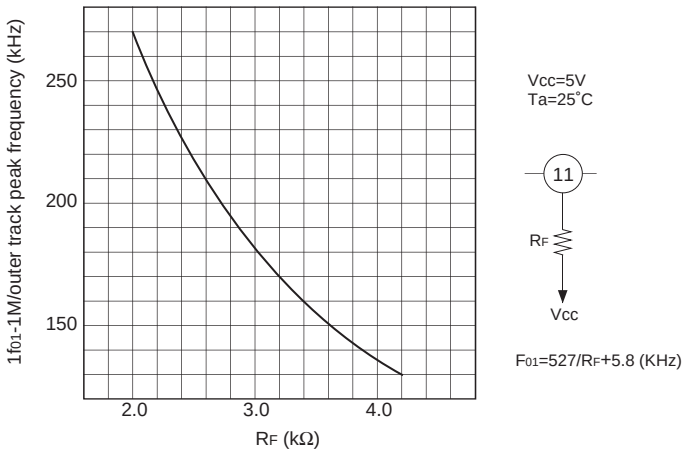
Normalized filter peak frequency vs. Ambient temperature



Normalized filter peak frequency vs.
Supply voltage characteristics

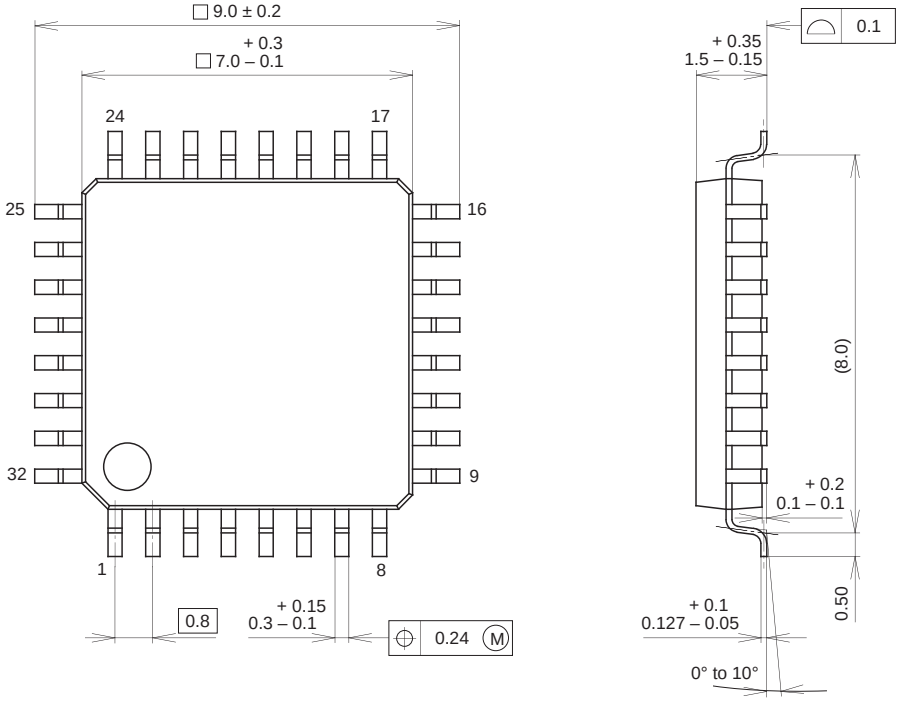


1M/outer track peak frequency vs. RF



Package Outline Unit : mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g