SONY

CXA1734S

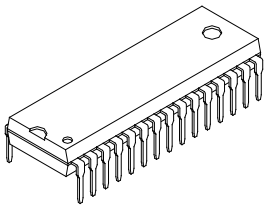
US Audio Multiplexing Decoder

For the availability of this product, please contact the sales office.

Description

The CXA1734S is an IC designed as a decoder for the Zenith TV Multi-channel System also corresponds with I²C BUS. Functions include stereo demodulation, SAP (Separate Audio Program) demodulation and dbx noise reduction. Various kinds of filters are built in while adjustment and mode control are all executed through I²C BUS.

30 pin SDIP (Plastic)



Features

- Audio multiplexing decoder and dbx noise reduction decoder are all included in a single chip. Almost any sort of signal processing is possible through this IC.
- All adjustments are possible through I²C BUS to allow for automatic adjustment.
- Various built-in filter circuits greatly reduce external parts.

Standard I/O Level

- Input level
  COMPIN (Pin 11) 245 mVrms
- Output level
  LOUT (Pin 29) 490 mVrms
  ROUT (Pin 28) 490 mVrms

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	11	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	1.35	W

Range of Operating Supply Voltage 9 ± 0.5 V

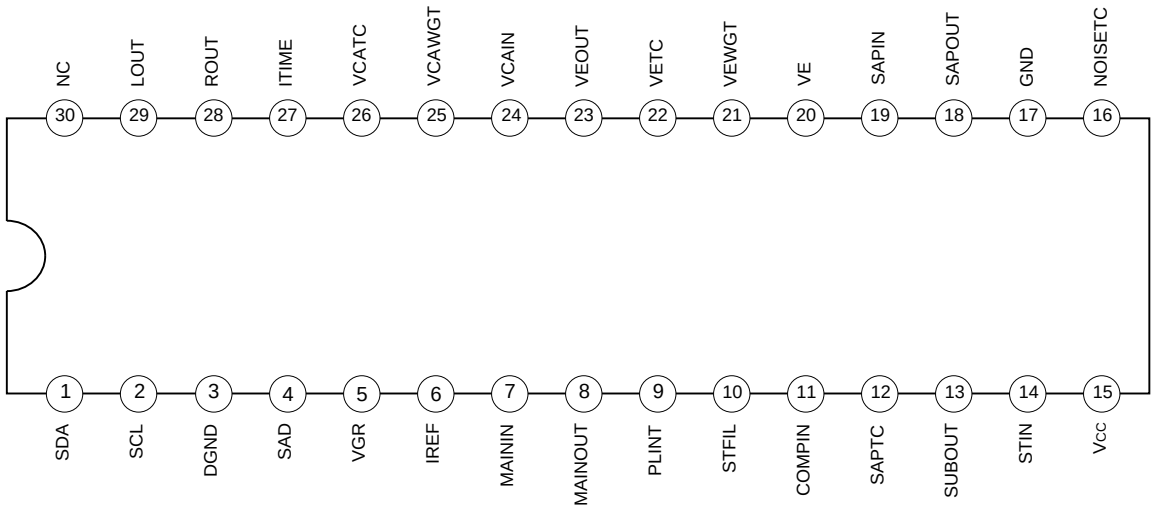
Applications

TV, VCR and other decoding systems for US audio multiplexing TV broadcasting

Structure

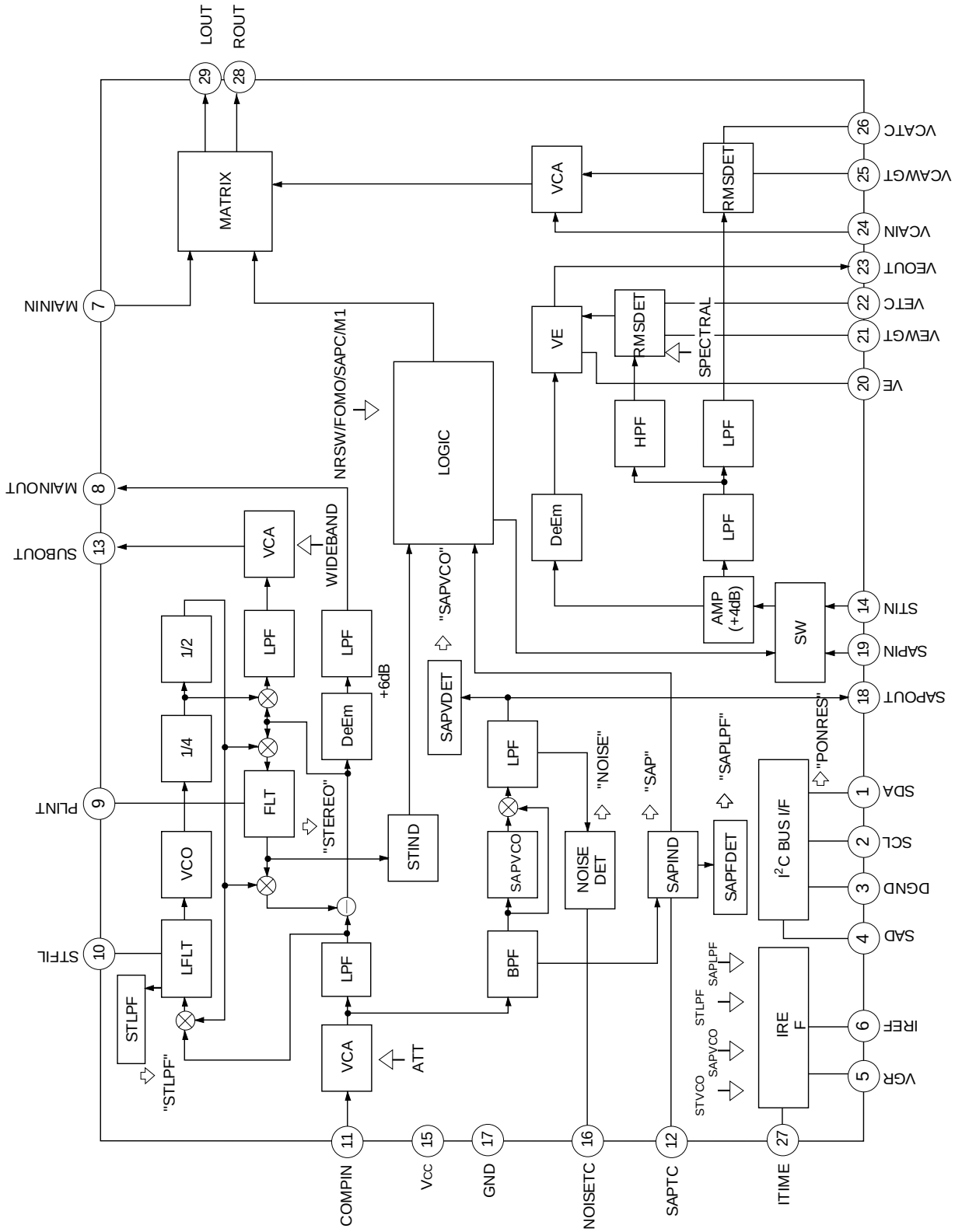
Bipolar silicon monolithic IC

Pin Configuration (Top View)

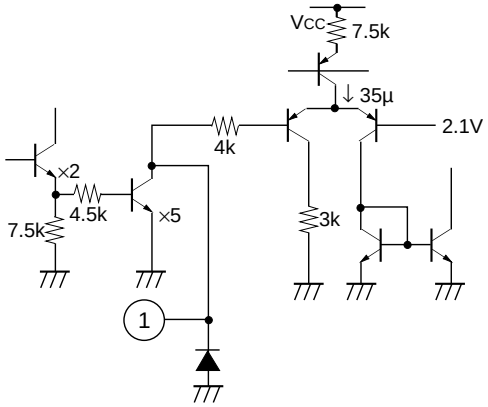
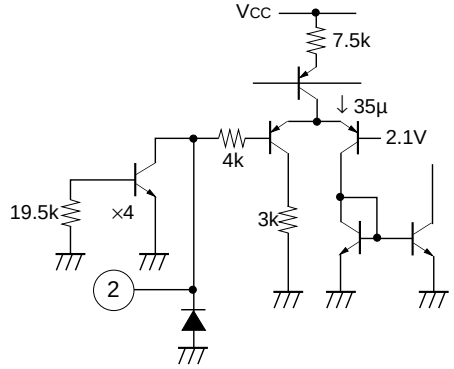
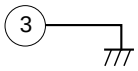
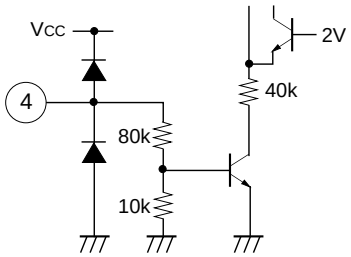
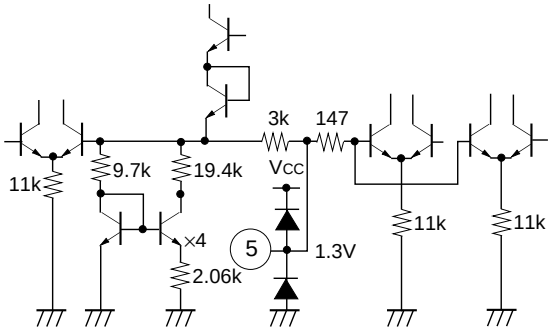


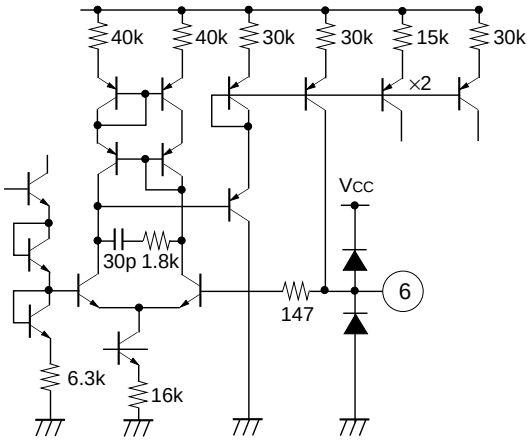
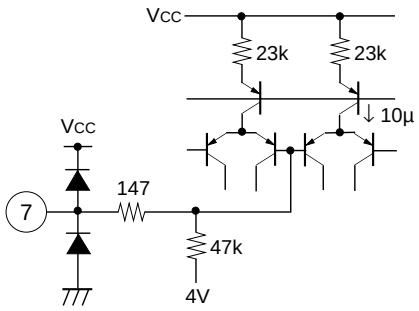
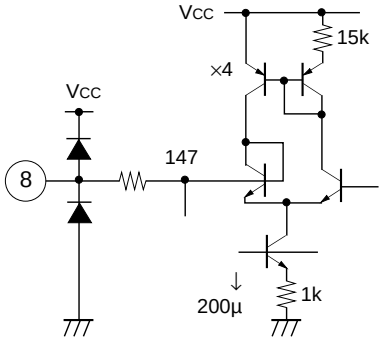
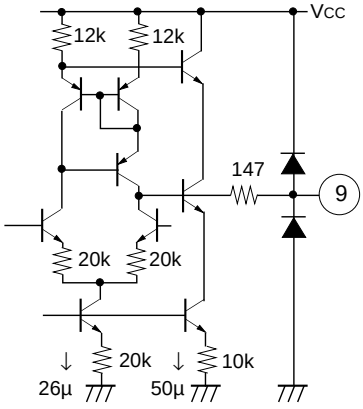
E94612B5Z-TE

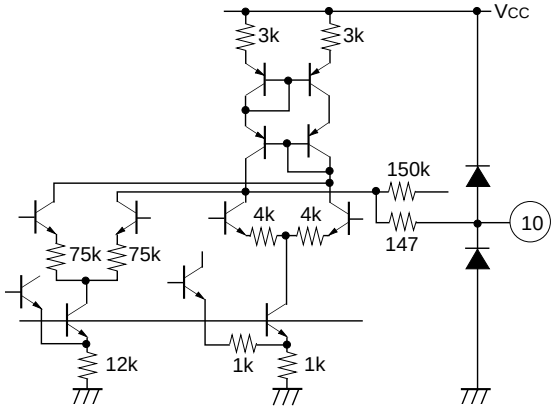
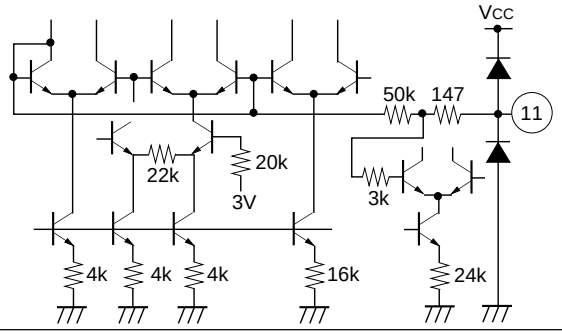
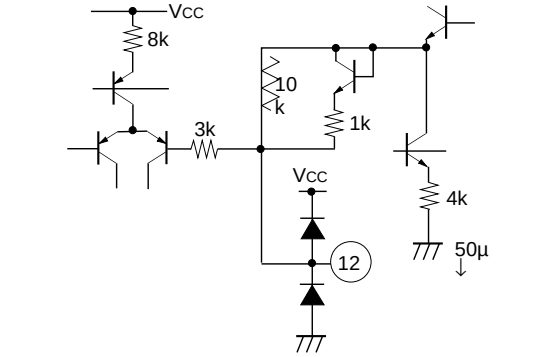
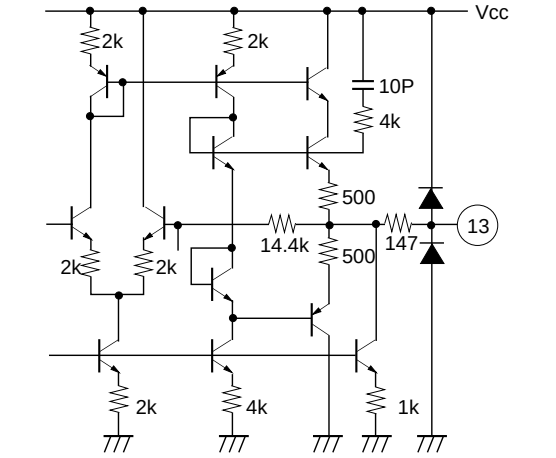
Block Diagram

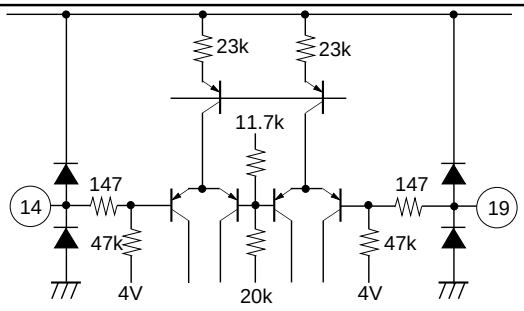
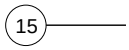
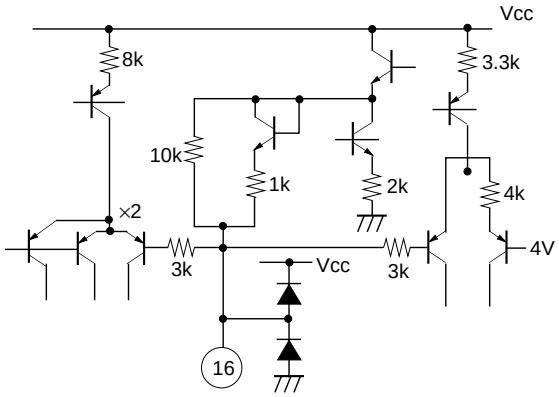
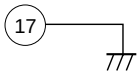
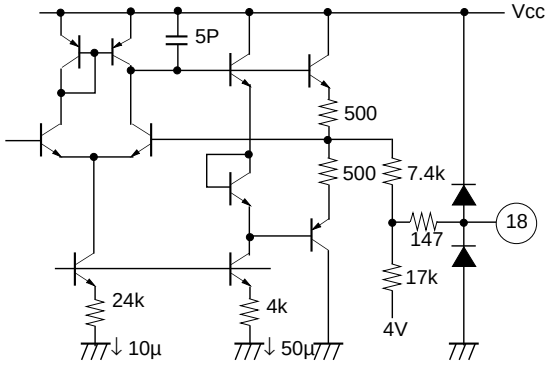
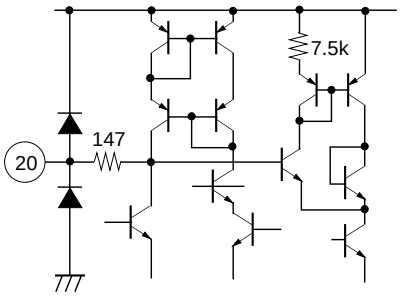


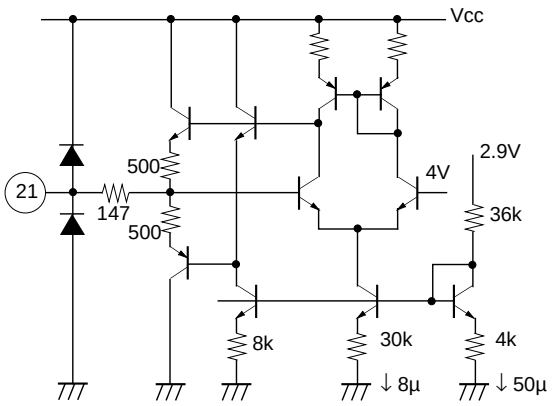
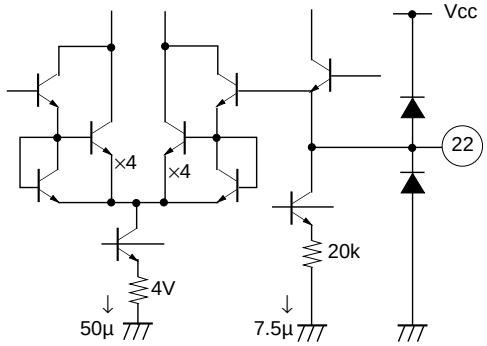
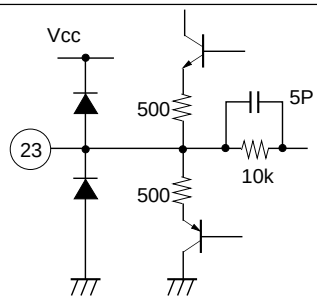
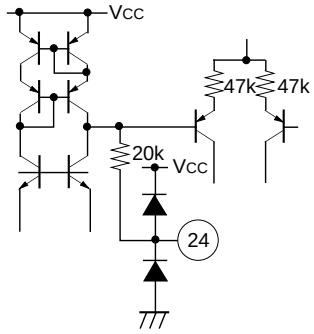
Pin Description (Ta = 25°C, V_{CC} = 9 V)

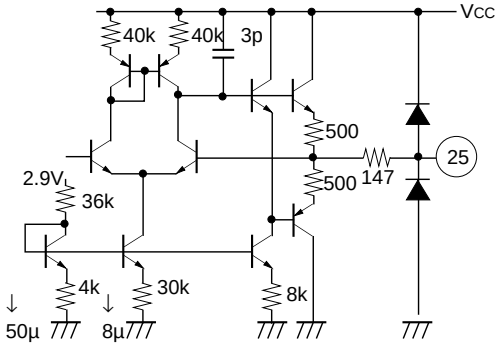
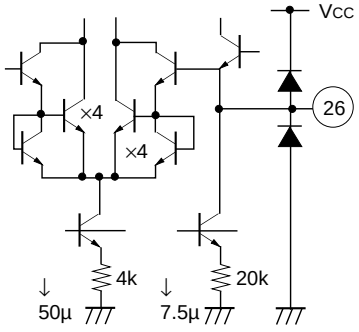
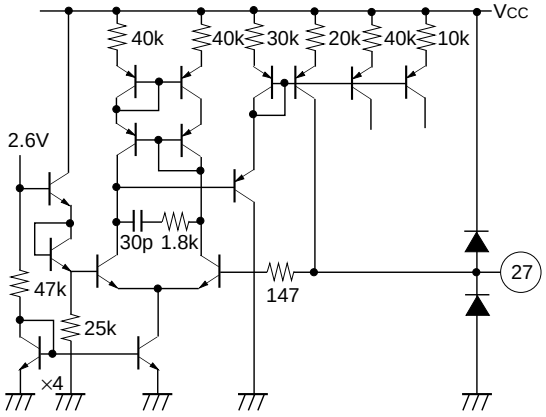
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	SDA	—		Serial data I/O pin. V_{IH} > 3.0 V V_{IL} < 1.5 V
2	SCL	—		Serial clock input pin. V_{IH} > 3.0 V V_{IL} < 1.5 V
3	DGND	—		Digital block GND.
4	SAD	—		Slave address control switch. The slave address is selected by changing the voltage applied to this pin.
5	VGR	1.3V		Band gap reference output pin. Connect a 10 µF capacitor between this pin and GND.

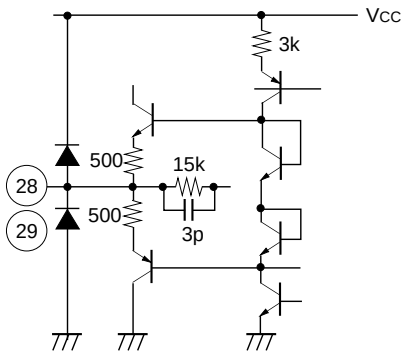
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	IREF	1.3V		Set the filter and VCO reference current. The reference current is adjusted with the BUS DATA based on the current which flows to this pin. (Connect a 62 kΩ ±1%) resistor between this pin and GND.)
7	MAININ	4.0V		Input the (L + R) signal from MAINOUT (Pin 8).
8	MAINOUT	4.0V		(L + R) signal output pin.
9	PLINT	6.3V		Pilot cancel circuit loop filter integrating pin. (Connect a 1 µF capacitor between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
10	STFIL	5.3V		Stereo block PLL loop filter integrating pin.
11	COMPIN	4.0V		Audio multiplexing signal input pin.
12	SAPTC	4.5V		Set the time constant for the SAP carrier detection circuit. (Connect a 4.7 µF capacitor between this pin and GND.)
13	SUBOUT	4.0V		(L - R) signal output pin.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
14	STIN	4.0V		Input the (L - R) signal from SUBOUT (Pin 13).
19	SAPIN	4.0V		Input the (SAP) signal from SAPOUT (Pin 18).
15	VCC	—		Supply voltage pin.
16	NOISETC	3.0V		Set the time constant for the noise detection circuit. (Connect a 4.7 µF capacitor and a 200 kΩ resistor between this pin and GND.)
17	GND	—		Analog block GND.
18	SAPOUT	4.0V		SAP FM detector output pin.
20	VE	4.0V		Variable de-emphasis integrating pin. (Connect a 2700 pF capacitor and a 3.3 kΩ resistor in series between this pin and GND.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	VEWGT	4.0V		Weight the variable de-emphasis control effective value detection circuit. (Connect a 0.047 µF capacitor and a 3 kΩ resistor in series between this pin and GND.)
22	VETC	1.7V		Determine the restoration time constant of the variable de-emphasis control effective value detection circuit. The specified restoration time constant can be obtained by connecting a 3.3 µF capacitor between this pin and GND.
23	VEOUT	4.0V		Variable de-emphasis output pin. (Connect a 4.7 µF non-polar capacitor between Pins 23 and 24.)
24	VCAIN	4.0V		VCA input pin. Input the variable de-emphasis output signal from Pin 23 via a coupling capacitor.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
25	VCAWGT	4.0V		Weight the VCA control effective value detection circuit. (Connect a 1 µF capacitor and a 3.9 kΩ resistor in series between this pin and GND.)
26	VCATC	1.7V		Determine the restoration time constant of the VCA control effective value detection circuit. The specified restoration time constant can be obtained by connecting a 10 µF capacitor between this pin and GND.
27	ITIME	1.3V		Set the reference current for the effective value detection timing current. The reference current is adjusted with the BUS DATA “SPECTRAL” based on the current which flows to this pin. The timing current determines the restoration time constant of the detection circuit and the variable de-emphasis characteristics. Connect a 43 kΩ (±1%) resistor between this pin and GND.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	ROUT	4.0V		Right channel output pin.
29	LOUT			Left channel output pin.
30	NC	—		—

Electrical Characteristics

COMPIN input level (100% modulation level)
- Main (L+R) =245mVrms (Pre-Emphasis : OFF)
- SUB (L-R) =490mVrms (dbx-TV : OFF)
- Pilot =49mVrms
- SAP Carrier =147mVrms

f_H=15.734kHz

No.	Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
			Mode	Input	Input signal	Output	Others				
1	Current consumption	Icc		—		—		22	32	42	mA
2	Main output level	Vmain	Mono	11	MAIN 1k 100% Pre-em ON	28 29	Using 15 kHz LPF	440	490	540	mVrms
3	De-emphasis frequency characteristics	FCdeem	Mono	11	MAIN 5k 30% Pre-em ON	28 29		–1.2	0	1.0	dB
4	Main LPF frequency characteristics	FCmain	Mono	11	MAIN 12k 30% Pre-em ON	28 29		–3.0	–1.0	1.0	
5	Main distortion	THDm	Mono	11	MAIN 1k 100% Pre-em ON	28 29	Using 15 kHz LPF	—	0.1	0.5	%
6	Main overload distortion	THDmmax	Mono	11	MAIN 1k 200% Pre-em ON	28 29	Using 15 kHz LPF	—	0.15	0.5	
7	Mono S/N	SNmain	Mono	11	NO Signal	28 29	Using 15 kHz LPF Compared with the TEST2 output level	61	69	—	dB
8	Sub output level	Vsub	ST	11	SUB 1k 100% NR-OFF	13	Using 15 kHz LPF	150	190	230	mVrms
9	Sub LPF frequency characteristics	FCsub	ST	11	SUB 12k 30% NR-OFF	13		–3.0	–0.5	1.0	dB
10	Sub distortion	THDsub	ST	11	SUB 1k 100% NR-OFF	13	Using 15 kHz LPF	—	0.1	1.0	%
11	Sub overload distortion	THDsmax	ST	11	SUB 1k 200% NR-OFF	13	Using 15 kHz LPF	—	0.5	2.0	
12	Sub S/N	SNsub	ST	11	f_H 0dB (49mVrms)	13	Using 15 kHz LPF Compared with the TEST8 output level	56	64	—	dB
13	Sub pilot leak	PCsub	ST	11	f_H 0dB (49mVrms)	13	Using f_H BPF	—	1.0	7.0	mVrms
14	ST on level	THst	ST	11	f_H	—	0dB=49mVrms	–8.0	–6.0	–4.0	dB
15	ST on/off hysteresis	HYst	ST	11	f_H	—	0dB=49mVrms	3.5	6.0	8.5	

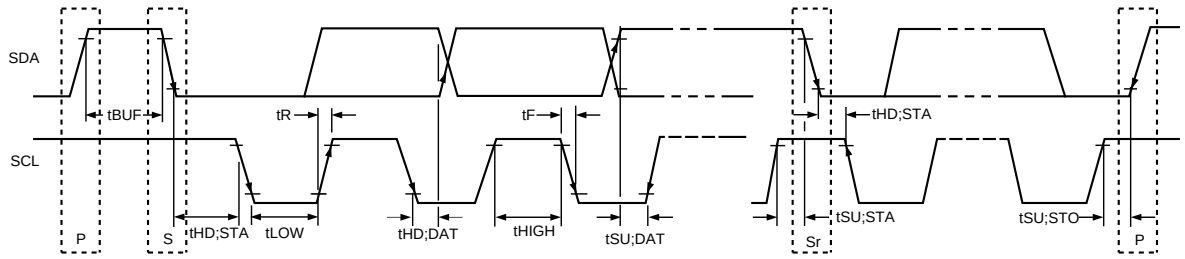
No.	Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
			Mode	Input	Input signal	Output	Others				
16	ST separation 1	STsep1	ST	11	ST 300Hz 30%, NR-ON	28 29	L→R R→L	23	35	—	dB
17	ST separation 2	STsep2	ST	11	ST 3kHz 30%, NR-ON	28 29	L→R R→L	23	35	—	
18	SAP output level	Vsap	SAP	11	SAP 1k 100% NR-OFF	18	Using 15kHz LPF	150	190	230	mVrms
19	SAP LPF frequency characteristics	FCsap	SAP	11	SAP 10k 30% NR-OFF	18		–3.0	0	2.5	dB
20	SAP distortion	THDsap	SAP	11	SAP 1k 100% NR-OFF	18	Using 15kHz LPF	—	2.5	6.0	%
21	SAP S/N	SNsap	SAP	11	SAP Carrier 147mVrms	18	Using 15kHz LPF Compared with the TEST18 output level	46	56	—	dB
22	SAP on level	THsap	SAP	11	SAP Carrier	—	0dB=147mVrms	–12	–9	–6.5	
23	SAP on/off hysteresis	HYsap	SAP	11	SAP Carrier	—	0dB=147mVrms	2.5	4	5.5	

I²C BUS block items (SDA, SCL)

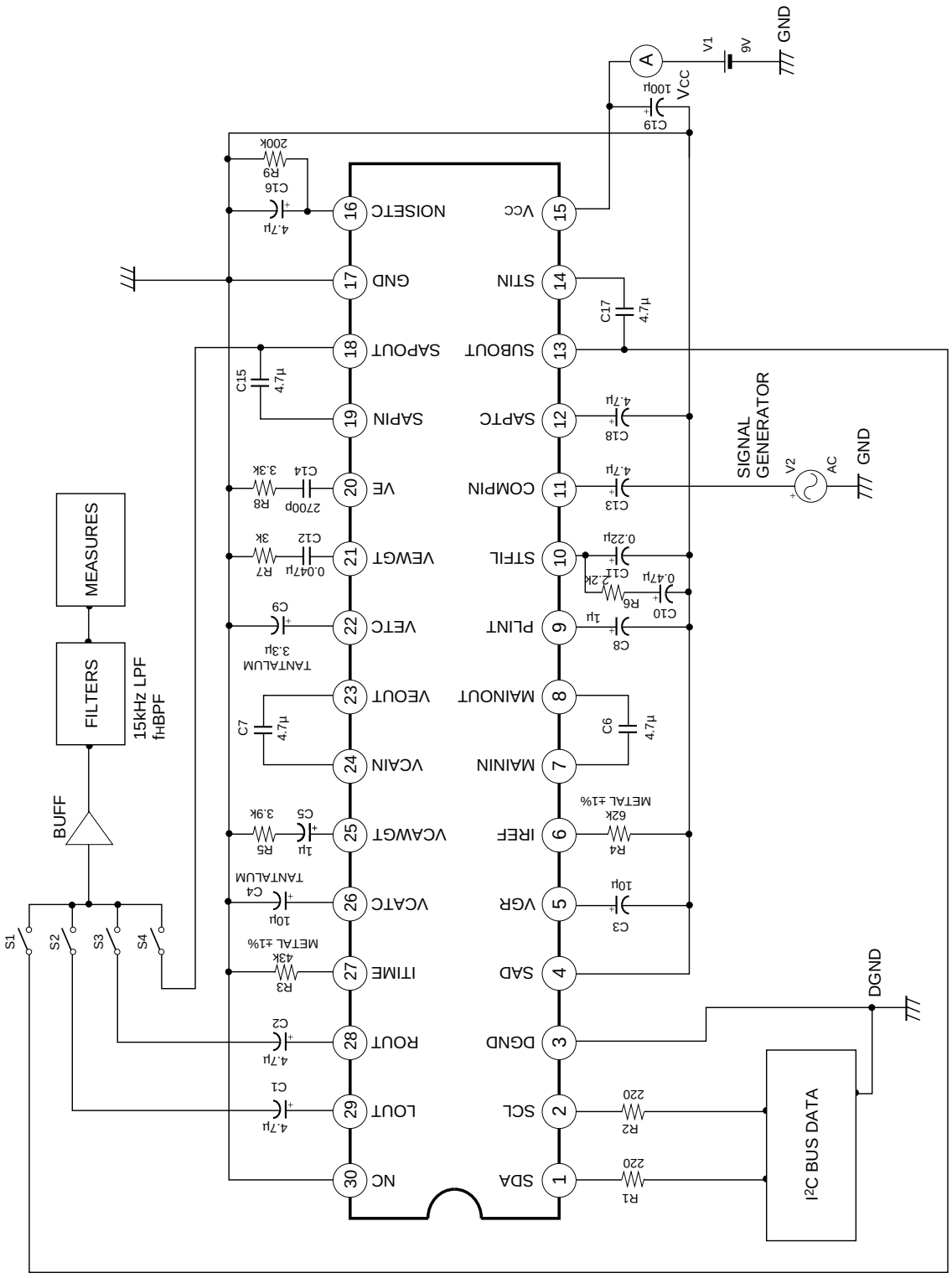
No.	Item	Symbol	Min.	Typ.	Max.	Unit
1	High level input voltage	V_{IH}	3.0	—	5.0	V
2	Low level input voltage	V_{IL}	0	—	1.5	
3	High level input current	I_{IH}	—	—	10	µA
4	Low level input current	I_{IL}	—	—	10	
5	Low level output voltage SDA (Pin 1) during 3 mA inflow	V_{OL}	0	—	0.4	V
6	Max. inflow current	I_{OL}	3	—	—	mA
7	Input capacitance	C_I	—	—	10	pF
8	Max. clock frequency	f_{SCL}	0	—	100	kHz
9	Minimum waiting time for data change	t_{BUF}	4.7	—	—	µs
10	Minimum waiting time for start of data transfer	$t_{HD:STA}$	4.0	—	—	
11	Low level clock pulse width	t_{LOW}	4.7	—	—	
12	High level clock pulse width	t_{HIGH}	4.0	—	—	
13	Minimum waiting time for start preparation	$t_{SU:STA}$	4.7	—	—	
14	Min. data hold time	$t_{HD:DAT}$	0	—	—	
15	Min. data preparation time	$t_{SU:DAT}$	250	—	—	ns
16	Rise time	t_R	—	—	1	µs
17	Fall time	t_F	—	—	300	ns
18	Minimum waiting time for stop preparation	$t_{SU:STO}$	4.7		—	µs

I²C BUS load conditions: Pull-up resistor 4 kΩ (Connect to +5 V)
Load capacity 200 pF (Connect to GND)

I²C BUS Control Signal



Electrical Characteristics Measurement Circuit



I²C BUS Register Data Standard Setting Values

Register	Number of bits	Classification	Standard setting	Contents	Setting value when electrical characteristics are measured
ATT	4	A	9	Center point	Adjustment point
STVCO	6	A	1F		
SAPVCO	4	A	8		
SAPLPF	4	A	8		
STLPF	6	A	1F		
SPECTRAL	6	A	1F		
WIDEBAND	6	A	1F		
TEST-DA	1	T	0	Normal mode	
TEST1	1	T	0		
NRSW	1	U	—	According to the mode control table	
FOMO	1	U	—		
M1	1	U	1	Mute OFF	
SAPC	1	S	—	Fixed by the set specifications	
ATTSW	1	S	—		

Classification A: Adjustment
U: User control
S: Proper to set
T: Test

List of Adjustment Contents

	Adjustment item	Adjustment data	Input pin	Input signal	Measurement item	Adjustment contents	Test mode setting
1	MAIN VCA	ATT	COMPIN (Pin 11)	100Hz 245mVrms	LOUT output level	Adjust as close to 490 mVrms as possible	
2	ST VCO	STVCO	None	None	ROUT output frequency	Adjust as close to 62.936 kHz as possible	TEST-DA=1
3	SAP VCO	SAPVCO	COMPIN (Pin 11)	$5f_H$ (78.67k) 147mVrms	STA7 (SAPVCO1) STA8 (SAPVCO2)	Adjust to the center of the SAPVCO1 = 0, SAPVCO2 = 1 condition	
4	ST & dbx FILTER	STLPF	COMPIN (Pin 11)	9.4kHz 600mVrms	STA3 (STLPF)	Adjust to the center of the STLPF = 1 condition	TEST1=1
5	SAP FILTER	SAPLPF	COMPIN (Pin 11)	88kHz 120mVrms	STA4 (SAPLPF)	Adjust to the center of the SAPLPF = 1 condition	TEST1=1
6	Low frequency ST separation	WIDEBAND	COMPIN (Pin 11)	ST-L 30% 300Hz	ROUT output level	Minimize the output level	
	High frequency ST separation	SPECTRAL	COMPIN (Pin 11)	ST-L 30% 3kHz	ROUT output level	Minimize the output level	

Adjustment Method

1 ATT adjustment

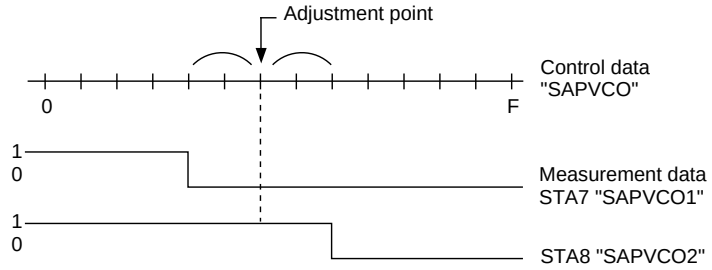
1. TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
2. Input a 100 Hz, 245 mVrms sine wave signal to COMPIN and monitor the LOUT output level. Then, adjust the “ATT” data for ATT adjustment so that LOUT output goes to the standard value.
3. Adjustment range: ±30%
   Adjustment bits: 4 bits

2 Stereo VCO adjustment

1. TEST BIT is set to “TEST1 = 0” and “TEST-DA = 1”.
2. Monitor the ROUT output (4 f_H free run) frequency in a no input state, and adjust “STVCO” adjustment data so that this frequency is as close to 4f_H (62.936 kHz) as possible.
3. Adjustment range: ±20%
   Adjustment bits: 6 bits

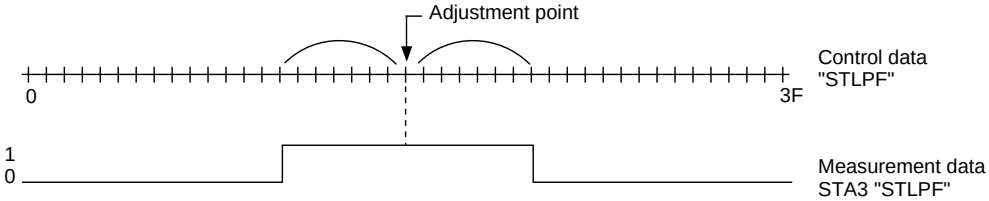
3 SAPVCO adjustment

1. TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
2. Input a 5f_H (SAP carrier , 78.67 kHz) , 147 mVrms sine wave signal to COMPIN. While monitoring the STATUS FLAG (STA7, STA8) condition, adjust “SAPVCO” adjustment data.
3. Adjustment range: ±20%
   Adjustment bits: 4 bits
   Align SAPVCO with the center of the STA7 = 0 and STA8 = 1 (adjustment OK) condition range.



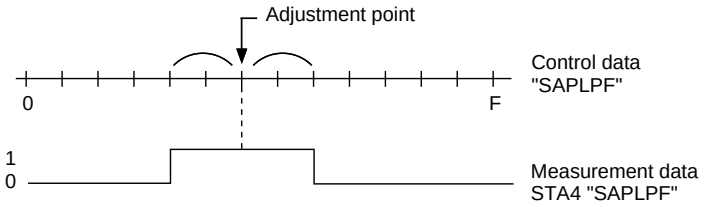
4 Stereo block dbx filter adjustment

1. TEST BIT is set to “TEST1 = 1” and “TEST-DA = 0”.
2. Input a 9.4 kHz, 600 mVrms sine wave signal to COMPIN. While monitoring the STATUS FLAG (STA3) condition, adjust the “STLPF” adjustment data.
3. Adjustment range: ±20%
   Adjustment bits: 6 bits
   Align STLPF with the center of the STA3 = 1 (adjustment OK) condition range.



5 SAP block filter adjustment

1. TEST BIT is set to “TEST1 = 1” and “TEST-DA = 0”.
2. Input a 88 kHz, 120 mVrms sine wave signal to COMPIN. While monitoring the STATUS FLAG (STA4) condition, vary and adjust the “SAPLPF” adjustment data.
3. Adjustment range: ±20%
   Adjustment bits: 4 bits
   Align SAPLPF with the center of the STA4 = 1 (adjustment OK) condition range.



6 Separation adjustment

1. TEST BIT is set to “TEST1 = 0” and “TEST-DA = 0”.
2. Set the unit to stereo mode and input the left channel only signal (modulation factor 30%, frequency 300 Hz) to COMPIN. At this time, adjust the “WIDEBAND” adjustment data to reduce ROUT output to the minimum.
3. Next, set the frequency only of the input signal to 3 kHz and adjust the “SPECTRAL” adjustment data to reduce ROUT output to the minimum.
4. Then, the adjustments in 2 and 3 above are performed to optimize the separation.
5. “WIDEBAND” “SPECTRAL”
   Adjustment range: ±30% Adjustment range: ±15%
   Adjustment bits: 6 bits Adjustment bits: 6 bits

Description of Operation

The US audio multiplexing system possesses the base band spectrum shown in Fig. 1.

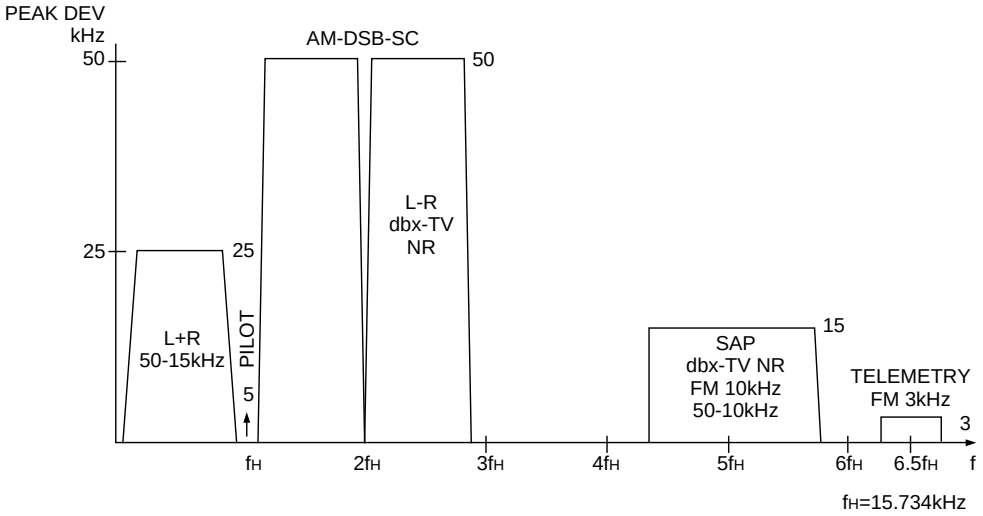


Fig. 1. Base band spectrum

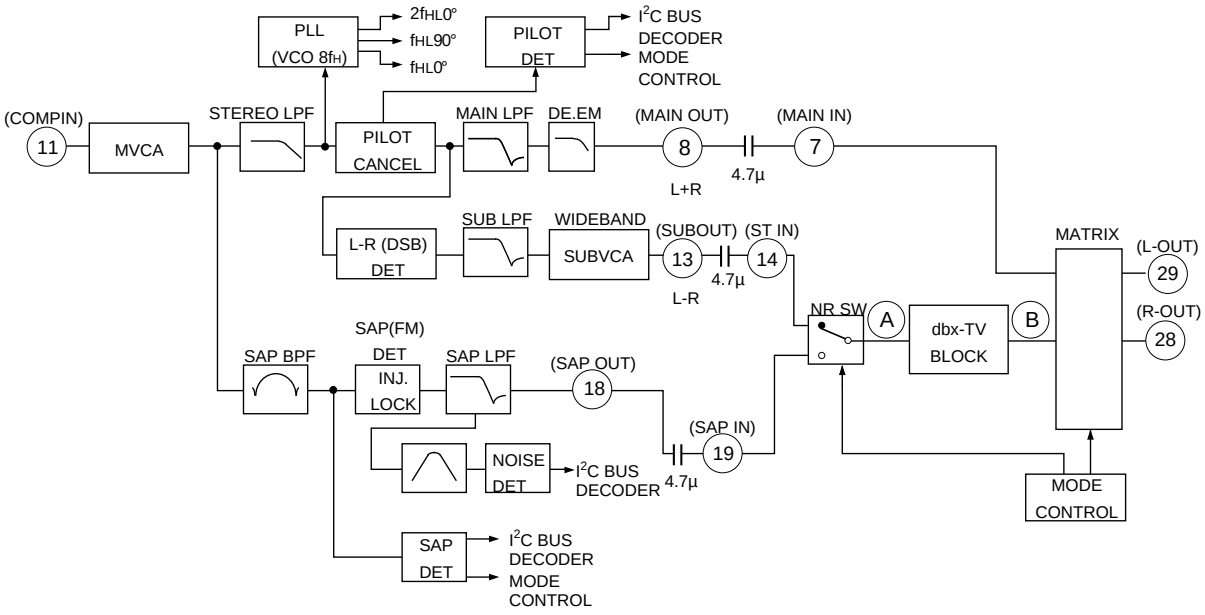


Fig. 2. Overall block diagram (See Fig. 3 for the dbx-TV block)

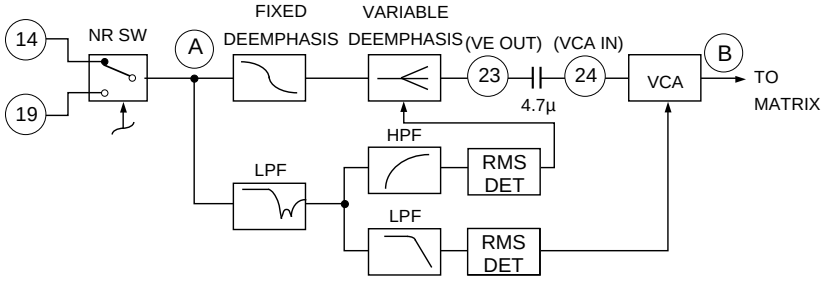


Fig. 3. dbx-TV block

(1) L + R (MAIN)

After the audio multiplexing signal input from COMPIN (Pin 11) passes through MVCA, the SAP signal and telemetry signal are suppressed by STEREO LPF. Next, the pilot signals are canceled. Finally, the L - R signal and SAP signal are removed by MAIN LPF, and frequency characteristics are flattened (de-emphasized) and input to the matrix.

(2) L - R (SUB)

The L - R signal follows the same course as L + R before the pilot signal is canceled. L - R has no carrier signal, as it is a suppressed-carrier double-sideband amplitude modulated signal (DSB-AM modulated). For this reason, the pilot signal is used to regenerate the carrier signal (quasi-sine wave) to be used for the demodulation of the L - R signal. In the last stage, the residual high frequency components are removed by SUB LPF and the L - R signal is input to the dbx-TV block via the NRSW circuit after passing through SUBVCA.

(3) SAP

SAP is an FM signal using $5f_H$ as a carrier as shown in the Fig.1. First, the SAP signal only is extracted using SAP BPF. Then, this is subjected to FM detection. Finally, residual high frequency components are removed and freqency characteristics flattened using SAP LPF, and the SAP signal is input to the dbx-TV block via the NRSW circuit. When there is no SAP signal, the Pin 18 output is soft muted.

(4) Mode discrimination

Stereo discrimination is performed by detecting the pilot signal amplitude. SAP discrimination is performed by detecting the $5f_H$ carrier amplitude. NOISE discrimination is performed by detecting the noise near 25 kHz after FM detection.

(5) dbx-TV block

Either the SAP signal or L - R signal input respectively from ST IN (Pin 14) or SAP IN (Pin 19) is selected by the mode control and input to the dbx-TV block.

The input signal then passes through the fixed de-emphasis circuit and is applied to the variable de-emphasis circuit. The signal output from the variable de-emphasis circuit passes through an external capacitor and is applied to VCA (voltage control amplifier). Finally, the VCA output is converted from a current to a voltage using an operational amplifier and then input to the matrix.

The variable de-emphasis circuit transmittance and VCA gain are respectively controlled by each of effective value detection circuits. Each of the effective value detection circuits passes the input signal through a predetermined filter for weighting before the effective value of the weighted signal is detected to provide the control signal.

(6) Others

“MVCA” is a VCA which adjusts the input signal level to the standard level of this IC. In addition, the input signal enters the decoder without passing through MVCA by setting to ATTSW = 1.

The signals (L + R, L - R, SAP) input to “MATRIX” are selected according to the BUS data and whether there is ST or SAP discrimination, and any one of the ST-L, ST-R, MONO or SAP signals is output to LOUT and ROUT.

“Bias” supplies the reference voltage and reference current to the other blocks. The currents flowing to the resistors connecting IREF (Pin 6) and ITIME (Pin 27) with GND become the reference current.

Register Specifications

Slave address

SAD pin	SLAVE RECEIVER	SLAVE TRANSMITTER
GND	80H	81H
Vcc	8AH	8BH

Register table

SUB ADDRESS	DATA							
MSB LSB	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
****0000	*	ATTSW	TEST-DA	TEST1	ATT [4] INPUT LEVEL adj			
****0001	*		STVCO [6] STEREO VCO adj					
****0010	(SAPVCO [4] SAP VCO adj)				(SAPLPF [4] SAP FILTER adj)			
****0011	*		STLPF [6] ST FILTER adj					
****0100	*		SPECTRAL [6]					
****0101	*		WIDEBAND [6]					
****0110	*				NRSW	FOMO	SAPC	M1

*: Don't Care

Status Register

When TEST1 = 0

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	SAP	NOISE	—	—	SAP VCO1	SAP VCO2

When TEST1 = 1

STA1	STA2	STA3	STA4	STA5	STA6	STA7	STA8
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
POWER ON RESET	STEREO	STLPF	SAPLPF	—	—	—	—

Description of Registers

Control registers

Register	Number of bits	Classification*	Contents
ATT	4	A	Input level adjustment
STVCO	6	A	STEREO VCO free running frequency adjustment
SAPVCO	4	A	SAP VCO free running frequency adjustment
SAPLPF	4	A	SAP filter adjustment
STLPF	6	A	STEREO and dbx filter adjustment
SPECTRAL	6	A	Adjustment of stereo separation (3 kHz)
WIDEBAND	6	A	Adjustment of stereo separation (300 Hz)
TEST-DA	1	T	Turn to DAC test mode and STVCO adjustment mode by means of TEST-DA = 1.
TEST1	1	T	Turn to test mode by means of TEST = 1. (Adjustment of STLPF and SAPLPF)
NRSW	1	U	Selection of the output signal (STEREO mode , SAP mode)
FOMO	1	U	Turn to forced MONO by means of FOMO = 1. (LOUT only is MONO during SAP output.)
M1	1	U	Selection of mute ON/OFF (0: mute ON, 1: mute OFF)
SAPC	1	S	Selection of SAP mode or L + R mode according to the presence of SAP broadcasting
ATTSW	1	S	Turns the input stage MVCA off when ATTSW = 1.

*Classification U: User control
A: Adjustment
S: Proper to set
T: Test

Status registers

Register	Number of bits	Contents	
PONRES	1	POWER ON RESET detection;	1: RESET
STEREO	1	Stereo discrimination of the input signal;	1: Stereo
SAP	1	SAP discrimination of the input signal;	1: SAP
NOISE	1	Noise level discrimination of the input signal mode;	1: Noise
STLPF	1	Status of STEREO filter adjustment;	1: OK range
SAPLPF	1	Status of SAP filter adjustment;	1: OK range
SAPVCO1	1	Status 1 of SAP VCO free running frequency adjustment;	0: OK range
SAPVCO2	1	Status 2 of SAP VCO free running frequency adjustment;	1: OK range

Description of Control Registers

ATT (4): Adjust the signal level input to COMPIN (Pin 11) to the reference level (245 mVrms).
Variable range of the input signal: 245 mVrms –5.0 dB to +3.0 dB
0 = Level min.
F = Level max.

STVCO (6): Adjust STEREO VCO free running frequency (f_0).
Variable range: f_0 ±20%
0 = Free running frequency min.
3F = Free running frequency max.

SAPVCO (4): Adjust SAPVCO free running frequency (f_0).
Variable range: f_0 ±20%
0 = Free running frequency min.
F = Free running frequency max.

SAPLPF (4): Adjust the filter f_0 of the SAP block.
Variable range: f_0 ±20%
0 = Frequency min.
F = Frequency max.

STLPF (6): Adjust the filter f_0 of the ST and dbx blocks.
Variable range: f_0 ±20%
0 = Frequency min.
3F = Frequency max.

SPECTRAL (6): Perform high frequency (fs = 3 kHz) separation adjustment.
0 = Level max.
3F = Level min.

WIDEBAND (6): Perform low frequency (fs = 300 Hz) separation adjustment.
0 = Level min.
3F = Level max.

TEST1 (1): Set filter adjustment mode.
0 = Normal mode
1 = STLPF (STA3) and SAPLPF (STA4) adjustment mode
In addition, the following outputs are present at Pins 28 and 29.
LOUT (Pin 29): SAP BPF OUT
ROUT (Pin 28): NR BPF OUT

TEST-DA (1): Set DAC output test mode and STVCO adjustment mode.
0 = Normal mode
1 = DAC output test mode and STVCO adjustment mode
LOUT (Pin 29): DA control DC level
ROUT (Pin 28): STEREO VCO oscillation frequency (4 f_H)

NRSW (1) Select stereo mode or SAP mode
0 = Stereo mode
1 = SAP mode

FOMO (1): Select forced MONO mode
0 = Normal mode
1 = Forced MONO mode

SAPC (1): Select the SAP signal output mode
When there is no SAP signal, the conditions for selecting SAP output are selected by SAPC.
0 = L + R output is selected
1 = SAP output is selected

ATTSW (1) MAIN VCA switch
0 = Normal mode
1 = MAIN VCA is passed.

M1 (1) Mute the LOUT and ROUT output
0 = Mute ON
1 = Mute OFF

Description of Mode Control

Priority ranking: TEST-DA > TEST1 > M1 > (NRSW & FOMO & SAPC)

<table>
<tr><th>Mode control</th><th>SAPC=0</th><th>SAPC=1</th></tr>
<tr><td>NRSW</td><td>“Select dbx input and LOUT & ROUT output”
Conditions: FOMO = 0
NRSW = 0 (MONO or ST output)

• During ST input: LOUT : L,
ROUT : R
• During other input: LOUT : L + R,
ROUT : L + R

NRSW = 1 (SAP output)
• When there is “SAP” during SAP discrimination
LOUT: SAP, ROUT: SAP
• When there is “No SAP”, output is the same as when NRSW = 0.</td><td>“Select dbx input and LOUT & ROUT output”
Conditions: FOMO = 0
NRSW = 0 (MONO or ST output)

As on the left

NRSW = 1 (SAP output)
• Regardless of the presence of SAP discrimination,
dbx input: “SAP”
LOUT: SAP, ROUT: SAP
However, when there is no SAP, SAPLPF output is soft muted (–7 dB)</td></tr>
<tr><td>FOMO</td><td colspan="2">“Forced MONO”
FOMO = 1
• During SAP output: LOUT: L + R, ROUT: SAP
• During ST or MONO output: LOUT: L + R, ROUT: L + R</td></tr>
<tr><td>SAPC</td><td colspan="2">Change the selection conditions for “MONO or ST output” and “SAP output”.
SAPC = 0: Switch to SAP output when there is SAP discrimination.
Do not switch to SAP output when there is no SAP discrimination.
SAPC = 1: Switch to SAP output regardless of whether there is SAP discrimination.</td></tr>
<tr><td>M1</td><td colspan="2">“MUTE”
M1 = 0
Output is muted.</td></tr>
<tr><td>TEST1</td><td colspan="2">“TEST1”
TEST1 = 1
Return adjustment data with STATUS REGISTER as an adjustment mode.
In addition, outputs are as follows.
LOUT: SAP BPF OUT
ROUT: NR BPF OUT</td></tr>
<tr><td>TEST-DA</td><td colspan="2">“TEST-DA”
TEST-DA = 1
Used to TEST of D/A.
LOUT: D/A output
ROUT: STVCO oscillation frequency (4 f_H)</td></tr>
</table>

Mode Control No. 1 (SAPC = 1)

Input signal mode	Mode detection			Mode control			dbx	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC	input	Lch	Rch
MONO[1)]	0	0	0	0	*	1	MUTE	L+R	L+R
	0	0	0	1	0	1	SAP	SAP	SAP
	0	0	0	1	1	1	SAP	L+R	SAP
	0	*	1	0	*	1	MUTE	L+R	L+R
	0	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	*	1	1	1	1	(SAP)	L+R	(SAP)
STEREO[1)]	1	0	*	0	0	1	L-R	L	R
	1	0	*	0	1	1	MUTE	L+R	L+R
	1	1	1	0	0	1	L-R	L	R
	1	1	1	0	1	1	MUTE	L+R	L+R
	1	0	0	1	0	1	SAP	SAP	SAP
	1	0	0	1	1	1	SAP	L+R	SAP
	1	*	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	*	1	1	1	1	(SAP)	L+R	(SAP)
MONO & SAP	0	1	*	0	0	1	MUTE	L+R	L+R
	0	1	*	0	1	1	MUTE	L+R	L+R
	0	1	0	1	0	1	SAP	SAP	SAP
	0	1	0	1	1	1	SAP	L+R	SAP
	0	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	1	(SAP)	L+R	(SAP)
STEREO & SAP	1	1	*	0	0	1	L-R	L	R
	1	1	*	0	1	1	MUTE	L+R	L+R
	1	1	0	1	0	1	SAP	SAP	SAP
	1	1	0	1	1	1	SAP	L+R	SAP
	1	1	1	1	0	1	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	1	(SAP)	L+R	(SAP)

Note)

(SAP) : The SAPOUT output signal is soft muted (approximately –7 dB).
The signal is soft muted when NOISE = 1.

* : Don't care.

1) : SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

Mode Control No. 2 (SAPC = 0)

Input signal mode	Mode detection			Mode control			dbx	Output	
	ST	SAP	NOISE	NRSW	FOMO	SAPC	input	Lch	Rch
MONO[1)]	0	0	*	*	*	0	MUTE	L+R	L+R
	0	1	1	0	0	0	MUTE	L+R	L+R
	0	1	1	0	1	0	MUTE	L+R	L+R
	0	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	0	1	1	1	1	0	(SAP)	L+R	(SAP)
STEREO[1)]	1	0	*	0	0	0	L-R	L	R
	1	0	*	0	1	0	MUTE	L+R	L+R
	1	0	*	1	0	0	L-R	L	R
	1	0	*	1	1	0	MUTE	L+R	L+R
	1	1	1	0	0	0	L-R	L	R
	1	1	1	0	1	0	MUTE	L+R	L+R
	1	1	1	1	0	0	(SAP)	(SAP)	(SAP)
	1	1	1	1	1	0	(SAP)	L+R	(SAP)
MONO & SAP	0	1	0	0	0	0	MUTE	L+R	L+R
	0	1	0	0	1	0	MUTE	L+R	L+R
	0	1	0	1	0	0	SAP	SAP	SAP
	0	1	0	1	1	0	SAP	L+R	SAP
	0	1	1	0	0	0	MUTE	L+R	L+R
	0	1	1	0	1	0	MUTE	L+R	L+R
	0	1	1	1	0	0	MUTE	L+R	L+R
	0	1	1	1	1	0	MUTE	L+R	L+R
STEREO & SAP	1	1	0	0	0	0	L-R	L	R
	1	1	0	0	1	0	MUTE	L+R	L+R
	1	1	0	1	0	0	SAP	SAP	SAP
	1	1	0	1	1	0	SAP	L+R	SAP
	1	1	1	0	0	0	L-R	L	R
	1	1	1	0	1	0	MUTE	L+R	L+R
	1	1	1	1	0	0	L-R	L	R
	1	1	1	1	1	0	MUTE	L+R	L+R

Note)

(SAP) : The SAPOUT output signal is soft muted (approximately –7 dB).
The signal is soft muted when NOISE = 1.

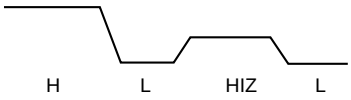
* : Don't care.

1) : SAP or NOISE discrimination may be made during MONO or STEREO input when the noise is inputted in the weak electric field.
"NOISE" status rises earlier than "SAP" status when the amount of noise is increased to COMPIN.

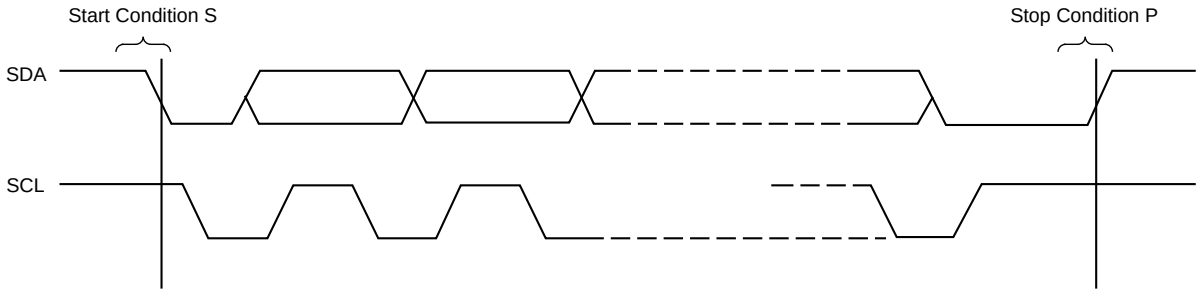
I²C BUS Signal

There are two I²C signals, SDA (Serial DATA) and SCL (Serial CLOCK) signal. SDA is a bidirectional signal.

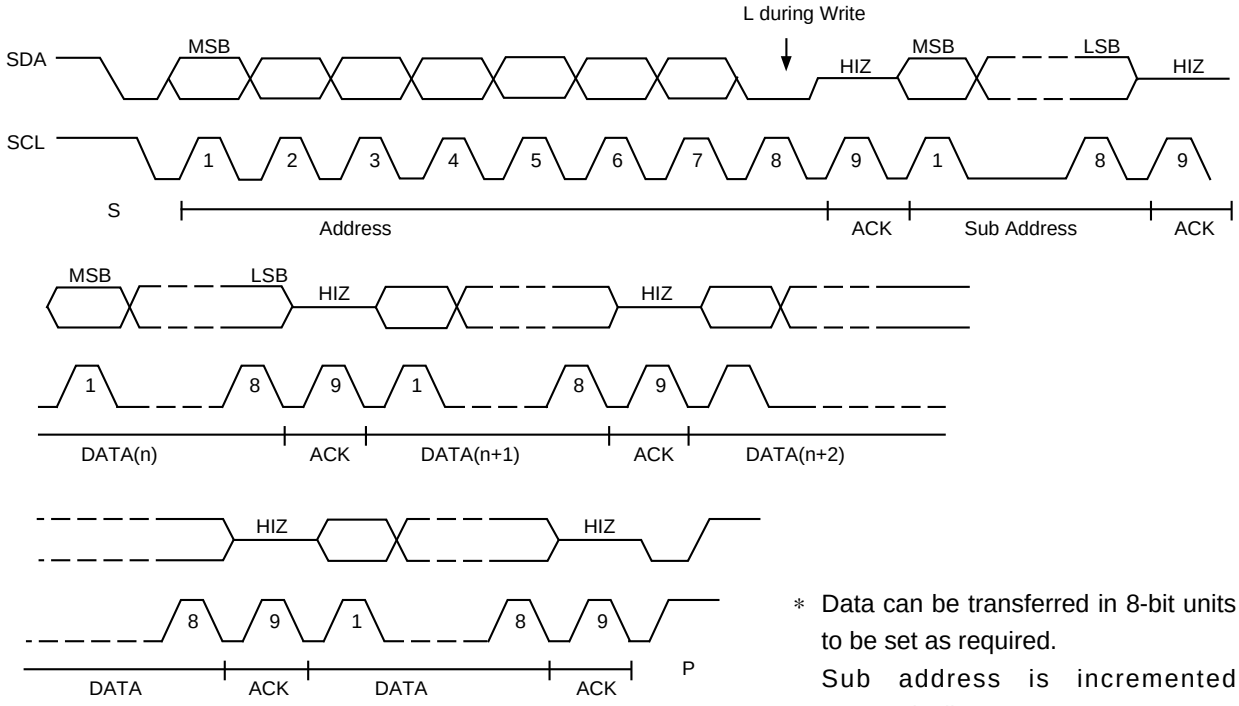
• Accordingly there are 3 values outputs, H, L and HIZ.



• I²C transfer begins with Start Condition and ends with Stop Condition.

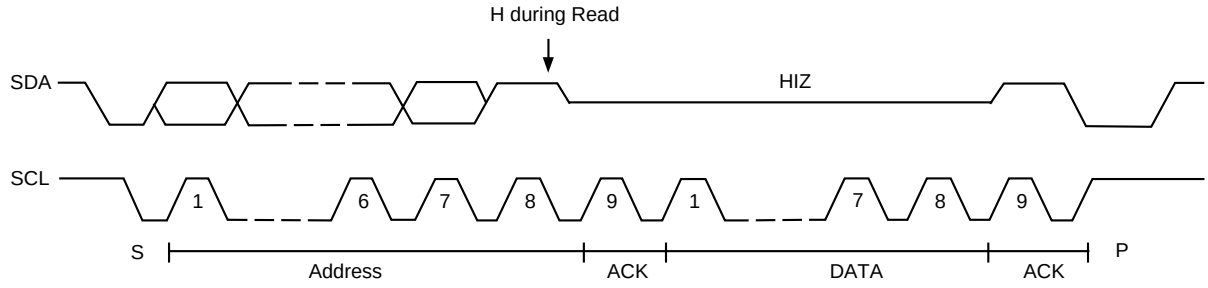


• I²C data Write (Write from I2C controller to the IC)

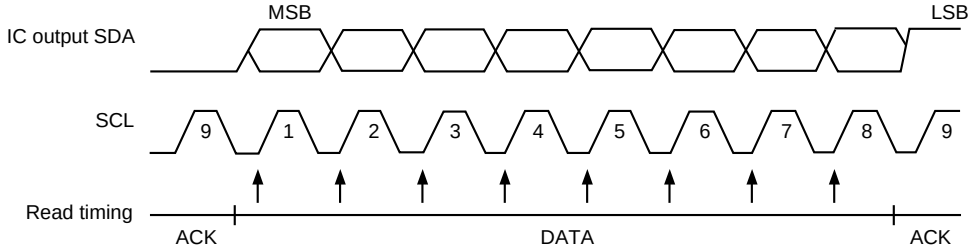


* Data can be transferred in 8-bit units to be set as required.
  Sub address is incremented automatically.

• I²C data Read (Read from the IC to I²C controller)

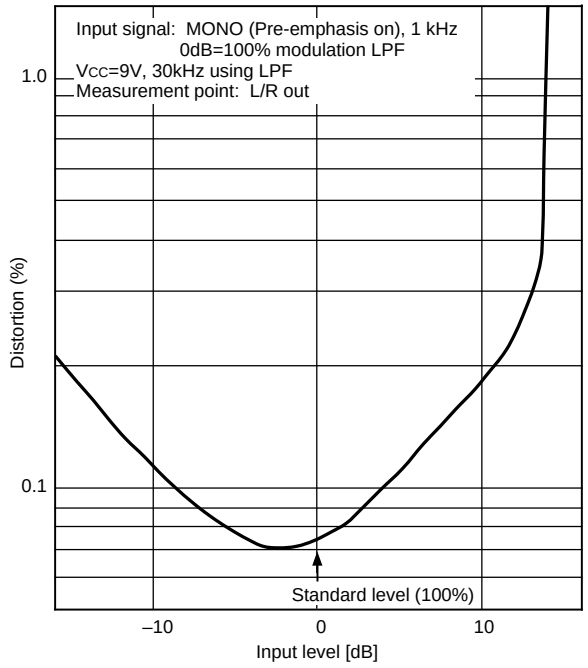


• Read timing

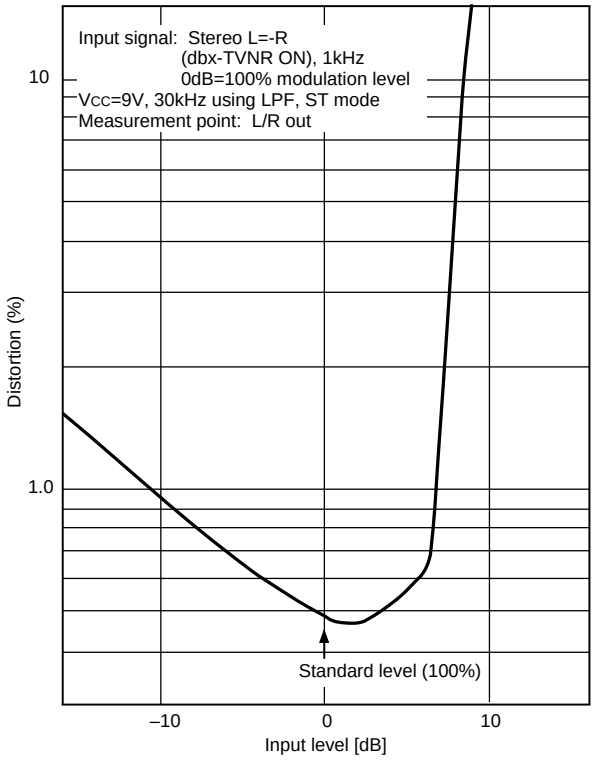


∗ Data Read is performed during SCL rise.

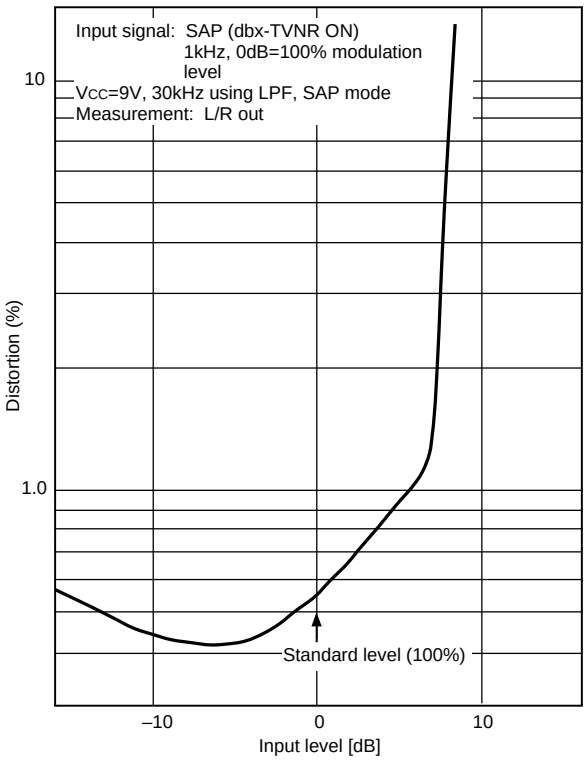
Input level vs. Distortion characteristics 1 (MONO)



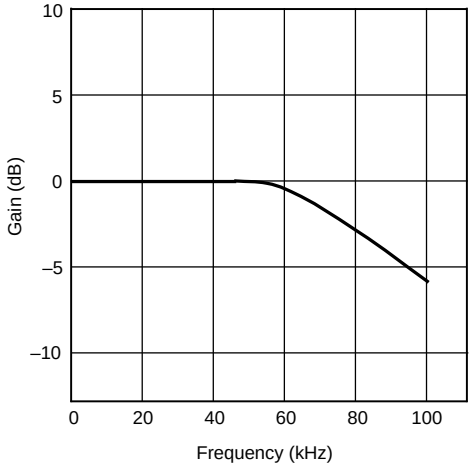
Input level vs. Distortion characteristics 2 (Stereo)



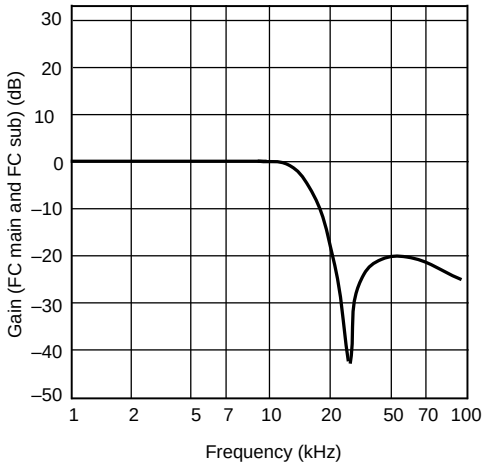
Input level vs. Distortion characteristics 3 (SAP)



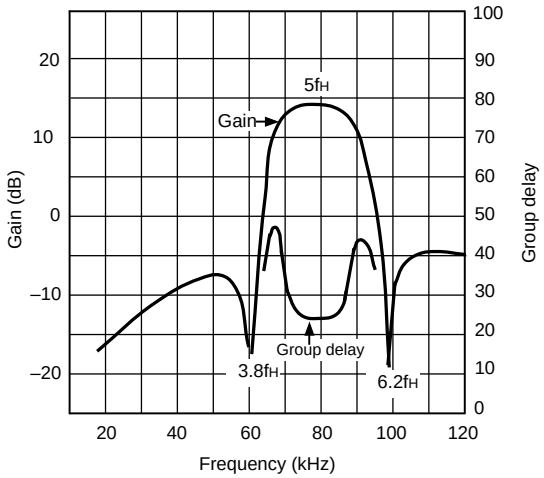
Stereo LPF frequency characteristics



Main LPF and Sub LPF frequency characteristics

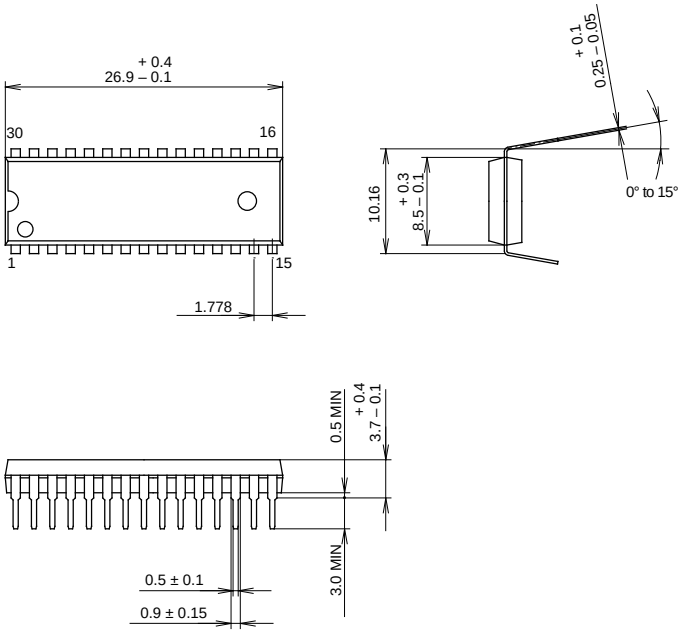


SAP frequency characteristics and group delay



Package Outline Unit : mm

30PIN SDIP (PLASTIC)



SONY CODE	SDIP-30P-01
EIAJ CODE	SDIP030-P-0400
JEDEC CODE	

PACKAGE STRUCTURE

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	1.8g