

2GHz-band PLL IC for Mobile Communications

Descriptions

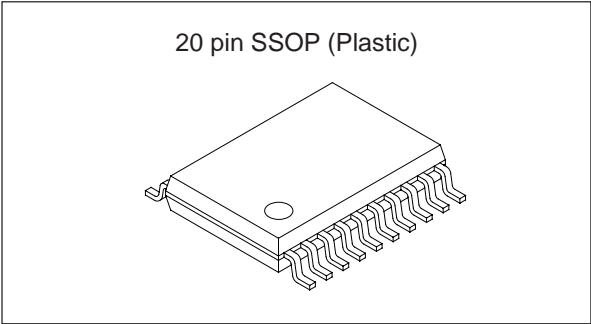
The CXA1787N is a frequency synthesizer PLL IC developed for use in mobile communication systems. This IC has low current consumption, small package and is suitable for portable sets of cellular telephone and others.

Features

- Low current consumption
I_{cc} = 8.0mA (typ.)
0.3mA (typ.) in power saving mode
- Maximum operating frequency
1.8GHz guaranteed
- Operating supply voltage range
2.7 to 5.5V
- Ultra small 20-pin SSOP package
- Two types of phase comparator output:
For external charge pump φR φP
Two internal charge pumps Do1 Do2

Applications

1.1GHz-band mobile communication equipment such as cellular telephones



Structure

Bipolar silicon monolithic IC

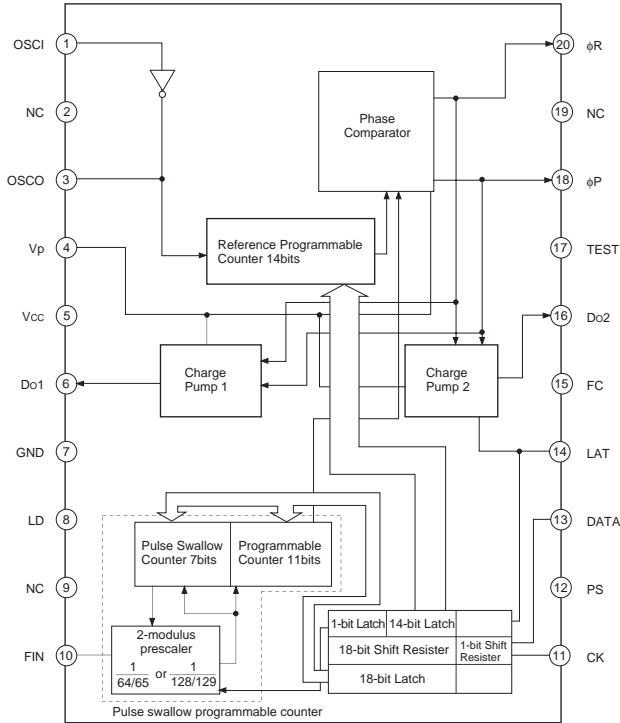
Absolute Maximum Ratings

| | | | |
|-------------------------------|------------------|-------------|----|
| • Supply voltage | V _{cc} | 7 | V |
| • Operating temperature | T _{opr} | -35 to +85 | °C |
| • Storage temperature | T _{stg} | -65 to +150 | °C |
| • Allowable power dissipation | P _D | 300 | mW |

Operating Condition

| | | | |
|----------------|-----------------|------------|---|
| Supply voltage | V _{cc} | 2.7 to 5.5 | V |
|----------------|-----------------|------------|---|

Block Diagram and Pin Configuration



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Pin Description

| Pin No. | Symbol | Typical pin voltage (DC) | Equivalent circuit | Description |
|---------|-----------------|--------------------------|--------------------|---|
| 1 | OSCI | 2.2V | | Reference frequency signal input. |
| 10 | FIN | | | VCO signal input. |
| 2 | NC | — | — | No connected. |
| 9 | | | | |
| 19 | | | | |
| 3 | OSCO | High: 2.2V Low: 2.0V | | Reference frequency signal output. Oscillator is formed by connecting the crystal resonator between this pin and the OSCI pin; the oscillator signal is used as the reference frequency signal. |
| 4 | V _P | 3V | — | Power supply for the charge pump outputs (Do1, Do2) and phase comparator outputs (φR, φP). |
| 5 | V _{CC} | 3V | — | Power supply. |
| 6 | Do1 | — | | Charge pump 1 output. |
| 16 | Do2 | | | Charge pump 2 output. Outputs only when the LAT pin is High; in high impedance when the LAT pin is Low. |
| 7 | GND | — | — | Ground. |
| 8 | LD | High: 2.2V Low: 0.1V | | Lock detection signal output. |
| 18 | φP | | | Phase comparator output. Used for the external charge pump. |
| 20 | φR | | | |
| 11 | CK | Open Low | | Clock input. |
| 13 | DATA | | | Data input. |
| 14 | LAT | | | Latch input. |

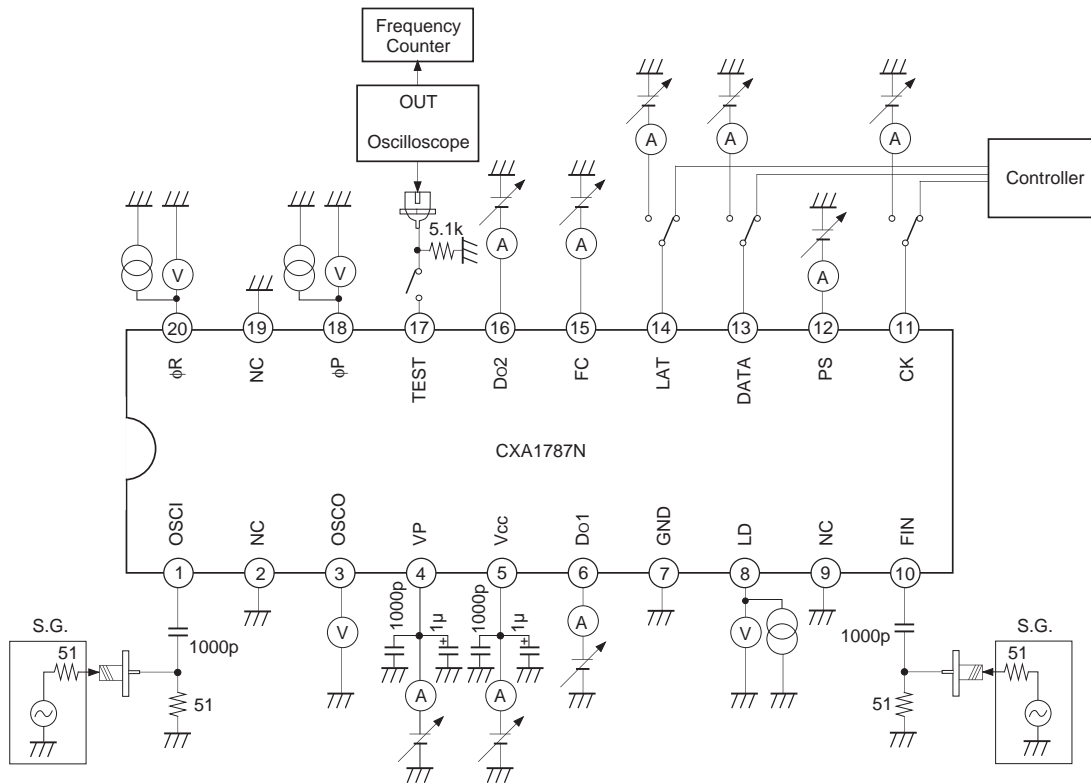
| Pin No. | Symbol | Typical pin voltage (DC) | Equivalent circuit | Description |
|---------|--------|--------------------------|--------------------|---|
| 12 | PS | Open High | | Power saving pin. Power saving mode when this pin is Low. |
| 15 | FC | | | Switching for the phases of phase comparator output and the output signals of counter (reference, programmable) output to the TEST pin. |
| 17 | TEST | High: 2.2V Low: 2.0V | | The signal output which is frequency-divided at the counter. |

Electrical Characteristics ($V_{CC} = V_P = 3V$, $T_a = 25^\circ C$, refer to the Electrical Characteristics Measurement Circuit)

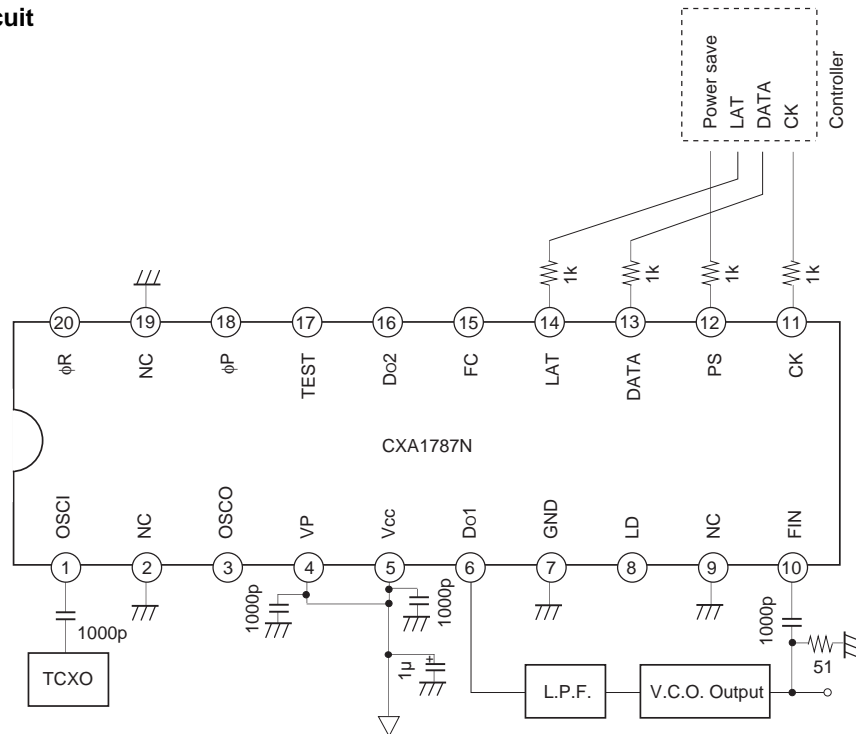
| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|-------------------------|--|-------------------------------------|-----------------------|-----------------------|-----------------|
| Current consumption | I _{CC} | | | 8.11 | 12.5 | mA |
| Current consumption (in power saving mode) | I _{CC} (PS) | | | 300 | 500 | μA |
| FIN operating frequency | f _{in} | V _{CC} = V _P = 2.7V to 5.5V T _a = -35°C to +85°C | 150 | | 1800 | MHz |
| FIN input level | P _{in} | V _{CC} = V _P = 2.7V to 5.5V T _a = -35°C to +85°C | -10 | | 6 | dBm |
| OSCI operating frequency | f _{osc} | V _{CC} = V _P = 2.7V to 5.5V T _a = -35°C to +85°C | 5 | | 20 | MHz |
| OSCI input level | V _{osc} | V _{CC} = V _P = 2.7V to 5.5V T _a = -35°C to +85°C | 0.5 | | 2 | V _{pp} |
| Do1 High output current Do2 | I _{OH} | | | | -1 | mA |
| Do1 Low output current Do2 | I _{OL} | | 1 | | | mA |
| Do1 High impedance Do2 leak current (leak current Do2 off) | I _{oz} | | -1 | | 1 | μA |
| φ _R φ _P LD High output voltage | V _{OH} | I _L = 0.1mA | 2 | 2.1 | | V |
| φ _R φ _P LD Low output voltage | V _{OL} | I _L = 0.1mA | | 80 | 500 | mV |
| CK DATA LAT PS | High input voltage | V _{IH} | | V _{CC} × 0.7 | | V |
| | High input current | I _{OH} | V _{IN} = V _{CC} | -1 | 1 | μA |
| | Low input voltage | V _{IL} | | | V _{CC} × 0.3 | V |
| | Low input current | I _{IL} | V _{IN} = GND except for PS | -1 | 1 | μA |
| PS | Low input current | I _{IL} | V _{IN} = GND | -30 | -15.5 | μA |

| | Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------|--------------------|----------|--|---------------------|------|---------------------|---------|
| FC | High input voltage | V_{IH} | | $V_{CC} - 0.05$ | | | V |
| | High input current | I_{IH} | $V_{IN} = V_{CC}$ | -1 | | 1 | μA |
| | Low input voltage | V_{IL} | | | | 0.05 | V |
| | Low input current | I_{IL} | $V_{IN} = GND$ | -50 | -20 | 1 | μA |
| CK DATA LAT PS | High input voltage | V_{IH} | $V_{CC} = V_P = 5.5V$ | $V_{CC} \times 0.7$ | | | V |
| | High input current | I_{IH} | $V_{CC} = V_P = 5.5V,$ $V_{IN} = V_{CC}$ | -1 | | 1 | μA |
| | Low input voltage | V_{IL} | $V_{CC} = V_P = 5.5V$ | | | $V_{CC} \times 0.3$ | V |
| | Low input current | I_{IL} | $V_{CC} = V_P = 5.5V,$ $V_{IN} = GND$ except for PS | -20 | 0 | 1 | μA |
| PS | Low input current | I_{IL} | $V_{CC} = V_P = 5.5V,$ $V_{IN} = GND$ | -60 | -30 | | μA |
| FC | High input voltage | V_{IH} | $V_{CC} = V_P = 5.5V$ | $V_{CC} - 0.05$ | | | V |
| | High input current | I_{IH} | $V_{CC} = V_P = 5.5V,$ $V_{IN} = V_{CC}$ | -1 | | 1 | μA |
| | Low input voltage | V_{IL} | $V_{CC} = V_P = 5.5V$ | | | 0.05 | V |
| | Low input current | I_{IL} | $V_{CC} = V_P = 5.5V,$ $V_{IN} = GND$ | -60 | -35 | 1 | μA |

Electrical Characteristics Measurement Circuit



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Data Setting Method

The data is set using three signals — CK, DATA, and LAT in this IC. In that case, the serial data as described below is input.

(1) Data input method

The 15 bits of data should be input to the reference counter latch and the 18 bits of data to the pulse swallow programmable counter latch to set the all initializing state in this IC. Every one bit of data is retrieved into the shift register at the rising edge of clock input to the CK pin when the data is input to the DATA pin. The input data is retrieved into the reference counter latch or the pulse swallow programmable counter latch according to the state of the final bit C.

The data is latched when the latch pulse is input to the LAT pin after 16 bits of data or 19 bits of data, which were added with the bit C, are sent to the shift register.

For actual use, first input the 16 bits (including the frequency division setting bit SW for 2-modulus prescaler) of reference counter data from the controller as indicated above. In this time, set the final bit C High.

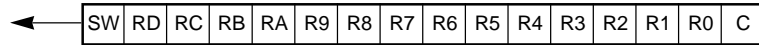
Next, input the 19 bits of pulse swallow programmable counter data in the same way. In this time, set the final bit C Low. Then, all of the interior state has been set. Hereafter, when only the programmable counter data is to be changed, only the latter 19 bits of programmable counter data should be changed. (In this case, set the bit C Low.)

(2) Control data construction

The control data consists of 16 bits for the reference counter and 19 bits for the pulse swallow programmable counter. The final bit of them is the identification code and the contents of data are discriminated by identifying the code. The frequency division value is composed of the binary values whose head is MSB as described on the next page.

(a) Data structure of reference counter

Input direction



(First, input the SW bit and input the C bit last.)

R0 to RD: Frequency division number of reference counter (Binary value with R0 as LSB)

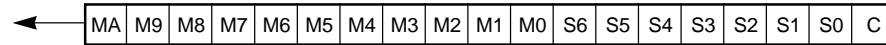
SW: Switching bit of frequency division numbers of 2-modulus pre-scaler block for programmable counter.

| | | |
|---------------------------|--------------------------|----------------------------|
| SW | 1 | 0 |
| Frequency division number | 64/65-frequency division | 128/129-frequency division |

C: This code decides the latch direction of data; set to High.

(b) Data structure of pulse swallow programmable counter

Input direction



(First, input the MA bit and input the C bit last.)

M0 to MA: Frequency division number of main counter (Binary value with M0 as LSB)

S0 to S6: Frequency division number of swallow counter (Binary value with S0 as LSB)

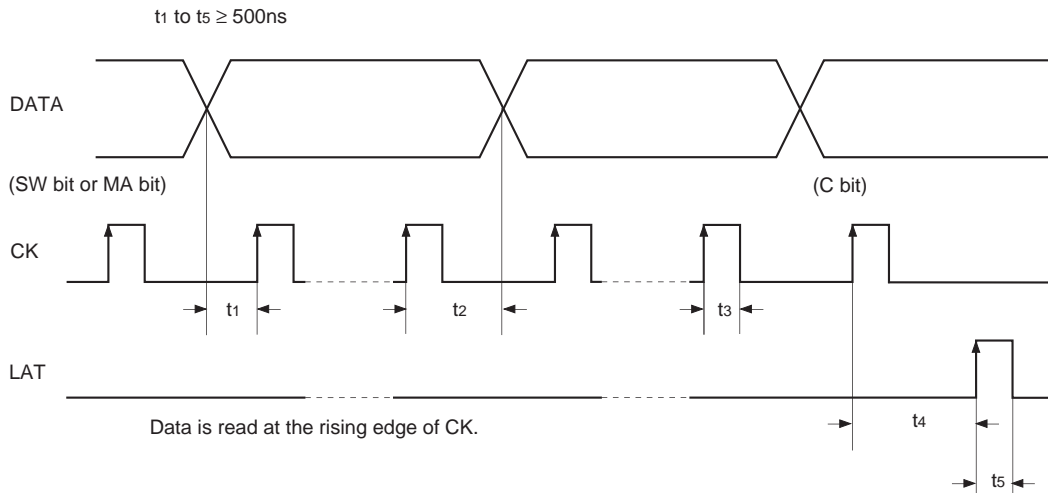
C: This code decides the latch direction of data; set to Low.

The frequency division value of programmable counter can be obtained with the following equation;

$$N \times M + S$$

N: Frequency division value of 2-modulus pre-scaler (64 or 128)
 (M > S) M: Main counter value
 S: Swallow counter value

(1) Data input timing



2. Power Save Pin (PS)

This pin is left High when it is open and in power saving mode at Low.

All circuits except for reference counter latch and pulse swallow programmable counter latch are set to off in the power saving mode. At that mode, Do1 and Do2 are high impedance and the data cannot be set.

* The data of reference counter and programmable counter are hold in power saving mode.

3. Do1 and Do2 Pins

These are the charge pump output pins. Do1 operates always. Do2 operates only when the LAT pin is High ; it is in high impedance state when the LAT pin is Low.

4. FC Pin

This pin switches the charge pump outputs (Do1, Do2) and the phases of phase comparator outputs (ϕP , ϕR). (Refer to the Table 1.)

5. TEST Pin

This pin is for monitoring the counter output signal. The reference counter output and the pulse swallow programmable counter output are switched according to the FC state as shown at Table 1.

This pin is emitter follower output High level = $V_{cc} - V_f$ and Low level = $V_{cc} - V_f - 200\text{mV}$ (200mV amplitude).

The DC bias current is decreased to save the power consumption so that the amplitude may not be monitored for monitoring the waveforms with oscilloscope. In that case, connect the TEST pin to ground with an approximately 5k Ω resistor.

Table 1. Phase comparator and TEST Pin outputs

| | FC: High or open | | | | FC: Low | | | |
|-------------|------------------|----------|----------|-------|---------|----------|----------|-------|
| | Do1 (2) | ϕR | ϕP | TEST | Do1 (2) | ϕR | ϕP | TEST |
| $f_r > f_p$ | H | L | L | f_r | L | H | H | f_p |
| $f_r = f_p$ | Z | L | H | f_r | Z | L | H | f_p |
| $f_r < f_p$ | L | H | H | f_r | H | L | L | f_p |

* Z: High impedance

H: High

L: Low

f_r : Output frequency of reference counter

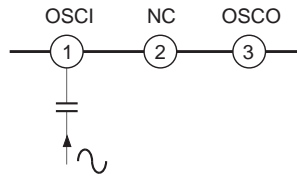
f_p : Output frequency of programmable counter

6. Reference signal (the input signal of reference counter)

The external oscillator signal can be used as the reference signal by inputting the signal of the external oscillator to the OSCI pin, and the reference signal can be also generated by connecting the crystal resonator to the OSCI and OSCO pins.

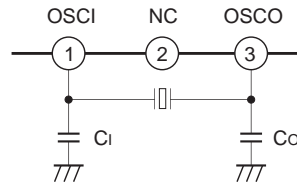
(1) Generation of the reference signal by the external oscillator

Input the signal to the OSCI pin via a capacitor as shown below when the external oscillator signal is use as the reference signal.



(2) Generation of the reference signal by the built-in oscillator

Connect the crystal resonator between OSCI and OSCO pins as shown below. Use the crystal resonator of several MHz and confirm the stability of the oscillation and others. The capacitance ratio of C_i and C_o should be 1 to 2:1, and their values should be selected so that the serial capacitance of C_i and C_o may be the load capacitance specified by the crystal vibrator.

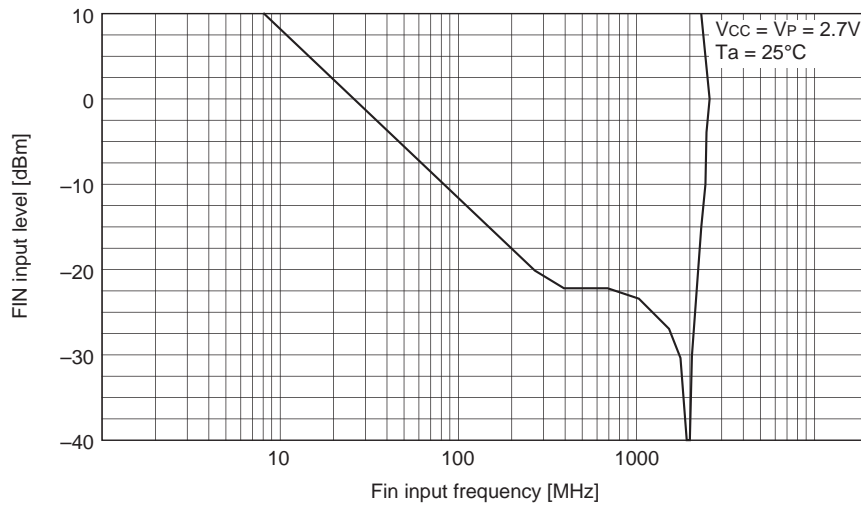


Notes on Operation

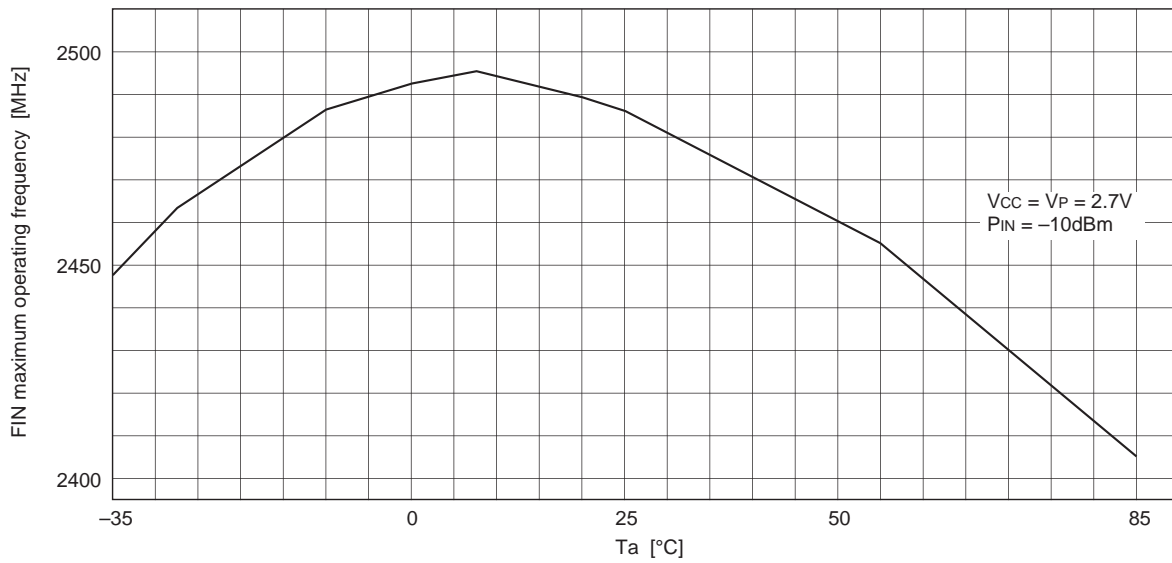
- This is ESD sensitive device due to handling the higher frequency signal of 2GHz; therefore prevent electrostatic damage more than 400V in the EIAJ system.
- Make the input route of the RF signal from the VCO as short as possible.
- Connect the V_{cc} and V_p pins to the ground respectively via the by-pass capacitors as short as possible because the frequency of signal used in this IC is higher.

Example of Representative Characteristics

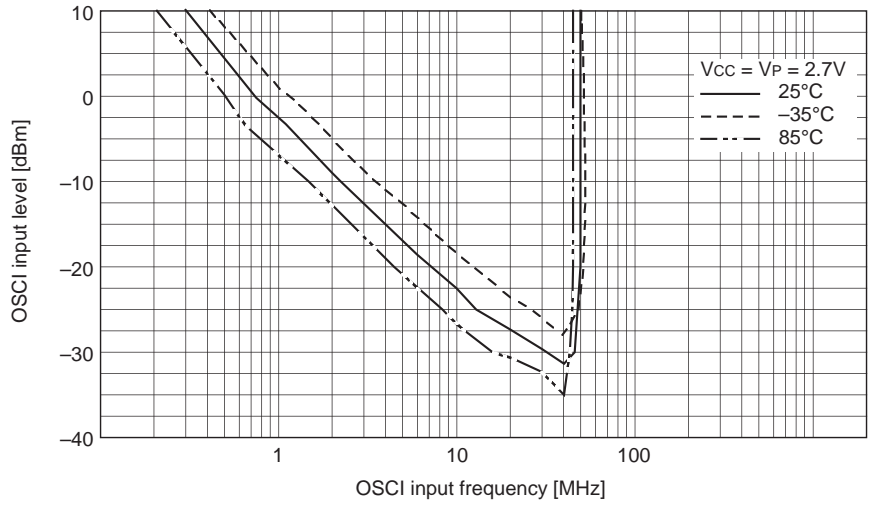
FIN input level vs. Fin input frequency



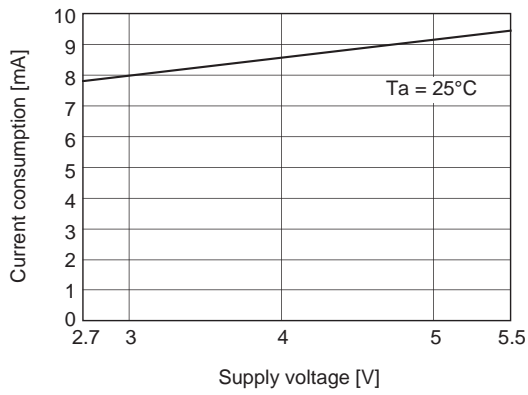
FIN maximum operating frequency vs. Ta



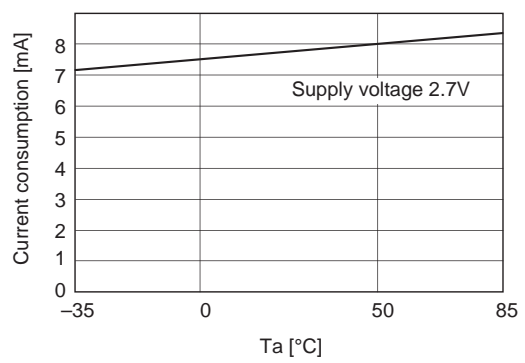
OSCI input level vs. input frequency



Current consumption vs. Supply voltage

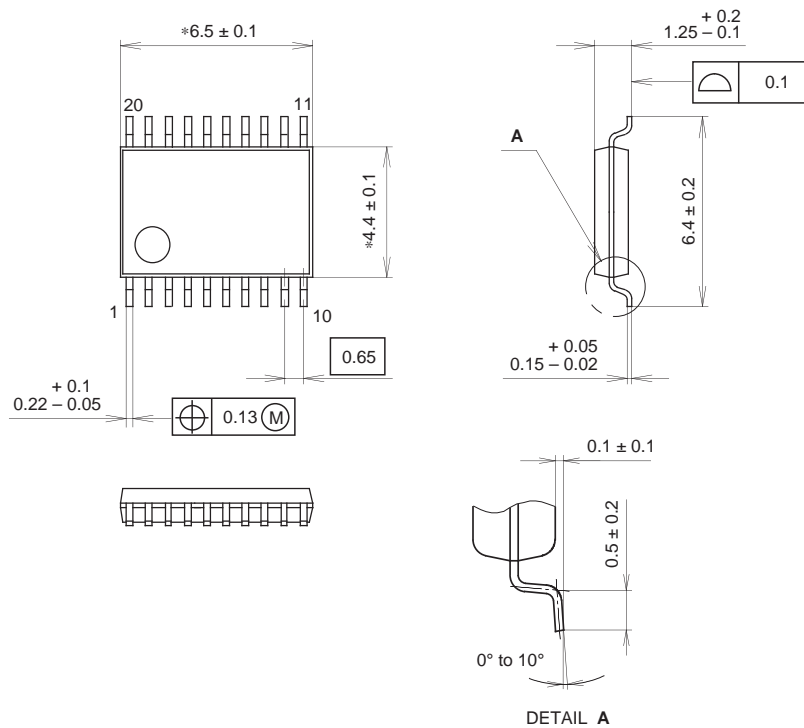


Current consumption vs. Ta



Package Outline Unit: mm

20PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

| | |
|------------|----------------|
| SONY CODE | SSOP-20P-L01 |
| EIAJ CODE | SSOP020-P-0044 |
| JEDEC CODE | _____ |

| | |
|------------------|----------------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER / PALLADIUM PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 0.1g |

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).