SONY

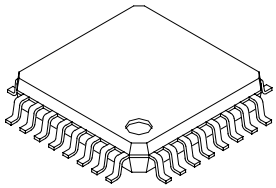
CXA1690Q

Head Amplifier for Digital CCD Cameras

Description

The CXA1690Q is a bipolar IC developed as a head amplifier for digital CCD cameras. The CXA1690Q provides the following functions: correlated double sampling, AGC for CCD signals, GCA for chroma signals, GCA for line signals, sample and hold for A/D converters, blanking, and reference voltage output/output driver for A/D converters.

32 pin QFP (Plastic)



Structure

Bipolar silicon monolithic IC

Applications

Digital CCD cameras

Features

- Permits higher sensitivity with a high-gain AGC amplifier
- Blanking function for the purpose of calibrating the deviation in black levels of the CCD output signals
- Permits output offset adjustment
- Provides a regulator output pin for the reference voltage for A/D converters
- Built-in GCA that amplifies video signals (chroma and line signals) from an external source
- Built-in sample-and-hold circuits (for both camera signals and video signals) required by external A/D converters

Absolute Maximum Ratings

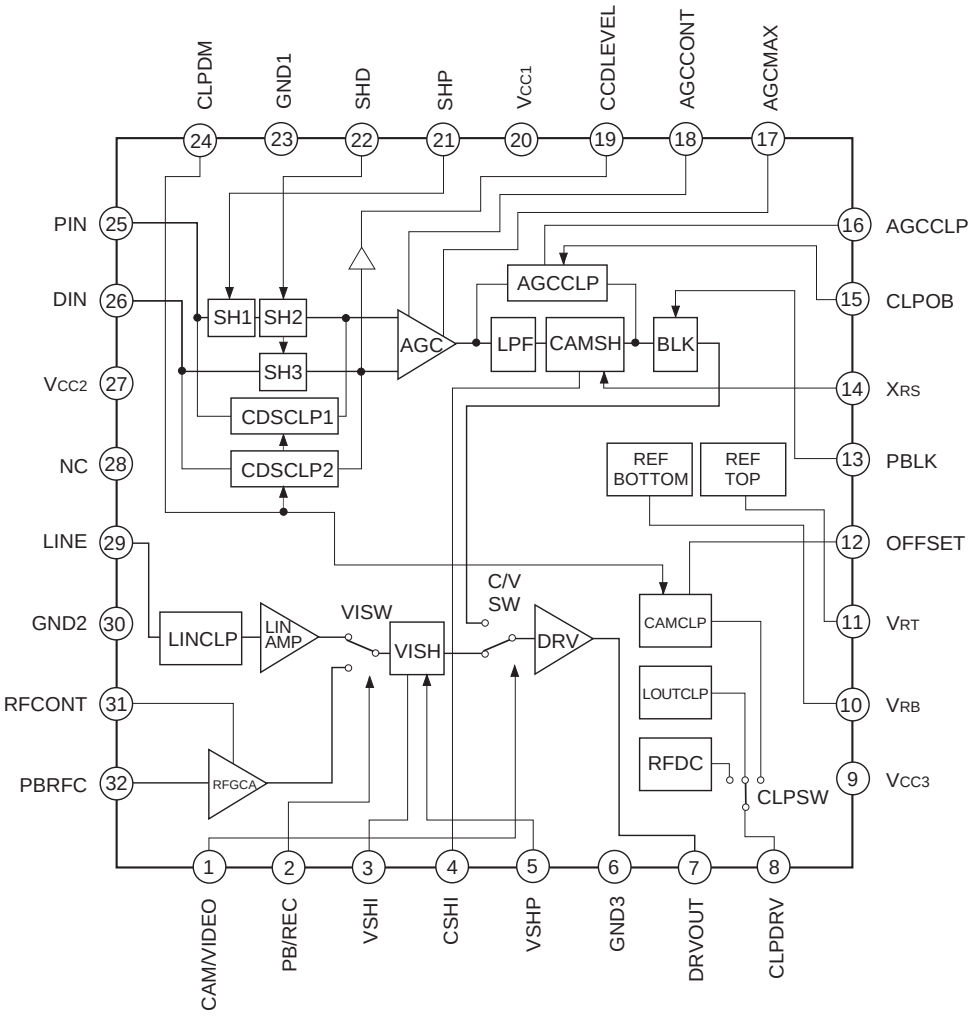
• Supply voltage	V_{CC}	14	V
• Operating temperature	Topr	–20 to +75	℃
• Storage temperature	Tstg	–65 to +150	℃
• Allowable power dissipation	P_D	460	mW

Operating Conditions

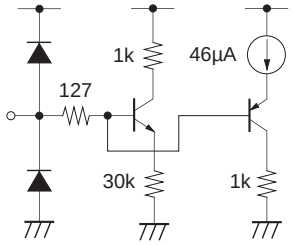
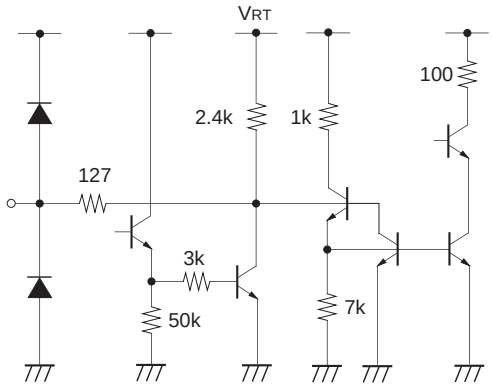
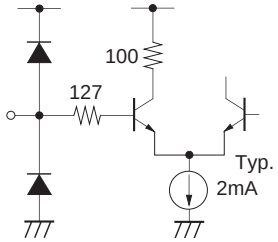
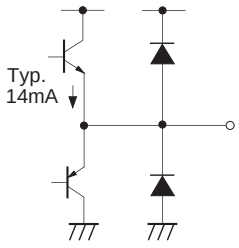
Supply voltage	$V_{CC1, 2, 3}$	4.5 to 5	V

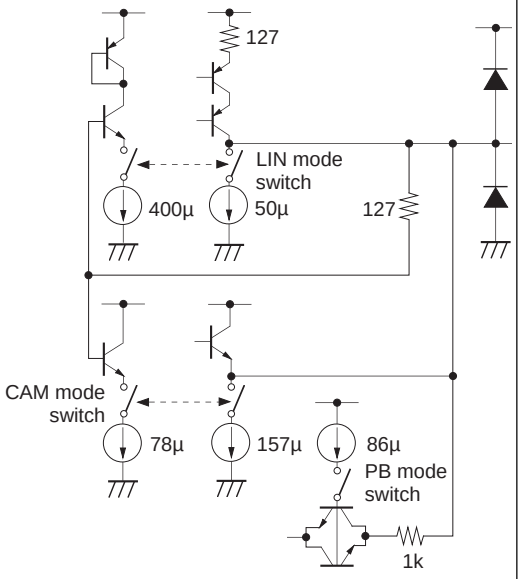
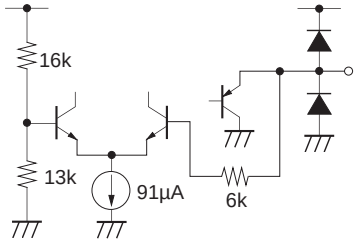
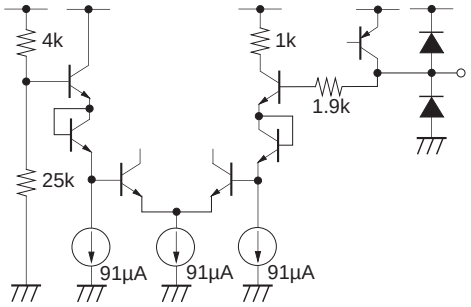
E93X02A8X-PS

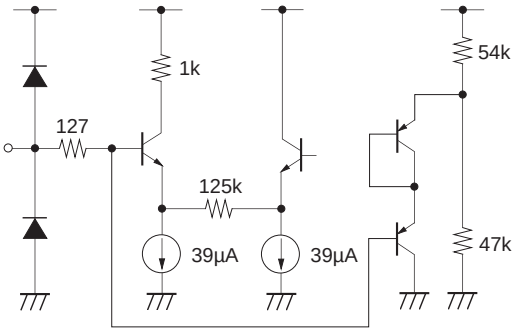
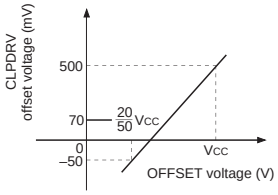
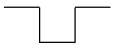
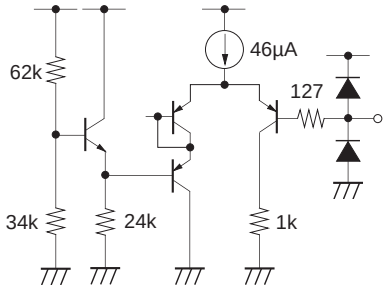
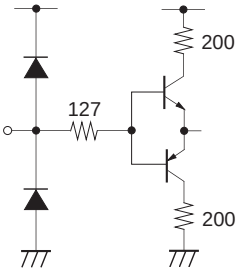
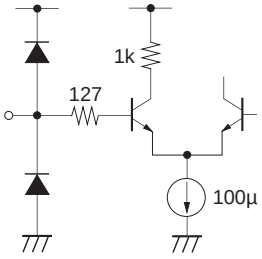
Block Diagram and Pin Configuration

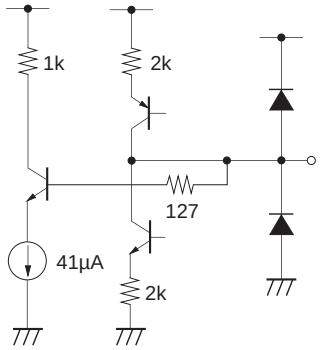
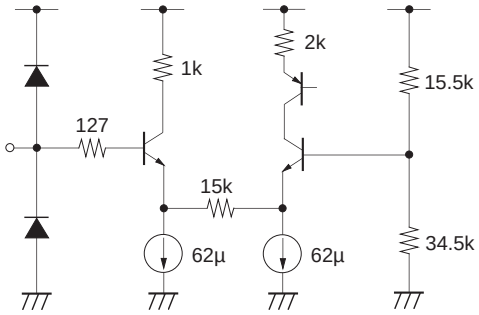
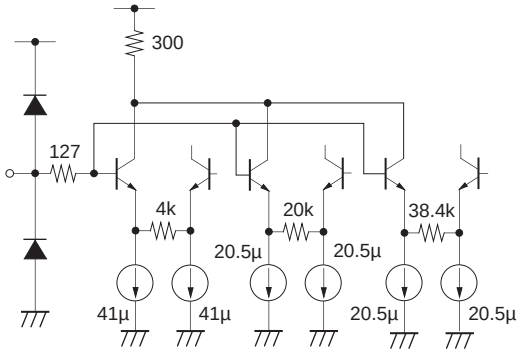
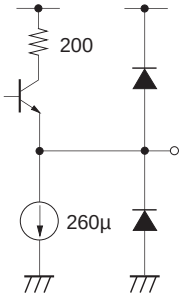


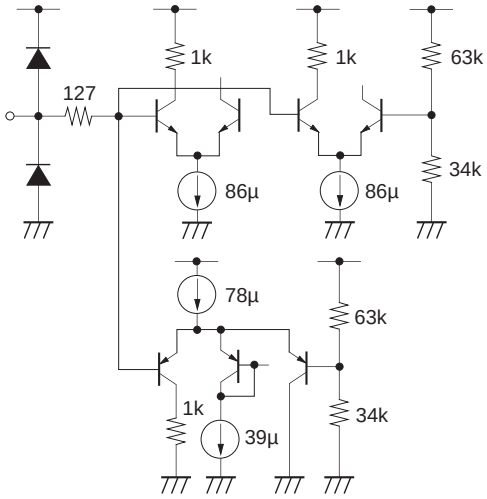
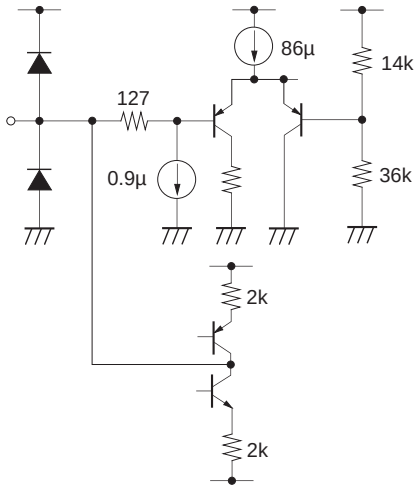
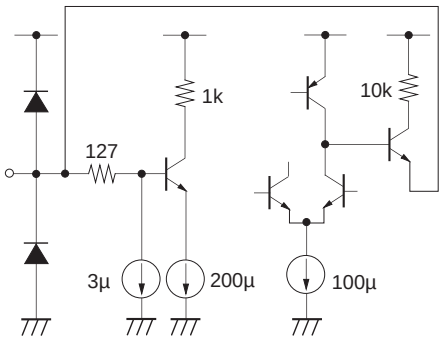
Pin Description (Vcc = 4.5V)

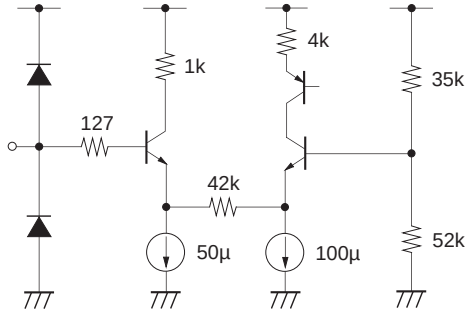
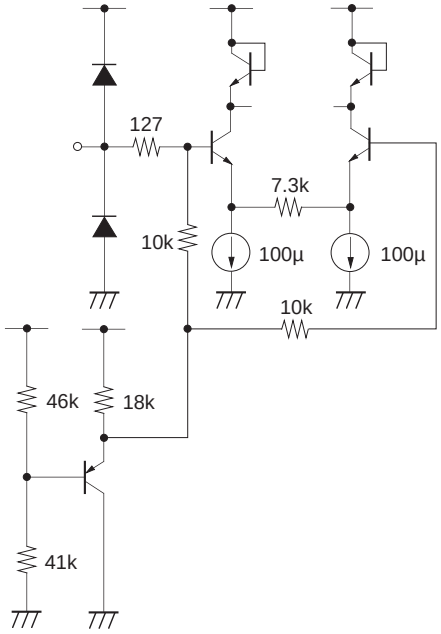
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin voltage</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>1</td><td>CAM VIDEO</td><td rowspan="2">H: Vcc
L: GND
$V_{TH} = \frac{18}{50}$ Vcc</td><td rowspan="2"> 
</td><td rowspan="2">Switches between CAM mode for the camera signal system and PB and LIN modes for the video signal system.
<table>
<tr><th colspan="2"></th><th>CAM VIDEO</th></tr>
<tr><th colspan="2"></th><th>High</th><th>Low</th></tr>
<tr><th rowspan="2">PB REC</th><th>High</th><td>Video system PB mode</td><td>Video system PB mode</td></tr>
<tr><th>Low</th><td>Camera system CAM mode</td><td>Video system LIN mode</td></tr>
</table></td></tr>
<tr><td>2</td><td>PB REC</td></tr>
<tr><td>3</td><td>VSHI</td><td>1.4V</td><td rowspan="2"> 
</td><td>This pin adjusts the slew rate when the video sample-and-hold circuit (VISH) built into the CXA1690 is sampling. Normally used open.
R = 1K: approx. +6dB;
R = 5K: approx. –6dB</td></tr>
<tr><td>4</td><td>CSHI</td><td>1.4V</td><td>This pin adjusts the slew rate when the camera sample-and-hold circuit (CAMSH) built into the CXA1690 is sampling. Normally used open.
R = 1K: approx. +6dB;
R = 5K: approx. –6dB</td></tr>
<tr><td>5</td><td>VSHP</td><td>Sampling
$V_{TH} = \frac{18}{50}$ Vcc</td><td> 
</td><td>Pulse input for VISH.</td></tr>
<tr><td>6
23
30</td><td>GND3
GND1
GND2</td><td>GND</td><td></td><td>Driver GND.
Camera signal GND.
Video signal GND.</td></tr>
<tr><td>7</td><td>DRVOUT</td><td>Camera system CAM mode black level: 1.3V
Video system LIN mode black level: 1.4V
Video system RF mode DC level: 2.2V</td><td> 
</td><td>Driver output.
Standard D range.
Camera system signal: 870mVp-p
Video system PB RFC signal: 500mVp-p
Video system LIN signal: 1.4Vp-p</td></tr>
</table>

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
8	CLPDRV	Camera system CAM mode black level: 2V Video system LIN mode clamp level: 2V Video system PB mode DC level: 3V		Clamps and outputs the DRVOUT (Pin 7) output signal. The switch for each mode is closed and the clamp potentials applied to this pin by selecting CAMVIDEO (Pin 1) or PBRFC (Pin 2).
9 20 27	Vcc3 Vcc1 Vcc2	Vcc		Driver V_{CC}. Camera signal V_{CC}. Video signal V_{CC}.
10	V_{RB}	2.02V		2V regulator output $V_{RB} – V_{RT}$ load: 160Ω or greater. Be sure to decouple this pin near the IC pins to prevent the oscillation and external noise when this pin is not used. (Recommended capacitor value: 4.7µF)
11	V_{RT}	3.88V		4V regulator output. Be sure to decouple this pin near the IC pins to prevent the oscillation and external noise when this pin is not used. (Recommended capacitor value: 4.7µF)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
12	OFFSET	Vcc to $\frac{20}{50}$Vcc		This pin offset adjusts the CLPDRV black level when the CXA1690 satisfies the operating conditions for the camera signal system (when CAMVI is High and PBREC is Low). VCC: approx. 500mV 20/50 VCC: approx. –50mV Preset: approx. 70mV 
13	PBLK	$V_{TH} = \frac{18}{50}$Vcc 		Pulse input for BLK (active: Low). This pin functions only when CAMVI is High and PBREC is Low, and calibrates the black level of the AGC output waveform. When the pulse is low, the DRVOUT potential is forced to 2V.
14	XRS	$V_{TH} = \frac{22}{50}$Vcc		High-speed S/H pulse input for CAMSH (active: Low). High-speed S/H pulse input for SH1 (active: Low). High-speed S/H pulse input for SH2 and SH3 (active: Low).
21	SHP	$V_{TH} = \frac{25}{50}$Vcc 		
22	SHD			
15	CLPOB	$V_{TH} = \frac{18}{50}$Vcc 		Clamp pulse input for AGCCLP (active: Low).

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
16	AGCCLP	Approx. 2.8V		Capacitor connection for AGCCLP clamping. 0.1 to 1µF
17	AGCMAX	Vcc to $\frac{20}{50}$ Vcc		AGC amplifier MAX gain adjustment.
18	AGCCONT	Vcc to $\frac{20}{50}$ Vcc		AGC amplifier gain adjustment. MIN GAIN for $\frac{20}{50}$ Vcc, MAX GAIN for Vcc for both AGCMAX and AGCCONT.
19	CCD LEVEL	DIN input CCD signal black level: approx. 2.6V		CCD level detector

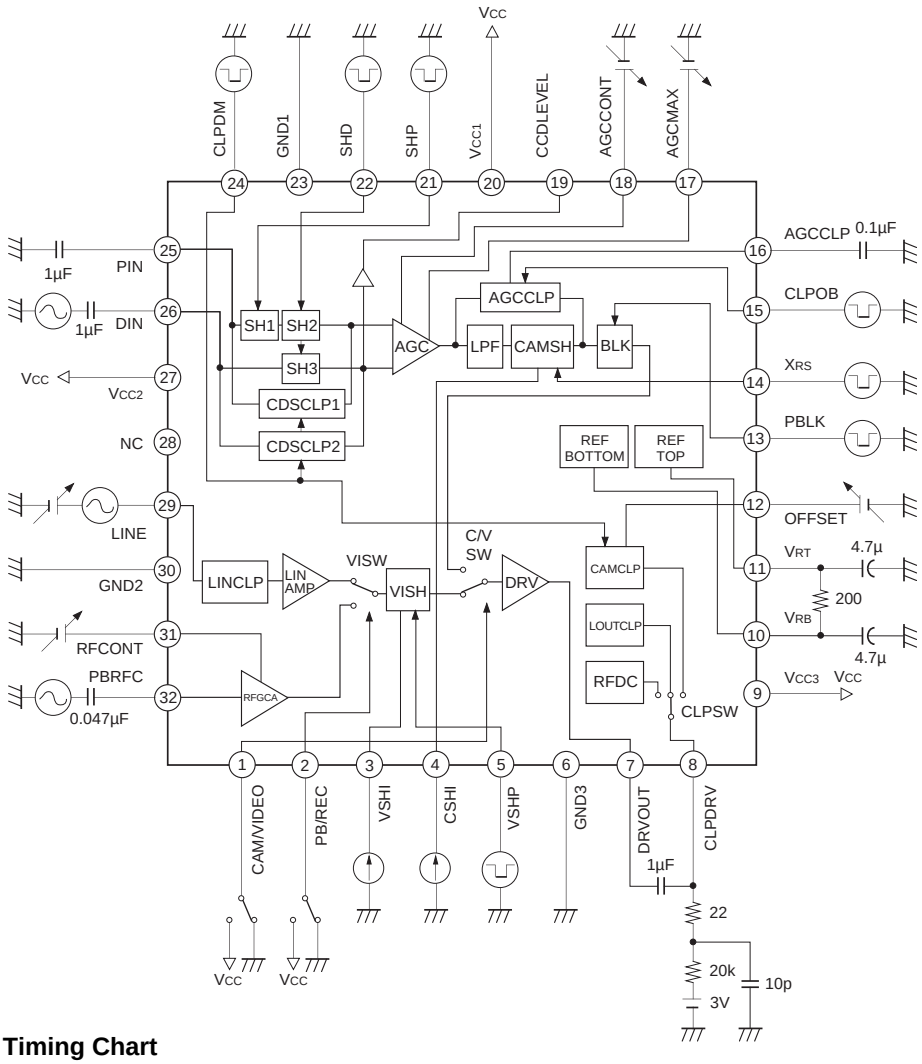
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	CLPDM	$V_{TH} = \frac{18}{50}Vcc$ 		Clamp pulse input (active: Low).
25	PIN DIN	Black level: approx. 2.6V		CCD signal input.
29	LINE	Clamp potential: approx. 2.5V		LIN signal input.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
31	RFCONT	Vcc to $\frac{20}{50}$ Vcc		RFGCA gain control.
32	PBRFC	approx. 2.8V		PBRFC signal input.

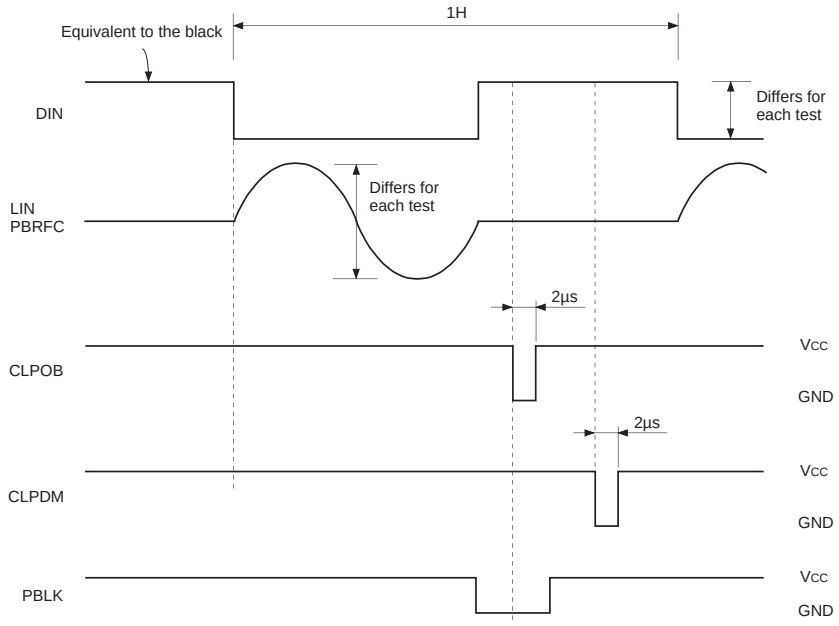
Electrical Characteristics (Ta = 25°C, $V_{CC1, 2, 3}$ = 4.5V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consump-tion	Camera mode	I_{DC}	CAM/VIDEO = 4.5V, PB/RFC = 0V	—	49	62	mA
	LINE mode	I_{DL}	CAM/VIDEO = 0V, PB/RFC = 4.5V	—	33	42	
	RF mode	I_{DR}	CAM/VIDEO = 4.5V, PB/RFC = 4.5V	—	33	42	
AGC	AGCCONT max.	A CONmax.	AGCMAX = 4.5V, AGCCONT = 4.5V	40	43	—	dB
	AGCCONT min.	A CONmin.	AGCMAX = 4.5V, AGCCONT = 1.8V	—	7.8	10	
	AGCMAX min.	A MAXmin.	AGCMAX = 1.8V, AGCCONT = 4.5V	—	19	21	
	Amount of variation in gain	AGC G	A CONmax.–A CONmin.	32	35	—	
	Dynamic range max.	AGCmax. D	AGCMAX = 4.5V, AGCCONT = 4.5V Level at which the CLPOUT output signal is saturated	1.9	2.05	—	V
	Dynamic range min.	AGCmin. D	AGCMAX = 4.5V, AGCCONT = 1.8V Level at which the CLPOUT output signal is saturated	1.9	2.05	—	
CAMCLP	Offset High	CAOF high	OFFSET = 4.5V	440	490	—	mV
	Offset Low	CAOF low	OFFSET = 1.8V	—	–65	–30	
	Offset Preset	CAOF pre	OFFSET = 0V	13	43	73	
REF	VRT DC level	VRTO	With 200Ω load	3.66	3.86	4.06	V
	VRB DC level	VRBO	With 200Ω load	1.88	2.03	2.18	
	VRT – VRB	ΔVR	With 200Ω load	1.73	1.83	1.93	
BLK	Offset	BLKOF	BLKOF (BLK = 4.5V) – BLKOF (BLK = 0V)	–5	7	15	mV
LINGCA	Gain	LIN G	Adjust the DC level so that LIN input = 15kHz, 500mVp-p sine wave LINCLP.	8.5	9.5	10.5	dB
RFGCA	RF CONT max.	RF CONmax.	RFCONT = 4.5V, 15kHz, 80mVp-p sine wave	14	17	—	
	RF CONT min.	RF CONmin.	RFCONT = 1.8V, 15kHz, 400mVp-p sine wave	—	0.5	2	

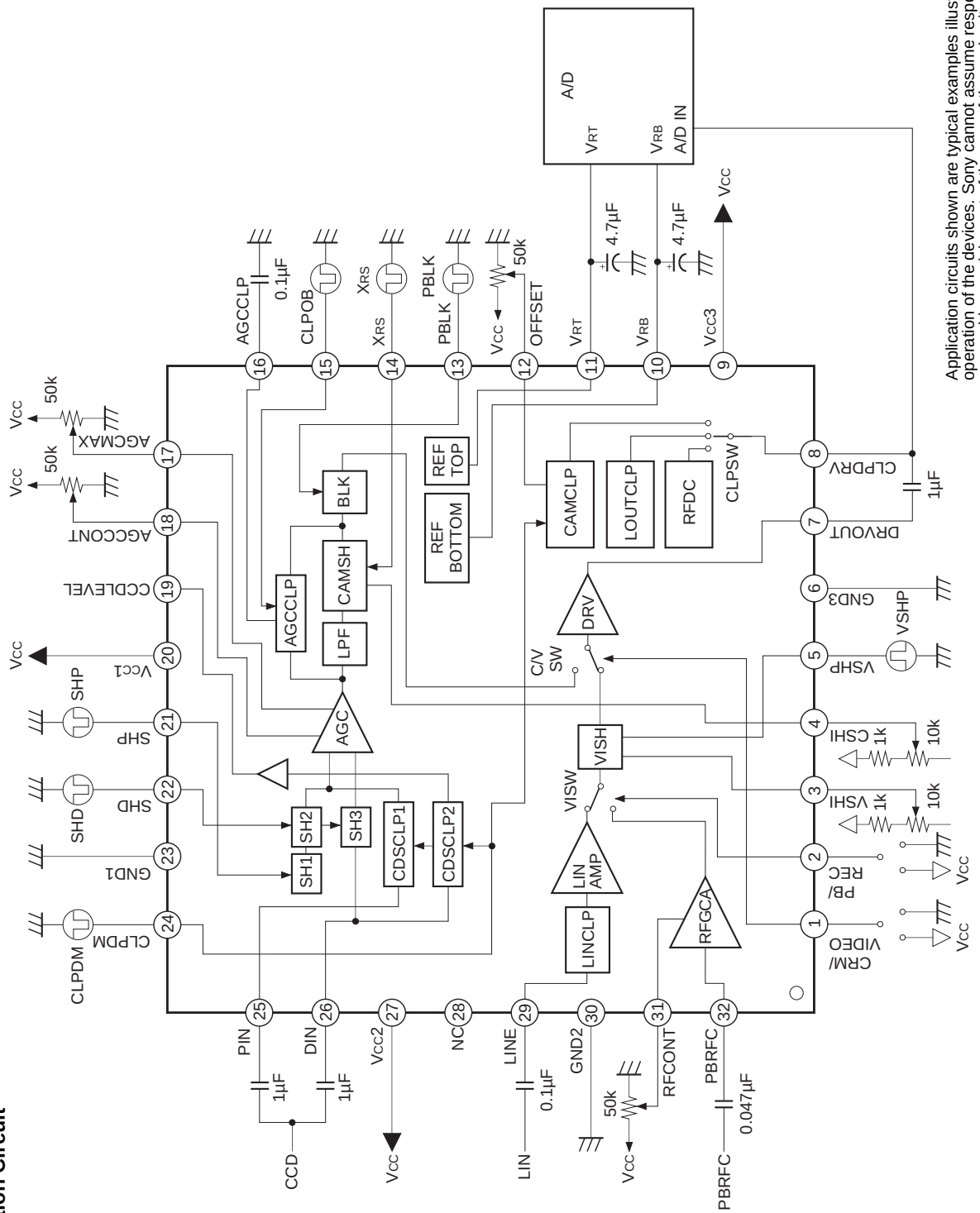
Electrical Characteristics Measurement Circuit



Measurement Timing Chart



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Camera signal processing system

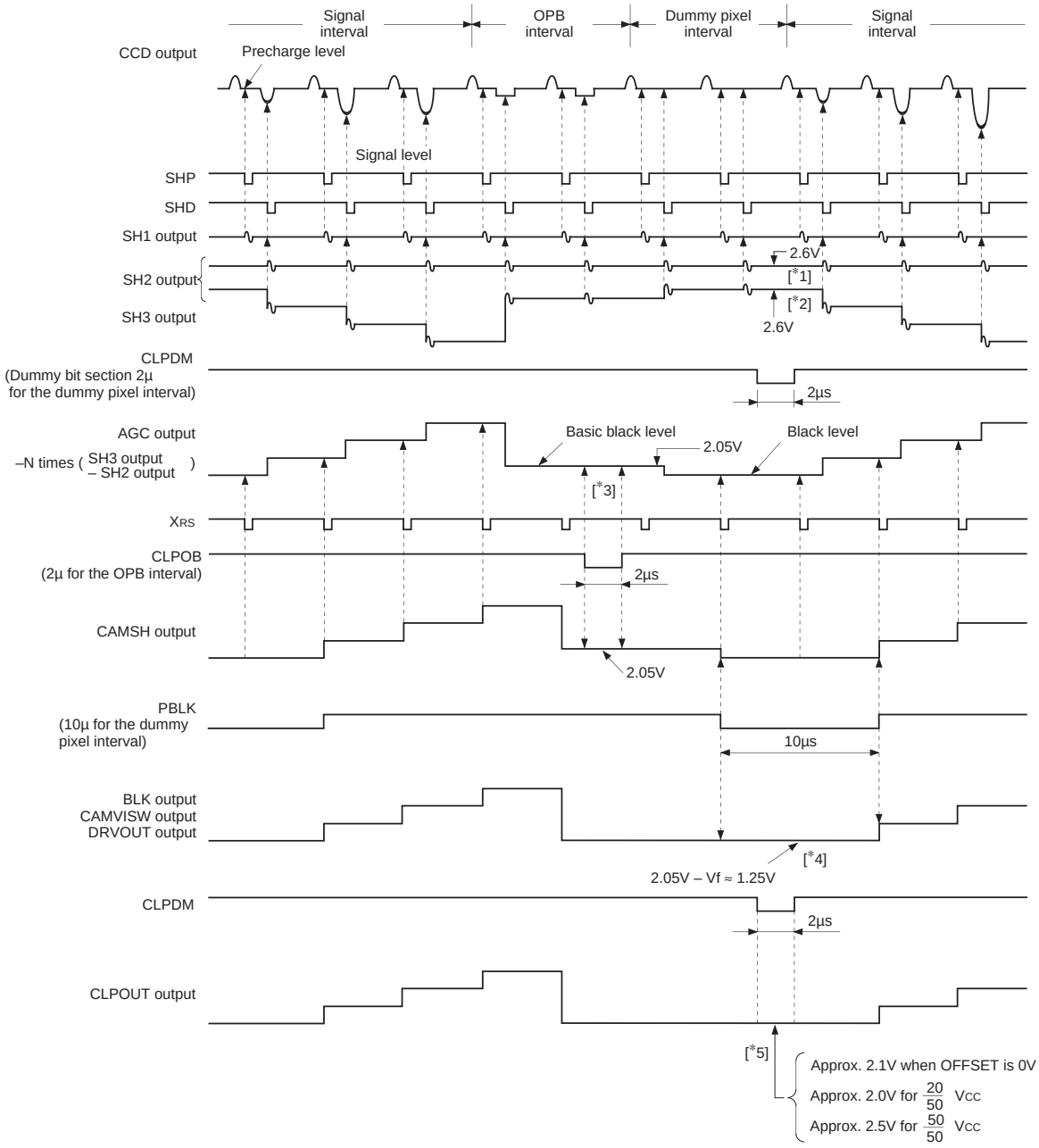
Process the video signal processing pins as follows only in camera mode.

<5> VSHP ... Connect to GND.
<29> LINE ... Connect to GND via the capacitor (approx. 0.01µF).
<31> RFCONT ... Connect to GND.
<32> PBRFC ... Connect to GND via the capacitor (approx. 0.01µF).

Operating conditions

The camera signal processing system operates when CAM/VIDEO is High, and PB/REC is Low.

Camera Signal Processing System Timing Chart



CDS:
The CCD signal from the CCD image sensor enters PIN and DIN where it is correlated double sampled (CDS: Correlated Double Sampling) by SH1, SH2 and SH3. The precharge level of the CCD output signal is sampled-and-held and output by the SH2 output, and the signal level is sampled-and-held and output by the SH3 output.

CDSCLP:
The CDSCLP stabilizes the DC level of the input signal, clamps (CLPDM) the input signal during the dummy pixel interval for the purpose of eliminating the AGC input offset, and combines the DC level ([*1], [*2]) of SH2 and SH3.

AGC:
The gain can be varied with the AGCMAX and AGCCONT voltage control (20/50) V_{CC} to V_{CC}. The maximum gain can be varied from 19 to 43dB for AGCMAX, and from 7.9 to 43dB for AGCCONT.

LPF:
A primary low-pass filter has been installed for the purpose of eliminating unused bands and white noise and improving S/N.

CAMSH:
The CAMSH is used for camera system signal processing. It is a sample-and-hold circuit which synchronizes the data read-in timing for the external A/D. The slew rate of the input signal for the sample-and-hold circuit can be controlled by adjusting the input current to the CSHI pin.

AGCCLP:
The basic black level is set ([*3]) by clamping it with the CLPOB clock during the OPB interval of the AGC output waveform. The capacitance for AGCCLP is connected to the AGCCLP pin.

BLK:
The black level is calibrated by blanking the black level signal of the AGC output waveform so that it does not fall below the basic black level and replacing the DC potential. ([*4])
The signal is blanked when PBLK is low.

C/VSW:
When the CAM/VIDEO and PB/REC pin voltages are set so that the camera signal processing system operates, C/VSW leads the BLK output (camera signal) into the DRV. In addition, when these voltages are set so that the video signal processing system operates, C/VSW leads the VISH output (video signal) into the DRV.

CLPSW:
By selecting the CAM/VIDEO and PB/REC pin voltages, either [CAMCLP] is connected and lead into the CLPDRV pin as the clamp for the output signal of the camera signal processing system, or [LOUTCLP] as the clamp for the LIN mode output signal or [RFDC] as the DC shift for the PBREC mode output signal of the video signal processing system.

DRV:
DRV drives the external A/D. RF mode or LIN mode signals for either the camera or video signals are input to the DRV and output from DRVOUT by switching C/VSW.

CAMCLP:
The signal black level interval is clamped by the CLPDM clock to bring camera system signals within the allowable input voltage range for the external A/D, and the signals are output to CLPOUT. ([*5])
In addition, the CAMCLP contains an OFFSET control pin which adjusts the CLP potential for the purpose of compensating the clamp level difference generated by the DRV.

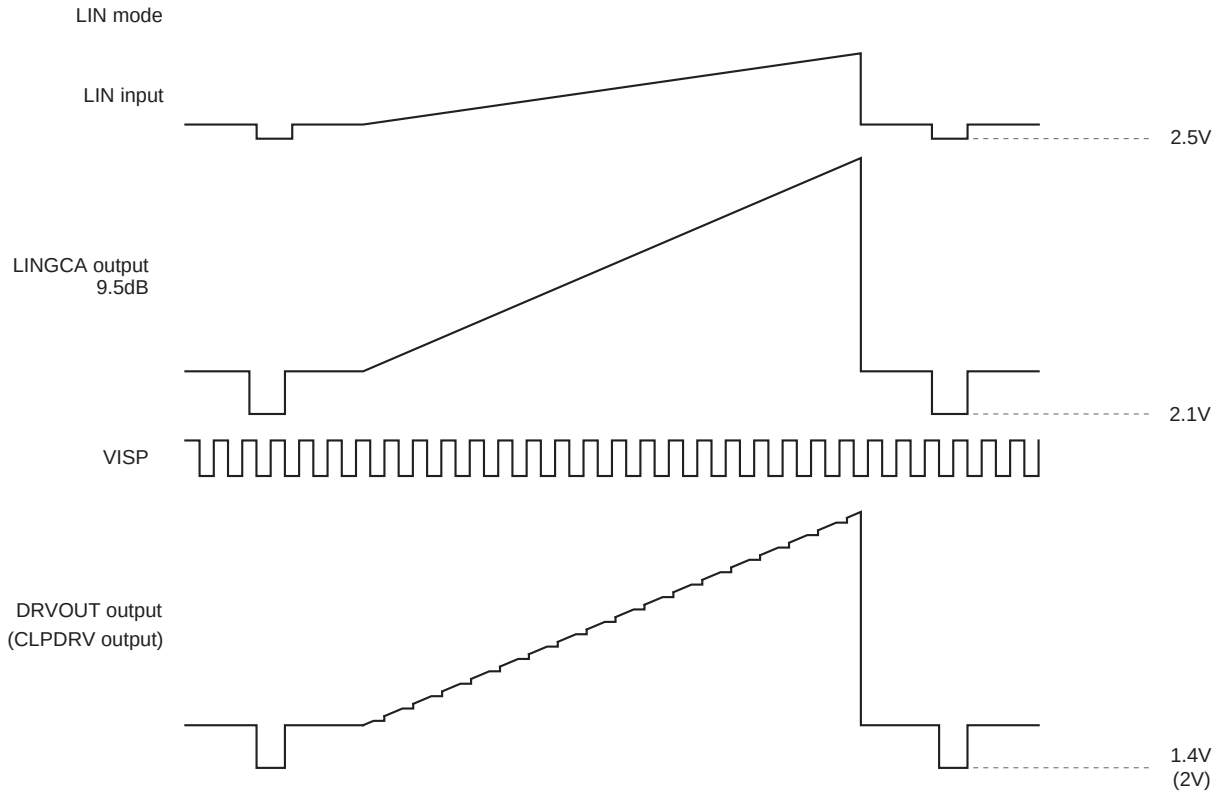
REFBOTTOM, REFTOP:
REFBOTTOM and REFTOP are reference voltage source for the external A/D. They are connected to VRB and VRT, and supply 2V and 4V to the A/D.

2. Video signal processing system

Operating conditions

The video signal processing system has two modes: LIN signal mode and PBREC signal mode.
The video signal processing system operates in LIN signal mode when CAM/VIDEO is Low, and PB/REC is High.
The video signal processing system operates in PBREC signal mode when PB/REC is High.

Video Signal Processing System Timing Chart



LIN signal mode

LINCLP:
The video signal enters the LIN pin. LINCLP sync tip clamps the input signal to allow full input.
The input signal level and frequency are respectively 500mVp-p (typ.) and DC up to approx. 7MHz.

LINAMP:
This is a 9.5dB gain amplifier.

VISW:
VISW switches between the LIN signal and PBRFC signal for the video signal processing system.
The signals are switched according to the input conditions of the CAM/VIDEO and PB/REC pins.

VISH:
The VISH is used for video signal processing system. It is a sample-and-hold circuit which synchronizes the data read-in timing for the external A/D. The slew rate of the input signal for the sample-and-hold circuit can be controlled by adjusting the input current to VSHI.

LOUTCLP:
LOUTCLP is a clamp circuit which operates when the LIN signal is output by the DRV. The clamp potential is 2V.

PBREC signal mode

RFGCA:

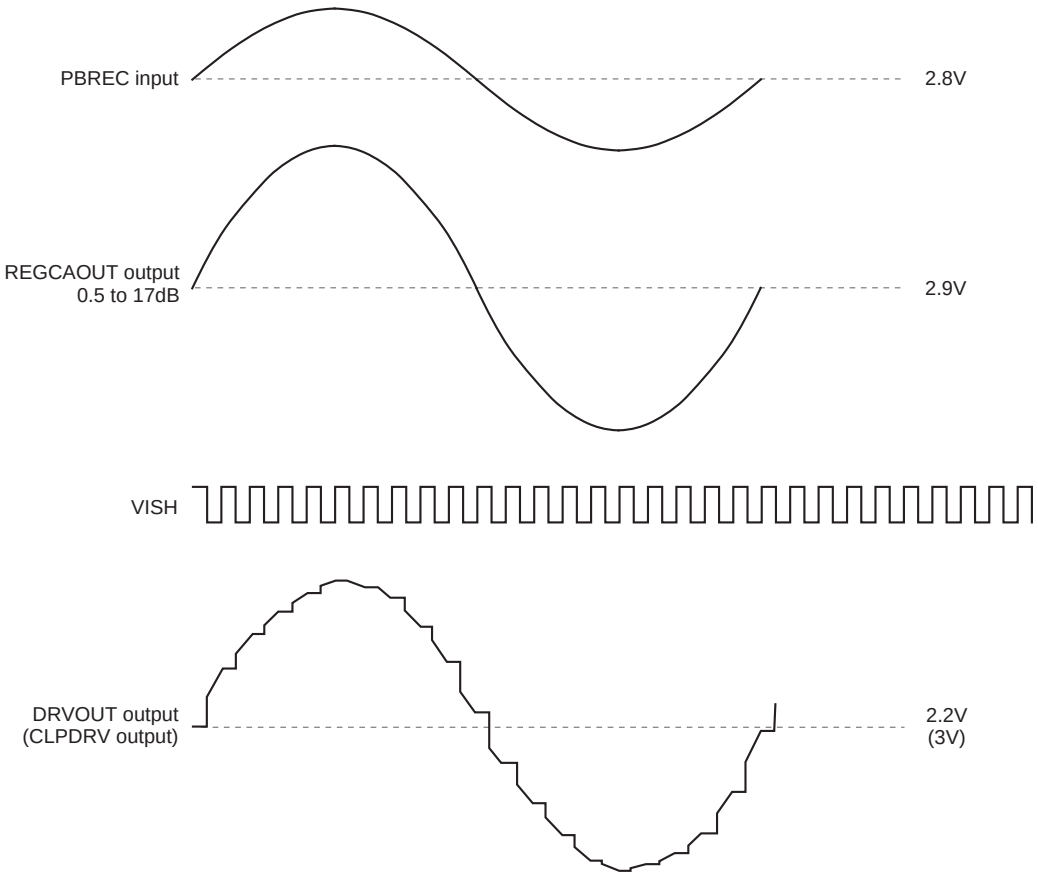
This is an amplifier which controls the gain of the video chroma RF signal input to PBRFC. The RFCONT voltage can be varied from (20/50) V_{CC} to V_{CC}, enabling the gain to be varied from 0.5 to 17dB.

The input signal level and frequency are respectively 200mVp-p (typ.) and DC up to approx. 1.5MHz.

RFDC:

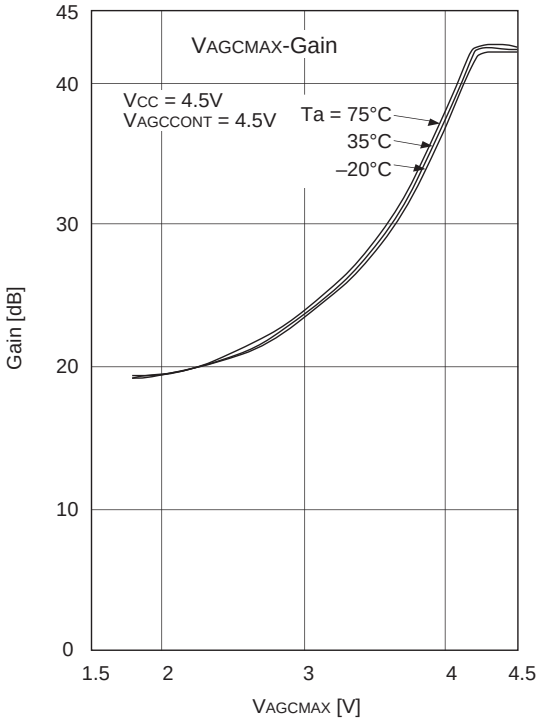
RFDC is a DC bias circuit which operates when the PBREC signal is output by the DRV. The DC bias potential is 3V.

PBREC mode

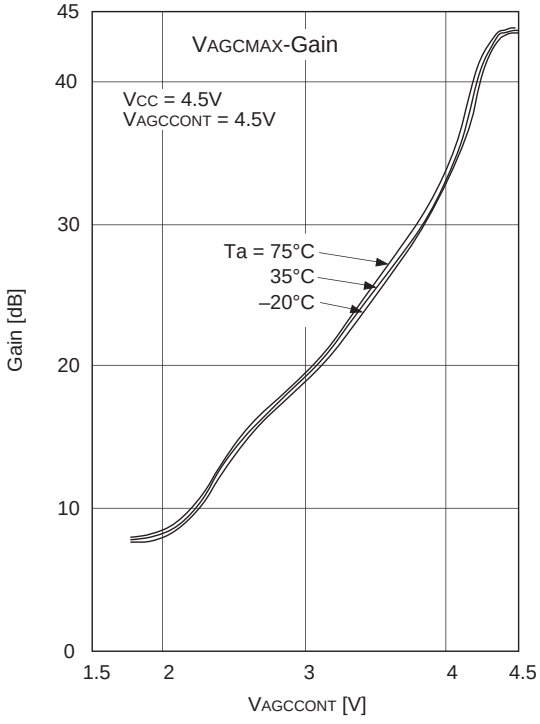


Example of Representative Characteristics

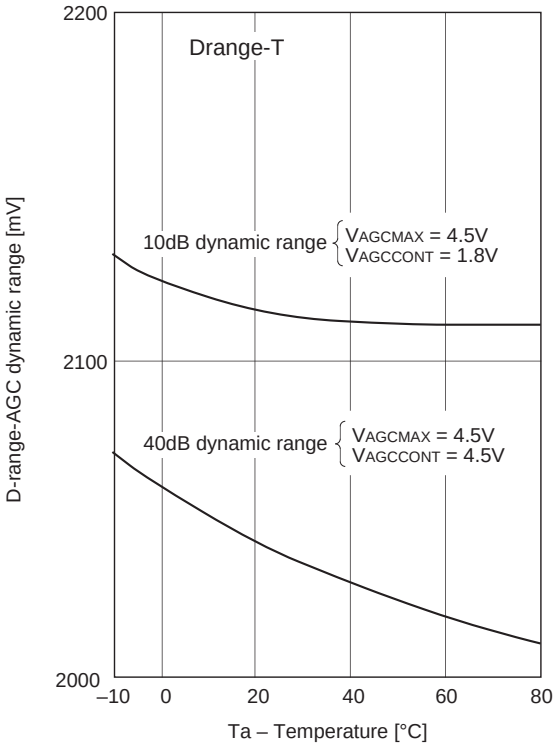
AGCMAX control temperature characteristics



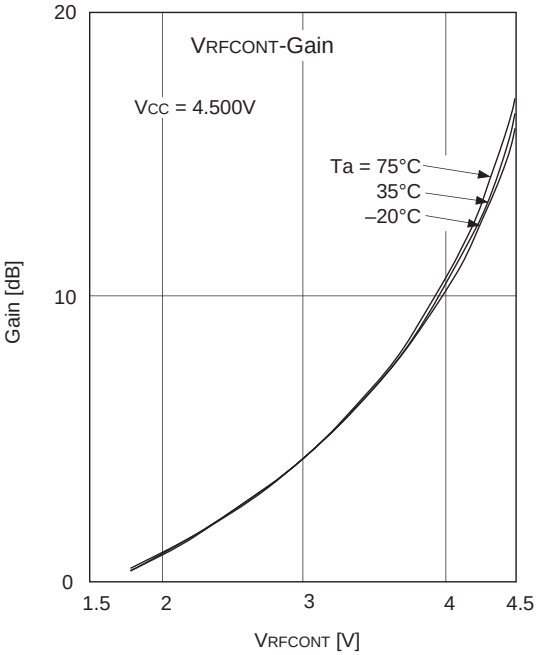
AGCCONT control temperature characteristics



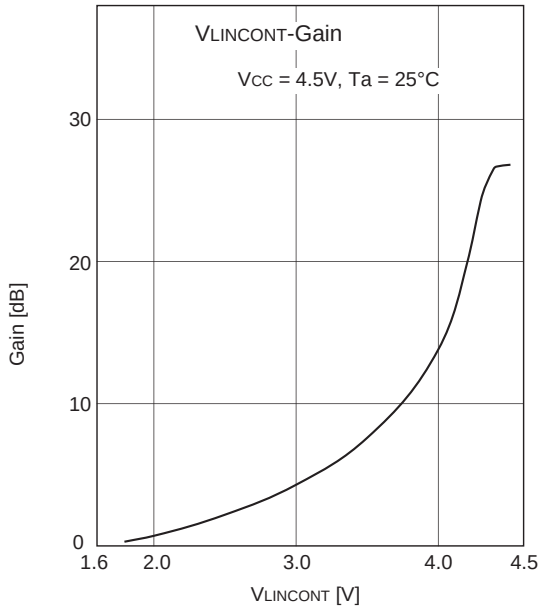
AGC dynamic range temperature characteristics



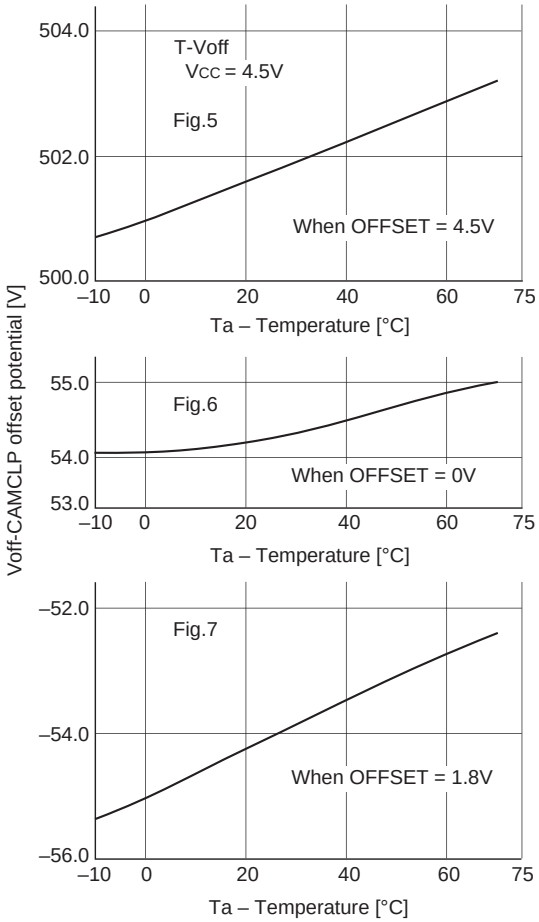
RFGCA gain control temperature characteristics



LINGCA gain control

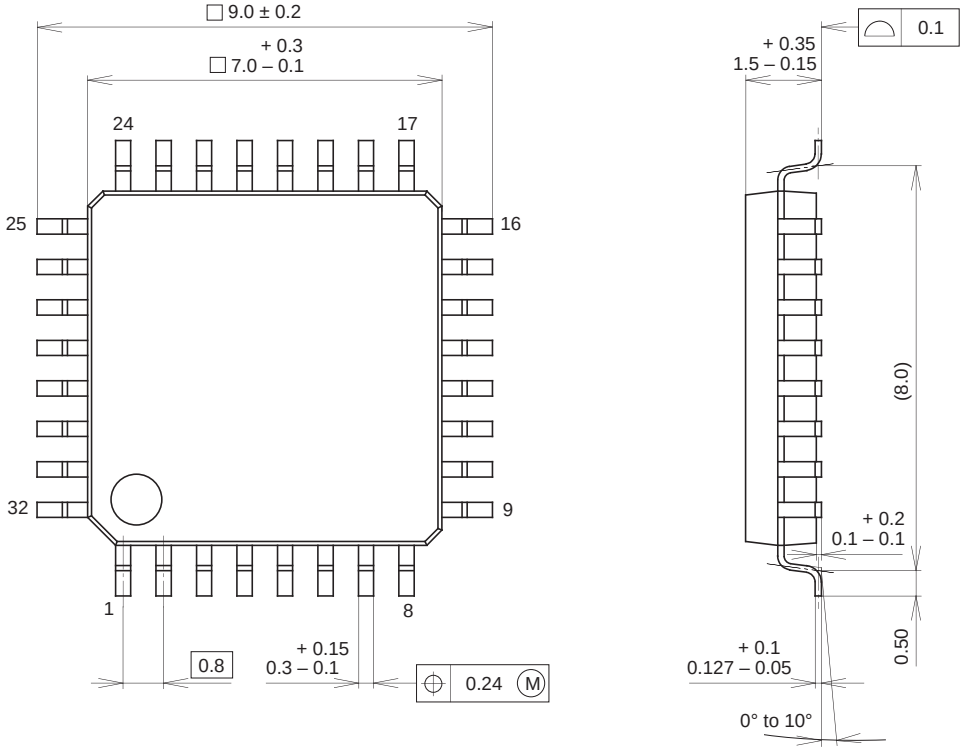


CAMCLP offset temperature characteristics



Package Outline Unit: mm

32PIN QFP (PLASTIC)



SONY CODE	QFP-32P-L01
EIAJ CODE	QFP032-P-0707
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g