SONY

CXA1512M/N

Motor Sensor Amplifier for 8mm Camcorder

For the availability of this product, please contact the sales office.

Description

The CXA1512M/N is developed as a motor sensor amplifier for 8mm videos.

CXA1512M
14pin SOP (Plastic)

CXA1512N
14pin SSOP (Plastic)

Features

- Uses a variable threshold comparator efficient against PG noise.
- FG frequency corresponds to up to 100kHz (High speed FF/REW compatible)
- Low current consumption (2/3 compared to CX20115)

Applications

8mm camcoder / DAT usage and others

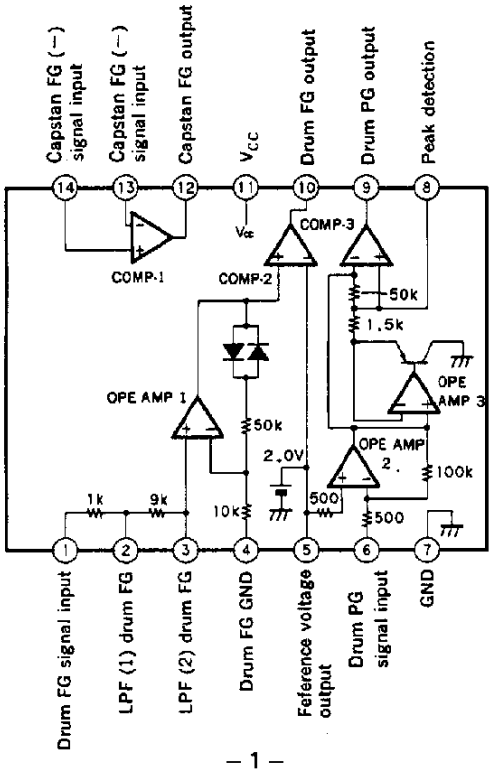
Absolute Maximum Ratings (Ta=75°C)

• Supply voltage	V_{CC}	11	V
• Operating temparature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−40 to +125	°C
• Allowable power dissipation	P_D	360	mW

Operating Range

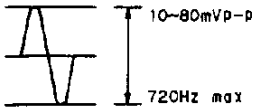
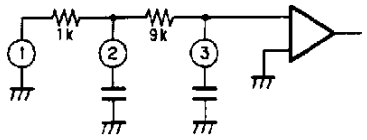
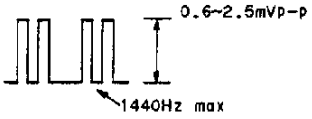
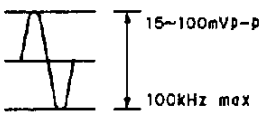
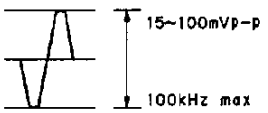
• Supply voltage	V_{CC}	4.0 to 5.5	V

Block Diagram



E90117-HP

Pin Description

Pin No.	Name	Waveform	Function
1	Drum FG signal input		Input pin of drum FG signal (sine wave)
2	Drum FG LPF (1)	—	 Connect capacitor and use.
3	Drum FG LPF (2)	—	
4	Drum FG	D.C.	GND pin of drum FG block Supplied from Pin 5 output
5	Reference voltage output	D.C.	2.0V is output as reference voltage. Use as ground voltage of drum FG and drum PG blocks.
6	Drum PG signal input		Input pin of drum PG signal (Intermittent half-wave sine wave)
7	GND	D.C.	—
8	Peak detection	—	Capacitor connecting pin of the drum PG peak detection amplifier block
9	Drum PG output		Output pin of drum PG block
10	Drum FG output		Output pin of drum FG block
11	V_{CC}	D.C.	—
12	Capstan FG output		Output pin of capstan FG block
13	Capstan FG (−) signal input		Input pin of capstan FG (−) signal (sine wave)
14	Capstan FG (+) signal input		Input pin of capstan FG (+) signal (sine wave)

Electrical Characteristics

DC Items (Ta=25°C, V_{CC}=5.0V)

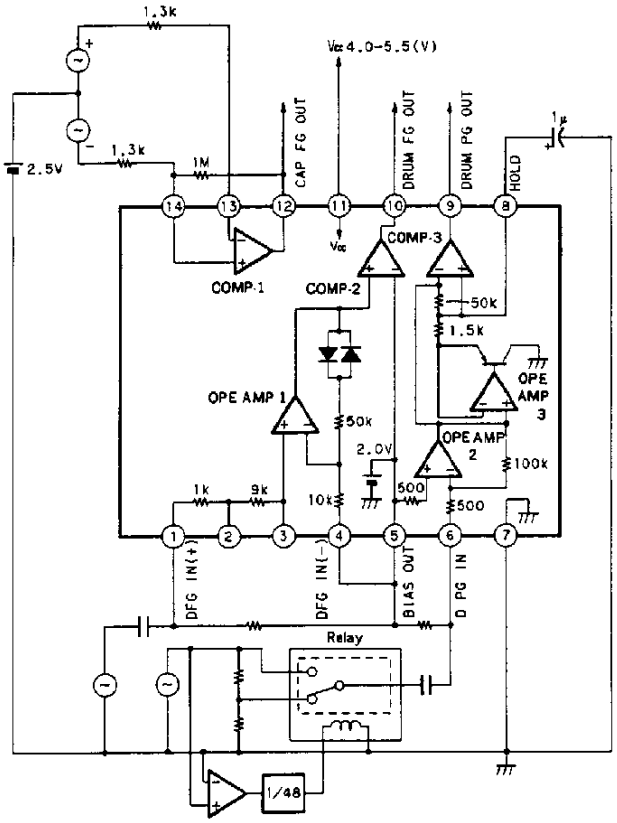
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	V9, V10, V12=0V	2.1	3.2	4.8	mA
(CAP-FG)						
Input bias current	I13, 14	V13, V14=2.5V	—		1.0	μA
Input offset current	[I13-I14]	V13, V14=2.5V	—		100	nA
In-phase input voltage range L		Variation of Pins 13, 14 current when voltage at same pins varies from 2.5V to 1V.	0.5	1.0	2.0	times
In-phase input voltage range H		Variation of Pins 13, 14 current when voltage at same pins varies from 2.5V to 3.5V.	0.5	1.0	2.0	times
Output L level	V12L	V12L=0.5mA V14−V13=−3mV	—		1.0	V
Output H level	V12L	V12L=−50μA V14−V13=+3mV	4.0		—	V

AC Items

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
(CAP-FG)		Vi (DC)=2.5V Vi (AC)=30mVp-p fi=100kHz				
Output L level	V12L		—		1.0	V
Output H level	V12H		4.0		—	V
Duty ratio			−20		+20	%
(DRUM-FG)		Vi (AC)=10Vp-p fi=720Hz				
Output L level	V10L		—		1.0	V
Output H level	V10H		4.0		—	V
Duty ratio			−30		+30	%
(DRUM-PG)						
Output L level	V9L		—		1.0	V
Output H level	V9L		4.0		—	V
Frequency	f9		29	30	31	Hz
(DRUM-FG)						
Input baias current	I1	V1, V4,=2.0V			600	nA
In-phase input voltage range L		Variation of Pin 1 current when voltage changes from 2.5V to 1V	0.5	1.0	2.0	times
In-phase input voltage range H		Variation of Pin 1 current when voltage changes from 2.5V to 3.5V	0.5	1.0	2.0	times
Output L level	V10L	I10=0.5mA V1−V4=−3mV	—		1.0	V
Output H level	V10H	I10=−50μA V1−V4=+3mV	4.0		—	V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
(DRUM-FG)						
Output L level	V9L	V9L=0.5mA V6−V5=−3mV	—		1.0	V
Output H level	V9H	V9L=−50μA V6−V5=+3mV	4.0		—	V
(V.REF)						
Ref voltage	V5		1.8	2.0	2.2	V
Output resistance	R_O	I5L=±1mA	—		2.0	Ω
Ripple elimination ratio	SVRR	V11=5±1V	40		—	dB

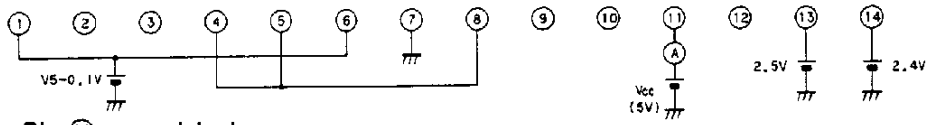
Test Circuit (AC Test)



Test Circuit

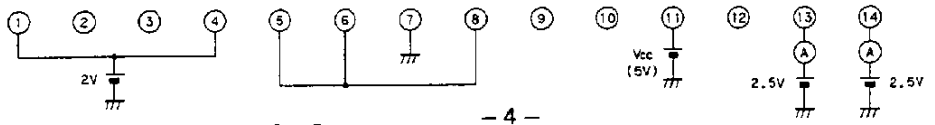
DC Test (A indicates DC current meter and V DC voltage meter)

- Current consumption



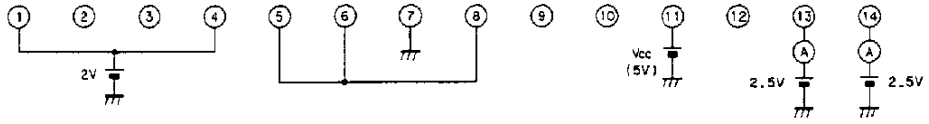
Pin ⑪ current test

- Input bias current



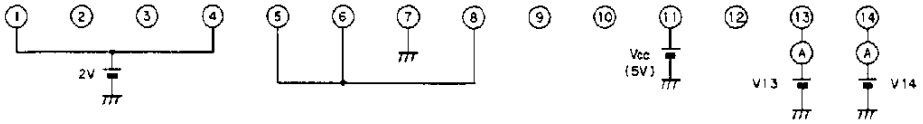
Current test at Pins ⑬, ⑭

● Input offset current



Pin ⑬ current — Pin ⑭ current

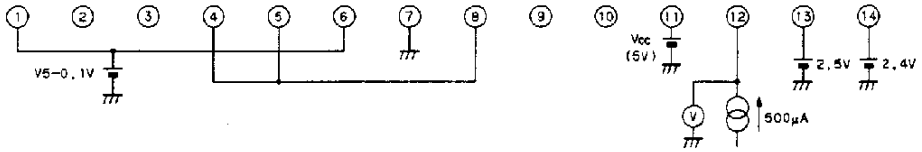
● In-phase input voltage range



Tested current value (1) of Pins 13 and 14 when those pins are at 2.5V
Tested current value (2) of Pins 13 and 14 when those pins are 1V
Tested current value (3) of Pins 13 and 14 when those pins are 3.5V
At L level (2)/(1) times At H level (3)/(1) times

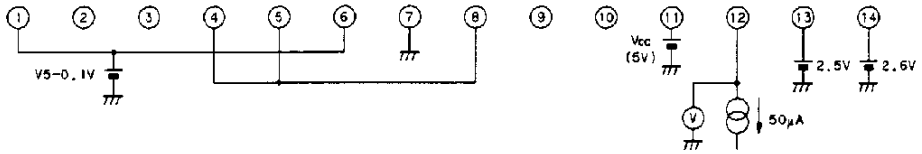
● Output level

L level



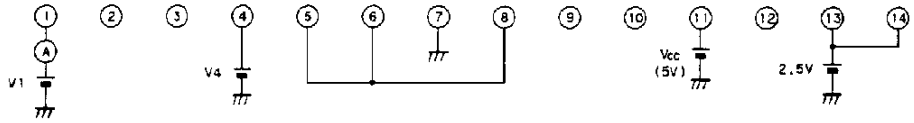
Voltage test of Pin ⑫ when that pin is at a current input mode of 500μA.

H level



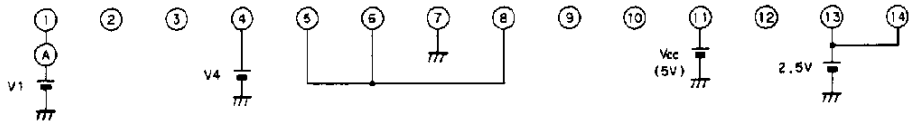
Voltage test of Pin ⑫ when that pin is at a current output mode of 50μA.

● Input bias current



Current test of Pin 1

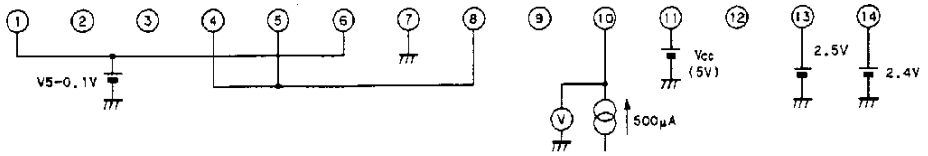
● In-phase input voltage range



Tested current value (1) of Pins ⑬ and ① when Pins ① and ④ are at 2V
Tested current value (2) of Pins ⑬ and ① when Pins ① and ④ are at 1V
Tested current value (3) of Pins ⑬ and ① when Pins ① and ④ are at 3.5V
At L level (2)/(1) times At H level (3)/(1) times

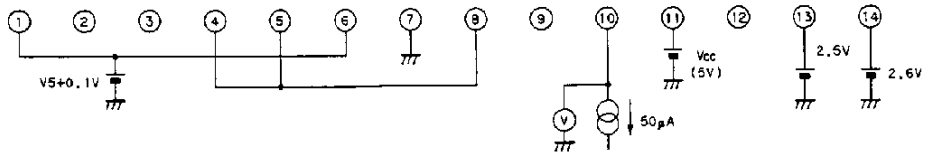
● Output level

L level



Voltage test of Pin ⑩ when that pin is at a current input mode of 500μA.

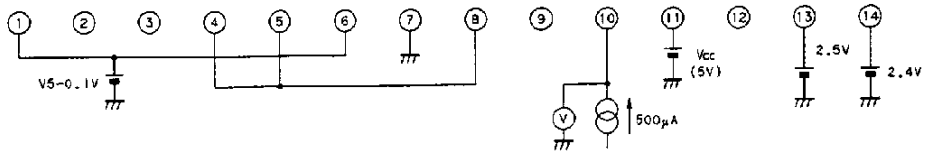
H level



Voltage test of Pin ⑩ when that pin is at a current output mode of 50μA.

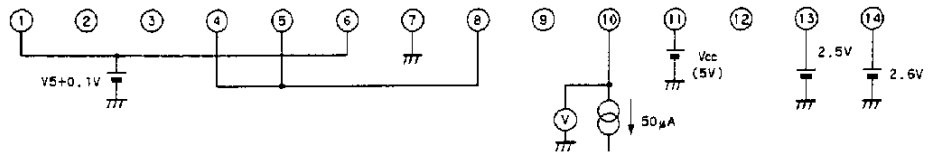
● Output level

L level



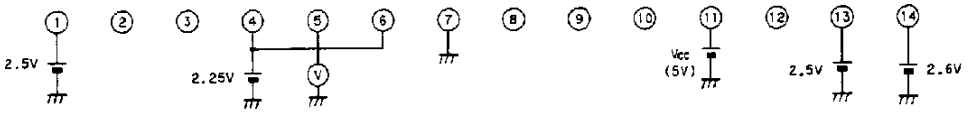
Voltage test of Pin ⑩ when that pin is at a current input mode of 500μA.

H level



Voltage test of Pin ⑩ when that pin is at a current output mode of 50μA.

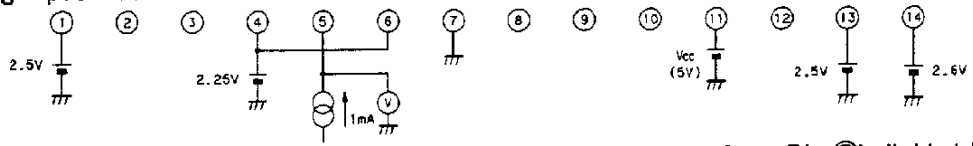
● Ref. voltage, ripple elimination ratio



Pin ⑤ voltage test

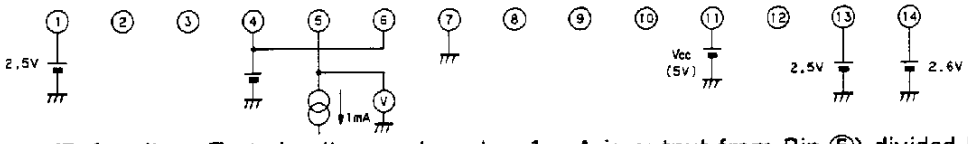
• Output resistance

During input mode



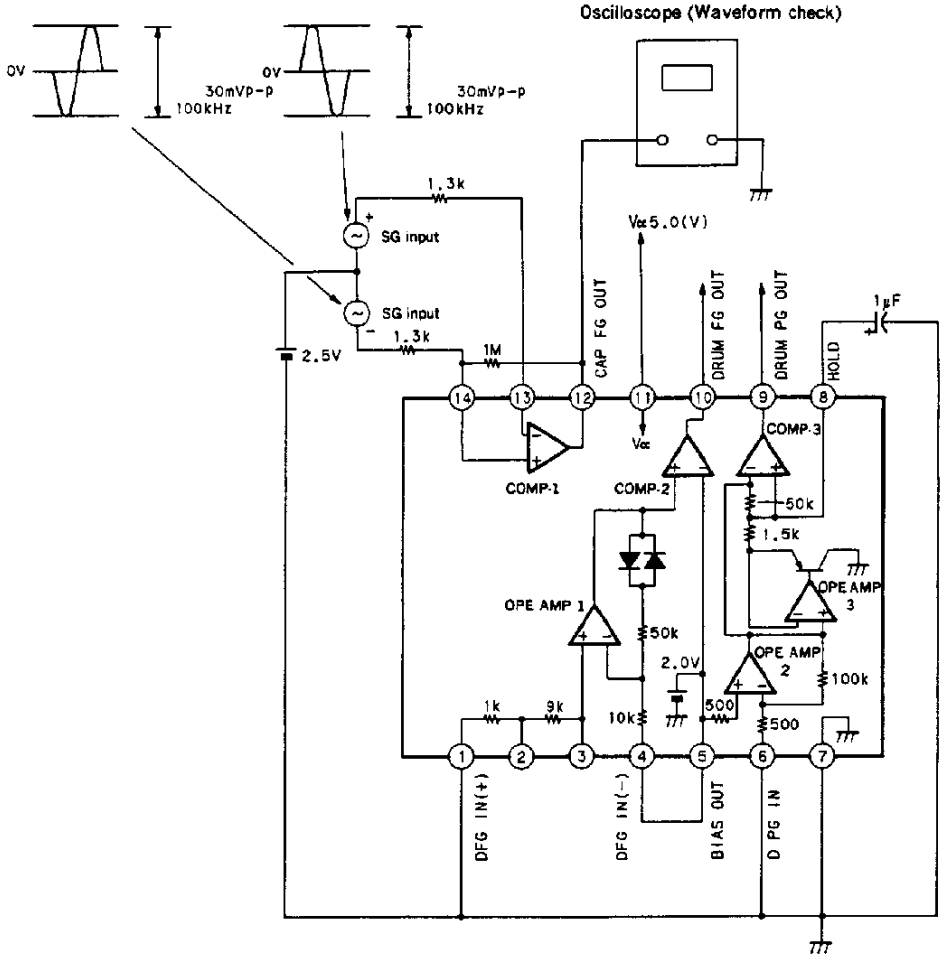
(Ref. voltage-Tested voltage value when 1 mA is output from Pin ⑤) divided by 1mA

During output mode



(Ref. voltage-Tested voltage value when 1 mA is output from Pin ⑤) divided by 1mA

AC Test (CAP FG)



Description of Operation

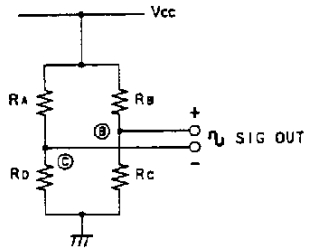
MR sensor

MR sensor (a magnetic resistor) is used for the capstan FG.

The capstan motor speed varies greatly from STOP to FF/REW.
To obtain a stable output level regardless of speed in such cases, the MR sensor is indispensable to this IC.

(Principle)

The MR element utilizes the change that occurs in the resistance value with the variation in magnetic flux.



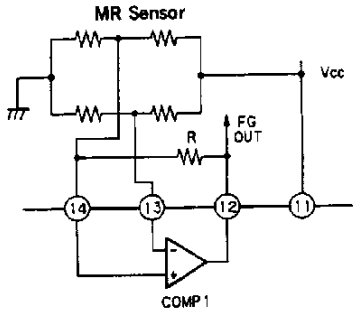
Explanation of respective blocks

The sensor amplifier block is composed of the following 3 blocks.

- Block for Capstan FG processing
- Block for Drum processing
- Block for Drum PG AMP processing

① Capstan FG

Exclusive to MR sensor, performs saturated amplification at the comparator. On the other hand, MR sensor produces a particular high frequency noise. As FG frequency is raised, the noise is sometimes mistakenly output. To this effect, this IC features hysteresis characteristics from the resistor inserted between Pins ⑫ and ⑬.



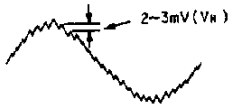
R: Hysteresis resistance

R is determined through the following formula

$R \fallingdotseq (V_{CC}/V_H)\ (R_{MR}/2)$

R_{MR}···Total resistance value of MR sensor

** V_H: Hysteresis voltage



② Drum FG

The variable reactance system is utilized (an output voltage corresponding to the number of revolutions is obtained.)

The capacitors inserted in Pins ② and ③ serve to elimitate the drive coil switching noise.

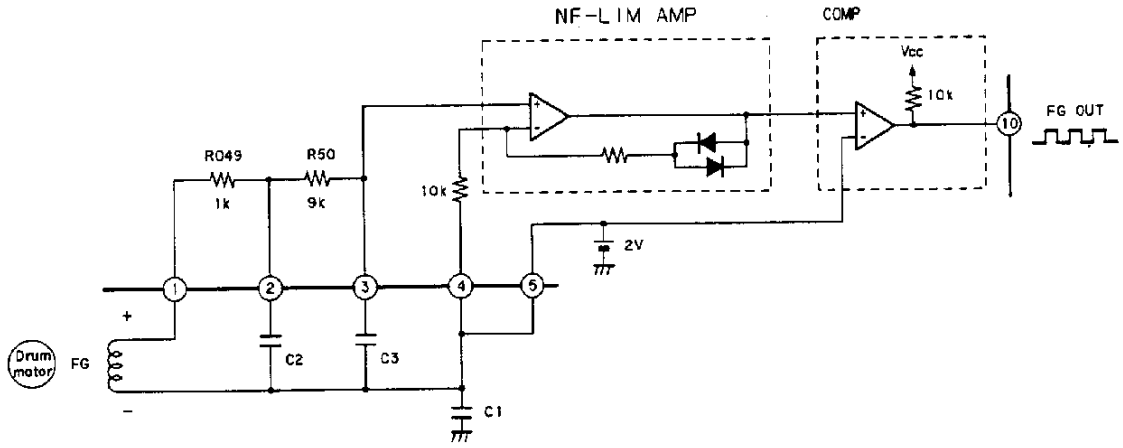
Drum FG is a non inverted input directly connecting Pin ① and the Bias Pin ⑤. That is Pin ① is biased passing through drum FG coil. Also, Pin4 that is an inverted input is connected to Pin ⑤.

As a result, both inverted and non-inverted inputs are externally biased, AM fluctuations become common mode noise to be eliminated by the input limiter amplifier.

For the setting of noise eliminating capacitors C3 and C2, an fC (cut off frequency) value around 20 times that of fFG during the drum motor steady-state revolution, is required

That is because of the phase relation between FG and PG. When FG frequency cut off are close, phase revolution occures.

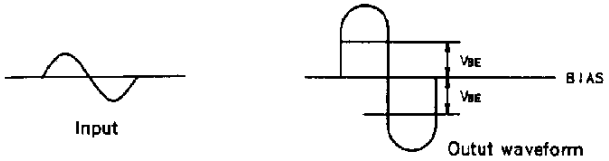
$fc \fallingdotseq 20 f_{FG}$ $\quad fc = \dfrac{1}{2\pi R_{049} C_2}$ $\quad \therefore C_2 = \dfrac{1}{4\times 10^4 \pi f_{FG}}$



Also C≒10C2

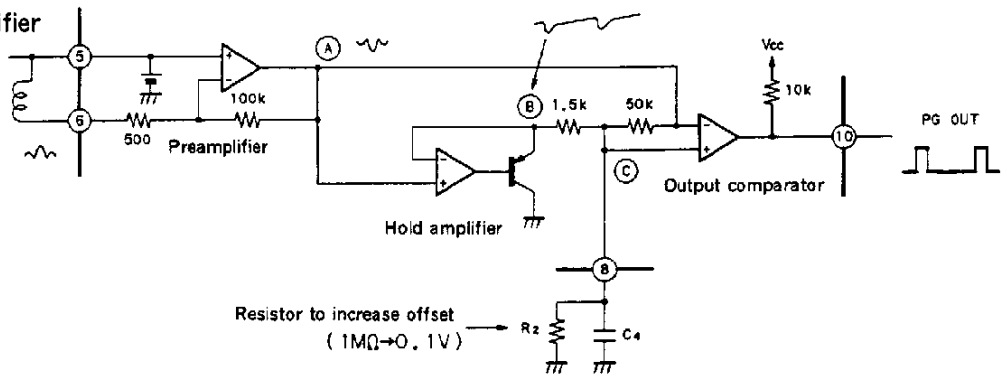
To compensate for the presision and temperature characteristics of the built-in resistor, use a resistor with ceramic B characteristics for C2 and C3.

FG signals passed through the L.P.F are input to the limiter amplifier.



This limiter output is converted into rectangular waves at the hysteresis camparator and output from Pin ⑩. The comparator features hysteresis characteristics of about 100mV. This is to prevent wrong output provoked by noise or other when the motor is stopped there are no FG signals.

③ Drum PG amplifier



The drum PG output level at 1mV is about 1/10 that of FG.

As a noise countermeasure, peak hold is utilized to vary the threshold level of converted rectangular waves.

As PG coil is connected between input Pin 6 and bias Pin 5.
PG signal is biased and input.
Input at Pin ⑥ is the preamplifier inverted input with an input impendance of about 500Ω. The preamplifier is composed of a PNP differential input with a gain of 46 dB. Accordingly, when input at Point A is at 1mVp-p, a PG signal of about 0.2 Vo-p can be obtained.

To prevent misoperation when the drum motor is stopped, a +3mV offset is applied to the output comparator +side. This is how it works. As the drum motor starts moving a PG signal is generated.
In the PG signal generating period Point A voltage decreases. As a result, and in order to lower the output, the hold amlifier passing through the 1.5kΩ resistor provoques an electric discharge by sucking up C electric charge and Point C voltage decreases to the minimum of Point A PG level. As PB period ends,, Point A goes to bias voltage. As Points C and A are connected by 50kΩ resistor, Point C voltage slowly closes down on Point A voltage at a C4 and 50kΩ time constant.
As the drum makes one revolution the PG generating period is on again, the hold amplifier electrically discharges C4 and lowers Point C voltage to the minimum value of Point A inverted PG signal. Point C voltage is held a little than the minimum value of Point A inverted PG signal. this is because up to just before the electric discharge of Point C C4 it is charge by means of a 50Ω resistor. As Point C voltage starts rising, during discharge by the hold amplifier, as it passed through 1.5kΩ resistor, and due to that time constant Point C voltage does not fully decrease within the PG period short time.

PG AMP waveforms is attached.

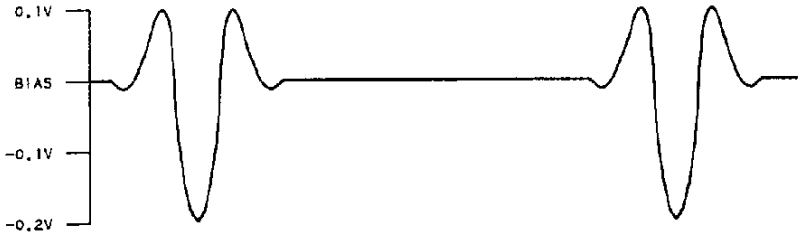
Notes on Operation

As a large curtrent flows through cpstan FG output Pins ⑫, ⑬ and ⑭, also, drum FG, PG output Pins ④, ⑤ and ⑥, mutual interference between capstan outputs easily occurs. To this effect keep output lines as short as possible and adopt a layout avoiding mutual closeness.

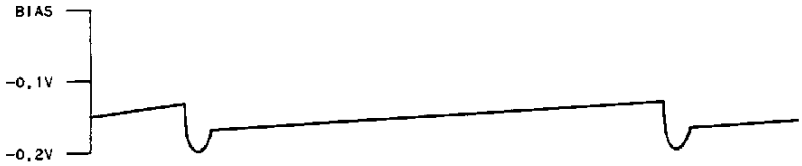
PG AMP Waveform

Pin 6 input
PG original signal

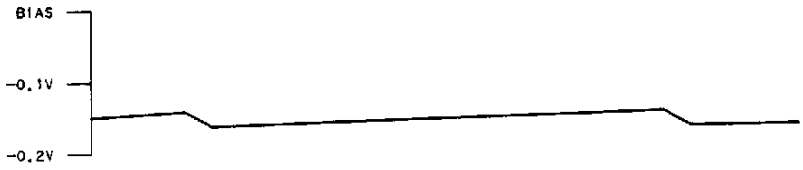
A point
Preamplifier
output signal



B point
Hold amplifier
output



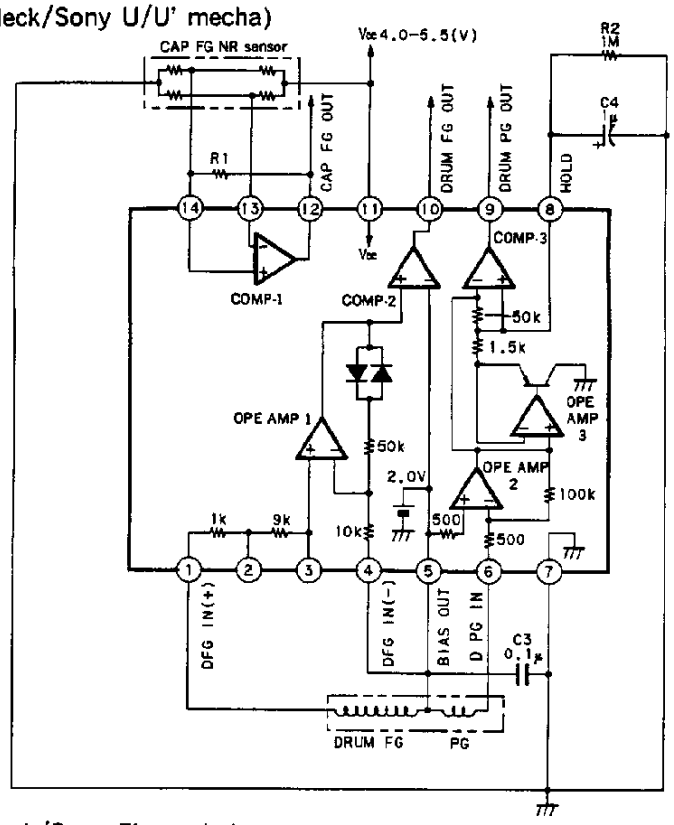
C point (Pin 8)
Hold capacitor
waveform



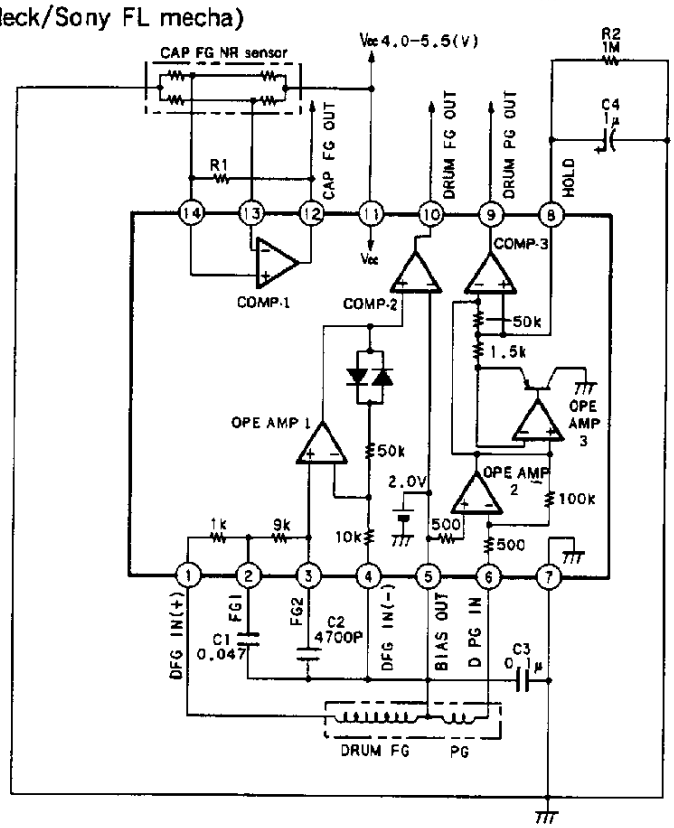
Pin 9
PG arranged output
waveform

Application Circuit

(For standard mechadeck/Sony U/U' mecha)



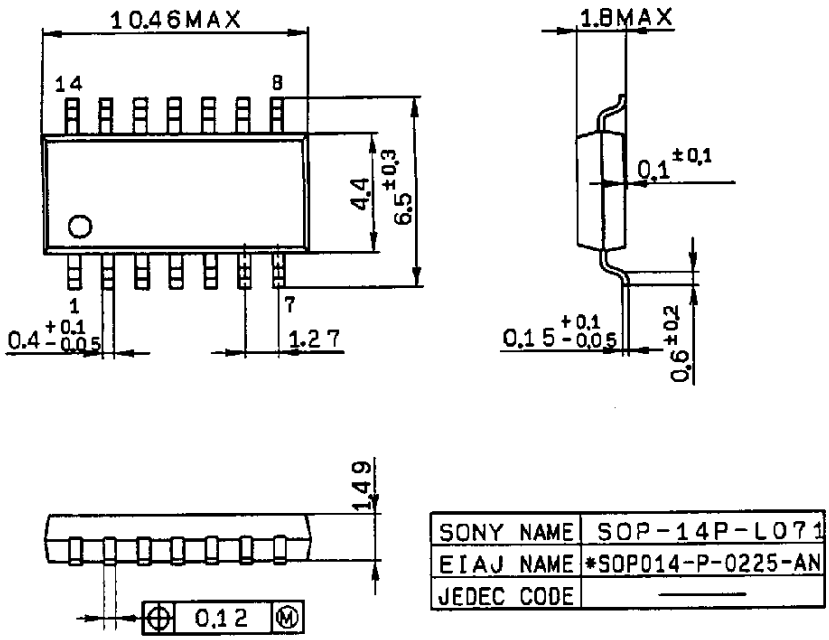
(For compact mechadeck/Sony FL mecha)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

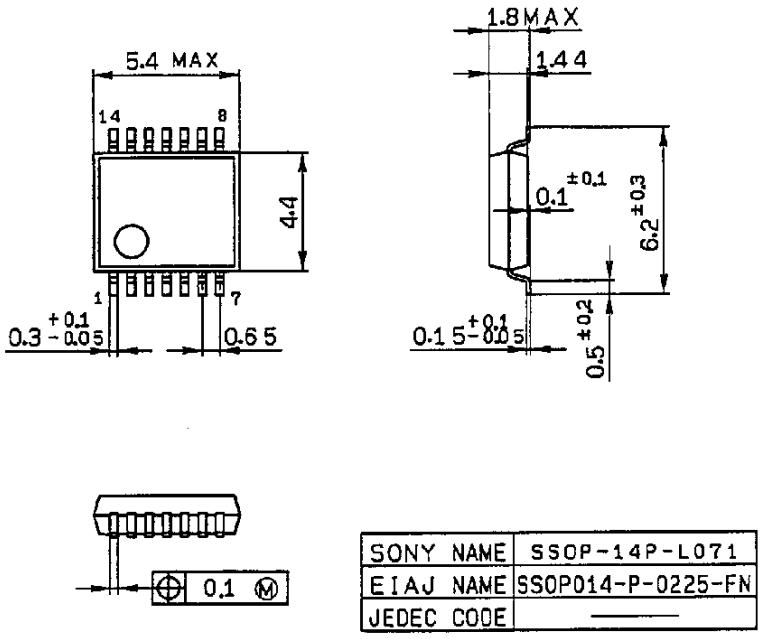
Package Outline Unit : mm

CXA1512M 14pin SOP (Plastic) 225mil



SONY NAME	SOP-14P-L071
EIAJ NAME	*SOP014-P-0225-AN
JEDEC CODE	———

CXA1512N 14pin SSOP (Plastic) 225mil



SONY NAME	SSOP-14P-L071
EIAJ NAME	SSOP014-P-0225-FN
JEDEC CODE	———