SONY

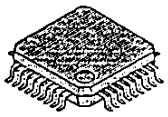
CXA1536Q

8 mm VCR AFM Stereo Matrix

Description

The CXA1536Q is an IC designed for 8 mm VCR stereo AFM matrix. In combination with a CXA1488R device it offers an effective implementation of an AFM audio stereo system.

36pin QFP (Plastic)



Features

- Matrix select functions for stereo
- Monaural discriminating function
- Bilingual discriminating function
- Incorporates a pulse signal generator for inserting a bilingual pilot signal
- Low current consumption

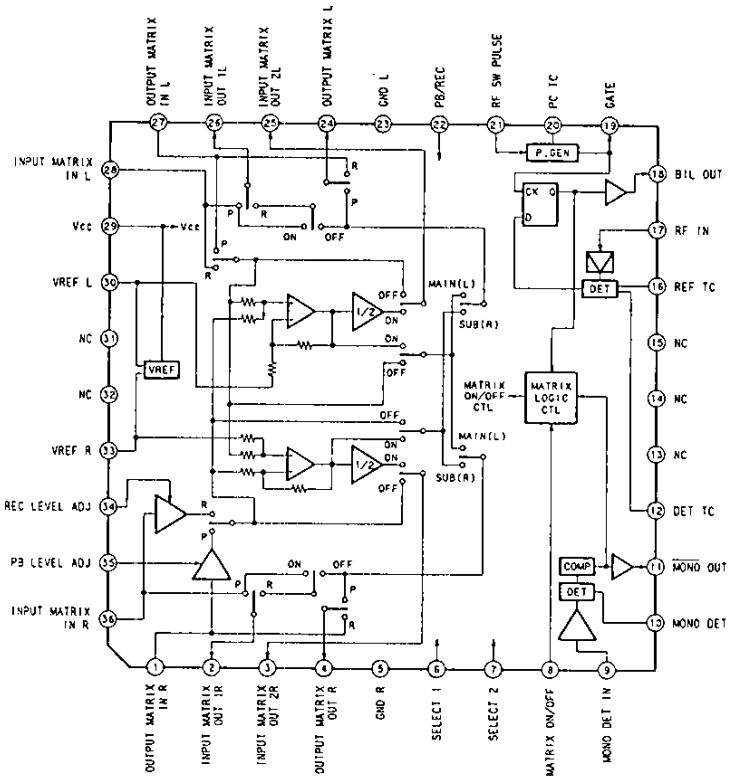
Application

8 mm VCR

Structure

Bipolar silicon monolithic IC

Block Diagram



E90801-HP

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Absolute Maximum Ratings (Ta = 25°C)

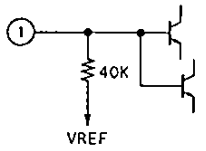
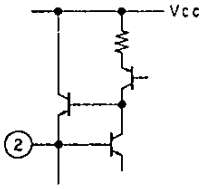
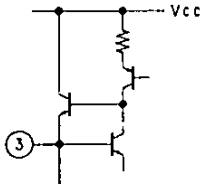
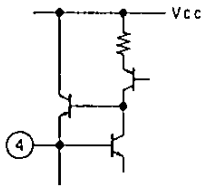
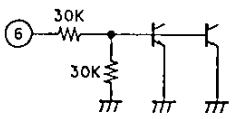
• Supply voltage	V_{CC}	7	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−40 to +150	°C
• Allowable power dissipation	P_D	320	mW

Operating Conditions

• Supply voltage	4.75 V	
• Supply voltage range	4.5 to 5.5	V

Pin Description

0 dBs = 2.191 Vp-p

No.	Symbol	DC voltage	AC voltage	Equivalent circuit	Remarks	
1	OUTPUT MATRIX IN R	2.375V	—		Reference input −15 dBs	
2	INPUT MATRIX OUT 1R	2.375V	−15dBs		With reference input	
3	INPUT MATRIX OUT 2R	2.375V	0V		With reference input	Recording stereo
			−15dBs			Other than recording stereo
4	OUTPUT MATRIX OUT R	2.375V	0V		With reference input	Playback Stereo
			−15dBs			Other than playback stereo
5	GND	—	—	—		
6	SELECT 1	—	—		High: right channel output Low: left channel output	

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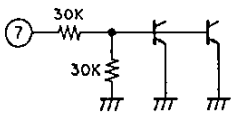
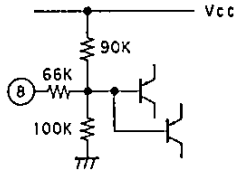
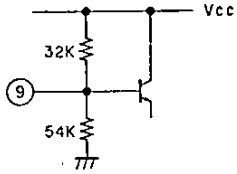
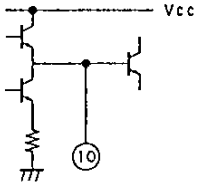
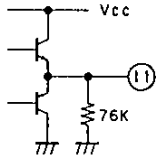
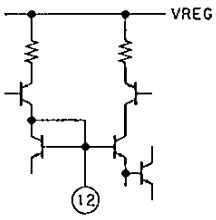
No.	Symbol	DC voltage	AC voltage	Equivalent circuit	Remarks	
7	SELECT 2	—	—		High: left channel output Low: right channel output	
8	MATRIX ON/OFF	2.5V	—		High: matrix on Open: automatic discrimination during playback Low: matrix off	
9	MONO DET IN	3V	—		Reference input	MONO ≧1.5V STEREO −15dBs
10	MONO DET	≧2.2V	—		With reference input	Mono
		≦1.8V				Stereo
11	$\overline{\text{MONO}}$ OUT	≦1V	—		With reference input	Mono
		≧3.5V				Stereo
12	DET TC	→	—		With reference input	NORMAL 3V BILINGUAL ≧3.3V
13	NC					
14	NC					
15	NC					

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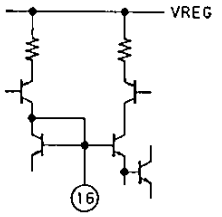
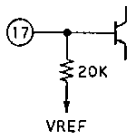
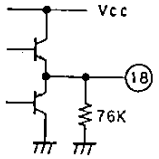
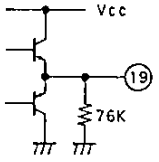
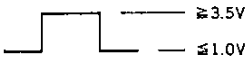
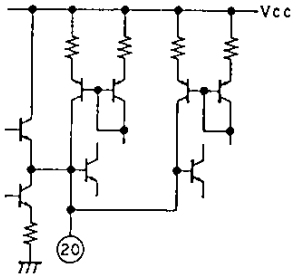
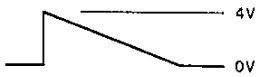
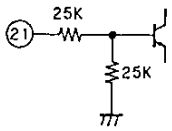
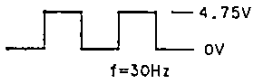
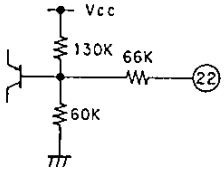
No.	Symbol	DC voltage	AC voltage	Equivalent circuit	Remarks
16	REF TC	→	—		With reference input: NORMAL 3.1V; BILINGUAL 3.1V
17	RF IN	2.375V	—		Reference input: NORMAL 150mVp-p; BILINGUAL 7dB 150mVp-p =0dB
18	BIL OUT	≦1 V	—		With reference input: Normal
		≧3.5V			With reference input: Bilingual
19	GATE OUT	→	—		
20	PC TC	→	—		
21	RF SW PULSE	—	—		Reference input 
22	PB/REC	1.5V	—		High: playback Low/open: record
23	GND	—	—		

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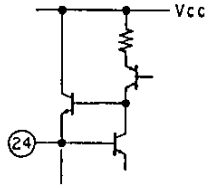
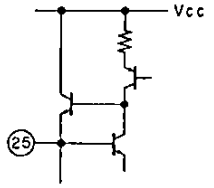
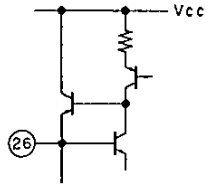
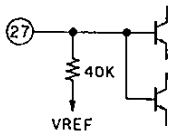
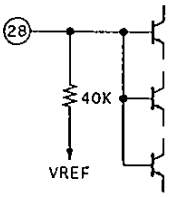
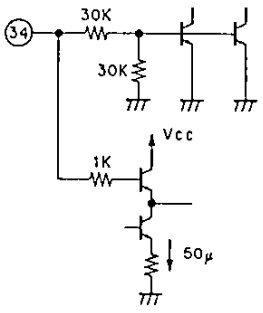
No.	Symbol	DC voltage	AC voltage	Equivalent circuit	Remarks
24	OUTPUT MATRIX OUT L	2.375V	−9dBs		With reference input: Playback stereo
			−15dB9		With reference input: Other than playback stereo
25	INPUT MATRIX OUT 2L	2.375V	−15dBs		With reference input
26	INPUT MATRIX OUT 1L	2.375V	−15dBs		With reference input
27	OUTPUT MATRIX IN L	2.375V	—		Reference input −15 dBs
28	INPUT MATRIX IN L	2.375V	—		Reference nput −15 dBs
29	V_{CC}	—	—		
30	VREF L	2.375V	—		
31	NC				
32	NC				
33	VREF R	2.375V	—		
34	REC LEVEL ADJ	—	—		Input voltage 1.8V−V_{CC}: ±3 dB variable ≦1 V: through

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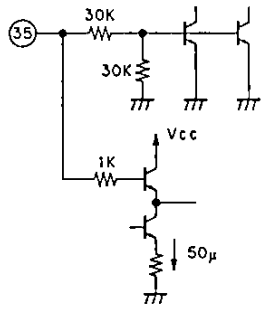
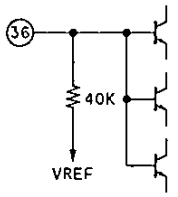
No.	Symbol	DC voltage	AC voltage	Equivalent circuit	Remarks
35	PB LEVEL ADJ	—	—		Input voltage 1.8V−V_{CC}: ±3 dB variable ≦1 V: through
36	INPUT MATRIX IN R	2.375V	—		Reference input −15 dBs

Electrical Characteristics (Ta=25°C, V_{CC}=4.75V) 0 dBs=2.191 Vp-p

No.	Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
			Input	Test point				
1	Current consumption recording	I_{CC} R		I_{CC}	4.8	6.1	7.4	mA
2	Current consumption playback	I_{CC} P		↓	6.0	7.6	9.2	mA
3	Reference voltage	VREF		TP11	2.300	2.375	2.450	V
	REC MATRIX ON MODE (left channel)							
4	Voltage gain 1	G_{RML1}	400Hz, −15dBs	TP9	−0.2	0	0.2	dB
5	Distortion factor 1	THD_{RML1}	400Hz, −5dBs	↓			0.1	%
6	Voltage gain 2	G_{RML2}	400Hz, −15dBs	TP8	−0.4	0	0.4	dB
7	Distortion factor 2	THD_{RML2}	400Hz, −5dBs	↓			0.1	%
8	Voltage gain 3	G_{RML3}	400Hz, −15dBs	TP7	−0.1	0	0.1	dB
9	Distortion factor 3	THD_{RML3}	400Hz, −5dBs	↓			0.1	%
10	Crosstalk	CT_{RML}	400Hz, −15dBs	TP1			−60	dB
11	Separation	SP_{RML}	400Hz, −15dBs, L/R left/right reverse phase inputs	TP8			−40	dB
	REC MATRIX OFF MODE (left channel)							
12	Voltage gain 1	G_{RL1}	400Hz, −15dBs	TP9, TP1	−0.5	0	0.5	dB
13	Distortion factor 1	THD_{RL1}	400Hz, −5dBs	↓			0.1	%
14	Voltage gain 2	G_{RL2}	400Hz, −15dBs	TP8	−0.2	0	0.2	dB
15	Distortion factor 2	THD_{RL2}	400Hz, −5dBs	↓			0.1	%
16	Crosstalk	CT_{RL}	400Hz, −15dBs	TP1			−60	dB

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PB MATRIX ON MODE (left channel)

No.	Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
			Input	Test point				
17	Voltage gain 1	G_{PML1}	400Hz, −15dBs	TP7	−0.5	0	0.5	dB
18	Distortion factor 1	THD_{PML1}	400Hz, −5dBs	↓			0.1	%
19	Voltage gain 2	G_{PML2}	400Hz, −15dBs	TP9	−0.1	0	0.1	dB
20	Distortion factor 2	THD_{PML2}	400Hz, −5dBs	↓			0.1	%
21	Crosstalk	CT_{PML}	400Hz, −15dBs	TP3			−60	dB
22	Separation	SP_{PML}	400Hz, −15dBs, left/right reverse phase inputs	TP7			−40	dB

PB MATRIX OFF MODE (left channel)

23	Voltage gain 1	G_{PL}	400Hz, −15dBs	TP7, TP3	−0.4	0	0.4	dB
24	Distortion factor 1	THD_{PL}	400Hz, −5dBs	↓			0.1	%
25	Crosstalk	CT_{PL}	400Hz, −15dBs	TP3			−60	dB

REC MATRIX ON MODE (right channel)

26	Voltage gain 1	G_{RMR}	400Hz, −15dBs	TP2	−0.5	0	0.5	dB
27	Distortion factor 1	THD_{RMR}	400Hz, −5dBs	↓			0.3	%
28	Crosstalk	CT_{RMR}	400Hz, −15dBs	TP9			−60	dB
29	Separation	SP_{RMR}	400Hz, −15dBs, left/right reverse phase inputs	TP2			−40	dB

REC MATRIX OFF MODE (right channel)

30	Voltage gain 1	G_{RR1}	400Hz, −15dBs	TP9, TP1	−0.5	0	0.5	dB
31	Distortion factor 1	THD_{RR1}	400Hz, −5dBs	↓			0.1	%
32	Voltage gain 2	G_{RR2}	400Hz, −15dBs	TP2	−0.3	0	0.3	dB
33	Distortion factor 2	THD_{RR2}	400Hz, −5dBs	↓			0.1	%
34	Crosstalk	CT_{RR}	400Hz, −15dBs	TP9			−60	dB

PR MATRIX ON MODE (right channel)

35	Voltage gain 1	G_{PMR}	400Hz, −15dBs	TP3	−0.5	0	0.5	dB
36	Distortion factor 1	THD_{PMR}	400Hz, −5dBs	↓			0.4	%
37	Crosstalk	CT_{PMR}	400Hz, −15dBs	TP9			−60	dB
38	Separation	SP_{PMR}	400Hz, −15dBs, left/right reverse phase inputs	TP3			−40	dB

PR MATRIX OFF MODE (right channel)

39	Voltage gain 1	G_{PR}	400Hz, −15dBs	TP3, TP7	−0.5	0	0.5	dB
40	Distortion factor 1	THD_{PR}	400Hz, −5dBs	↓			0.1	%
41	Crosstalk	CT_{PR}	400Hz, −15dBs	TP7			−60	dB

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ADJUST LEVEL

No.	Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
			Input	Test point				
42	REC LEVEL ADJUST range	V_{ADJ} J	400Hz, −15dBs, IN1 variable	TP2	1.8	3.0	V_{CC}	V
43	PB LEVEL ADJUST range	V_{ADJ} P	400Hz, −15dBs, IN2 variable	↓	1.8	3.0	V_{CC}	V

MONO DET

44	Discrimination level	V_{MON}	※ 1	TP4			1.5	Vp-p
45	Output level low	V_{MONL}	※ 1 V=0dBs	↓			1.0	V
46	Output level high	V_{MONH}	※ 1 V=−15dBs	↓	3.5			V

BILINGUAL DET

47	Discrimination level	V_3	※ 2	TP5	3.0	7.0		dB
48	Output level low	V_{3L}	※ 2 V=150mV	↓			1.0	V
49	Output level high	V_{3H}	※ 2 V=300mV	↓	3.5			V
50	Gate pulse width	T_P		TP6	1.2	1.3	1.4	msec
51	Gate pulse width output level low	V_{PL}		↓			1.0	V
52	Gate pulse width output level high	V_{PH}		↓	3.5			V

CONTROL LOGIC THRESHOLD

53	PB/REC L	$V_{P/RL}$	400Hz, −15dBs	TP9			1.0	V
54	PB/REC H	$V_{P/RH}$	400Hz, −15dBs	↓	3.5			V
55	MATRIX ON/OFF L	V_{MATL}	400Hz, −15dBs	↓			1.0	V
56	MATRIX ON/OFF H	V_{MATH}	400Hz, −15dBs	↓	4.2			V
57	SELECT 1 L	V_{S1L}	400Hz, −15dBs	TP7			1.0	V
58	SELECT 1 H	V_{S1H}	400Hz, −15dBs	↓	3.5			V
59	SELECT 2 L	V_{S2L}	400Hz, −15dBs	TP3			1.0	V
60	SELECT 2 H	V_{S2H}	400Hz, −15dBs	↓	3.5			V

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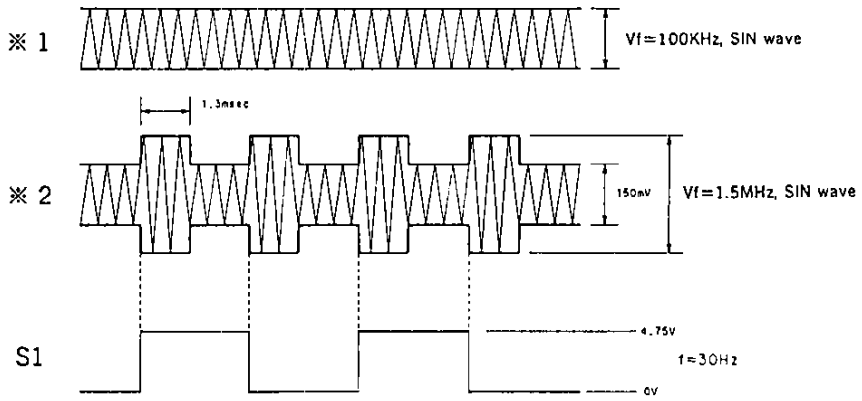
Input Signal



Note: In this specification, when a signal level of 7 dB standard, minimum 3 dB, is input, it indicates a bilingual discrimination. If tested under the previous test conditions, then if the results are 3 dB or below the above specification will be met.

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Switch Mode Table

MODE \ SW			PB/REC	MATRIX ON/OFF	SELECT1	SELECT2
REC	MONO		L	L	L	H
	STEREO		L	H	—	—
	BILINGUAL	MAIN/SUB	L	L	L	L
		MAIN/MAIN	L	L	L	H
		SUB/SUB	L	L	H	L
PB (AUTO)	MONO		H	OPEN	L	H
	STEREO		H	OPEN	L	L
	BILINGUAL	MAIN/SUB	H	OPEN	L	L
		MAIN/MAIN	H	OPEN	L	H
		SUB/SUB	H	OPEN	H	L
PB (MANUAL)	MONO		H	L	L	H
	STEREO		H	H	L	L
	BILINGUAL	MAIN/SUB	H	L	L	L
		MAIN/MAIN	H	L	L	H
		SUB/SUB	H	L	H	L

	PB/REC	MATRIX ON/OFF	SELECT1	SELECT2
H	PB	ON	Right channel output	Left channel output
L	REC	OFF	Left channel output	Right channel output

Test Program Table

No.	Switch No.				Input point	Remarks
	SW1	SW2	SW3	SW4		
1	a	a	b	b		
2	↓	↓	↓	a		
3	↓	↓	↓	↓		
4	b	b	a	b	IN5	Common to left and right channels
5	↓	↓	↓	↓	↓	Common to left and right channels
6	↓	↓	↓	↓	↓	
7	↓	↓	↓	↓	↓	
8	↓	↓	↓	↓	IN4	REC MATRIX ON/OFF MODE and common to left and right channels
9	↓	↓	↓	↓	↓	REC MATRIX ON/OFF MODE and common to left and right channels
10	↓	↓	↓	↓	IN5	
11	↓	↓	↓	↓	IN5, 6	IN5 and IN6 are reverse phase inputs
12	↓	a	b	↓	IN5	
13	↓	↓	↓	↓	↓	
14	↓	b	↓	↓	↓	
15	↓	↓	↓	↓	↓	
16	↓	↓	↓	↓	↓	

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No.	Switch No.				Input point	Remarks
	SW1	SW2	SW3	SW4		
17	b	b	a	a	IN4	
18	↓	↓	↓	↓	↓	
19	↓	↓	↓	↓	IN5	PB MATRIX ON/OFF MODE and common to left and right channels
20	↓	↓	↓	↓	↓	PB MATRIX ON/OFF MODE and common to left and right channels
21	↓	↓	↓	↓	IN5	
22	↓	↓	↓	↓	IN3, 4	IN3 and IN4 are reverse phase inputs
23	↓	a	b	↓	IN4	
24	↓	↓	↓	↓	↓	
25	↓	b	↓	↓	↓	
26	↓	↓	a	b	IN6	
27	↓	↓	↓	↓	↓	
28	↓	↓	↓	↓	↓	
29	↓	↓	↓	↓	IN5, 6	IN5 and IN6 are same phase inputs
30	a	↓	b	↓	IN6	
31	↓	↓	↓	↓	↓	
32	b	↓	↓	↓	↓	
33	↓	↓	↓	↓	↓	
34	↓	↓	↓	↓	↓	
35	↓	↓	a	a	IN3	
36	↓	↓	↓	↓	↓	
37	↓	↓	↓	↓	IN6	
38	↓	↓	↓	↓	IN3, 4	IN3 and IN4 are same phase inputs
39	a	↓	b	↓	IN3	
40	↓	↓	↓	↓	↓	
41	b	↓	↓	↓	↓	
42	↓	↓	↓	b	IN6	DC voltage applied to IN1 ; range of voltage on IN1 for TP2 output level to vary ±3 dB.
43	↓	↓	↓	a	IN3	DC voltage applied to IN2 ; range of voltage on IN2 for TP2 output level to vary ±3 dB.
44	↓	↓	↓	↓	IN8	Input level to IN8 for TP4 to go from high to low.
45	↓	↓	↓	↓	↓	
46	↓	↓	↓	↓	↓	
47	↓	↓	↓	↓	IN7	Voltage on IN7 increased ; voltage level for TP5 to go high at 150 mV.
48	↓	↓	↓	↓	↓	
49	↓	↓	↓	↓	↓	
50	↓	↓	↓	b		Pulse width output on TP6.
51	↓	↓	↓	↓		Low level output on TP6.
52	↓	↓	↓	↓		High level output on TP6.

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No.	Switch No.				Input point	Remarks
	SW1	SW2	SW3	SW4		
53	a	b	b	c	IN5, IN9	Increase the voltage on IN9 from 0 V; voltage on IN9 for the IN5 signal to be output from TP9.
54	↓	↓	↓	↓	↓	
55	↓	↓	c	b	IN5, IN10	Increase the voltage on IN10 from 0 V; voltage on IN10 for the IN5 signal to be output from TP9.
56	↓	↓	↓	↓	↓	
57	c	↓	b	a	IN4, IN11	Increase the voltage on IN11 from 0 V; voltage on IN11 for the IN4 signal to be output from TP7.
58	↓	↓	↓	↓	↓	
59	b	c	↓	↓	IN4, IN12	Increase the voltage on IN12 from 0 V; voltage on IN12 for the IN4 signal to be output from TP3.
60	↓	↓	↓	↓	↓	

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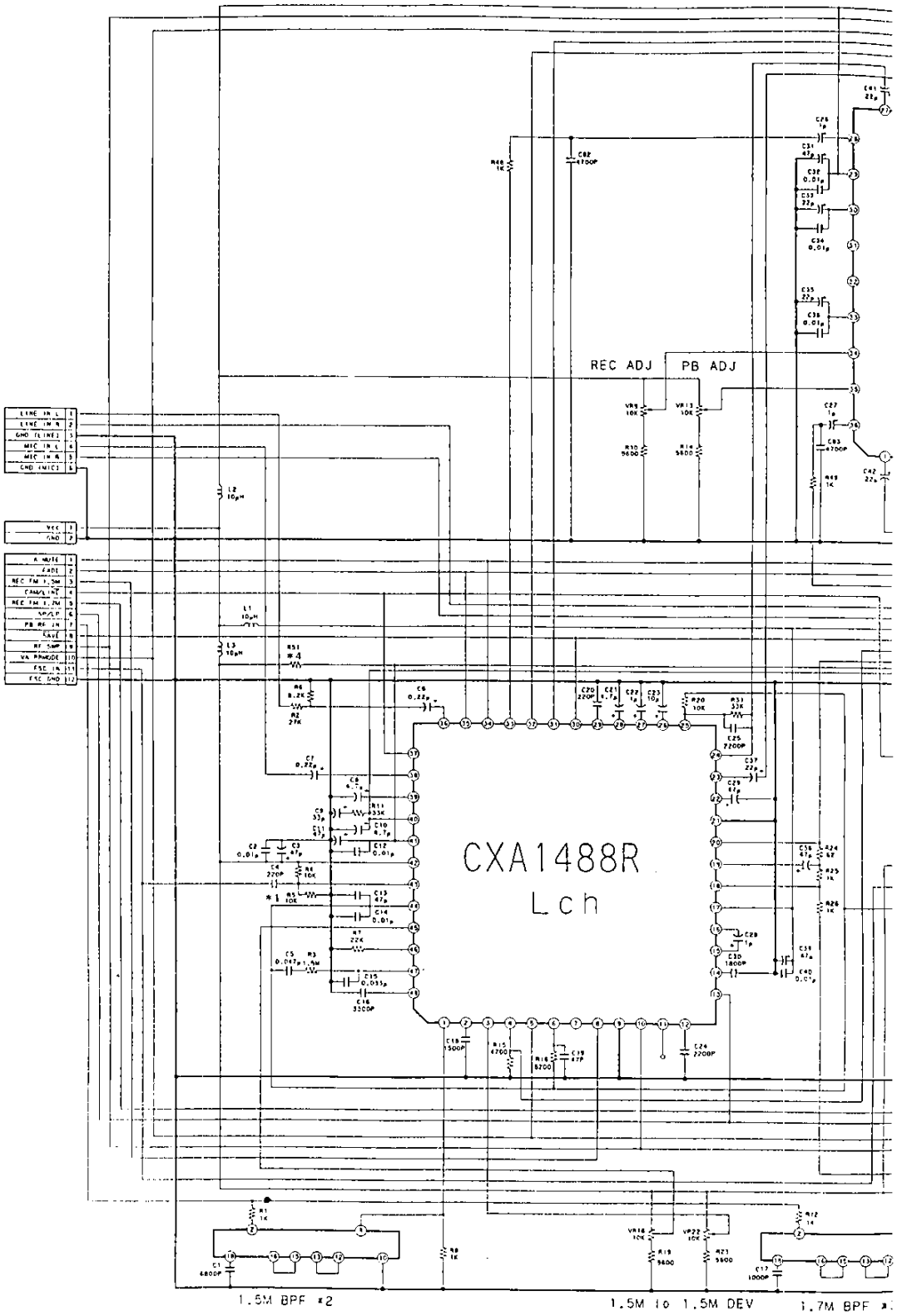
Stereo Application Circuit (8 mm VCR AFM)



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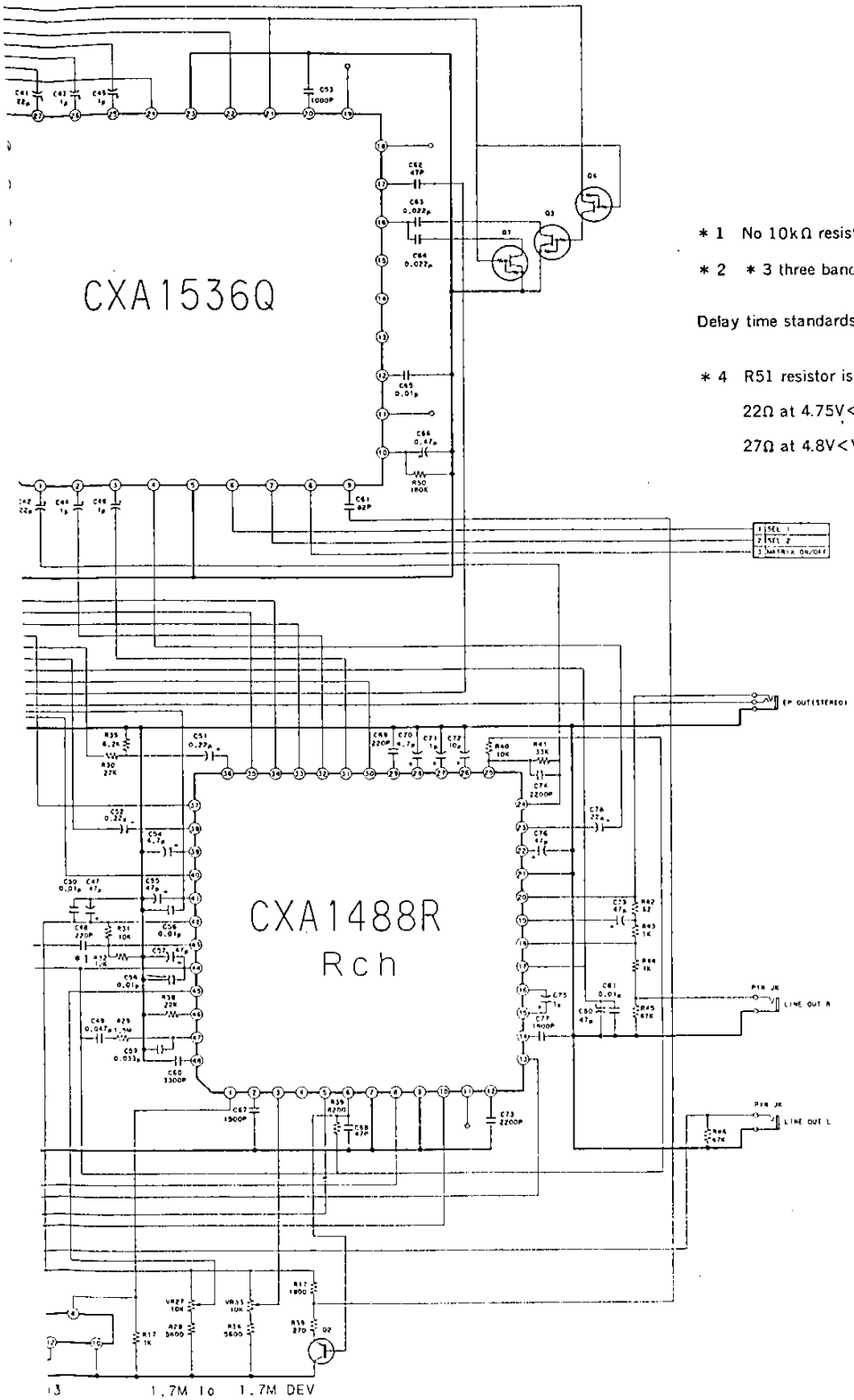

* 1 No 10kΩ resistor for PAL

* 2 * 3 three band-pass filters

Delay time standards { 1.5 MHz 3.3 ±0.5 μs / 1.7 MHz 5.1 ±1.0 μs }

* 4 R51 resistor is determined by the voltage at V_{CC}

22Ω at $4.75V < V_{CC} < 4.9V$

27Ω at $4.8V < V_{CC} < 5.1V$

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

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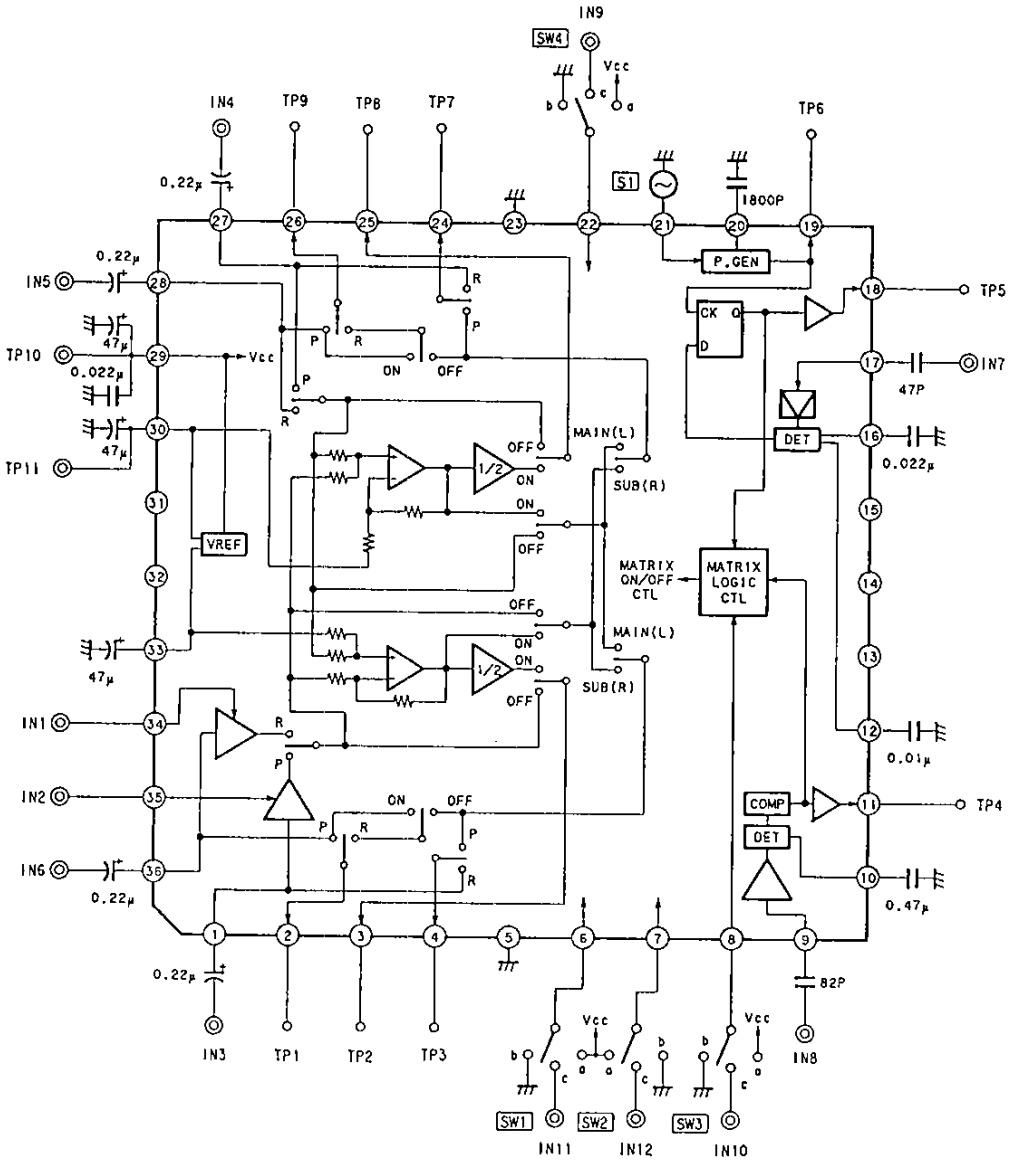
Test Circuit



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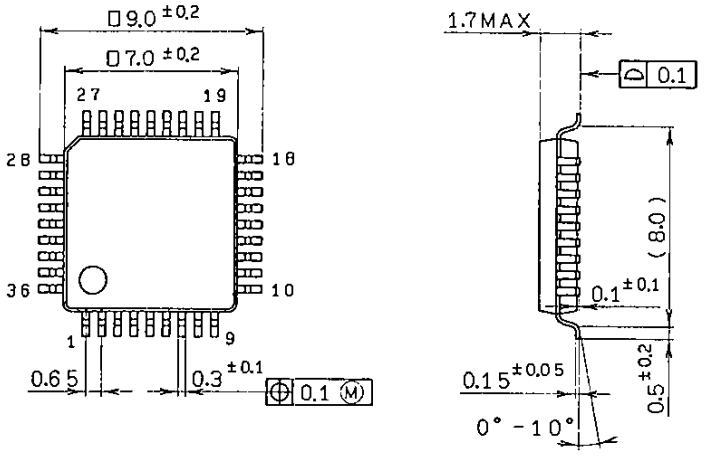
Package Outline Unit : mm

36pin QFP (Plastic)



SONY NAME	QFP-36P-L061
EIAJ NAME	*QFP036-P-0707-BY
JEDEC CODE	———

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