

FM Stereo/AM Radio

For the availability of this product, please contact the sales office.

Description

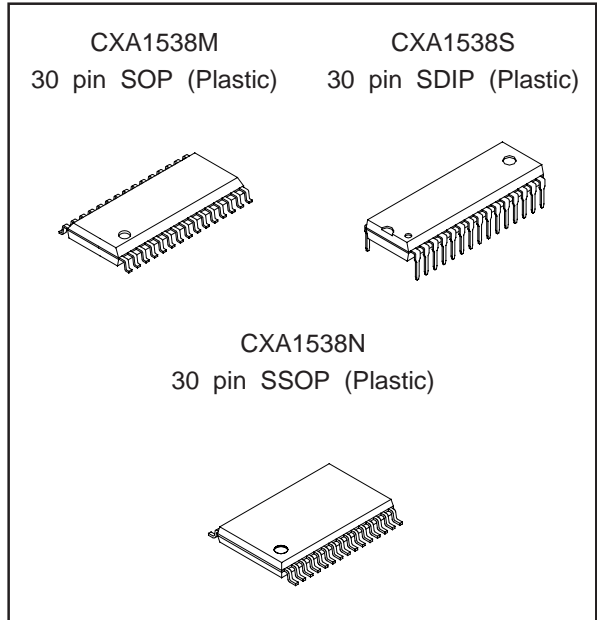
The CXA1538M/N/S is high performance one-chip bipolar ICs designed for FM stereo/AM radios. These include an FM/AM front end, FM/AM IF amplifier, FM/AM detection output and FM stereo demodulator output.

Features

- Low current consumption
(In FM mode $I_D=11.0$ mA, in AM mode 8.5 mA, $V_{CC}=6.0$ V)
- Built-in LED drive circuit for tuning
- Built-in LED drive circuit for stereo indicator
- Built-in muting circuit for the FM band
- Few external parts

Absolute Maximum Ratings ($T_a=25$ °C)

• Supply voltage	V_{CC}	14	V
• Operating temperature	T_{opr}	-10 to +60	°C
• Storage temperature	T_{stg}	-55 to +150	°C
• Junction temperature	T_{jmax}	125	°C
• Allowable power dissipation	P_D		
	CXA1538M	500	mW
	CXA1538N	410	mW
	CXA1538S	1050	mW



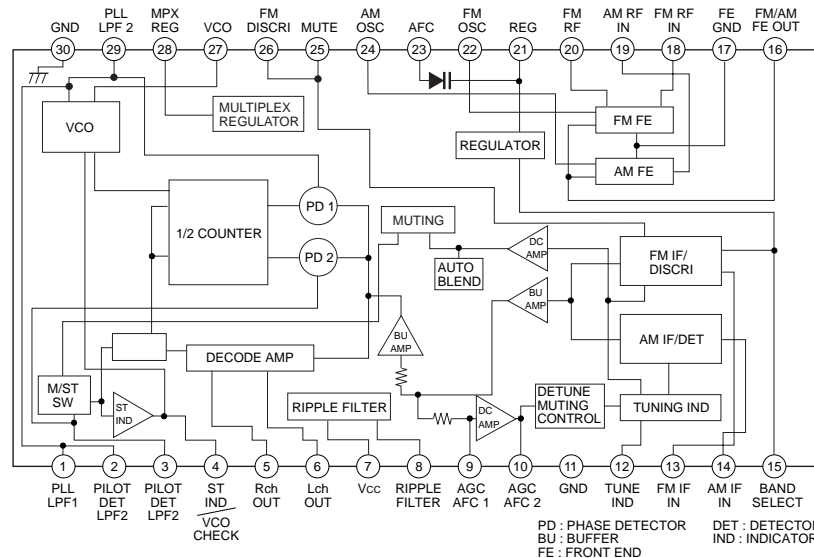
Recommended Operating Conditions

Supply voltage	V_{CC}	2 to 9	V
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Structure

Bipolar silicon monolithic IC

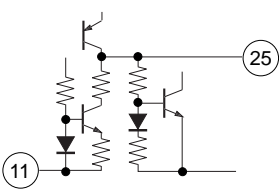
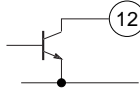
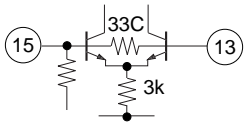
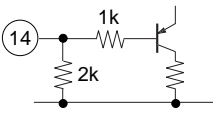
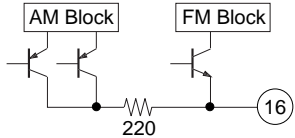
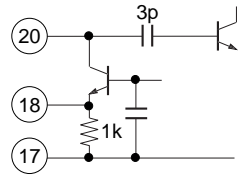
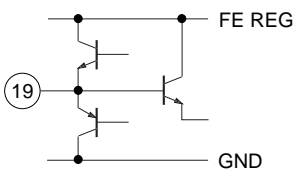
Block Diagram

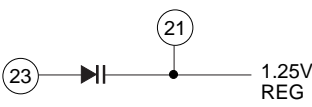
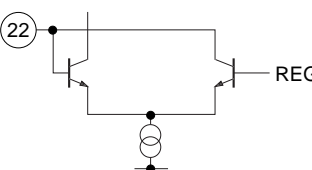
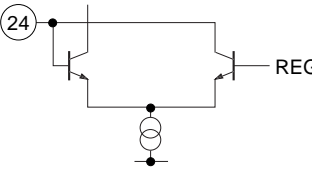
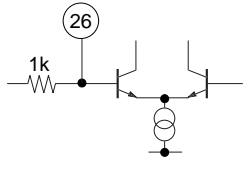
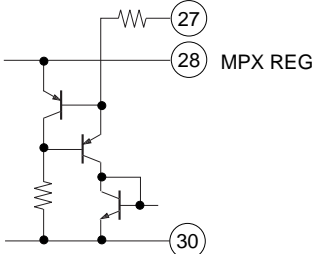


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Pin Description and Equivalent Circuit

No.	Symbol	Pin Voltage (V)				Equivalent circuit	Description
		V _{CC} =3 V		V _{CC} =6 V			
		FM	AM	FM	AM		
1	PLL LPF1	0.97	0.97	0.97	0.97		LPF for PLL
29	PLL LPF2						
2	PILOT DET LPF1	0.95	0.95	0.95	0.95		LPF's C (1µF) for PILOT DET inserted between pins 2 and 3
3	PILOT DET LPF2						
4	ST IND VCO CHECK	1.6	1.6	4.5	4.5		Stereo indicator drive circuit and output for VCO check
5	Rch OUT	0.66	0.66	1.5	1.5		Stereo Rch output pin
6	Lch OUT	0.66	0.66	1.5	1.5		Stereo Lch output pin
7	V _{CC}	3.0	3.0	6.0	6.0		Supply pin
8	Ripple FILTER	2.7	2.7	4.0	4.0		Ripple filter
9	AGC/AFC1	1.32	1.15	1.32	1.15		AFC pin in J band, determines time constant of AGC in AM (depending on external capacitor).
10	AGC/AFC2	1.15	1.47	1.15	1.47		AFC pin in W band, determines time constant of AGC in AM (depending on external capacitor).

No.	Symbol	Pin Voltage (V)				Equivalent circuit	Description
		V _{CC} =3 V		V _{CC} =6 V			
		FM	AM	FM	AM		
11	GND	0	0	0	0		GND of FM/AM IF and DET stage
25	MUTE	0.05	0.01	0.05	0.01		Time constant for muting provided
12	TUNE IND	1.6	1.6	4.5	4.5		FM/AM tuning indicator drive circuit
13	FM IF IN	1.35	0	1.35	0		FM IF input pin
15	BAND SELECT						FM/AM band switching pin : AM at GND and FM at OPEN
14	AM IF IN	0	0	0	0		AM IF input pin
16	FM/AM FE OUIT	0.57	0.2	0.8	0.2		AM/FM IF output pin to connect with IF filter
17	FE GND	0	0	0	0		GND of FM/AM front end
18	FM RF IN	0.3	0	0.3	0		FM RF amplifier circuit for FM RF input
20	FM RF	1.25	1.25	1.25	1.25		FM RF amplifier circuit to connect to RF tank circuit
19	AM RF IN	1.25	1.25	1.25	1.25		AM RF input to connect to bar antenna

No.	Symbol	Pin Voltage (V)				Equivalent circuit	Description
		V _{CC} =3 V		V _{CC} =6 V			
		FM	AM	FM	AM		
21	REG	1.25	1.25	1.25	1.25		Regulator output
23	AFC						Variable capacitance for AFC
22	FM OSC	1.25	1.25	1.25	1.25		FM local oscillation circuit
24	AM OSC	1.25	1.25	1.25	1.25		AM local oscillation circuit
26	FM DISCRI	2.30	2.70	3.60	4.00		Phase shift circuit to connect to ceramic discriminator
27	VCO						VCO control pin for stereo demodulation
28	MPX REG	1.65	1.65	1.65	1.65		Regulator for MPX
30	GND	0	0	0	0		GND of MPX block

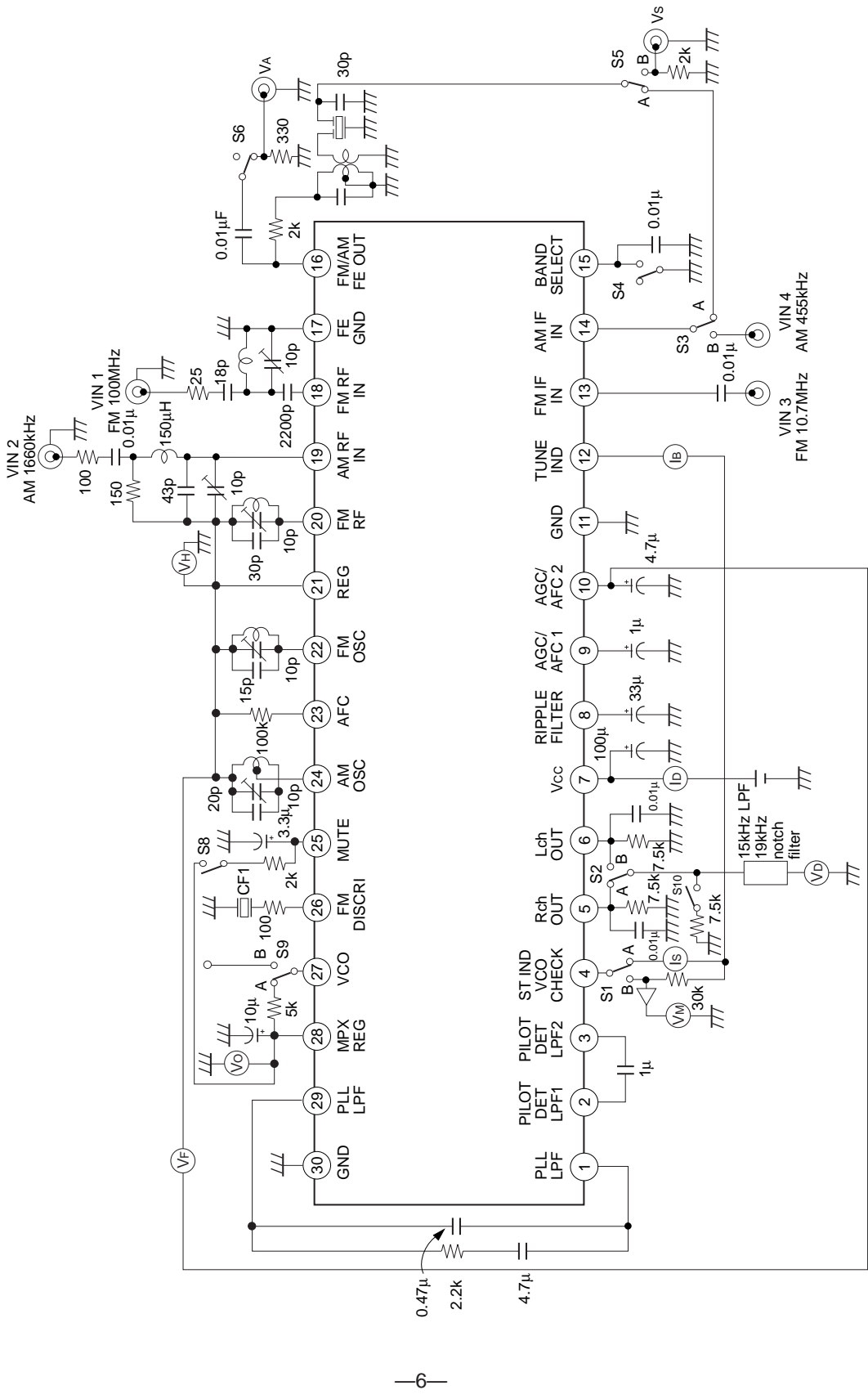
Electrical Characteristics

(Ta=25 °C, Vcc=6 V)

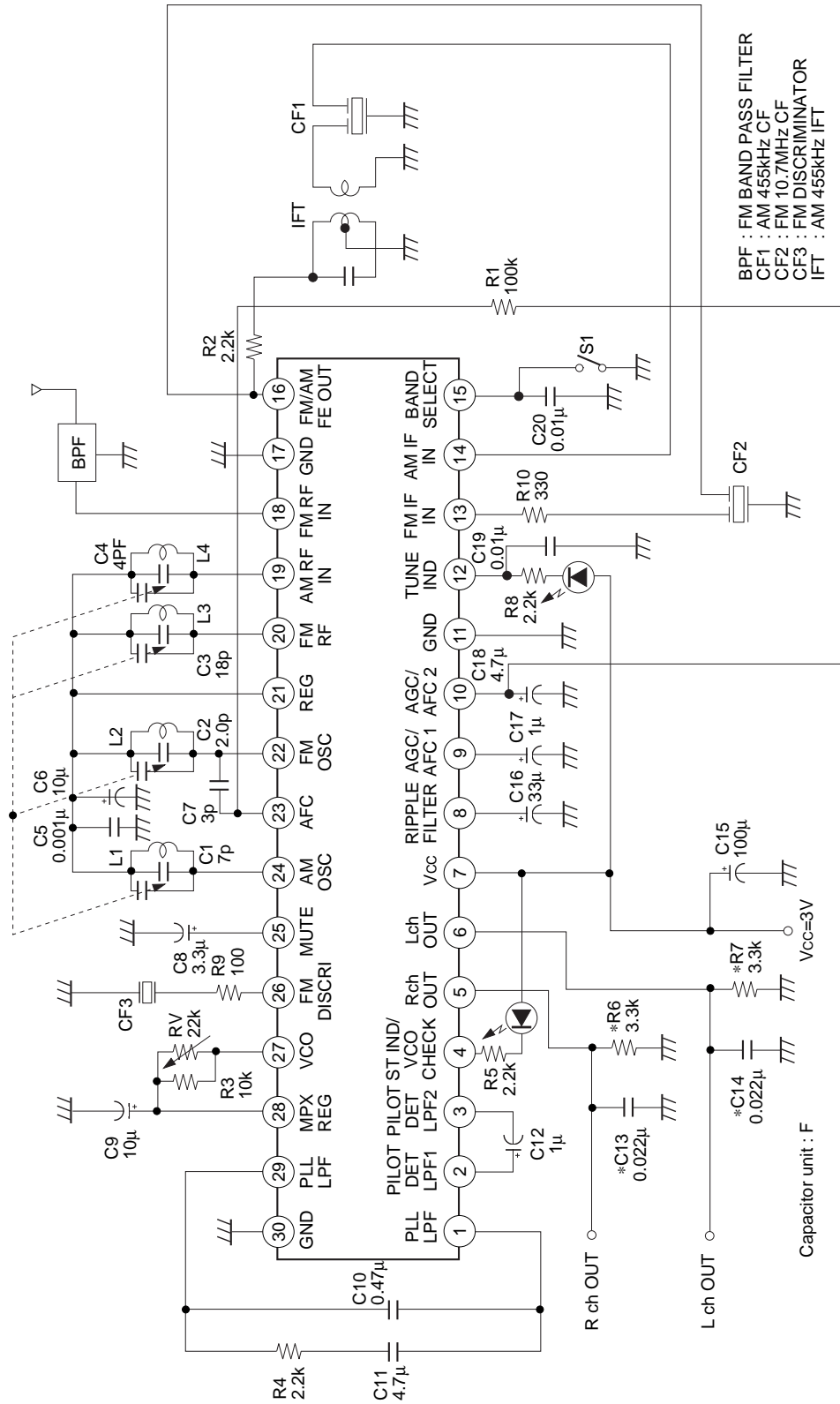
Item	Symbol	Test Point	Output waveform and Test method	SW condition										Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	8	9	10					
Circuit current (1)	ID1	ID	AM no signal V1 to V5 input short	A	A	A	B	A	B	OFF	A	OFF	5.0	8.5	12.0	mA	
Circuit current (2)	ID2	ID	FM no signal	▼	▼		A					▼	7.0	11.0	15.0	mA	
Separation	SEP	VD	Separation when VIN3=50 dBμV, 10.7 MHz, 1 kHz, 22.5 kHz dev input	B	/							▼	30	40	—	dB	
FM MUTE	A1	VD	Attenuation of noise level When VIN3=no signal, S8 ON/OFF	A	A							ON / OFF	16	23	30	dB	
STEREO indicator output	Is	Is	VIN3=60 dBμV, 10.7 MHz CW Pilot ON							▼	OFF		1.8	3.0	5.0	mA	
FM front end voltage gain (1)	GV1	VA	VIN1=40 dBμV, 100 MHz CW VA=10.7 MHz CW		▼						A		28	35	42	dB	
FM detection (MONO/STEREO) output level L, R	VD1	VD	VIN3=90 dBμV, 10.7 MHz 1 kHz 22.5 kHz dev VD=1 kHz sine wave		A / B						B		35.0	77.5	138	mVrms	
FM-IF knee level	VD2	VIN3	VIN3=90 dBμV, 10.7 MHz Input level at -3 dB of 1 kHz 22.5 kHz dev output		A								—	25	31	dBμV	
FM-IF distortion L, R (MONO)	THD1	VD	VIN3=90 dBμV, 10.7 MHz 1 kHz 75 kHz dev		A / B								—	0.1	2.0	%	
FM-IF distortion L, R (STEREO)			VD=1 kHz sine wave		▼									0.1	2.0	%	
FM-IF center frequency deviation	ΔF1	VF	VIN3=90 dBμV, 10.7 MHz CW		A								-50	0	+50	kHz	
FM meter current (1)	IB1	IB	VIN3=60 dBμV, 10.7 MHz CW										1.8	3.5	7.0	mA	
M/ST switching level by IF input	V11	Is	VIN3=10.7 MHz										M→ST 38	43	48	dBμV	
													ST→M 35	41	46	dBμV	
Auto blend	V12	VIN3					▼	▼				▼	1	10	41	dB	
AM front end voltage gain (2)	GV2	VB	VIN2=60 dBμV, 1660 kHz CW VB=455 kHz CW			▼	B	B				A	19	24	28	dB	
AM-IF voltage gain (4)	GV3	VIN4	VIN4 level at output of 15.5 mVrms		▼	B		A					15	21	29	dBμV	
AM detection output level (L, R)	VD3	VD	VIN4=85 dBμV 455 kHz (1 kHz 30 % MOD) VD=1 kHz sine wave		A / B								35.0	77.5	138	mVrms	
AM meter current (2)	IB2	IB	VIN4=85 dBμV, 455 kHz CW		A	▼							1.3	3.0	7.0	mA	
AM detection output distortion (L, R)	THD2	VD	VIN2=95 dBμV, 1660 kHz (1 kHz 30 % MOD) VD=1 kHz sine wave	▼	▼	A	▼	▼	▼	▼	▼	▼	—	0.6	2.0	%	

0 dBμV=1 μV

Electrical Characteristics Test Circuit

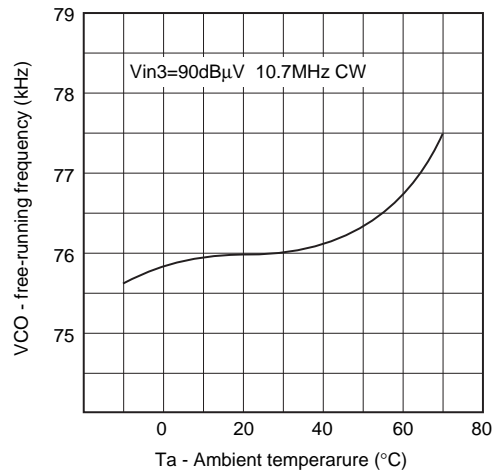
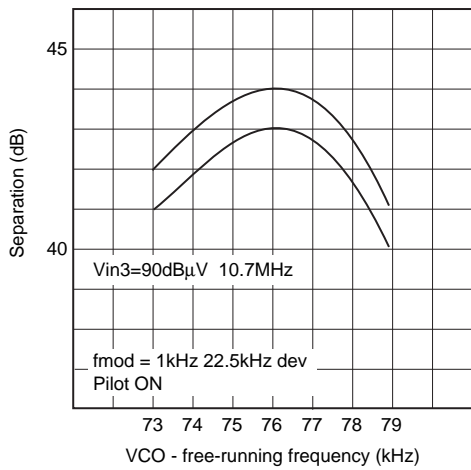
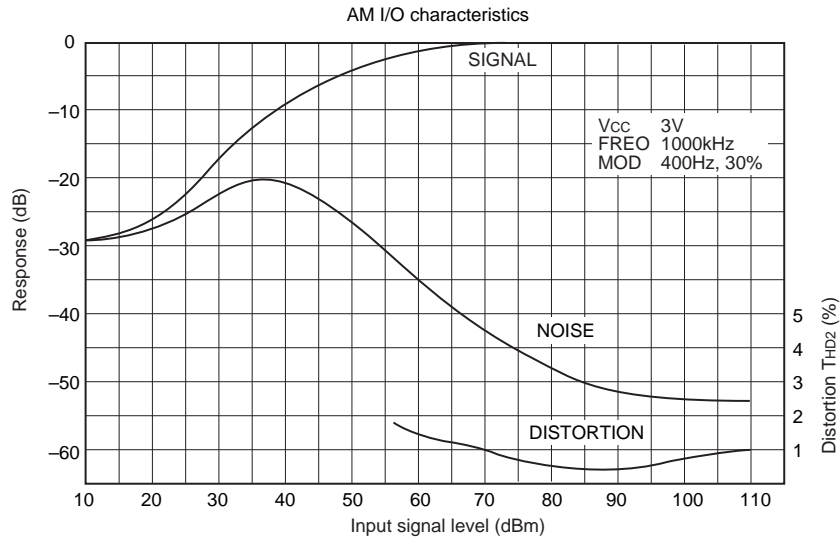
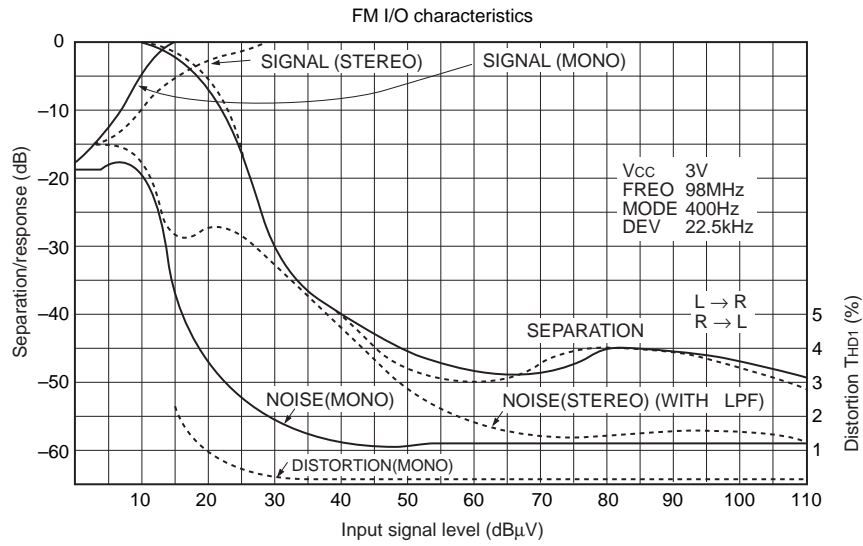


Application Circuit



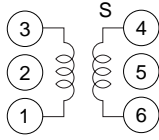
Note) This circuit is an application example and is not guaranteed for all applications.
 For C, R (C13, C14, R6, R7) marked*, refer to "2. MPX circuit" of "Notes on Usage."

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Coil data

AM OSC

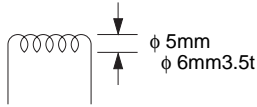


Core diameter \varnothing 0.06 mm 2 UEW

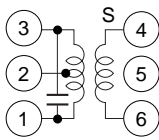
f (kHz)	L (μ H)	Q _o	Number of windings (t)	
			1 to 3	4 to 6
796	270	125	107	29

Equivalent to L-5K7H5 R12-1684X, Mitsumi Electric Co., Ltd. or 7TRS-8441 TOKO Co., Ltd.

FM RF



AM IFT

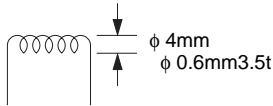


Core diameter \varnothing 0.07 mm UEW

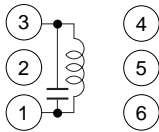
Co (pF)	Q _o	Number of windings (t)		
		1 to 2	2 to 3	4 to 6
180	90	111	35	7

Equivalent to 21K7H5 R12-8558A, Mitsumi Electric Co., Ltd. or 7MC-7789N TOKO Co., Ltd.

FM OSC



FM Discriminator

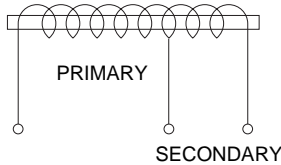


Core diameter \varnothing 0.1 mm 2 UEW

Co (pF)	Q _o	Number of windings (t)		
		1 to 3		
82	95	111		

Equivalent to 119ASC-12200Z, TOKO Co., Ltd.

AM Bar Antenna



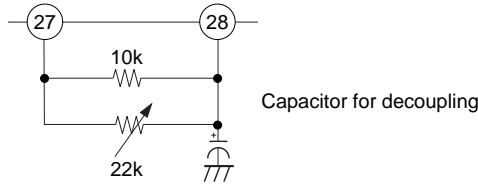
f (kHz)	L (μ H)	Primary	Secondary
796	650	91 t	20 t

BPF	PFE8 (88 to 108 MHz)	Soshin Electric Co., Ltd.	
CF1	SFU-455B	Murata Mfg. Co., Ltd. or BFCFL-455	TOKO Co., Ltd.
CF2	SFE10.7MA5	Murata Mfg. Co., Ltd.	
CF3	CDA10.7MG1	Murata Mfg. Co., Ltd.	
VC	PVC2LXT16L	Mitsumi Electric Co., Ltd.	
VC (Rear Mount)	HU22124N700	TOKO Co., Ltd.	
	PVC2LXT16B	Mitsumi Electric Co., Ltd.	

Notes on Usage

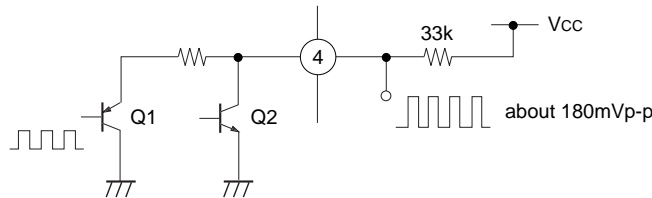
1. VCO free run frequency adjustment method

As this IC has built-in oscillation capacitance, the oscillation frequency can be controlled with an external resistor.



1) VCO Adjustment Method

Pin 4 is the stereo indicator and VCO check pin. Therefore, in stereo mode (when stereo indicator drive Tr Q2 is switched on), pin 4 voltage lowers down, Q1 is cut off and VCO oscillation waveform can not be seen. In AM mode as well, the oscillation waveform can not be seen as VCO turns off. Adjust the free run frequency at 76 kHz \pm 50 Hz.

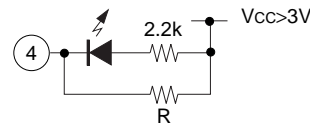
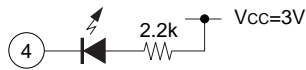


In this IC, tuner and MPX sections are directly connected. Therefore, free run frequency is not stable, being affected by noise except in reception mode. For free run adjustment, input signals from either RF or IF. (Input signal should be RF [Tuning frequency] or fo of the discriminator using IF (10.7 MHz) and input more than 60 dB μ .)

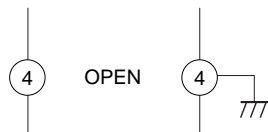
2) How to Deal with pin 4 After Adjustment.

With the use of a stereo indicator.

When Vcc is 3 V or more, insert a bypass resistance R to prevent LED malfunction.



Without the use of a stereo indicator.

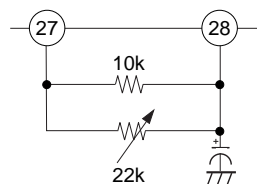


Turn pin 4 to open or connect to GND.

3) Control Resistor of VCO Oscillation Frequency

For the VCO control resistor of this iC, a carbon film resistor suffices.

For easier adjustment of temperature characteristics and VCO free run frequency, the following combination is recommended.



2. MPX circuit

1) MPX load resistance

When power supply voltage is over 3 V, change the MPX load resistor R6, R7 from 3.3 k Ω to 6.8 k Ω . In this case, the output level is increased by about 6 dB.

2) Time constant of de-emphasis

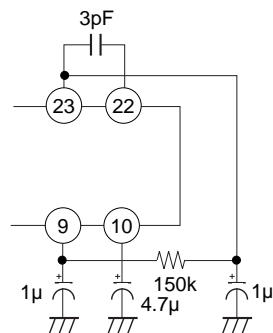
Refer to the following table as the time constant is determined at C13, C14, R6 and R7.

	3.3 k Ω	6.8 k Ω	R6, R7
50 μ s	0.015 μ F	0.0082 μ F	C13, C14
75 μ s	0.022 μ F	0.012 μ F	

3. AFC circuit

1) This IC has a built-in variable capacitances.

Change to the following circuit when designing J band, because the standard circuit is for W band.



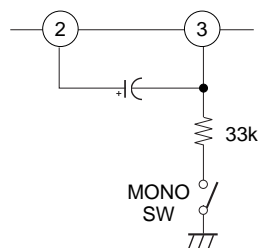
2) AFC pull-in range is expanded by increasing the capacitance of standard circuit C7 3 pF.

Adjust the value of capacitance according to the set specification.

4. Auto blend circuit

This IC has a built-in auto blend circuit and a MONO switch is not required as a rule. This circuit controls the separation in proportion to the signal level and reduces noise automatically for stereo reception below the mid electric field when the electric field strength reaches lower than about 40 dB μ . When the electric field strength turns below 10 to 15 dB μ , MONO operation is automatically activated.

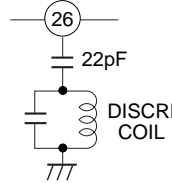
To switch MONO mode on externally, ground pin 3 with 33 k Ω .



5. FM discriminator

For FM detection, the quadrature detection system is adopted. As a phase shifter, a ceramic resonator (CF 3 discriminator) applies to achieve adjustment-free detection. Though the sensitivity and selectability will be slightly affected, the discriminator can be replaced by a coil as shown below. Combining CF2 (FMIF) and CF3 (PM discriminator) poses problems with the distortion factor when deviation with the IF band central frequency f_0 occurs. To this effect, use pairs of the same rank as indicated in the chart.

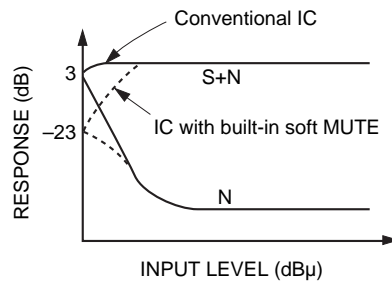
	f_0 of CF2 and CF3
A Red	10.70 MHz
B Blue	10.67 MHz
C Orange	10.73 MHz
D Black	10.64 MHz
E White	10.76 MHz



6. FM muting circuit

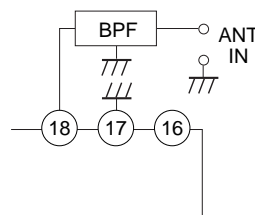
This IC has a built-in soft muting circuit.

As shown in the following I/O characteristics diagram, 23 dB (Typ.) muting is applied and noise level reduced during weak electric field and out of tune instances.



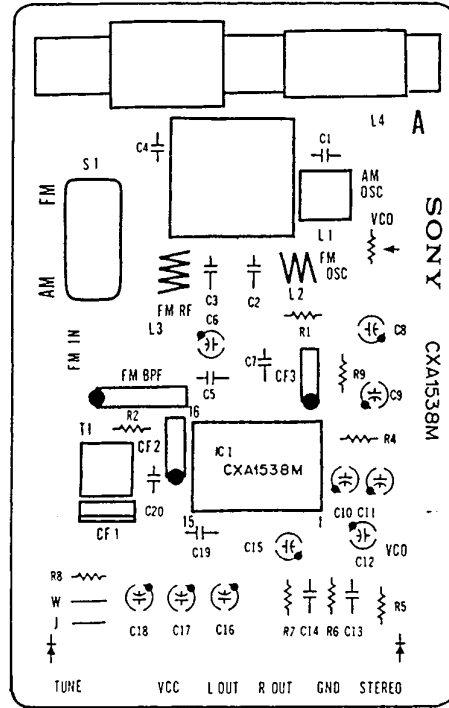
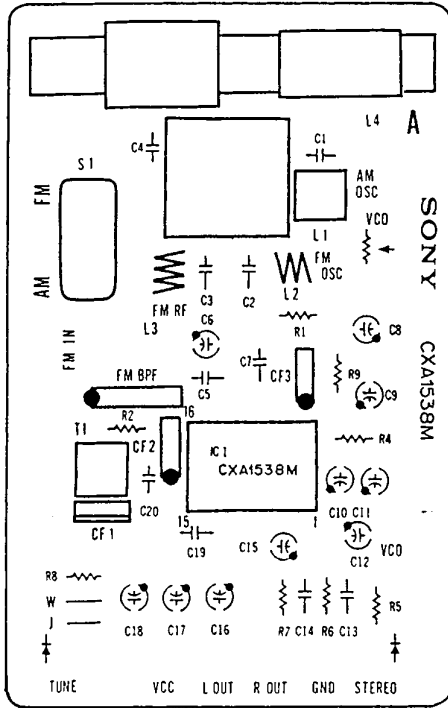
7. Notes on patterns

- 1) Positions of FM ANT and OSC coils
 Locate those at right angles to each others to avoid inductance M through coupling. Further, insert a pin 21 pattern between patterns of pins 22, 20 and coils.
- 2) Tuning circuit
 As the capacitances C1 to C4, L2 and L3 are the constants on the standard circuit board, check the constants when a new circuit board is used.
- 3) Grounding pins
 Pin 17 is a grounding pin for AM, FM and FE ; pin 11 for IF ; and pin 30 for MPX. Use as thick as possible a pattern since the grounding between ANT IN, BPF and pin 17 significantly stability, NF and characteristics affects.

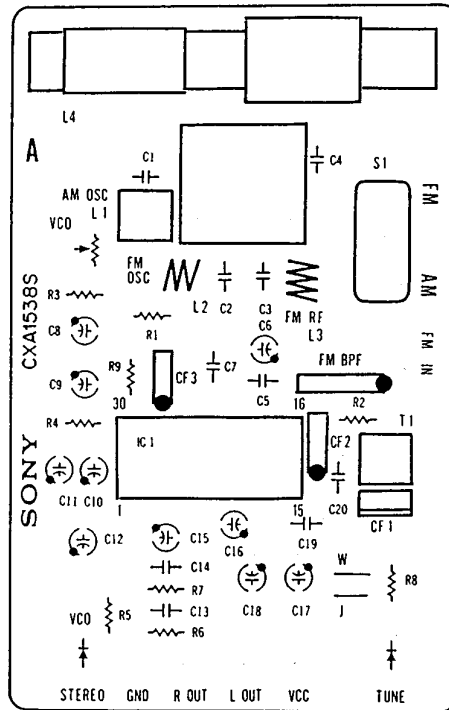
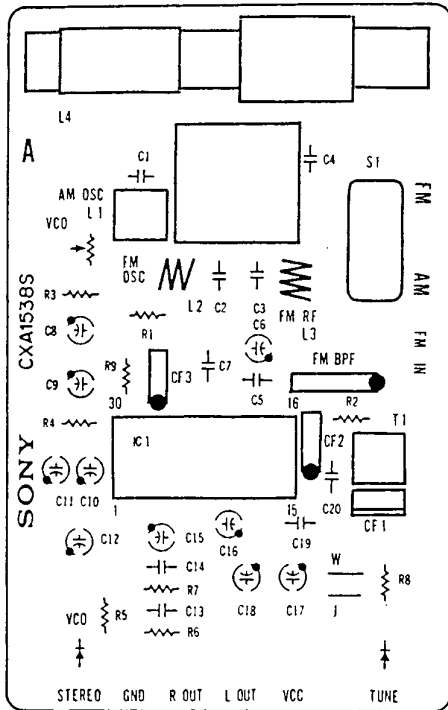


- 4) Ground bypass capacitors C5 (0.001 μ F) and C6 (10 μ F) connected to pin 21 as close as possible to pin 17.

CXA1538M



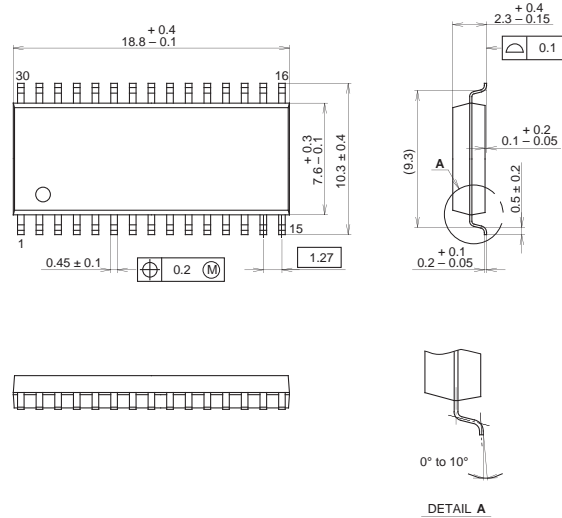
CXA1538S



Package Outline Unit : mm

CXA1538M

30PIN SOP(PLASTIC)

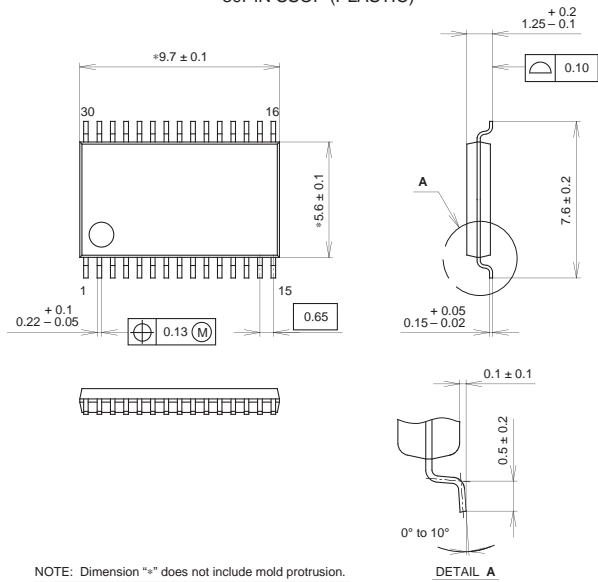


SONY CODE	SOP-30P-L03
EIAJ CODE	SOP030-P-0375
JEDEC CODE	

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g

CXA1538N

30PIN SSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

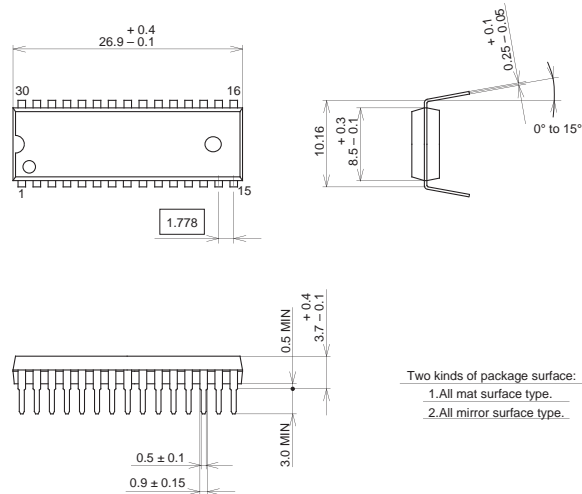
SONY CODE	SSOP-30P-L01
EIAJ CODE	SSOP030-P-0056
JEDEC CODE	

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

CXA1538S

30PIN SDIP (PLASTIC)



Two kinds of package surface:
 1. All mat surface type.
 2. All mirror surface type.

PACKAGE STRUCTURE

SONY CODE	SDIP-30P-01
EIAJ CODE	SDIP030-P-0400
JEDEC CODE	

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.8g

NOTE : PALLADIUM PLATING

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).