

# AN5392FBQ

Luminance and color difference drive/cutoff signal processor IC with I<sup>2</sup>C bus

## ■ Overview

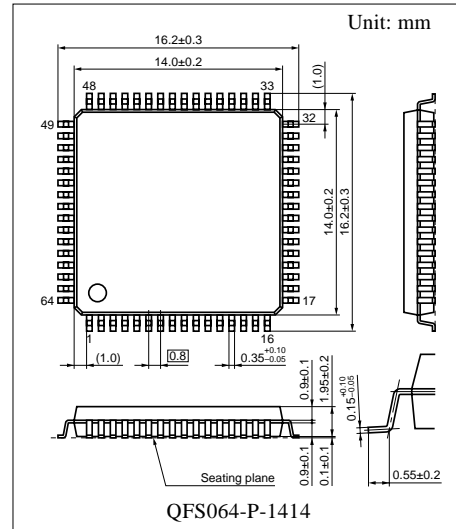
The AN5392FBQ is an RGB processor IC which converts the luminance and color difference signal into a primary color signal. This IC supports all kinds of input signal from hi-vision, wide, NTSC, PAL, VGA, etc. for maximum rationalization and high performance of the end products.

## ■ Features

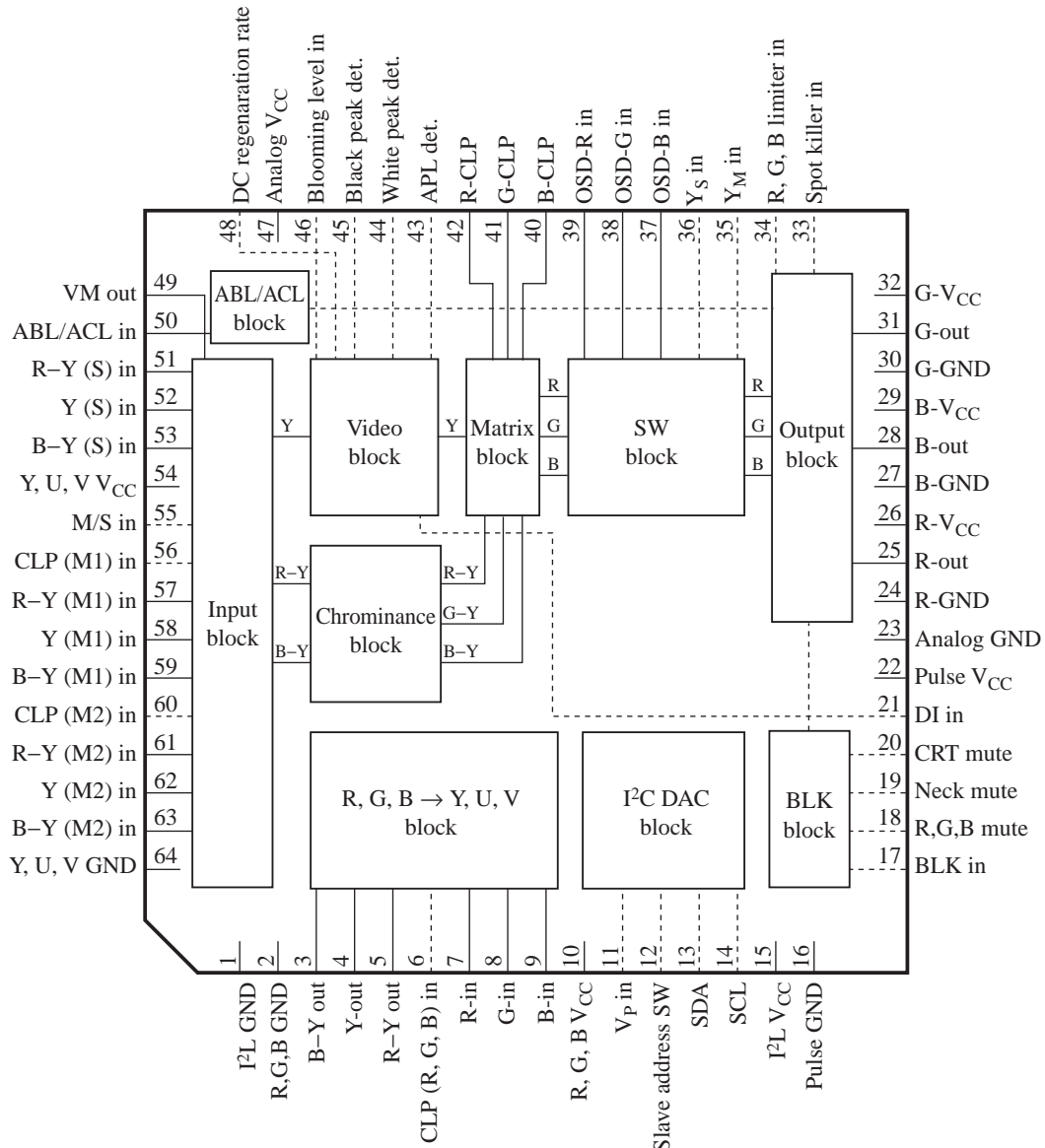
- A wider band signal processing (Y: 30 MHz/−3 dB, color difference: 15 MHz/−3 dB)
- High picture quality thanks to a large variety of built-in correction circuit for Y signal
- Y, C−Y signal conversion circuit built in for RGB signal for a personal computer
- Possible to mount in a high density thanks to SMD package

## ■ Applications

- Hi-vision TV, wide TV, projection TV, plasma display panel (PDP)



■ Block Diagram



### ■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	I <sup>2</sup> L GND	33	Spot killer input
2	R, G, B GND	34	R, G, B limiter input
3	B-Y output	35	Y <sub>M</sub> input
4	Y-output	36	Y <sub>S</sub> input
5	R-Y output	37	OSD-B input
6	CLP (R, G, B) input	38	OSD-G input
7	R-input	39	OSD-R input
8	G-input	40	B-CLP filter
9	B-input	41	G-CLP filter
10	R, G, B V <sub>CC</sub>	42	R-CLP filter
11	V <sub>P</sub> input	43	APL detection filter
12	Slave address SW	44	White peak detection filter
13	SDA	45	Black peak detection filter
14	SCL	46	Blooming level input
15	I <sup>2</sup> L V <sub>CC</sub>	47	Analog V <sub>CC</sub>
16	Pulse GND	48	DC regeneration rate
17	BLK input	49	VM output
18	R, G, B mute input	50	ABL/ACL input
19	Neck mute input	51	R-Y (S) input (Pr (S) input)
20	CRT mute input	52	Y (S) input
21	DI input	53	B-Y (S) input (Pb (S) input)
22	Pulse V <sub>CC</sub>	54	Y, U, V V <sub>CC</sub>
23	Analog GND	55	M/S input
24	R-GND	56	CLP (M1) input
25	R-output	57	R-Y (M1) input (Pr (M1) input)
26	R-V <sub>CC</sub>	58	Y (M1) input
27	B-GND	59	B-Y (M1) input (Pb (M1) input)
28	B-output	60	CLP (M2) input
29	B-V <sub>CC</sub>	61	R-Y (M2) input (Pr (M2) input)
30	G-GND	62	Y (M2) input
31	G-output	63	B-Y (M2) input (Pb (M2) input)
32	G-V <sub>CC</sub>	64	Y, U, V GND

### ■ Absolute Maximum Ratings

Parameter	Symbol		Rating	Unit
Supply voltage	$V_{CC}$	$V_{CC1}$	10.0	V
		$V_{CC2}$	5.6	
Supply current	$I_{CC}$	$I_{CC1}$	70.0	mA
		$I_{CC2}$	34.0	
Power dissipation *2	$P_D$		685	mW
Operating ambient temperature *1	$T_{opr}$		-20 to +70	°C
Storage temperature *1	$T_{stg}$		-55 to +150	°C

Note) \*1: Except for the operating ambient temperature and storage temperature, all ratings are for  $T_a = 25^\circ\text{C}$ .

\*2: The power dissipation  $P_D$  shown is for the independent IC without a heat sink in the free air at  $T_a = 70^\circ\text{C}$ .

### ■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	$V_{CC1}$	8.1 to 9.9	V
	$V_{CC2}$	4.5 to 5.5	

### ■ Electrical Characteristics at $V_{CC1} = 9\text{ V}$ , $V_{CC2} = 5\text{ V}$ , $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC characteristics						
Circuit current 1 *1	$I_{CC1}$	$V_{CC1} = 9\text{ V}$ , $V_{CC2} = 5\text{ V}$ No signal input	39	51	63	mA
Circuit current 2 *1	$I_{CC2}$	$V_{CC1} = 9\text{ V}$ , $V_{CC2} = 5\text{ V}$ No signal input	20	25	30	mA
Y-system						
Video voltage gain	$AY_G$	Input: Sine wave 0.2 V[p-p] $f = 1\text{ MHz}$ , contrast: max.	4.7	5.6	6.7	Times
Video voltage gain variation amount	$\Delta AY$	Ratio between R,G and B Drive: typ.	-2.5	0	+2.5	dB
Frequency characteristics	$f_Y$	Input: Sine wave 0.2 V[p-p] $f = 30\text{ MHz}$ , contrast: max.	-6	-3	+1	dB
Typical output pedestal	$DC_p$	Brightness: typ.	2.6	3.0	3.4	V
Brightness variable range	$V_{BR}$	Brightness: min. → max.	1.8	2.2	2.6	V
Contrast ratio	$A_{CON}$	Contrast: min. → max.	25	30	—	dB
APL detection voltage	$V_{APL}$	Input: Total white 0.7 V[0-p] APL detection pin 43 voltage	0.7	1.0	1.3	V
APL detection ratio	$\Delta_{APL}$	Input: Total white 0.7 V[0-p] → 0.35 V[0-p] APL detection pin 43 voltage ratio	0.46	0.54	0.66	Times

Note) \*1:  $I_{CC1}$  is a total amount of the current flowing through pin 10, pin 26, pin 29, pin 32, pin 47 and pin 54.

$I_{CC2}$  is a total amount of the current flowing through pin 15 and pin 33.

**■ Electrical Characteristics at  $V_{CC1} = 9\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
DC regeneration ratio 1	DC <sub>1</sub>	Input signal: APL 10% → 90%, APL det. pin 0 V	96	102	107	%
DC regeneration ratio 2	DC <sub>2</sub>	Input signal: APL 10% → 90%, DC regeneration SW/on, polarity: –	65	75	85	%
DC regeneration ratio 3	DC <sub>3</sub>	Input signal: APL 10% → 90%, DC regeneration SW: On, polarity: +	115	125	135	%
Output blooming level	V <sub>BL</sub>	Blooming DC = 3.8 V, pin 43: 0 V, brightness: max.	5.7	6.7	7.7	V
Output blooming level variation amount	ΔV <sub>BL</sub>	Blooming DC = 3.8 V → 4.2 V, pin 43: 0 V, brightness: max.	–1.18	–0.93	–0.68	V
White gradation correction 1 *2	Yγ <sub>1</sub>	Gain: max., level: typ. → max. White gradation SW: On	9.0	14	18.0	%
White gradation correction 2 *2	Yγ <sub>2</sub>	Gain: max., level: typ. → min. White gradation SW: On	–24	–18	–12	%
Black extension characteristics 1 *3	Y <sub>BL1</sub>	Output amplitude: 0 V[p-p] Level: typ., gain: min. → max.	–0.1	0	+0.1	V
Black extension characteristics 2 *3	Y <sub>BL2</sub>	Output amplitude: 1.0 V[0-p] Level: typ., gain: min. → max.	–0.49	–0.37	–0.25	V
Black extension characteristics 3 *3	Y <sub>BL3</sub>	Output amplitude: 2.2 V[0-p] Level: typ., gain: min. → max.	–0.1	0	+0.1	V
Black extension characteristics 4 *4	Y <sub>BL4</sub>	Black detection: Open → 3 V Level: typ., gain: typ.	–1.10	–0.82	–0.55	V
Black extension characteristics 5 *4	Y <sub>BL5</sub>	Black detection: Open → 3 V Level: typ., gain: max.	–2.00	–1.55	–1.00	V
Black extension characteristics 6 *4	Y <sub>BL6</sub>	Black detection: Open → 3 V Level: min. → max., gain: typ.	–0.48	–0.30	–0.12	V
White character correction 1 *2	V <sub>W1</sub>	Blooming DC adjustment Level: max., gain: min. → typ.	10.0	25.0	40.0	%
White character correction 2 *2	V <sub>W2</sub>	Blooming DC adjustment Level: min., gain: min. → max.	–9.3	0	9.3	%
White character correction off *2	W <sub>OFF</sub>	P <sub>R</sub> , P <sub>B</sub> input: +0.2 V[p-p] Level: max., gain: min. → max.	–0.2	0	+0.2	V
ABL off *5	V <sub>ABL1</sub>	ABL/ACL pin: 7.5 V Level: min., gain: min. → max.	–0.1	0	+0.1	V
ABL start 1 *5	V <sub>ABL2</sub>	ABL/ACL pin: 3 V Level: min. → max., gain: max.	0.28	0.39	0.50	V

Note) \*2: Control a blooming DC voltage (pin 46)

\*3: Black gradation SW: On

\*4: Black gradation SW: On, brightness: max.

\*5: ABL SW: On, brightness: max.

**■ Electrical Characteristics at  $V_{CC1} = 9\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
ABL start 2 <sup>*5</sup>	$V_{ABL3}$	ABL/ACL pin: 3 V Level: min., gain: min. → max.	-0.84	-0.64	-0.44	V
ABL gain 1 <sup>*5</sup>	$A_{ABL}$	ABL/ACL pin: 5 V → 3 V Level: typ., gain: max.	-0.48	-0.37	-0.26	V
ACL off <sup>*6</sup>	$A_{ACL1}$	ABL/ACL pin: 7.5 V Level: min., gain: min. → max.	-5	0	+5	%
ACL start 1 <sup>*6</sup>	$A_{ACL2}$	ABL/ACL pin: 3 V Level: min. → max., gain: typ.	10	20	30	%
ACL start 2 <sup>*6</sup>	$A_{ACL3}$	ABL/ACL pin: 3 V Level: min., gain: min. → typ.	-45	-35	-25	%
ACL gain 1 <sup>*6</sup>	$A_{ACL4}$	ABL/ACL pin: 5 V → 3 V Level: typ., gain: typ.	-34	-22	-10	%
Color difference-system						
Color difference voltage gain <sup>*7</sup>	$G_R$	Input: Sine wave 0.2 V[p-p] f = 1 MHz, R-Y in → R-out	9.5	11.4	13.7	Times
Color difference frequency characteristics <sup>*7</sup>	fc	Input: Sine wave 0.2 V[p-p] f = 10 MHz	-6	-3	+2	dB
B-Y axis gain adjusting range NTSC 1 <sup>*7</sup>	$G_{B-Y1}$	B-Y gain: min., brightness: max. Tint SW: NTSC	0.28	0.45	0.61	Times
B-Y axis gain adjusting range NTSC 2 <sup>*7</sup>	$G_{B-Y2}$	B-Y gain: max., brightness: max. Tint SW: NTSC	1.00	1.25	1.60	Times
B-Y axis gain adjusting range HD 1 <sup>*7</sup>	$G_{B-Y3}$	B-Y gain: min., brightness: max. Tint SW: HD	0.50	0.78	1.18	Times
B-Y axis gain adjusting range HD 2 <sup>*7</sup>	$G_{B-Y4}$	B-Y gain: max., brightness: max. Tint SW: HD	1.18	2.00	2.80	Times
Tint variable range	$T_C$	Tint: min. → max. B-Y gain, drive RB: Adjustment	± 33	± 48	± 68	°
Color control <sup>*7</sup>	$C_{CON}$	Color: typ. → max. Contrast: typ.	3	6	9	dB
Color residue <sup>*7</sup>	$C_{MIN}$	Color: min., B-Y gain: max. Contrast: max.	-50	0	+50	mV[p-p]
R-Y angle adjusting range <sup>*7</sup>	$\theta_R$	R-Y axis: min. → max.	10	17	24	°

Note) \*5: ABL SW: On, brightness: max.

\*6: ACL SW: On

\*7: Adjust tint, drive R, B.

**■ Electrical Characteristics at  $V_{CC1} = 9\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color difference-system (continued)						
Matrix ratio (G–Y/R–Y) HD *7	M1	Tint SW: HD G–Y matrix: HD	0.23	0.30	0.35	Times
Matrix ratio (G–Y/R–Y) NTSC 1 *7	M2	Tint SW: NTSC G–Y matrix: NTSC 1	0.38	0.51	0.58	Times
Matrix ratio (G–Y/R–Y) NTSC 2 *7	M3	Tint SW: NTSC G–Y matrix: NTSC 2	0.26	0.34	0.40	Times
Matrix ratio (G–Y/R–Y) NTSC 3 *7	M4	Tint SW: NTSC G–Y matrix: NTSC 3	0.26	0.34	0.40	Times
Matrix ratio (G–Y/B–Y) HD *7	M5	Tint SW: HD G–Y matrix: HD	0.07	0.10	0.13	Times
Matrix ratio (G–Y/B–Y) NTSC 1 *7	M6	Tint SW: NTSC G–Y matrix: NTSC 1	0.15	0.19	0.23	Times
Matrix ratio (G–Y/B–Y) NTSC 2 *7	M7	Tint SW: NTSC G–Y matrix: NTSC 2	0.22	0.28	0.34	Times
Matrix ratio (G–Y/B–Y) NTSC 3 *7	M8	Tint SW: NTSC G–Y matrix: NTSC 3	0.13	0.17	0.21	Times
OSD						
$Y_S$ input threshold voltage *8	$Y_{STH}$	Pin 36 > 2.1 V: OSD Pin 36 < 0.9 V: Main & sub	0.9	1.5	2.1	V
M/S input threshold voltage *8	M/S <sub>TH</sub>	Pin 55 > 2.1 V: Sub Pin 55 < 0.9 V: Main (M1, M2)	0.9	1.5	2.1	V
$Y_M$ input threshold voltage *8	$Y_{MTH}$	Pin 35 > 2.1 V: Half tone Pin 35 < 0.9 V: Main & sub	0.9	1.5	2.1	V
CLP input threshold voltage	CLP <sub>TH</sub>	Pin 56, 60 (main, sub, OSD) Pin 6 (RGB)	0.9	1.5	2.1	V
Pulse width can be clamped	$W_M$	Pin 56, 60 (main, sub, OSD) Pin 6 (RGB)	0.8	—	—	μs
OSD gain	$G_{OSD}$	Input: Sine wave 0.2 V[p-p] f = 1 MHz, $Y_S$ pin: 5 V	5.0	6.0	7.2	Times
OSD frequency characteristics	$f_{OSD}$	Input: Sine wave 0.2 V[p-p] f = 30 MHz, $Y_S$ pin: 5 V	–7	–3	+1	dB
OSD contrast ratio 1	OSD <sub>C1</sub>	Contrast: max. → typ. $Y_S$ pin: 5 V	–3	–1	+1	dB
OSD contrast ratio 2	OSD <sub>C2</sub>	Contrast: typ. → min. $Y_S$ pin: 5 V	–16	–11	–7	dB

Note) \*7: Adjust tint, drive R, B

\*8: SW priority:  $Y_S > M/S > M1/M2$  (I<sup>2</sup>C),  $Y_S$ :  $Y_M$  is valid at low.

**■ Electrical Characteristics at  $V_{CC1} = 9\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y, U, V						
Y, U, V frequency characteristics	$f_{YUV}$	Input: Sine wave 0.2 V[p-p], $f = 30\text{ MHz}$	-6	-2	+2	dB
Y, U, V output pedestal	$DC_{YUV}$		2.6	3.0	3.4	V
Y, U, V output pedestal potential difference	$\Delta V_{YUV}$		-0.3	0	+0.3	V
Y, U, V matrix ratio 1	$M_{YUV1}$	R-in: Sine wave 0.2 V[p-p], $f = 1\text{ MHz} \rightarrow Y\text{-out}$	0.24	0.3	0.36	Times
Y, U, V matrix ratio 2	$M_{YUV2}$	G-in: Sine wave 0.2 V[p-p], $f = 1\text{ MHz} \rightarrow Y\text{-out}$	0.47	0.59	0.71	Times
Y, U, V matrix ratio 3	$M_{YUV3}$	B-in: Sine wave 0.2 V[p-p], $f = 1\text{ MHz} \rightarrow Y\text{-out}$	0.08	0.11	0.14	Times
Cutoff drive						
BLK input threshold voltage <sup>*9</sup>	$BLK_{TH}$	BLK SW: On	0.9	1.5	2.1	V
Neck mute input threshold voltage <sup>*9</sup>	$N_{TH}$		0.9	1.5	2.1	V
CRT mute input threshold voltage <sup>*9</sup>	$C_{TH}$		0.9	1.5	2.1	V
RGB mute input threshold voltage <sup>*9</sup>	$M_{TH}$		0.9	1.5	2.1	V
DI input threshold voltage	$D_{TH}$	Pin 21 > 2.1 V: Detection inhibited Pin 21 < 0.9 V: Normal	0.9	1.5	2.1	V
Cutoff variable range (R, B) <sup>*10</sup>	$\Delta L_{RB}$	Cutoff R, B: min. $\rightarrow$ max. Cutoff SW: min. $\rightarrow$ max.	1.6	2.0	2.4	V
Cutoff variable range (G)	$\Delta L_G$	Cutoff G: min. $\rightarrow$ max.	0.7	1.0	1.3	V
Drive variable range (R, B)	$\Delta G_D$	Drive R, B: min. $\rightarrow$ max.	9.0	11.5	14.0	dB
R, G, B pedestal potential difference	$\Delta V_P$	Cutoff: typ., brightness: typ.	-0.3	0	+0.3	V
Output blanking level	BLK	BLK SW: On, BLK (pin 17): 5 V	1.1	1.5	1.9	V
I <sup>2</sup> C · DAC						
SCL · SDA input threshold voltage	$V_{TH}$	$V_{CC2} = 5\text{ V}$	1.5	—	3.0	V
Sink ability at ACK	$V_{ACK}$	$I = 3\text{ mA}$ , when pull-up is 1.6 k $\Omega$	—	—	0.4	V
Maximum clock frequency		$V_{CC2} = 5\text{ V}$	100	—	—	kHz
Slave address changeover threshold voltage	$AD_{TH}$	$V_{CC2} = 5\text{ V}$	0.7	2.2	4.0	V
$V_P$ input threshold voltage	$V_{PTH}$	$V_{CC2} = 5\text{ V}$	0.9	1.5	2.1	V

Note) \*9: Priority: RGB mute, CRT mute, neck mute > single color adjustment (I<sup>2</sup>C) > BLK SW (I<sup>2</sup>C) > BLK pulse

\*10: Drive R, B adjustment



■ Electrical Characteristics at  $V_{CC1} = 9\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Y system</b>						
Y (M1) input dynamic range	$D_{YIN1}$	$V_{CC1} = 9\text{ V}$ , $V_{46} = 1.5\text{ V}$ Contrast: typ.	—	1.4	—	V[p-p]
Y (M2) input dynamic range	$D_{YIN2}$	$V_{CC1} = 9\text{ V}$ , $V_{46} = 1.5\text{ V}$ Contrast: typ.	—	1.4	—	V[p-p]
Y (sub) input dynamic range	$D_{YIN3}$	$V_{CC1} = 9\text{ V}$ , $V_{46} = 1.5\text{ V}$ Contrast: typ.	—	1.4	—	V[p-p]
R, G, B output dynamic range	$D_{OUT}$	$V_{CC1} = 9\text{ V}$ for pedestal 3 V	—	4.5	—	V[p-p]
APL detection stop	$APL_S$	BLK, DI = 5 V	—	0	—	V
Black extension inhibition delay	$t_{HBLACK}$	BLK, delay from DI input	—	60	—	ns
DC regeneration ratio 4	DC4	Input signal: APL10% → 90% DC regeneration pin: Open	—	100	—	%
S/N	S/N	Band width 20 MHz	—	-56	—	dB
Y output amplitude dependence on ambient temperature	$Y/\Delta T$	-20°C to +70°C	—	±2	—	%
Y signal delay time	$t_{dY}$	f = 5 MHz	—	15	—	ns
VM out gain	$A_{VM}$	Input: Sine wave 0.2 V[p-p], f = 1 MHz	—	1.0	—	Times
VM out pedestal level	$DC_{VM}$		—	3.9	—	V
Pedestal level fluctuation at M/S changeover	$\Delta V_{PM/S}$	At high speed switching within 1H period	—	±50	—	mV
<b>Color difference system</b>						
Pr, Pb input (M1) dynamic range	$D_{CIN1}$	Tint SW: HD mode	—	±0.7	—	V[p-p]
Pr, Pb input (M2) dynamic range	$D_{CIN2}$	Tint SW: HD mode	—	±0.7	—	V[p-p]
Pr, Pb input (sub) dynamic range	$D_{CIN3}$	Tint SW: HD mode	—	±0.7	—	V[p-p]
B-Y input (M1) dynamic range	$D_{PB1N}$	Tint SW: NTSC mode	—	±1.3	—	V[p-p]
B-Y input (M2) dynamic range	$D_{PB2N}$	Tint SW: NTSC mode	—	±1.3	—	V[p-p]
B-Y input (sub) dynamic range	$D_{PB3N}$	Tint SW: NTSC mode	—	±1.3	—	V[p-p]
R-Y angle adjusting range 2	$\theta_{R2}$	R-Y axis: min.	—	0	—	°
Color difference contrast ratio	$C_{CONT}$	Contrast: min. → max.	—	29	—	dB

■ Electrical Characteristics at  $V_{CC1} = 9\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color difference system (continued)						
Tint dependence on ambient temperature	TC/T	$-20^\circ\text{C}$ to $+70^\circ\text{C}$	—	$\pm 2$	—	$^\circ$
(C–Y)/Y ratio HD	C/Y <sub>HD</sub>	Tint SW: HD mode Contrast: max., color: typ.	—	1.3	—	Times
(C–Y)/Y ratio NTSC	C/Y <sub>NTSC</sub>	Tint SW: NTSC mode Contrast: max., color: typ.	—	1.0	—	Times
Color difference signal delay time	t <sub>dC</sub>	f = 5 MHz	—	30	—	ns
Color difference output amplitude ambient temperature dependence	C/ $\Delta$ T	$-20^\circ\text{C}$ to $+70^\circ\text{C}$	—	$\pm 4$	—	%
Cross-talk						
Y cross-talk Y (M1 $\leftrightarrow$ M2)	CT <sub>1</sub>	f = 10 MHz	—	–52	—	dB
Y cross-talk (M1, M2 $\leftrightarrow$ Sub)	CT <sub>2</sub>	f = 10 MHz	—	–54	—	dB
Y cross-talk (M1, M2, sub $\leftrightarrow$ OSD)	CT <sub>3</sub>	f = 10 MHz	—	–53	—	dB
Color difference cross-talk (M1 $\leftrightarrow$ M2)	CT <sub>4</sub>	f = 10 MHz	—	–52	—	dB
Color difference cross-talk Pr, Pb (M1, M2 $\leftrightarrow$ Sub)	CT <sub>5</sub>	f = 10 MHz	—	–54	—	dB
Color difference cross-talk (M1, M2, sub $\leftrightarrow$ OSD)	CT <sub>6</sub>	f = 10 MHz	—	–52	—	dB
Color difference cross-talk (OSD $\leftrightarrow$ M1, M2, sub)	CT <sub>7</sub>	f = 10 MHz	—	–47	—	dB
Cross-talk between OSDs	CT <sub>8</sub>	f = 10 MHz	—	–42	—	dB
OSD						
OSD signal delay	t <sub>dOSD</sub>	f = 5 MHz	—	10	—	ns
Y <sub>S</sub> rise delay	t <sub>RYs</sub>		—	19	—	ns
Y <sub>S</sub> fall delay	t <sub>FYS</sub>		—	18	—	ns
Y <sub>M</sub> rise delay	t <sub>RYM</sub>		—	20	—	ns
Y <sub>M</sub> fall delay	t <sub>FYM</sub>		—	15	—	ns
M/S rise delay	t <sub>RM/S</sub>		—	24	—	ns
M/S fall delay	t <sub>FM/S</sub>		—	25	—	ns
Pedestal fluctuation at Y <sub>S</sub> changeover	$\Delta V_{PYS}$	Y <sub>S</sub> : Variation amount from low to high	—	–60	—	mV
Pedestal fluctuation at Y <sub>M</sub> changeover	$\Delta V_{PYM}$	Y <sub>M</sub> : Variation amount from low to high	—	–10	—	mV

■ Electrical Characteristics at  $V_{CC1} = 9\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OSD (continued)						
OSD input dynamic range	$D_{OSD}$		—	1.4	—	V[p-p]
OSD output amplitude ambient temperature dependency	$\frac{OSD}{\Delta T}$	$-20^\circ\text{C}$ to $+70^\circ\text{C}$	—	$\pm 2$	—	%
Cutoff drive						
Drive variable range (G)	$\Delta G_D$	Drive G: min. → max.	—	2.6	—	dB
Blanking delay	$t_{dBLK1}$	BLK → BLK output	—	40	—	ns
Pedestal fluctuation to contrast variation	$\Delta V_{PCONT}$	Contrast: min. → max.	—	0	—	mV
Pedestal fluctuation to color variation	$\Delta V_{PCOLOR}$	Contrast: min. → max.	—	0	—	mV
Pedestal fluctuation to tint variation	$\Delta V_{PTINT}$		—	0	—	mV
Output pedestal potential ambient temperature dependency	$\frac{\Delta V_P}{\Delta T}$	$-20^\circ\text{C}$ to $+70^\circ\text{C}$	—	-1.2	—	mV/ $^\circ\text{C}$
Spot killer operation	$V_{SP}$	Lower 9 V-system $V_{CC}$ , pin 33: C = 10 $\mu\text{F}$	—	7.8	—	V
I <sup>2</sup> C DAC						
4 · 5 · 6 DAC DNLE	L1	1LSB = {data (max.) – data (min.)}/ ( $2^N - 1$ )	0.1	1.0	1.9	$\frac{LSB}{Step}$
8-bit DAC DNLE (excluding 40, 80, C0)	L2	1LSB = {data (max.) – data (min.)}/ ( $2^N - 1$ )	0.1	1.0	1.9	$\frac{LSB}{Step}$
8-bit DAC DNLE (only for 40, 80, C0)	L3	1LSB = {data (max.) – data (min.)}/ ( $2^N - 1$ )	-1.0	1.0	+2.0	$\frac{LSB}{Step}$
7-bit DAC DNLE (excluding 40)	L4	1LSB = {data (max.) – data (min.)}/ ( $2^N - 1$ )	0.1	1.0	1.9	$\frac{LSB}{Step}$
7-bit DAC DNLE (only for 40)	L5	1LSB = {data (max.) – data (min.)}/ ( $2^N - 1$ )	-1.0	1.0	+2.0	$\frac{LSB}{Step}$
Y, U, V						
Y, U, V signal delay	$t_{dYUV}$	R, G, B in → Y, C–Y out, f = 5 MHz	—	5	—	ns
Y, U, V input dynamic range	$D_{YUV}$		—	1.4	—	V
Y, U, V matrix ratio 4	$M_{YUV4}$	R-in: Sine wave 0.2 V[p-p], f = 1 MHz → R-Y out	—	0.7	—	Times
Y, U, V matrix ratio 5	$M_{YUV5}$	R-in: Sine wave 0.2 V[p-p], f = 1 MHz → B-Y out	—	-0.3	—	Times
Y, U, V matrix ratio 6	$M_{YUV6}$	G-in: Sine wave 0.2 V[p-p], f = 1 MHz → R-Y out	—	-0.59	—	Times
Y, U, V matrix ratio 7	$M_{YUV7}$	G-in: Sine wave 0.2 V[p-p], f = 1 MHz → B-Y out	—	-0.59	—	Times

■ Electrical Characteristics at  $V_{CC1} = 9\text{ V}$ ,  $V_{CC2} = 5\text{ V}$ ,  $T_a = 25^\circ\text{C}$  (continued)

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y, U, V (continued)						
Y, U, V matrix ratio 8	$M_{YUV8}$	B-in: Sine wave 0.2 V[p-p], f = 1 MHz → R-Y out	—	-0.11	—	Times
Y, U, V matrix ratio 9	$M_{YUV9}$	B-in: Sine wave 0.2 V[p-p], f = 1 MHz → B-Y out	—	0.89	—	Times

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description
1 2		<p>GND:</p> <ul style="list-style-type: none"> <li>GND pin</li> <li>Pin 1: I<sup>2</sup>L GND pin</li> <li>Pin 2: Y,U,V → R,G,B conversion circuit GND pin</li> <li>Pin 16: Pulse-system GND pin</li> <li>Pin 23: Main signal-system GND pin</li> <li>Pin 24: R signal output circuit GND pin</li> <li>Pin 27: B signal output circuit GND pin</li> <li>Pin 30: G signal output circuit GND pin</li> <li>Pin 64: Input circuit GND pin</li> </ul>
3 4 5		<p>Y, R-Y, B-Y out:</p> <p>Y, R-Y, B-Y output pin for R, G, B → Y, U, V conversion circuit</p> <ul style="list-style-type: none"> <li>Pin 3: B-Y output pin</li> <li>Pin 4: Y output pin</li> <li>Pin 5: R-Y output pin</li> <li>Output dynamic range: 1.5 V to 7.5 V</li> <li>Output pedestal is about 3 V.</li> <li>Recommended use range: -4 mA to +4 mA</li> </ul>
6		<p>CLP (R, G, B) in:</p> <p>Clamp pulse input pin for R, G, B → Y, U, V conversion circuit</p> <ul style="list-style-type: none"> <li>Input threshold voltage: 1.5 V (to clamp at high)</li> <li>Clamps the signal inputted from the next pin Pin 7, pin 8, pin 9</li> <li>Recommended clamp pulse width NTSC: 2.5 μs HD: 1.0 μs</li> <li>Recommended use range: 0 V to 5 V</li> </ul>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
<p>7 8 9</p>		<p>R, G, B in: R, G, B input pin for R, G, B → Y, U, V conversion circuit</p> <ul style="list-style-type: none"> <li>• Pin 7: R signal input pin</li> <li>• Pin 8: G signal input pin</li> <li>• Pin 9: B signal input pin</li> <li>• Input 0.7 V[0-p] for both HD and NTSC.</li> <li>• Drive this pin with a low impedance. High impedance is likely to cause variation on white balance with user volume.</li> <li>• Clamps the input signal with pin 6 clamp pulse</li> <li>• Recommended use range: Do not apply DC voltage from outside.</li> </ul>
<p>10</p>		<p>V<sub>CC</sub> 9 V: Signal-system power supply pin</p> <ul style="list-style-type: none"> <li>• Pin 10: Power supply pin for Y, U, V → R, G, B conversion circuit (pair with Pin 2 GND)</li> <li>• Pin 26: R signal output circuit power supply pin (pair with pin 24 GND)</li> <li>• Pin 29: B signal output circuit power supply pin (pair with pin 27 GND)</li> <li>• Pin 32: G signal output circuit power supply pin (pair with pin 30 GND)</li> <li>• Pin 47: Main power supply pin (pair with pin 23 GND)</li> <li>• Pin 54: Input circuit power supply pin (pair with pin 64 GND)</li> <li>• Apply 9 V for use.</li> <li>• Recommended use range: 8.1 V to 9.9 V</li> </ul>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
11		<p><math>V_P</math> in: V-latch DAC <math>V_P</math> pulse input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 1.5 V</li> <li>• High input: <math>V_{11} &gt; 2.1</math> V</li> <li>• Low input: <math>V_{11} &gt; 0.9</math> V</li> <li>• The data for color, tint, brightness and contrast are rewritten at the timing of high-to-low-going <math>V_P</math> pulse in DAC SW13-6 (V-latch mode). In the through mode, the data are rewritten at the timing of the data sent, regardless of <math>V_P</math> pulse.</li> <li>• This pin does not affect a blanking operation.</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>
12		<p>Slave address SW: Slave address changeover pin for this IC</p> <ul style="list-style-type: none"> <li>• <math>V_{12} = 5</math> V: Slave address 86</li> <li>• <math>V_{12} = 0</math> V: Slave address 84</li> <li>• Set a slave address carefully so as not to overlap with the other ICs in the same set.</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>
13		<p>SDA: I<sup>2</sup>C bus data input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 2 V</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>
14		<p>SCL: I<sup>2</sup>C clock input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 2 V</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>
15		<p><math>V_{CC} 5</math> V: Power supply pin for I<sup>2</sup>L and pulse-system</p> <ul style="list-style-type: none"> <li>• Pin 15: I<sup>2</sup>L power supply pin (pair with pin 1 GND)</li> <li>• Pin 22: Pulse-system power supply pin (pair with pin 16 GND)</li> <li>• Apply 5 V for use.</li> <li>• Recommended use range: 4.5 V to 5.5 V</li> </ul>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
16	Refer to pin 1	Refer to pin 1
17		<p>BLK in:</p> <p>BLK input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 1.5 V</li> <li>• High-level input: <math>V_{17} \geq 2.1 \text{ V}</math></li> <li>• Low-level input: <math>V_{17} \leq 0.9 \text{ V}</math></li> <li>• Gives BLK to R, G, B output at input = high</li> <li>• Inhibits black gradation correction, white gradation correction and APL detection (DC transfer amount correction) at input = high.</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>
18 19 20		<p>R, G, B mute, neck mute, CRT mute:</p> <p>Input pin for R, G, B mute, neck mute, CRT mute</p> <ul style="list-style-type: none"> <li>• Pin 18: R, G, B mute</li> <li>• Pin 19: Neck mute</li> <li>• Pin 20: CRT mute</li> <li>• Input threshold voltage: 1.5 V</li> <li>• High-level input: <math>V_{18,19,20} \geq 2.1 \text{ V}</math></li> <li>• Low-level input: <math>V_{18,19,20} \leq 0.9 \text{ V}</math></li> <li>• If input is high, R, G and B output are forcibly given BLK. And as pin 18, pin 19 are ORed, BLK is given whenever any of those pins are given high level. At this time, BLK in (pin 17), BLK-SW (I<sup>2</sup>C) and single color adjustment SW (I<sup>2</sup>C) become invalid.</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>
21		<p>DI in:</p> <p>DI input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 1.5 V</li> <li>• High-level input: <math>V_{21} \geq 2.1 \text{ V}</math></li> <li>• Low-level input: <math>V_{21} \leq 0.9 \text{ V}</math></li> <li>• Inhibiting black gradation correction, white gradation correction and APL detection (DC transmission amount correction) at input = high.</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>
22	Refer to pin 15	Refer to pin 15
23	Refer to pin 1	Refer to pin 1
24	Refer to pin 1	Refer to pin 1

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
25		<p>R, G, B out: R, G, B output pin</p> <ul style="list-style-type: none"> <li>• Pin 25: R output pin</li> <li>• Pin 28: B output pin</li> <li>• Pin 31: G output pin</li> <li>• Output dynamic range: 1.5 V to 7.5 V</li> <li>• Use output pedestal typ. value of approx. 3 V.</li> <li>• Recommended use range: -4 mA to +4 mA</li> </ul>
26	Refer to pin 10	Refer to pin 10
27	Refer to pin 1	Refer to pin 1
28	Refer to pin 25	Refer to pin 25
29	Refer to pin 10	Refer to pin 10
30	Refer to pin 1	Refer to pin 1
31	Refer to pin 25	Refer to pin 25
32	Refer to pin 10	Refer to pin 10
33		<p>Spot killer in: Spot killer pin</p> <ul style="list-style-type: none"> <li>• Use this pin to discharge electricity on CRT swiftly when the set is turned off.</li> <li>• This pin raises DC voltage of R, G, B output pins (pin 25, pin 28, pin 31) when G output <math>V_{CC}</math> 9 V (pin 32) is lowered.</li> </ul>
34		<p>R, G, B limiter in: R, G, B output upper limiter pin</p> <ul style="list-style-type: none"> <li>• Limits R, G, B output pin voltage (pin 25, pin 28, pin 31) so as not to become higher than pin 34 voltage plus <math>1 V_{BE}</math>.</li> <li>• Recommended use range: 3 V to 9 V</li> </ul>
35		<p><math>Y_M</math> in: Half tone switching signal input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 1.5 V             <ol style="list-style-type: none"> <li>1) <math>2.1 V &lt; V_{35}</math> Lowers the signal amplitude inputted from M1, M2 and sub by 9 dB.</li> <li>2) <math>V_{35} &lt; 0.9 V</math> Normal</li> </ol> </li> <li>• Priority order of signal switching <math>M1/M2 (I^2C SW) &lt; M/S &lt; Y_M &lt; Y_S</math></li> <li>• Recommended use range: 0 V to 5 V</li> </ul>



■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
36		<p><math>Y_S</math> in:</p> <p>OSD signal switching signal input pin</p> <ul style="list-style-type: none"> <li>Input threshold voltage: 1.5 V                             <ol style="list-style-type: none"> <li><math>2.1\text{ V} &lt; V_{36}</math> Outputs OSD signal inputted from pin 37, pin 38, pin 39.</li> <li><math>V_{36} &lt; 0.9\text{ V}</math> Normal</li> </ol> </li> <li>Signal switching priority order <math>M1/M2 (I^2C\ SW) &lt; M/S &lt; Y_M &lt; Y_S</math></li> <li>Recommended use range: 0 V to 5 V</li> </ul>
37 38 39		<p>OSD in:</p> <p>OSD signal input pin for analog signal</p> <ul style="list-style-type: none"> <li>Pin 37: B signal input pin</li> <li>Pin 38: G signal input pin</li> <li>Pin 39: R signal input pin</li> <li>Input signal typ. is 0.7 V [0-p] from black to white level.</li> <li>Drive with a low impedance.</li> <li>Clamps the input signal with the clamp pulse of the following pins:                             <ul style="list-style-type: none"> <li>Pin 56, I<sup>2</sup>C bus M1/M2 switch: M1</li> <li>Pin 60, I<sup>2</sup>C bus M1/M2 switch: M2</li> </ul> </li> <li>Recommended use range:                             <ul style="list-style-type: none"> <li>Do not apply DC voltage from outside.</li> </ul> </li> </ul>
40 41 42		<p>B, G, R CLP:</p> <p>Pin to clamp the main signal with the voltage proportioned to bright data.</p> <ul style="list-style-type: none"> <li>Pin 40: B signal clamp pin</li> <li>Pin 41: G signal clamp pin</li> <li>Pin 42: R signal clamp pin</li> <li>Shorten the distance from the pin to the external capacitor.</li> <li>Recommended use range: 0 V to 5 V (Do not apply the DC voltage from outside.)</li> </ul>
43		<p>APL det.:</p> <p>Main signal APL detection pin</p> <ul style="list-style-type: none"> <li>Output the voltage in proportion to the APL of main signal</li> <li>Fit an RC filter to this pin.                             <ul style="list-style-type: none"> <li>R: adjusts detection sensitivity</li> <li>C: adjusts tracking characteristics</li> </ul> </li> <li>Recommended use range: 0 V to 3 V</li> </ul>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
44		<p><b>White peak det.:</b>                  Detects the brightest level of main signal</p> <ul style="list-style-type: none"> <li>• Fit an external RC filter between this pin and V<sub>CC</sub></li> <li>• Carrying out white gradation correction and blooming control with this detection voltage</li> </ul> <p>R: Adjusts detection sensitivity                  C: Adjusts tracking characteristics</p> <ul style="list-style-type: none"> <li>• Recommended use range: 0 V to 9 V</li> </ul>
45		<p><b>Black peak det.:</b>                  Detects the darkest level of main signal</p> <ul style="list-style-type: none"> <li>• Fit an external RC filter</li> <li>• Carries out black gradation correction with this detected voltage</li> </ul> <p>R: Adjusts detection sensitivity                  C: Adjusts tracking characteristics</p> <ul style="list-style-type: none"> <li>• Recommended use range: 0 V to 9 V</li> </ul>
46		<p><b>Blooming level in:</b>                  Input pin to determine a blooming level</p> <p>• Recommended use range: 1.5 V to 5 V</p>
47	Refer to pin 10	Refer to pin 10

Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
48		<p>DC regeneration ratio:</p> <p>Pin to determine DC regeneration ratio</p> <ul style="list-style-type: none"> <li>Adjusting DC regeneration ratio with the resistor to be connected between this pin and GND</li> <li>DC regeneration ratio comes closer to 100% when R is raised.</li> <li>Recommended use range: 0 μA to -200 μA</li> </ul>
49		<p>VM out:</p> <p>VM output pin</p> <ul style="list-style-type: none"> <li>Output dynamic range: 1.5 V to 7.5 V</li> <li>Use output pedestal typ. value of approx. 3 V</li> <li>Recommended use range: -4 mA to +4 mA</li> </ul>
50		<p>ABL/ACL in:</p> <p>Control voltage input pin for ABL/ACL</p> <ul style="list-style-type: none"> <li>Apply the voltage inversely proportioned to CRT screen brightness</li> <li>Operating range is 7 V to 2 V</li> <li>Possible to control contrast and brightness in inverse proportion to the applied voltage (controlling main signal and OSD signal)</li> <li>Recommended use range: 0 V to 9 V</li> </ul>
51		<p>R-Y (S) in, B-Y (S) in:</p> <p>Sub signal R-Y, B-Y input pin</p> <ul style="list-style-type: none"> <li>Pin 51: R-Y (S) signal input pin</li> <li>Pin 53: B-Y (S) signal input pin</li> <li>Input ±0.35 V for both HD and NTSC.</li> <li>Drive this pin with a low impedance. High impedance is likely to cause variation of white balance with the user volume.</li> <li>Clamps the input signal with the clamp pulse of the following pins:                     <ul style="list-style-type: none"> <li>Pin 56, I<sup>2</sup>C bus M1/M2 switch: M1</li> <li>Pin 60, I<sup>2</sup>C bus M1/M2 switch: M2</li> </ul> </li> <li>Recommended use range:                     <ul style="list-style-type: none"> <li>Do not apply DC voltage from outside.</li> </ul> </li> </ul>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
52		<p>Y (S) in: Sub signal Y input pin</p> <ul style="list-style-type: none"> <li>• Input 0.7 V[0-p] (B-W) for both HD and NTSC.</li> <li>• Drive this pin with a low impedance. High impedance is likely to cause variation of white balance with the user volume.</li> <li>• Clamps the input signal with the clamp pulse of the following pins: Pin 56, I<sup>2</sup>C bus M1/M2 switch: M1 Pin 60, I<sup>2</sup>C bus M1/M2 switch: M2</li> <li>• Recommended use range: Do not apply DC voltage from outside</li> </ul>
53	Refer to pin 51	Refer to pin 51
54	Refer to pin 10	Refer to pin 10
55		<p>M/S in: M/S (main/sub) switching signal input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 1.5 V</li> <li>1) <math>2.1\text{ V} &lt; V_{55}</math> Outputs the signal inputted from M1 or M2.</li> <li>2) <math>V_{55} &lt; 0.9\text{ V}</math> Outputs the signal inputted from M1 or M2.</li> </ul> <p>Note) If you switch over a multi-screen in a high speed within 1H period, WB will be changed. Be careful on use. The degree of WB changes depending upon the setting of DAC.</p> <ul style="list-style-type: none"> <li>• Priority order of signal switching over <math>M1/M2\ (I^2C\ SW) &lt; M/S &lt; Y_M &lt; Y_S</math></li> <li>• Recommended use range: 0 V to 5 V</li> </ul>
56		<p>CLP (M1) in: Main signal (M1) signal clamp pulse input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 1.5 V (clamps at high)</li> <li>• Clamps the signal inputted from the next pin Pin 57, pin 58, pin 59</li> <li>• Recommended clamp pulse width NTSC: 2.5 μs, HD: 1.0 μs</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>

Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
57		<p>R–Y (M1) in, B–Y (M1) in: Main (M1) signal R–Y, B–Y input pin</p> <ul style="list-style-type: none"> <li>• Pin 57: R–Y (M1) signal input pin</li> <li>• Pin 59: B–Y (M1) signal input pin</li> <li>• Input <math>\pm 0.35</math> V for both HD and NTSC.</li> <li>• Drive this pin with a low impedance. High impedance is likely to cause variation of white balance with the user volume.</li> <li>• Clamps the input signal with the clamp pulse of pin 56:</li> <li>• Recommended use range: Do not apply DC voltage from outside.</li> </ul>
58		<p>Y (M1) in: Main signal (M1) Y input pin</p> <ul style="list-style-type: none"> <li>• Input <math>0.7 V_{BW}</math> for both HD and NTSC.</li> <li>• Drive this pin with a low impedance. If it is driven with a high impedance, WB is likely to be changed.</li> <li>• Clamps the input signal with pin 56 clamp pulse.</li> <li>• Recommended use range: Do not apply DC voltage from outside.</li> </ul>
59	Refer to pin 57	Refer to pin 57
60		<p>CLP (M1) in: Main (M2) signal clamp pulse input pin</p> <ul style="list-style-type: none"> <li>• Input threshold voltage: 1.5 V (clamps at high)</li> <li>• Clamps the signal inputted from the next pin. Pin 61, pin 62, pin 63</li> <li>• Recommended clamp pulse width NTSC: 2.5 <math>\mu</math>s HD: 1.0 <math>\mu</math>s</li> <li>• Recommended use range: 0 V to 5 V</li> </ul>

### Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
61		<p>R–Y (M2) in, B–Y (M2) in: Main (M2) signal R–Y, B–Y input pin</p> <ul style="list-style-type: none"> <li>• Pin 61: R–Y (M2) signal input pin</li> <li>• Pin 63: B–Y (M2) signal input pin</li> <li>• Input <math>\pm 0.35</math> V for both HD and NTSC.</li> <li>• Drive this pin with a low impedance. High impedance is likely to cause variation of white balance with the user volume.</li> <li>• Clamps the input signal with the clamp pulse of pin 60:</li> <li>• Recommended use range: Do not apply DC voltage from outside.</li> </ul>
62		<p>Y (M2) in: Main (M2) signal Y input pin</p> <ul style="list-style-type: none"> <li>• Input <math>0.7 V_{BW}</math> for both HD and NTSC.</li> <li>• Drive this pin with a low impedance. High impedance is likely to cause variation of white balance with the user volume.</li> <li>• Clamps the input signal with the clamp pulse of pin 60:</li> <li>• Recommended use range: Do not apply DC voltage from outside.</li> </ul>
63	Refer to pin 61	Refer to pin 61
64	Refer to pin 1	Refer to pin 1

■ Application Circuit Example (Basic Circuit)

