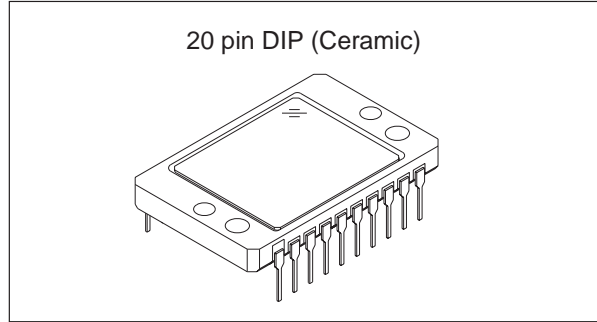


Diagonal 11mm (Type 2/3) Progressive Scan CCD Image Sensor with Square Pixel for B/W Cameras

Description

The ICX285AL is a diagonal 11 mm (Type 2/3) interline CCD solid-state image sensor with a square pixel array. High sensitivity and low smear are achieved through the adoption of EXview HAD CCD technology. Progressive scan allows all pixel's signals to be output independently within approximately 1/15 second. Also, the adoption of high frame rate readout mode supports 60 frames per second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter.

This chip is suitable for image input applications such as still cameras which require high resolution, etc.

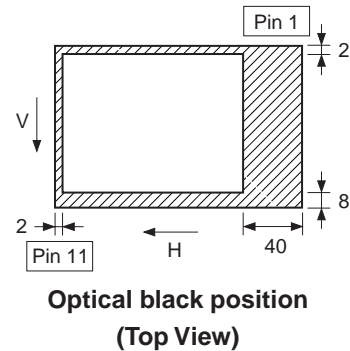


Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High horizontal and vertical resolution (both approximately 1024 TV-lines) still images without a mechanical shutter
- Supports high frame rate readout mode (effective 256 lines output, 60 frame/s)
- Square pixel
- Aspect ratio: 4:3
- Horizontal drive frequency: 28.64 MHz
- High sensitivity, low smear
- Low dark current, excellent anti-blooming characteristics
- Continuous variable-speed shutter
- Horizontal register: 5.0 V drive

Device Structure

- Interline CCD image sensor
- Image size: Diagonal 11 mm (Type 2/3)
- Total number of pixels: 1434 (H) × 1050 (V) approx. 1.50M pixels
- Number of effective pixels: 1392 (H) × 1040 (V) approx. 1.45M pixels
- Number of active pixels: 1360 (H) × 1024 (V) approx. 1.40M pixels
- Chip size: 10.2 mm (H) × 8.3 mm (V)
- Unit cell size: 6.45 μm (H) × 6.45 μm (V)
- Optical black: Horizontal (H) direction: Front 2 pixels, rear 40 pixels
Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 20
Vertical 3
- Substrate material: Silicon



EXview HAD CCD™

* EXview HAD CCD is a trademark of Sony Corporation.
EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a basic structure of HAD (Hole-Accumulation-Diode) sensor.

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

USE RESTRICTION NOTICE (December 1, 2003 ver.)

This USE RESTRICTION NOTICE ("Notice") is for customers who are considering or currently using the CCD products ("Products") set forth in this specifications book. Sony Corporation ("Sony") may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a Sony subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of Sony on such a use restriction notice when you consider using the Products.

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications which may pose a life- or injury- threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your Sony sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

Design for Safety

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Export Control

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

No License Implied

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that Sony and its licensors will license any intellectual property rights in such information by any implication or otherwise. Sony will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

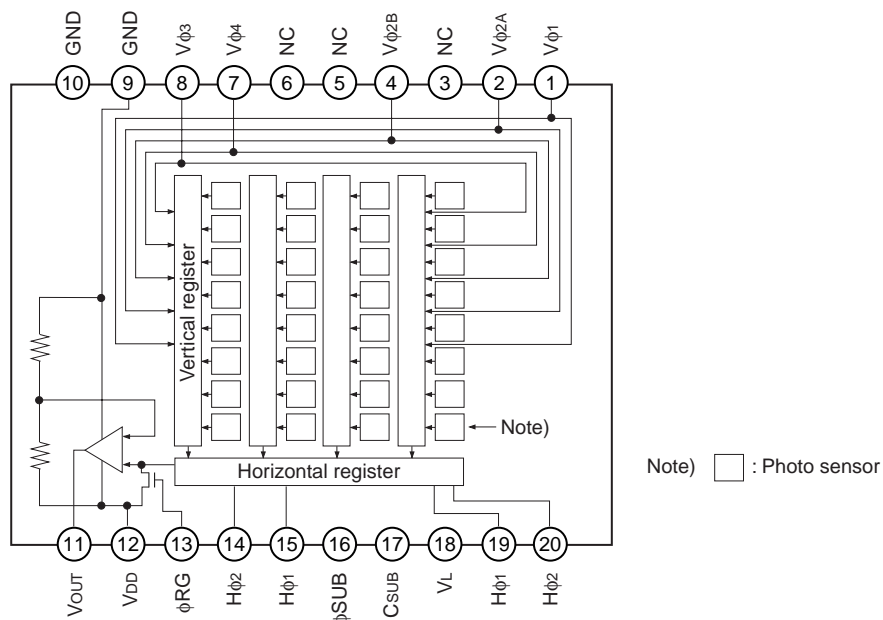
Governing Law

- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

Other Applicable Terms and Conditions

- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	V ϕ ₁	Vertical register transfer clock	11	V _{OUT}	Signal output
2	V ϕ _{2A}	Vertical register transfer clock	12	V _{DD}	Supply voltage
3	NC		13	ϕ RG	Reset gate clock
4	V ϕ _{2B}	Vertical register transfer clock	14	H ϕ ₂	Horizontal register transfer clock
5	NC		15	H ϕ ₁	Horizontal register transfer clock
6	NC		16	ϕ SUB	Substrate clock
7	V ϕ ₄	Vertical register transfer clock	17	C _{SUB}	Substrate bias ^{*1}
8	V ϕ ₃	Vertical register transfer clock	18	V _L	Protective transistor bias
9	GND	GND	19	H ϕ ₁	Horizontal register transfer clock
10	GND	GND	20	H ϕ ₂	Horizontal register transfer clock

^{*1} DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1 μ F.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against ϕ SUB	V_{DD} , V_{OUT} , ϕ RG – ϕ SUB	–40 to +12	V	
	$V_{\phi 2A}$, $V_{\phi 2B}$ – ϕ SUB	–50 to +15	V	
	$V_{\phi 1}$, $V_{\phi 3}$, $V_{\phi 4}$, V_L – ϕ SUB	–50 to +0.3	V	
	$H_{\phi 1}$, $H_{\phi 2}$, GND – ϕ SUB	–40 to +0.3	V	
	C_{SUB} – ϕ SUB	–25 to	V	
Against GND	V_{DD} , V_{OUT} , ϕ RG, C_{SUB} – GND	–0.3 to +22	V	
	$V_{\phi 1}$, $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 3}$, $V_{\phi 4}$ – GND	–10 to +18	V	
	$H_{\phi 1}$, $H_{\phi 2}$ – GND	–10 to +6.5	V	
Against V_L	$V_{\phi 2A}$, $V_{\phi 2B}$ – V_L	–0.3 to +28	V	
	$V_{\phi 1}$, $V_{\phi 3}$, $V_{\phi 4}$, $H_{\phi 1}$, $H_{\phi 2}$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H_{\phi 1}$ – $H_{\phi 2}$	–6.5 to +6.5	V	
	$H_{\phi 1}$, $H_{\phi 2}$ – $V_{\phi 4}$	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Performance guarantee temperature		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +24 V (Max.) when clock width < 10 μ s, clock duty factor < 0.1%.
+16 V (Max.) is guaranteed for power-on and power-off.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L		*2			
Substrate clock	ϕ SUB		*3			
Reset gate clock	ϕ RG		*3			

*2 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*3 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC characteristics

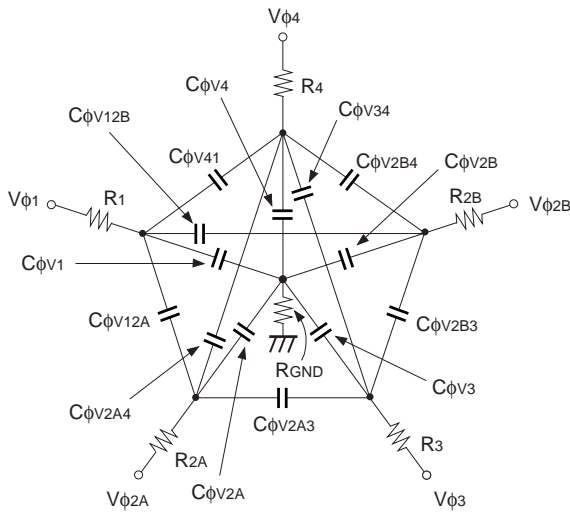
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		9	11	mA	

Clock Voltage Conditions

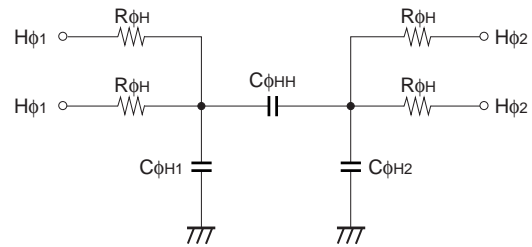
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	-0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	-0.2	0	0.05	V	2	
	$V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}$	-7.3	-7.0	-6.7	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V_{\phi V}$	6.5	7.0	7.35	V	2	$V_{\phi V} = V_{VnH} - V_{VnL} (n = 1 \text{ to } 4)$
	$V_{VH3} - V_{VH}$	-0.25		0.1	V	2	
	$V_{VH4} - V_{VH}$	-0.25		0.1	V	2	
	V_{VHH}			1.4	V	2	High-level coupling
	V_{VHL}			1.3	V	2	High-level coupling
	V_{VLH}			1.4	V	2	Low-level coupling
	V_{VLL}			0.8	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.75	5.0	5.25	V	3	
	V_{HL}	-0.05	0	0.05	V	3	
	V_{CR}	$V_{\phi H}/2$			V	3	Cross-point voltage
Reset gate clock voltage	$V_{\phi RG}$	3.0	3.3	5.5	V	4	
	$V_{RGLH} - V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} - V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	21.25	22.0	22.75	V	5	

Clock Equivalent Circuit Constants

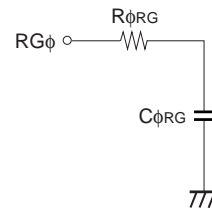
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1$		5600		pF	
	$C\phi V2A$		6800		pF	
	$C\phi V2B$		22000		pF	
	$C\phi V3$		8200		pF	
	$C\phi V4$		22000		pF	
Capacitance between vertical transfer clocks	$C\phi V12A$		150		pF	
	$C\phi V12B$		390		pF	
	$C\phi V2A3$		270		pF	
	$C\phi V2B3$		470		pF	
	$C\phi V14$		2200		pF	
	$C\phi V34$		330		pF	
	$C\phi V2A4$		390		pF	
	$C\phi V2B4$		560		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1$		47		pF	
	$C\phi H2$		39		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		74		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		4		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		1300		pF	
Vertical transfer clock series resistor	$R1, R3$		30		Ω	
	$R2A, R2B$		32		Ω	
	$R4$		20		Ω	
Vertical transfer clock ground resistor	R_{GND}		60		Ω	
Horizontal transfer clock series resistor	$R\phi H$		7.5		Ω	
Reset gate clock ground resistor	$R\phi RG$		24		Ω	



Vertical transfer clock equivalent circuit



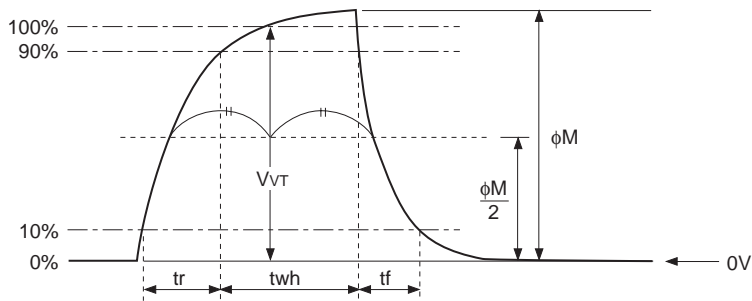
Horizontal transfer clock equivalent circuit



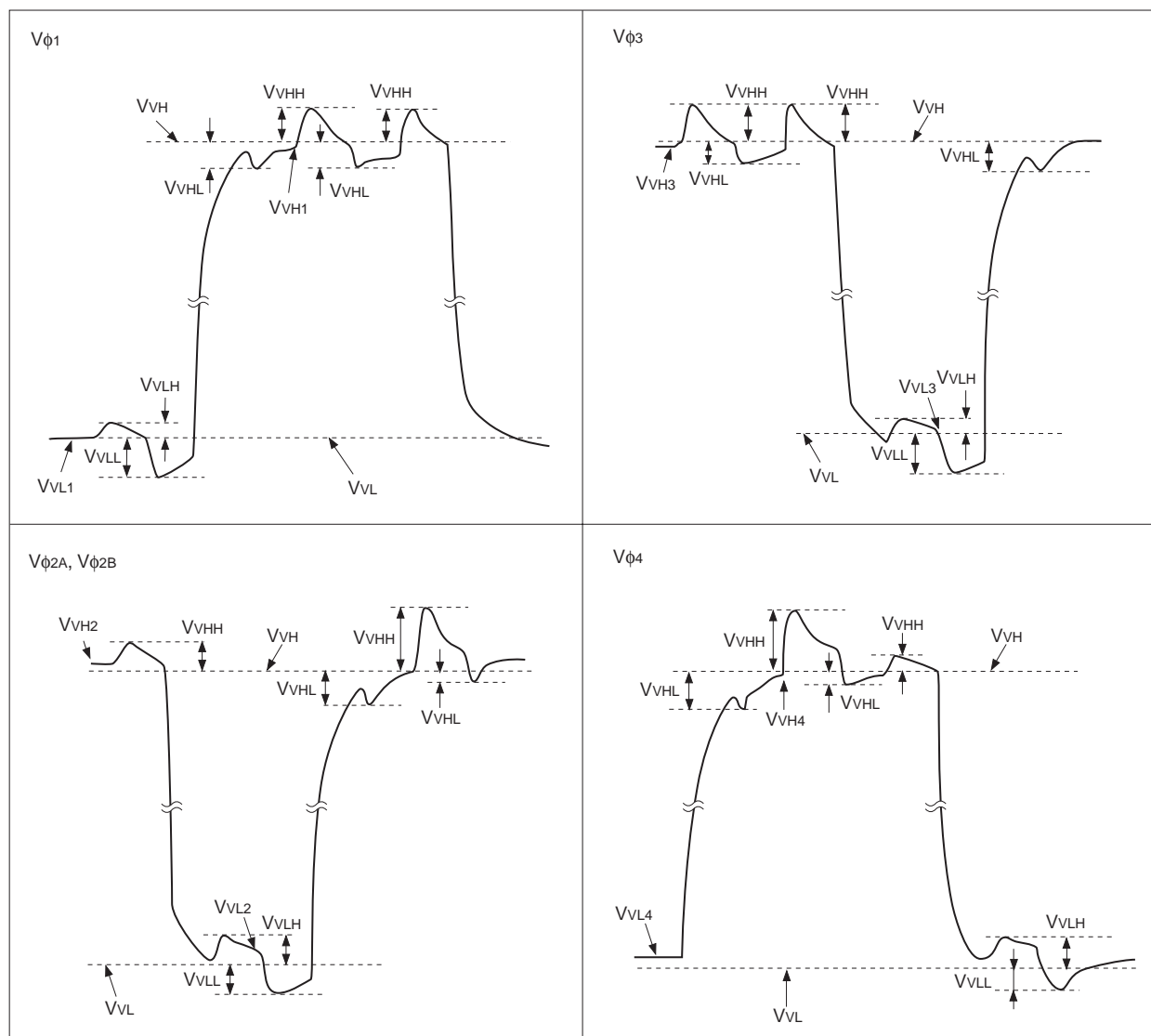
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

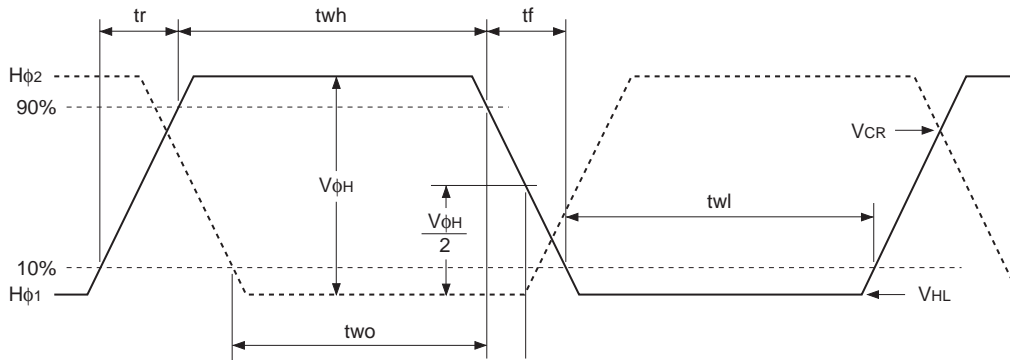


$$V_{VH} = (V_{VH1} + V_{VH2})/2$$

$$V_{VL} = (V_{VL3} + V_{VL4})/2$$

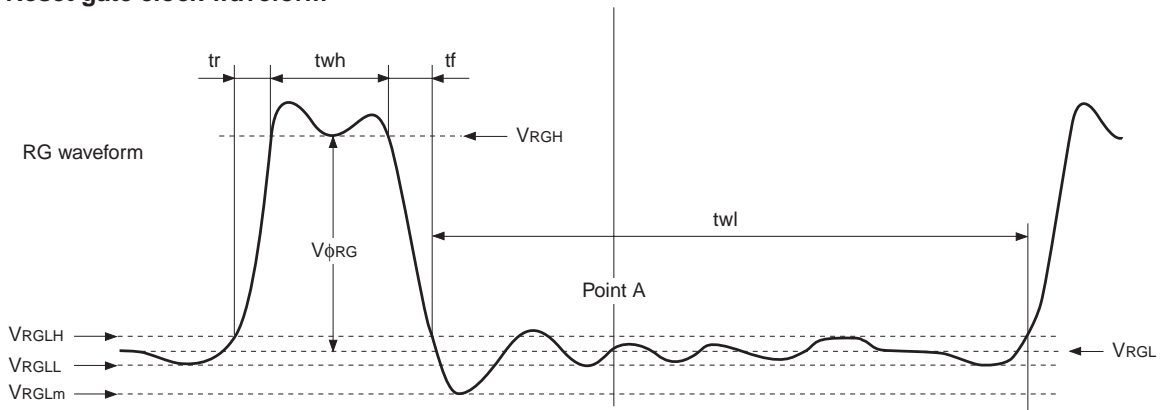
$$V_{\phi v} = V_{VHn} - V_{VLn} \quad (n = 1 \text{ to } 4)$$

(3) Horizontal transfer clock waveform



Cross-point voltage for the Hφ₁ rising side of the horizontal transfer clocks Hφ₁ and Hφ₂ waveforms is V_{CR}. The overlap period for t_{wh} and t_{wl} of horizontal transfer clocks Hφ₁ and Hφ₂ is two.

(4) Reset gate clock waveform



V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.

In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

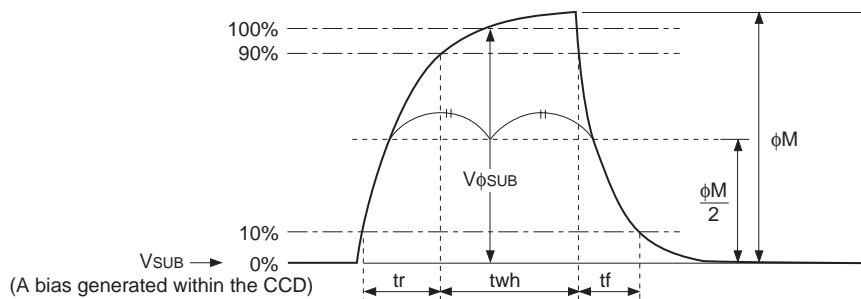
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming V_{RGH} is the minimum value during the interval t_{wh}, then:

$$V_{φRG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is V_{RGLm}.

(5) Substrate clock waveform



Clock Switching Characteristics (Horizontal drive frequency: 28.64 MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V _T	2.8	3.0					0.5			0.5		μs	During readout	
Vertical transfer clock	V _{φ1} , V _{φ2} , V _{φ3} , V _{φ4}										15	250	ns	When using CXD3400N	
Horizontal transfer clock	During imaging	H _{φ1}	10	12.5		10	12.5		5	7.5		5	7.5	ns	rf ≥ rf – 2ns
		H _{φ2}	10	12.5		10	12.5		5	7.5		5	7.5		
	During parallel-serial conversion	H _{φ1}							0.01			0.01		μs	
		H _{φ2}							0.01			0.01			
Reset gate clock	φ _{RG}	4	8			24		2			2		ns		
Substrate clock	φ _{SUB}	3.5	3.9						0.5			0.5	μs	When draining charge	

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	H _{φ1} , H _{φ2}	8	10		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

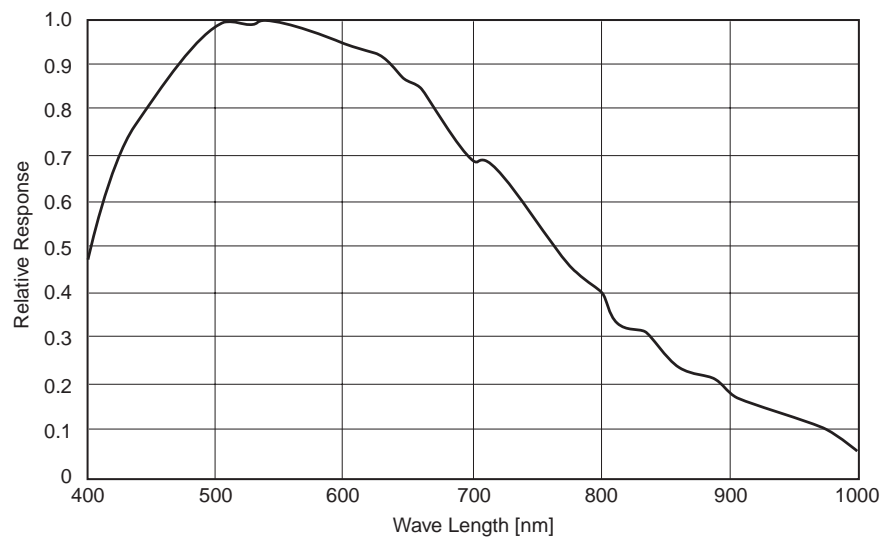


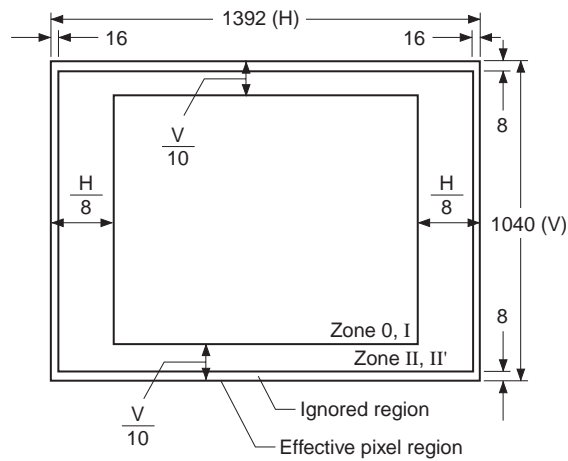
Image Sensor Characteristics

(Ta = 25°C)

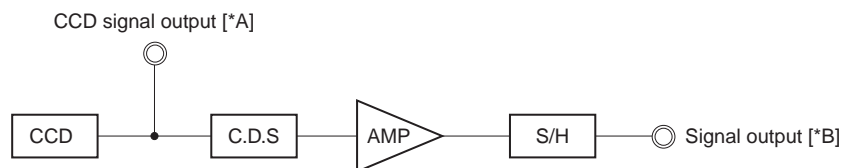
Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity 1	S1	1040	1300		mV	1	1/30 s accumulation
Sensitivity 2	S2		4000		mV	2	1/30 s accumulation
Saturation signal	Vsat	850			mV	3	Ta = 60°C
Smear	Sm		-110	-100	dB	4	Progressive scan mode
			-98	-88			High frame rate readout mode
Video signal shading	SH			20	%	5	Zone 0 and I
				25			Zone 0 to II'
Dark signal	Vdt			11	mV	6	Ta = 60°C, 15 frame/s
Dark signal shading	ΔVdt			4	mV	7	Ta = 60°C, 15 frame/s, *1
Lag	Lag			0.5	%	8	

*1 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System

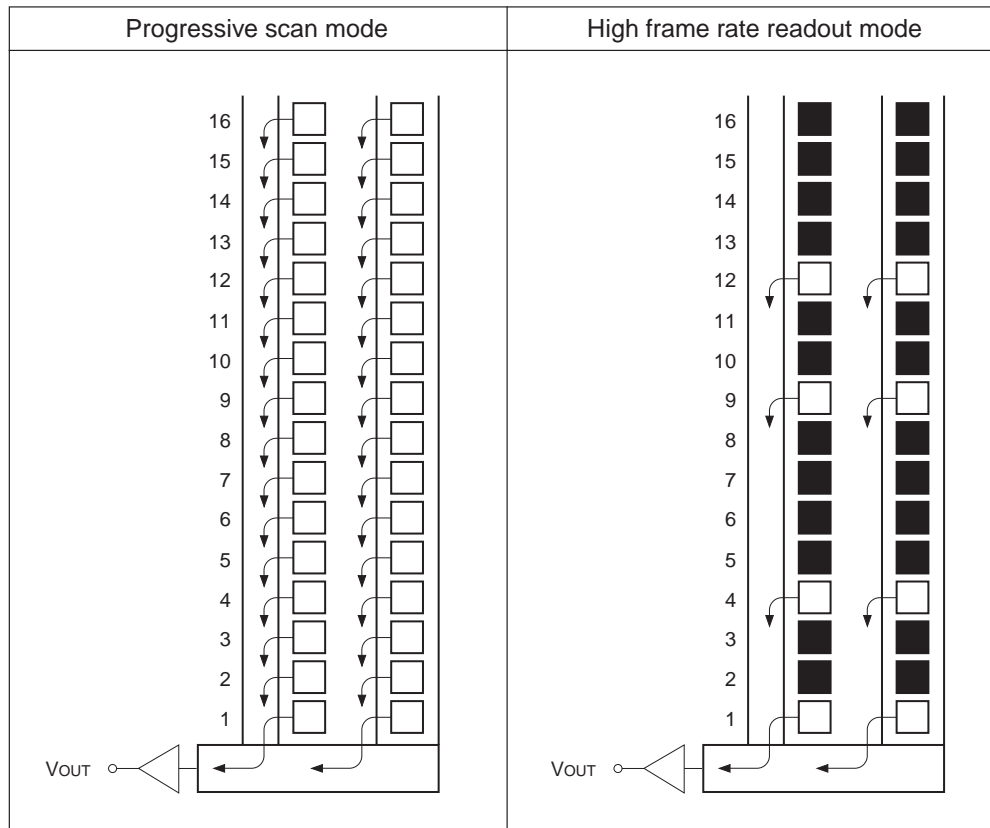


Note) Adjust the amplifier gain so that the gain between [*A] and [*B] equals 1.

Image Sensor Characteristics Measurement Method

- Readout modes

The diagram below shows the output methods for the following two readout modes.



Note) Blacked out portions in the diagram indicate pixels which are not read out.
Output starts from line 1 in high frame rate readout mode.

1. Progressive scan mode

In this mode, all pixel signals are output in non-interlace format in 1/15 s.

All pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode

All effective areas are scanned in approximately 1/60 s by reading out two out of eight lines (1st and 4th lines, 9th and 12th lines, and so on). The vertical resolution is approximately 256 TV-lines.

This readout mode emphasizes processing speed over vertical resolution.

- **Measurement conditions**

- (1) In the following measurements, the substrate voltage is set to the value indicated on the device, and the device drive conditions are at the typical values of the progressive scan mode, bias and clock voltage conditions.
- (2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value measured at point [*B] of the measurement system.

- **Definition of standard imaging conditions**

- (1) Standard imaging condition I:

Use a pattern box (luminance: 706 cd/m², color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

- (2) Standard imaging condition II:

This indicates the standard imaging condition I with the IR cut filter removed.

- (3) Standard imaging condition III:

Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity 1

Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/100 s, measure the signal output (V_{S1}) at the center of the screen, and substitute the value into the following formula.

$$S_1 = V_{S1} \times \frac{100}{30} \text{ [mV]}$$

2. Sensitivity 2

Set to standard imaging condition II. After selecting the electronic shutter mode with a shutter speed of 1/500 s, measure the signal output (V_{S2}) at the center of the screen, and substitute the value into the following formula.

$$S_2 = V_{S2} \times \frac{500}{30} \text{ [mV]}$$

3. Saturation signal

Set to standard imaging condition III. After adjusting the luminous intensity to 20 times the intensity with the average value of the signal output, 200 mV, measure the minimum value of the signal output.

4. Smear

Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of signal output, 200 mV. Then after the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (V_{sm} [mV]) of the signal output and substitute the value into the following formula.

$$S_m = 20 \times \log \left(\frac{V_{sm}}{200} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB]} \text{ (1/10 V method conversion value)}$$

5. Video signal shading

Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 200 mV. Then measure the maximum (V_{max} [mV]) and minimum (V_{min} [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (V_{max} - V_{min})/200 \times 100 [\%]$$

6. Dark signal

Measure the average value of the signal output (V_{dt} [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading

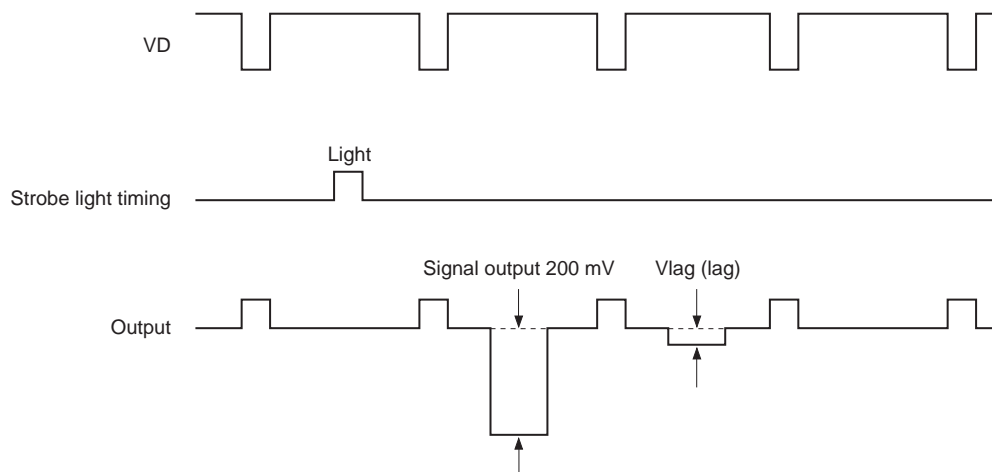
After measuring 6, measure the maximum (V_{dmax} [mV]) and minimum (V_{dmin} [mV]) values of the dark signal output and substitute the values into the following formula.

$$\Delta V_{dt} = V_{dmax} - V_{dmin} [\text{mV}]$$

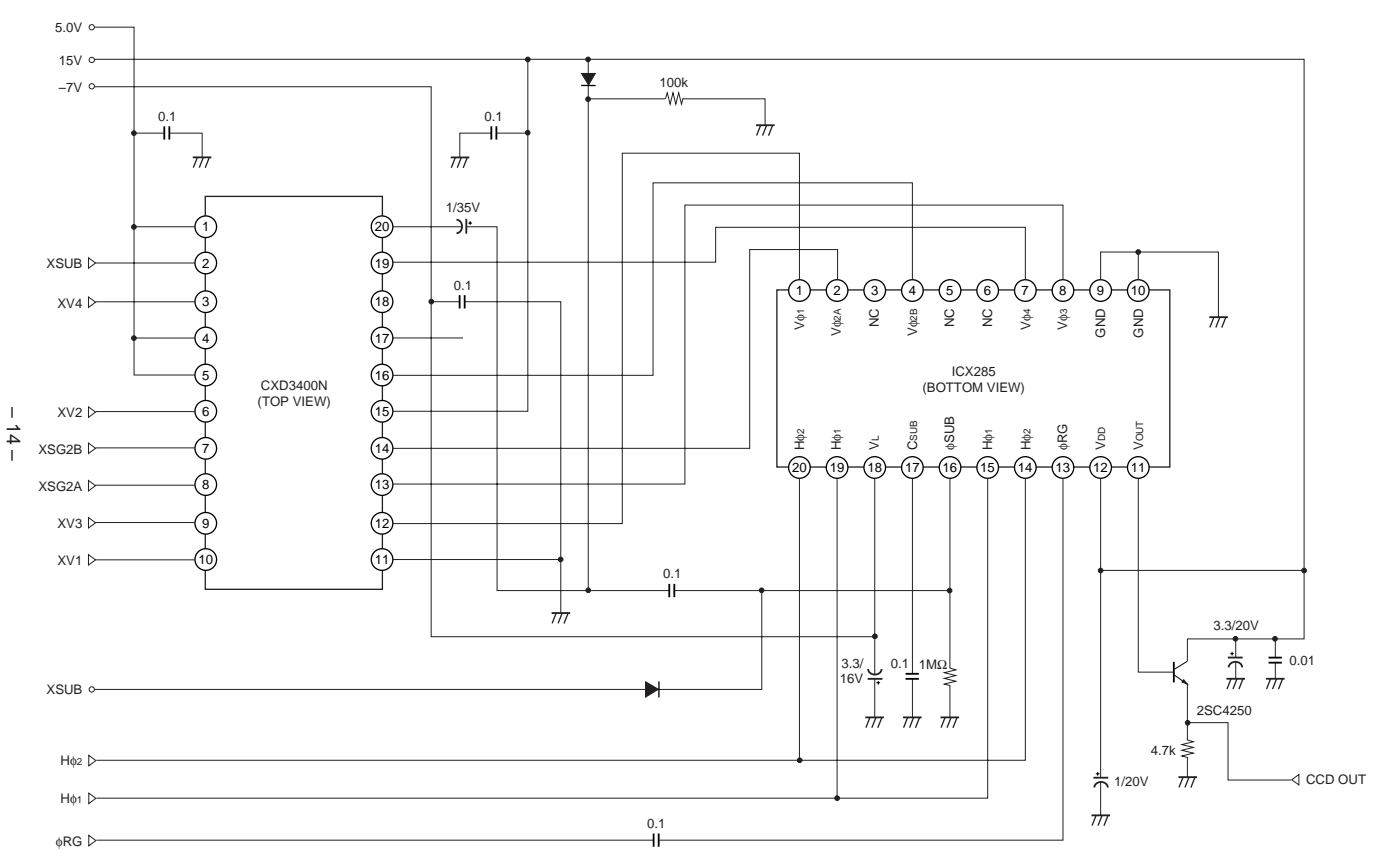
8. Lag

Adjust the signal output generated by strobe light to 200 mV. After setting the strobe light so that it strobos with the following timing, measure the residual signal (V_{lag}). Substitute the value into the following formula.

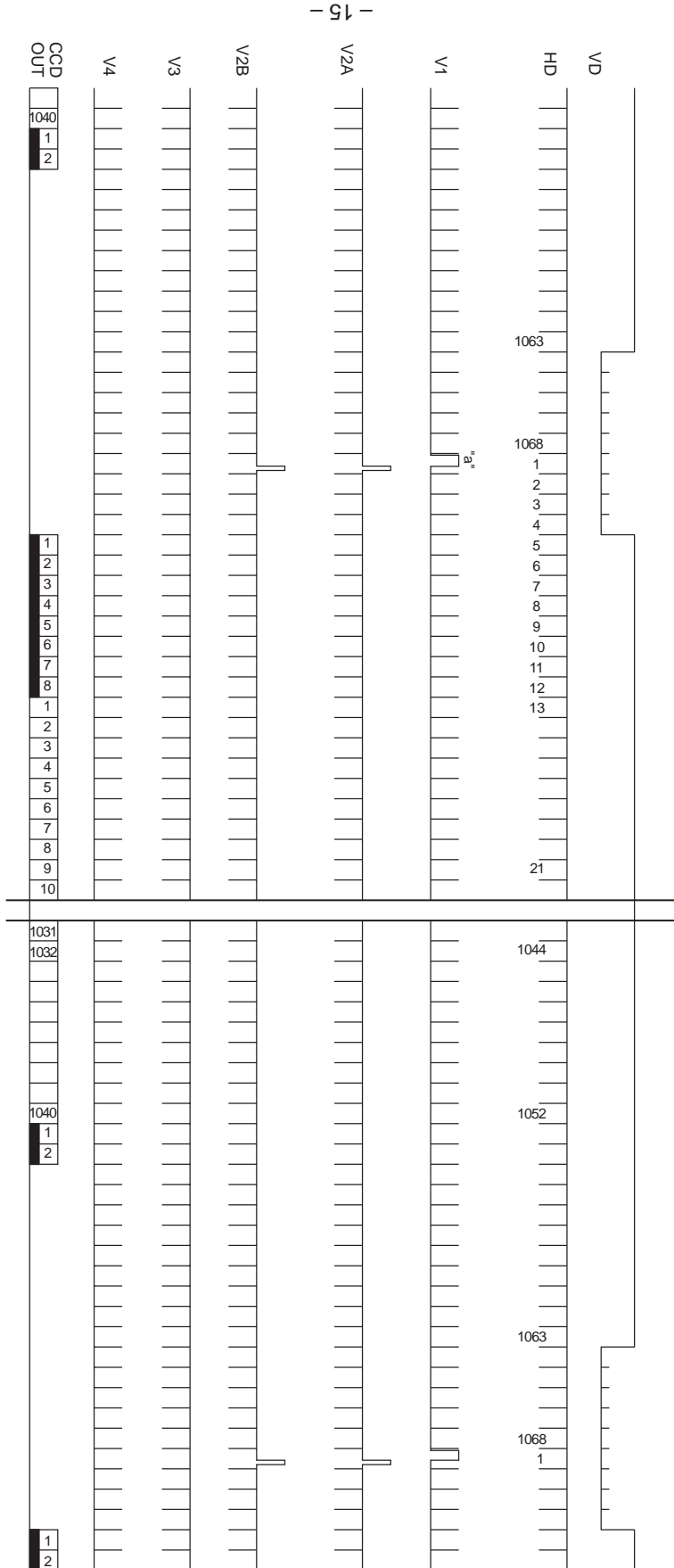
$$Lag = (V_{lag}/200) \times 100 [\%]$$



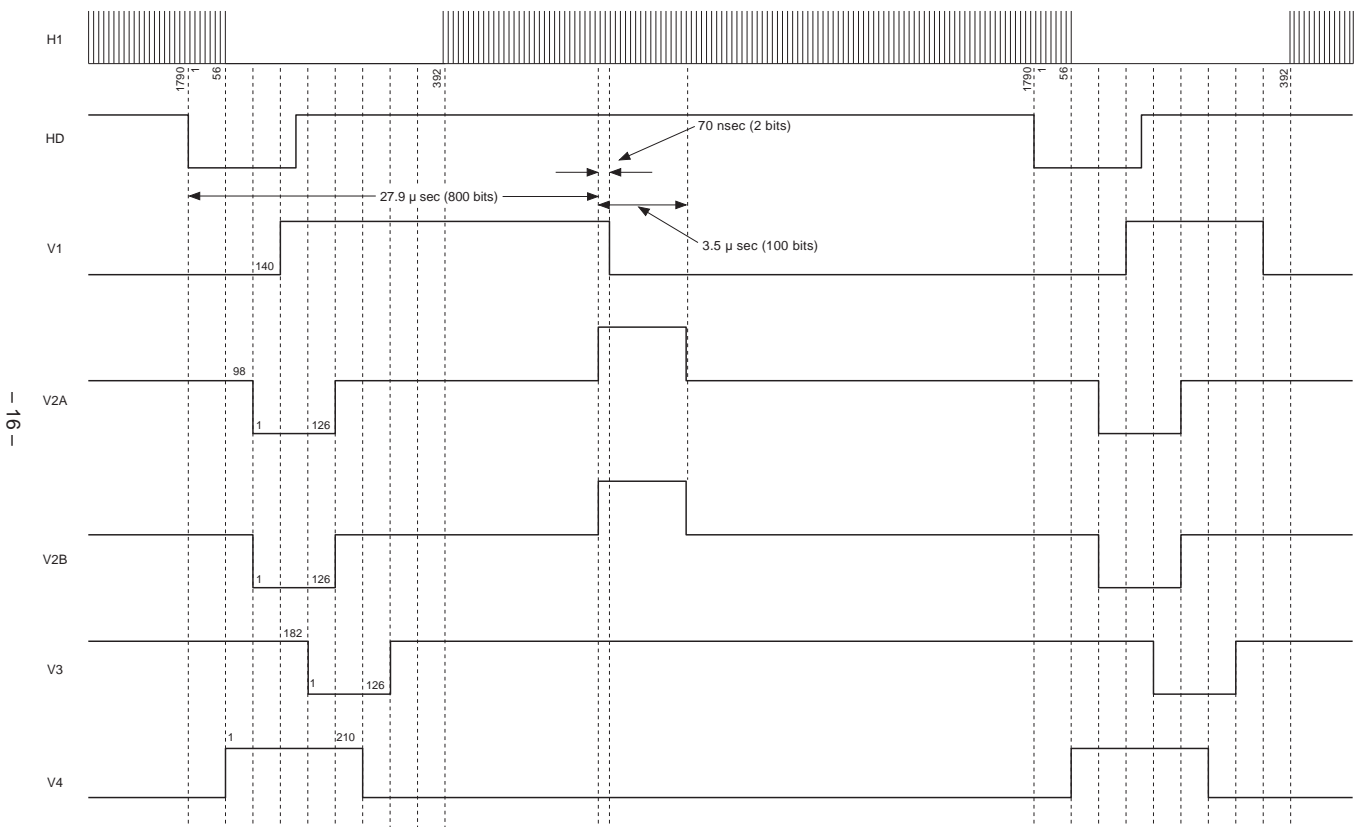
Drive Circuit



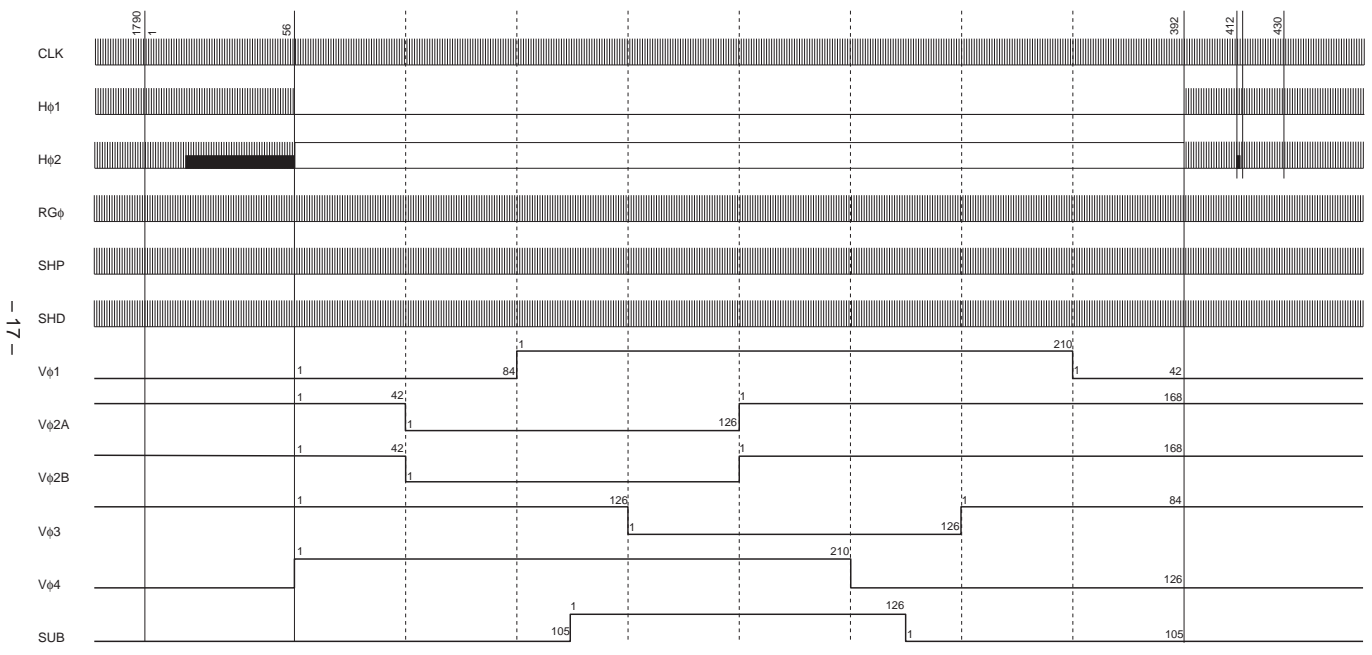
Drive Timing Chart (Vertical Sync) Progressive Scan Mode



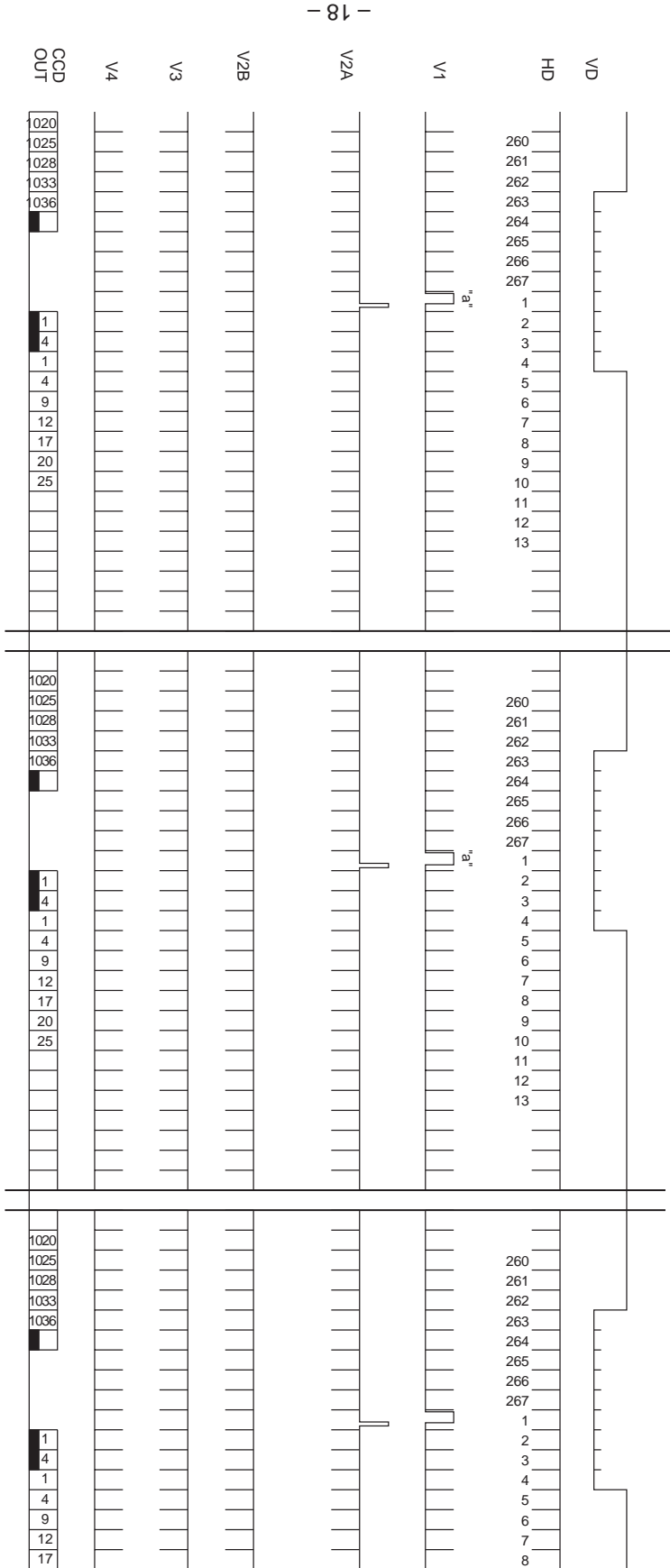
Drive Timing Chart (Vertical Sync "a" Enlarged) Progressive Scan Mode



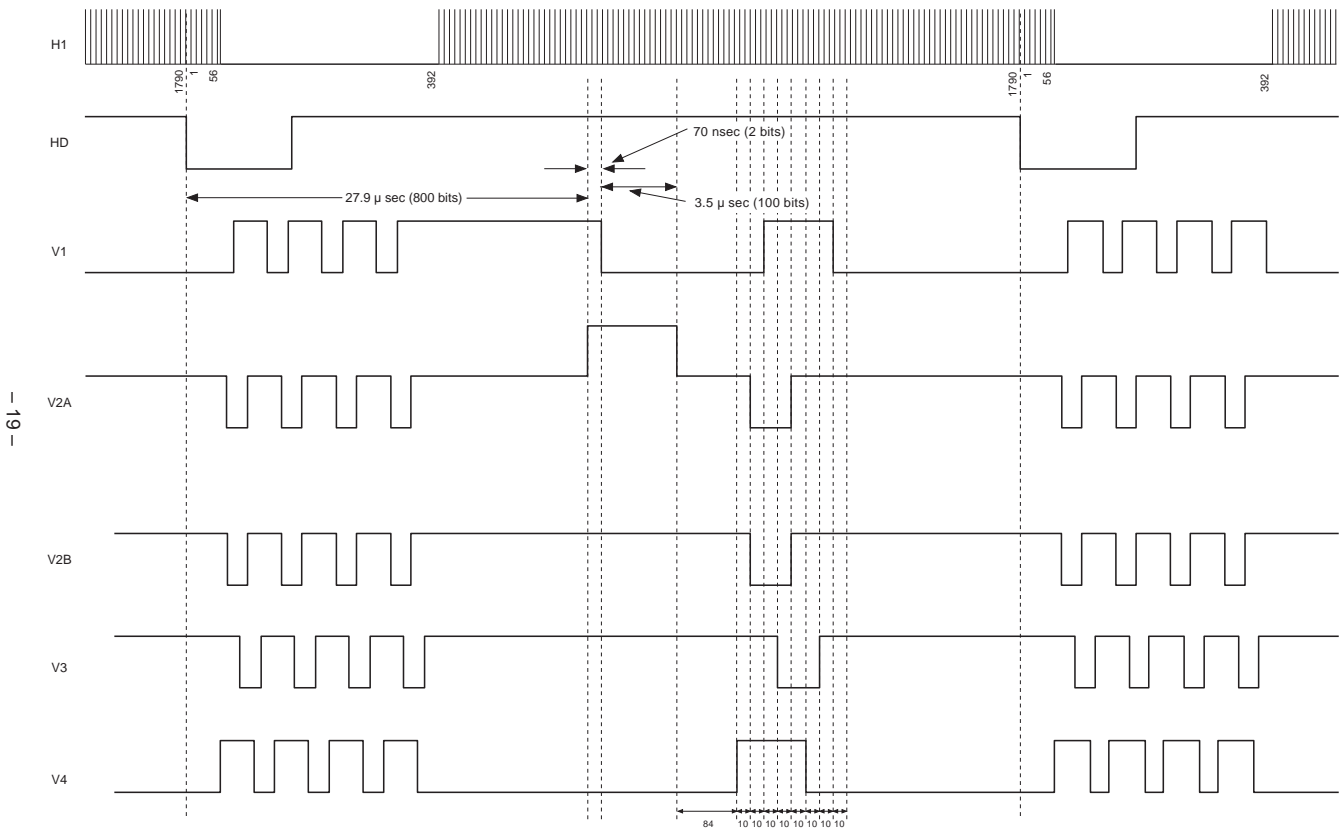
Drive Timing Chart (Horizontal Sync) Progressive Scan Mode



Drive Timing Chart (Vertical Sync) High Frame Rate Readout Mode

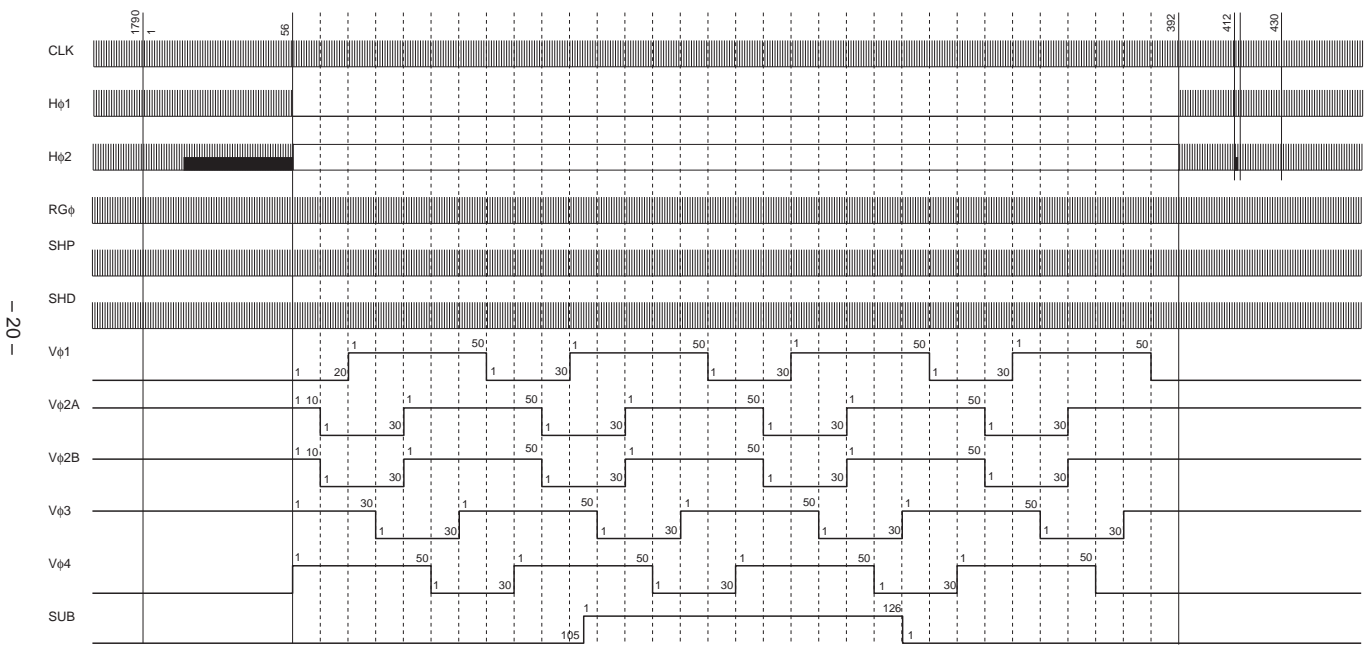


Drive Timing Chart (Vertical Sync "a" Enlarged) High Frame Rate Readout Mode



- 19 -

Drive Timing Chart (Horizontal Sync) High Frame Rate Readout Mode



- 20 -

Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensor.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

- a) Perform all assembly operations in a clean room (class 1000 or less).
- b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

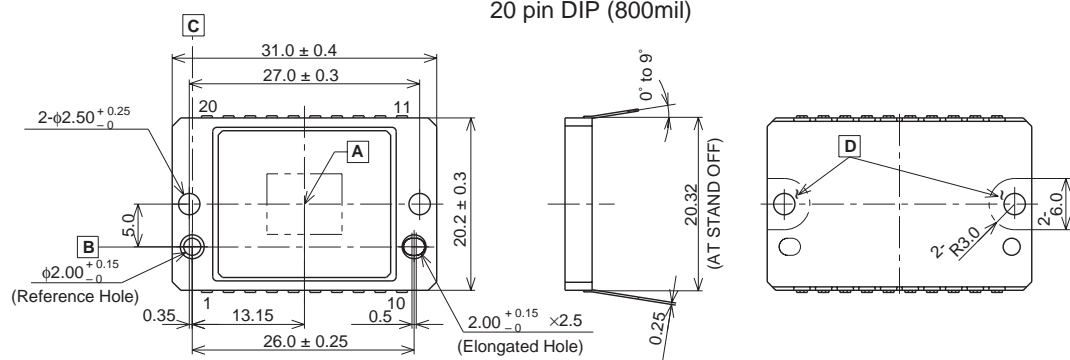
4) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

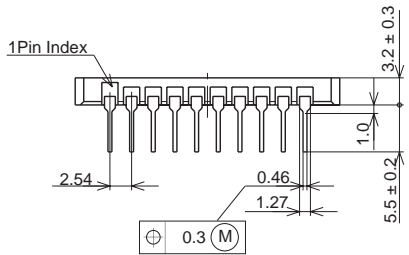
6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm

20 pin DIP (800mil)



- 22 -



1. "A" is the center of the effective image area.
2. The straight line "B" which passes through the center of the reference hole and the elongated hole is the reference axis of vertical direction (V).
3. The straight line "C" which passes through the center of the reference hole at right angle to vertical reference line "B" is the reference axis of horizontal direction (H).
4. The bottom "D" is the height reference. (Two points are specified.)
5. The center of the effective image area specified relative to the reference hole is (H, V) = (13.15, 5.0) ± 0.15mm.
6. The angle of rotation relative to the reference line "B" is less than ± 1°
7. The height from the bottom "D" to the effective image area is 1.46 ± 0.15mm.
8. The tilt of the effective image area relative to the bottom "D" is less than 60µm.
9. The thickness of the cover glass is 0.75mm and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.90g
DRAWING NUMBER	AS-A11(E)

Sony Corporation