



SANYO Semiconductors DATA SHEET

STK672-070-E — Thick-Film Hybrid IC Unipolar Constant-current Chopper (external excitation PWM) Circuit with Built-in Microstepping Controller Stepping Motor Driver (sine wave drive) Output Current 1.5A (no heat sink*)

Overview

The STK672-070-E is a stepping motor driver hybrid IC that uses power MOSFETs in the output stage. It includes a built-in microstepping controller and is based on a unipolar constant-current PWM system. The STK672-070-E supports application simplification and standardization by providing a built-in 4 phase distribution stepping motor controller. It supports five excitation methods: 2 phase, 1-2 phase, W1-2 phase, 2W1-2 phase, and 4W1-2 phase excitations, and can provide control of the basic stepping angle of the stepping motor divided into 1/16 step units. It also allows the motor speed to be controlled with only a clock signal.

The use of this hybrid IC allows designers to implement systems that provide high motor torques, low vibration levels, low noise, fast response, and high-efficiency drive.

This product is provided in a smaller package than SANYO's earlier STK672-040-E for easier mounting in end products.

Applications

- Facsimile stepping motor drive (send and receive)
- Paper feed and optical system stepping motor drive in copiers
- Laser printer drum drive
- Printer carriage stepping motor drive
- X-Y plotter pen drive
- Other stepping motor applications

Note*: Conditions: $V_{CC1} = 24V$, $I_{OH} = 1.5A$, 2W1-2 excitation mode.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

61108HKIM/D1803SI(OT) No.7307-1/18

Features

- Can implement stepping motor drive systems simply by providing a DC power supply and a clock pulse generator.

<Control Block Features>

- One of five drive types can be selected with the drive mode settings (M1, M2, and M3)
 - 1) 2 phase excitation drive
 - 2) 1-2 phase excitation drive
 - 3) W1-2 phase excitation drive
 - 4) 2W1-2 phase excitation drive
 - 5) 4W1-2 phase excitation drive
- Phase retention even if excitation is switched.
- Provides the MOI phase origin monitor pin.
- The CLK input counter block can be selected to be one of the following by the high/low setting of the M3 input pin.
 - 1) Rising edge only
 - 2) Both rising and falling edges
- The CLK input pin includes built-in malfunction prevention circuits for external pulse noise.
- ENABLE and RESET pins provided. These are Schmitt trigger inputs with built-in 20kΩ (typical) pull-up resistors.
- No noise generation due to the difference between the A and B phase time constants during motor hold since external excitation is used.
- Microstepping operation supported even for small motor currents, since the reference voltage Vref can be set to any value between 0V and 1/2VCC2.

<Driver Block>

- External excitation PWM drive allows a wide operating supply voltage range (VCC1 = 10 to 45V) to be used.
- Current detection resistor (0.22Ω) built-in the hybrid IC itself.
- Power MOSFETs adopted for low drive loss.
- Provides a motor output drive current of IOH = 1.5A. (at Tc = 105°C)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	VCC1 max	No signal	52	V
Maximum supply voltage 2	VCC2 max	No signal	-0.3 to +7.0	V
Input voltage	VIN max	Logic input pins	-0.3 to +7.0	V
Output current	IOH max	0.5s, 1 pulse, with VCC1 applied	2.0	A
Repeated avalanche capacity	Ea max		25	mJ
Allowable power dissipation	Pd max	θc-a = 0	6.5	W
Operating IC substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	VCC1	With signals applied	10 to 45	V
Supply voltage 2	VCC2	With signals applied	5 ± 5%	V
Input voltage	VIH		0 to VCC2	V
Phase driver withstand voltage	VDSS	Tr1, 2, 3, and 4 (the A, \bar{A} , B, and \bar{B} outputs)	100 (min)	V
Output current 1	IOH1	Tc = 105°C, CLK ≥ 200Hz	1.5	A
Output current 2	IOH2	Tc = 80°C, CLK ≥ 200Hz	1.7	A

STK672-070-E

Electrical Characteristics at $T_c = 25^\circ\text{C}$, $V_{CC1} = 24\text{V}$, $V_{CC2} = 5\text{V}$

Parameters	Symbols	Conditions	Rating			unit
			min	typ	max	
Control supply current	I_{CC}	Pin 6, with ENABLE pin held low.		2.1	14	mA
Output saturation voltage	V_{sat}	$R_L = 12\Omega$		0.65	1.2	V
Average output current	I_{oave}	Load: $R = 3.5\Omega / L = 3.8\text{mH}$ For each phase	0.445	0.5	0.56	A
FET diode forward voltage	V_{df}	$I_f = 1\text{A}$		1	1.8	V
[Control Inputs]						
Input voltage	V_{IH}	Except for the V_{ref} pin	4			V
	V_{IL}	Except for the V_{ref} pin			1	V
Input current	I_{IH}	Except for the V_{ref} pin	0	1	10	μA
	I_{IL}	Except for the V_{ref} pin	125	250	510	μA
[Vref Input Pin]						
Input voltage	V_I	Pin 7	0		2.5	V
Input current	I_I	Pin 7, 2.5V input	330	415	545	μA
[Control Outputs]						
Output voltage	V_{OH}	$I = -3\text{mA}$, pins MOI	2.4			V
	V_{OL}	$I = +3\text{mA}$, pins MOI			0.4	V
[Current Distribution Ratio (A-B)]						
2W1-2, W1-2, 1-2	V_{ref}	$\theta = 1/8$		100		%
2W1-2, W1-2	V_{ref}	$\theta = 2/8$		92		%
2W1-2	V_{ref}	$\theta = 3/8$		83		%
2W1-2, W1-2, 1-2	V_{ref}	$\theta = 4/8$		71		%
2W1-2	V_{ref}	$\theta = 5/8$		55		%
2W1-2, W1-2	V_{ref}	$\theta = 6/8$		40		%
2W1-2	V_{ref}	$\theta = 7/8$		21		%
2	V_{ref}			100		%
PWM frequency	f_c		37	47	57	kHz

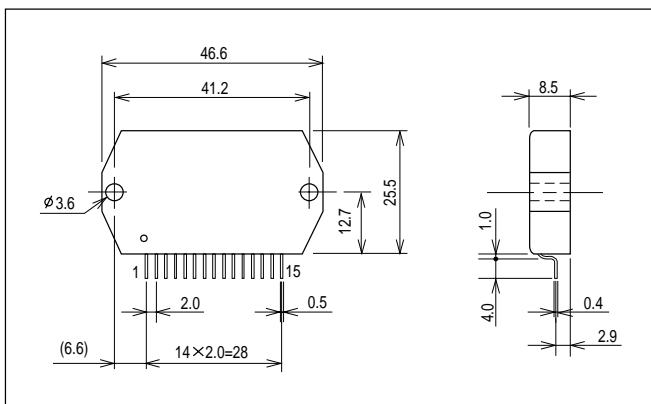
Note: A constant-voltage power supply must be used.

The design target value is shown for the current distribution ratio.

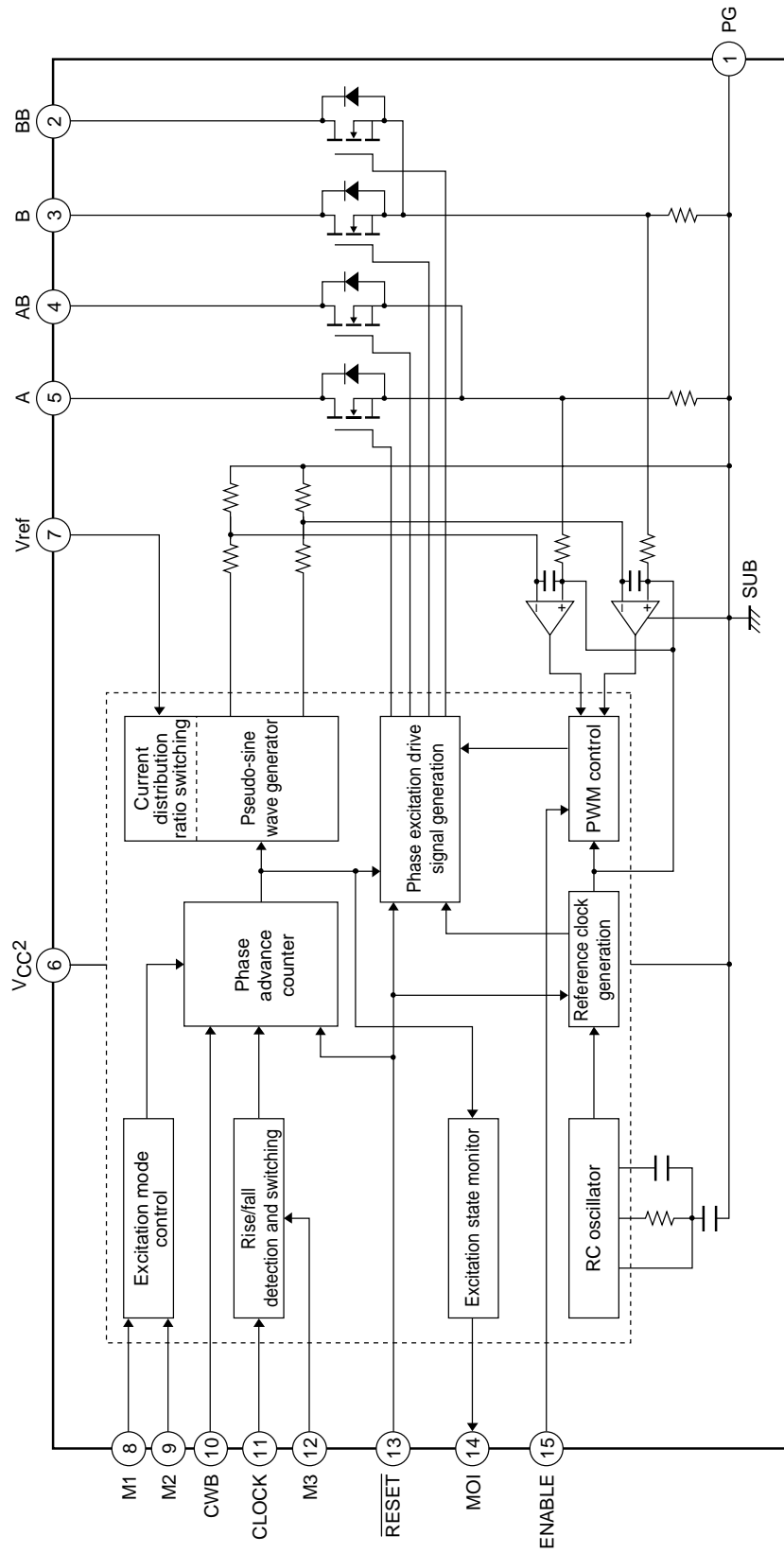
Package Dimensions

unit:mm (typ)

4186



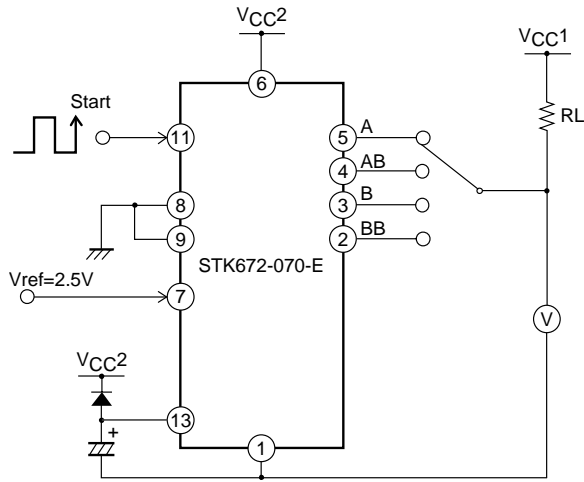
Internal Block Diagram



A13256

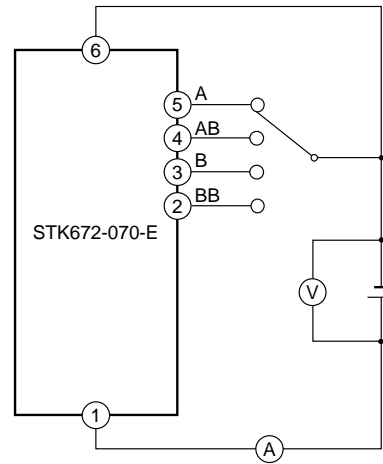
Test Circuit Diagrams

V_{sat}



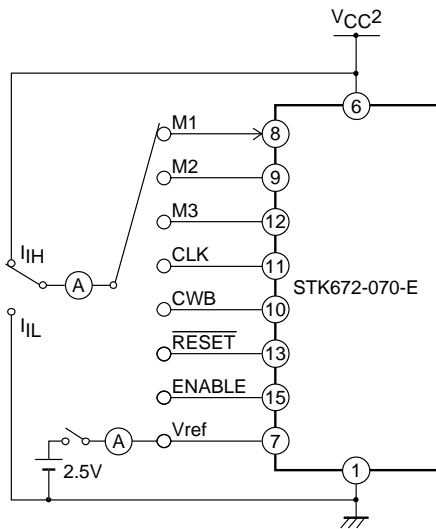
A13257

V_{df}



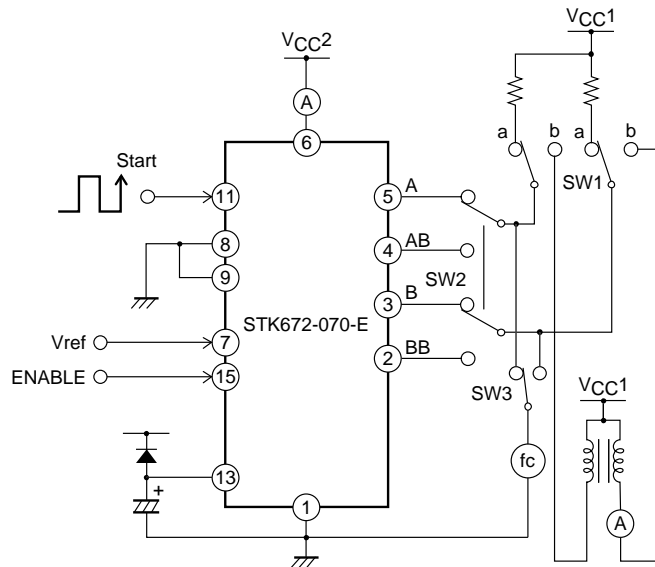
A13258

I_H, I_L



A13259

I_{oave}, I_{CC}, f_c

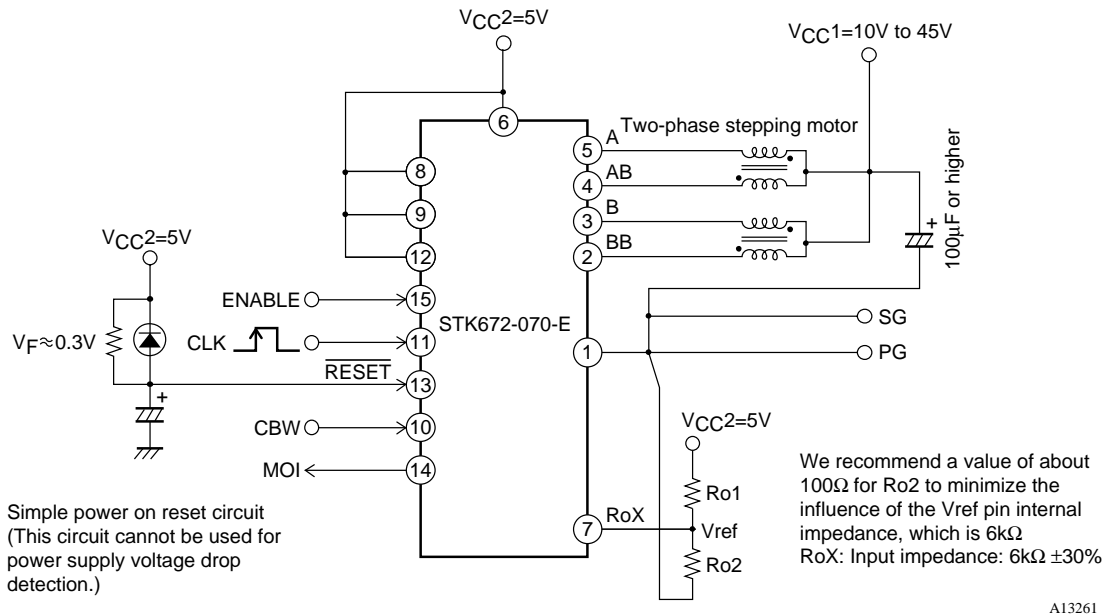


A13260

For I_{oave} measurement: Set switch SW1 to the b position, provide the V_{ref} input and switch over switch SW2.
 For f_c measurement: Set SW1 to the a position, set V_{ref} to 0V, and switch over switch SW3.
 For I_{CC} measurement: Set the ENABLE input to the low level.

Power-on Reset

The application must perform a power-on reset operation when V_{CC2} power is first applied to this hybrid IC. Application circuit that used 2W1-2 phase excitation (microstepping operation) mode.



A13261

Setting the Motor Current

The motor current I_{OH} is set by the Vref voltage on the hybrid IC pin 7. The following formula gives the relationship between I_{OH} and Vref.

$$RoX = (Ro2 \times 6k\Omega) \div (Ro2 + 6k\Omega) \quad (1)$$

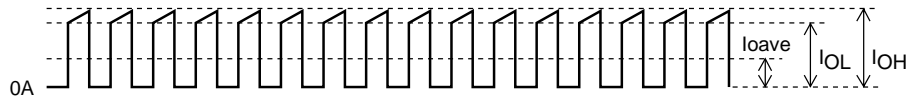
$$Vref = V_{CC2} \times RoX \div (Ro1 + RoX) \quad (2)$$

$$I_{OH} = \frac{1}{K} \times \frac{Vref}{Rs} \quad (3)$$

K: 5.16 (Voltage divider ratio),

Rs: 0.22Ω (This is the hybrid IC's internal current detection resistor. It has a tolerance of ±3%.)

Applications can use motor currents from the current (0.05 to 0.1A) set by the duty of the frequency set by the oscillator up to the limit of the allowable operating range, I_{OH} = 1.5A



Motor current waveform

A13262

Function Table

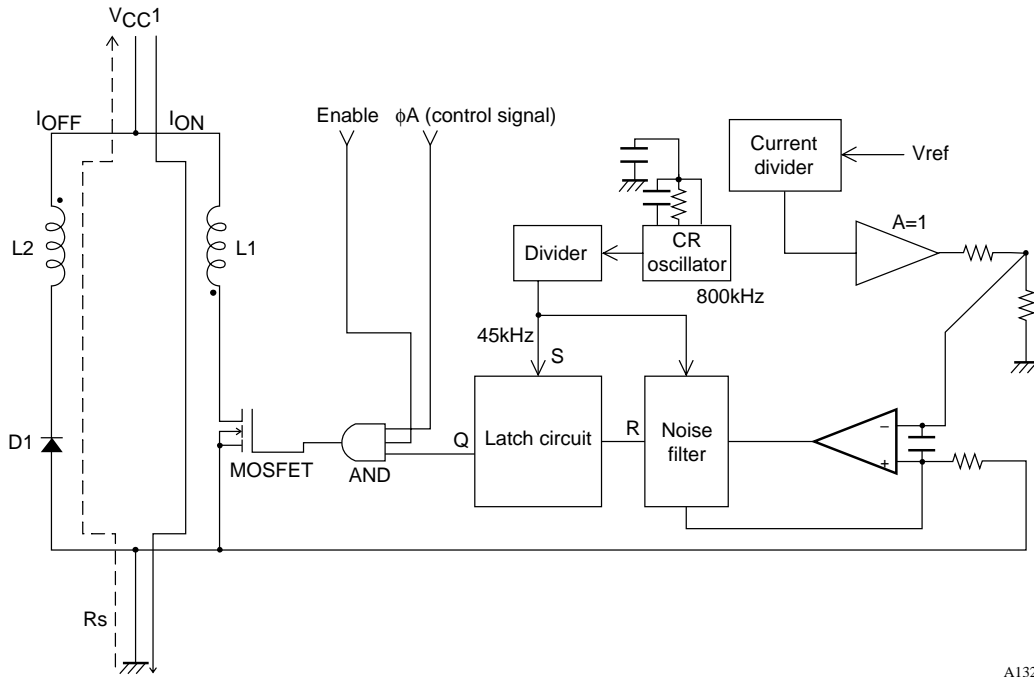
M2	0	0	1	1	Phase switching clock edge timing	
M1	0	1	0	1		
M3	1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only
	0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising and falling edges

	Forward	Reverse
CWB	0	1

ENABLE	Motor current is cut off when low
RESET	Active low

Functional Description

External Excitation Chopper Drive Block Description



Driver Block Basic Circuit Structure

Since this hybrid IC adopts an external excitation method, no external oscillator circuit is required.

When a high level is input to ϕA in the basic driver block circuit shown in the figure and the MOSFET is turned on, the comparator + input will go low and the comparator output will go low. Since a set signal with the PWM period will be input, the Q output will go high, and the MOSFET will be turned on as its initial value.

The current I_{ON} flowing in the MOSFET passes through L1 and generates a potential difference in R_s . Then, when the R_s potential and the V_{ref} potential become the same, the comparator output will invert, and the reset signal Q output will invert to the low level. Then, the MOSFET will be turned off and the energy stored in L1 will be induced in L2 and the current I_{OFF} will be regenerated to the power supply. This state will be maintained until the time when an input to the latch circuit set pin occurs.

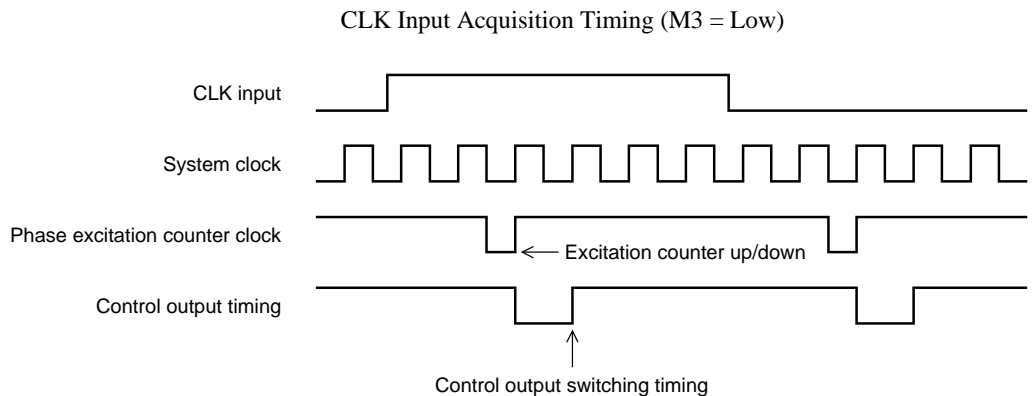
In this manner, the Q output is turned off and on repeatedly by the reset and set signals, thus implementing constant current control. The resistor and capacitor on the comparator input are spike removal circuit elements and synchronize with the PWM frequency. Since this hybrid IC uses a fixed frequency due to the external excitation method and at the same time also adopts a synchronized PWM technique, it can suppress the noise associated with holding a position when the motor is locked.

Input Pin Functions

Pin No.	Symbol	Function	Pin circuit type
11	CLK	Phase switching clock	Built-in pull-up resistor CMOS Schmitt trigger input
10	CWB	Rotation direction setting (CW/CCW)	Built-in pull-up resistor CMOS Schmitt trigger input
15	ENABLE	Output cutoff	Built-in pull-up resistor CMOS Schmitt trigger input
8, 9, 12	M1, M2, M3	Excitation mode setting	Built-in pull-up resistor CMOS Schmitt trigger input
13	RESET	System reset	Built-in pull-up resistor CMOS Schmitt trigger input
7	Vref	Current setting	Input impedance 6kΩ (typ.) ±30%

Input Signal Functions and Timing

- CLK (phase switching clock)
 - 1) Input frequency range: DC to 50kHz
 - 2) Minimum pulse width: 10µs
 - 3) Duty: 40 to 60% (However, the minimum pulse width takes precedence when M3 is high.)
 - 4) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
 - 5) Built-in multi-stage noise rejection circuit
 - 6) Function:
 - When M3 is high or open: The phase excited (driven) is advanced one step on each CLK rising edge.
 - When M3 is low: The phase is advanced one step by both rising and falling edges, for a total of two steps per cycle.



A13264

- CWB (Method for setting the rotation direction)
 - 1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
 - 2) Function:
 - When CWB is low: The motor turns in the clockwise direction.
 - When CWB is high: The motor turns in the counterclockwise direction.
 - 3) Notes: When M3 is low, the CWB input must not be changed for about 6.25µs before or after a rising or falling edge on the CLK input.

- ENABLE (Controls the on/off state of the A, \bar{A} , B, and \bar{B} excitation drive outputs and selects either operating or hold as the internal state of this hybrid IC.)
 - 1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure
 - 2) Function:
 - When ENABLE is high or open: Normal operating state
 - When ENABLE is low: This hybrid IC goes to the hold state and excitation drive output (motor current) is forcibly turned off. In this mode, the hybrid IC system clock is stopped and no inputs other than the reset input have any effect on the hybrid IC state.

• M1, M2, and M3 (Excitation mode and CLK input edge timing selection)

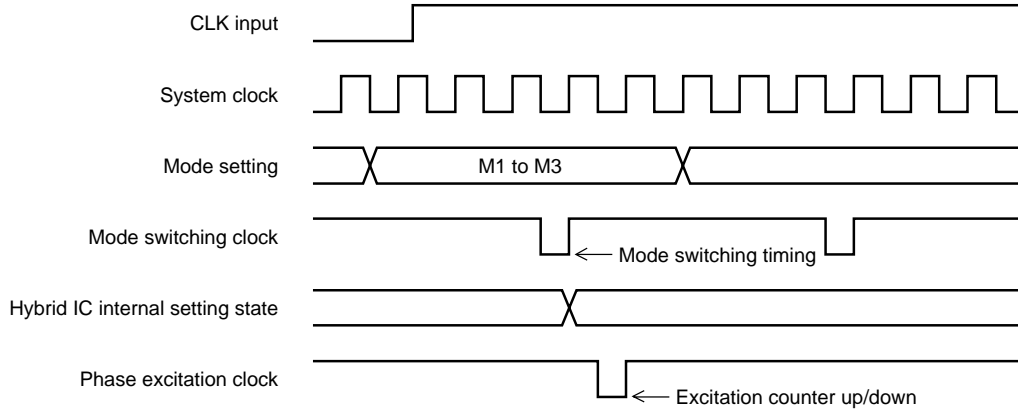
1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure

2) Function:

M2	0	0	1	1	Phase switching clock edge timing
M1	0	1	0	1	
M3	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Rising and falling edges

3) Valid mode setting timing: Applications must not change the mode in the period 5μs before or after a CLK signal rising or falling edge.

Mode Setting Acquisition Timing



A13265

• $\overline{\text{RESET}}$ (Resets all parts of the system.)

1) Pin circuit type: Built-in pull-up resistor (20kΩ, typical) CMOS Schmitt trigger structure

2) Function:

- All circuit states are set to their initial values by setting the $\overline{\text{RESET}}$ pin low. (Note that the pulse width must be at least 10μs.)

At this time, the A and \overline{B} phases are set to their origin, regardless of the excitation mode. The output current goes to about 71% after the reset is released.

3) Notes: When power is first applied to this hybrid IC, Vref must be established by applying a reset. Applications must apply a power on reset when the VCC2 power supply is first applied.

• Vref (Sets the current level used as the reference for constant-current detection.)

1) Pin circuit type: Analog input structure

2) Function:

- Constant-current control can be applied to the motor excitation current at 100% of the rated current by applying a voltage less than the control system power supply voltage VCC2 minus 2.5V.

- Applications can apply constant-current control proportional to the Vref voltage, with this value of 2.5V as the upper limit.

Output Pin Functions

Pin No.	Symbol	Function	Pin circuit type
14	MOI	Phase excitation origin monitor	Standard CMOS structure

Output Signal Functions and Timing

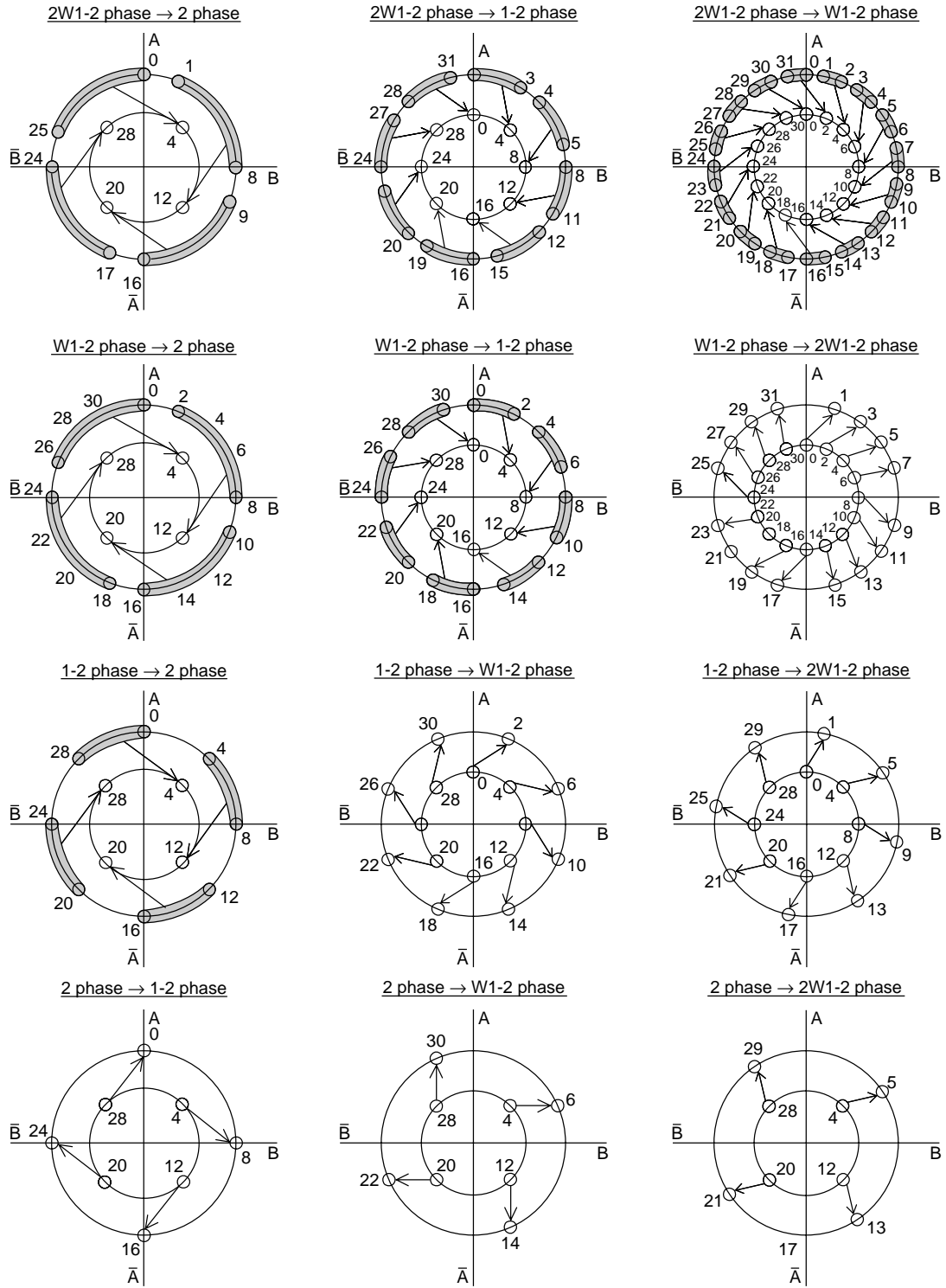
• A, \overline{A} , B, and \overline{B} (Motor phase excitation outputs)

1) Function:

- In the 4 phase and 2 phase excitation modes, a 3.75μs (typical) interval is set up between the A and \overline{A} and B and \overline{B} output signal transition times.

Phase States During Excitation Switching

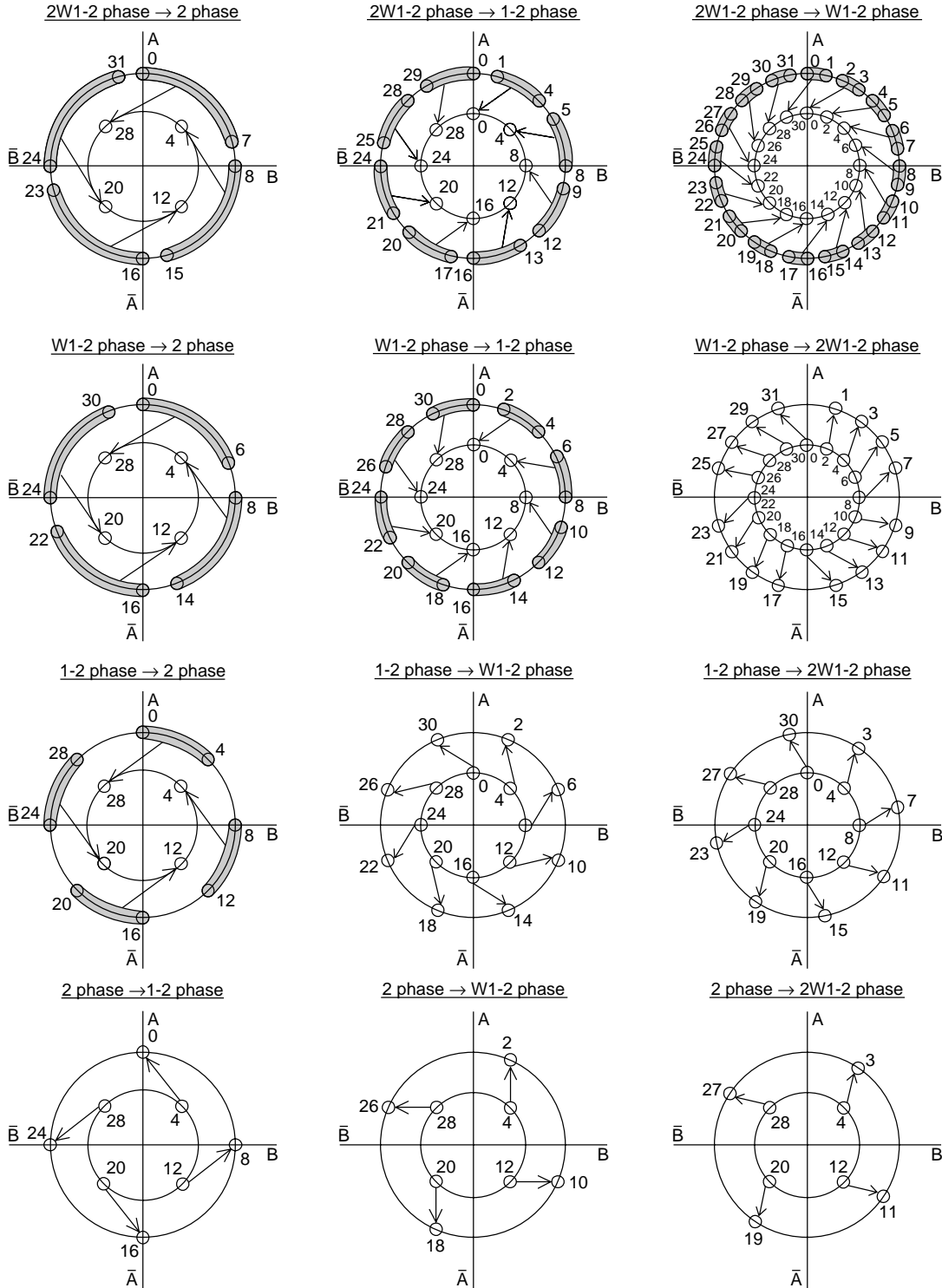
- Excitation phases before and after excitation mode switching <clockwise direction>



○ → Excitation phase according to the first clock input pulse after changing the excitation mode setting (M1 and M2)
 ↖ Excitation phase immediately before setting the excitation mode

A13266

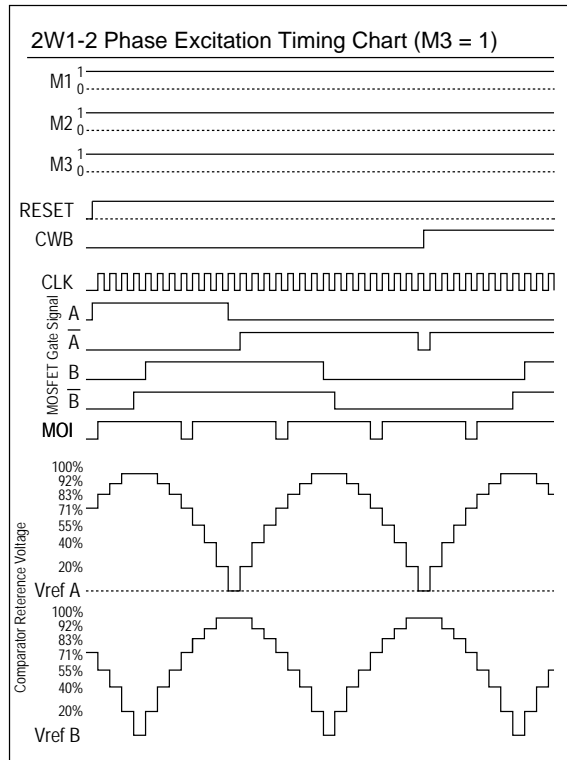
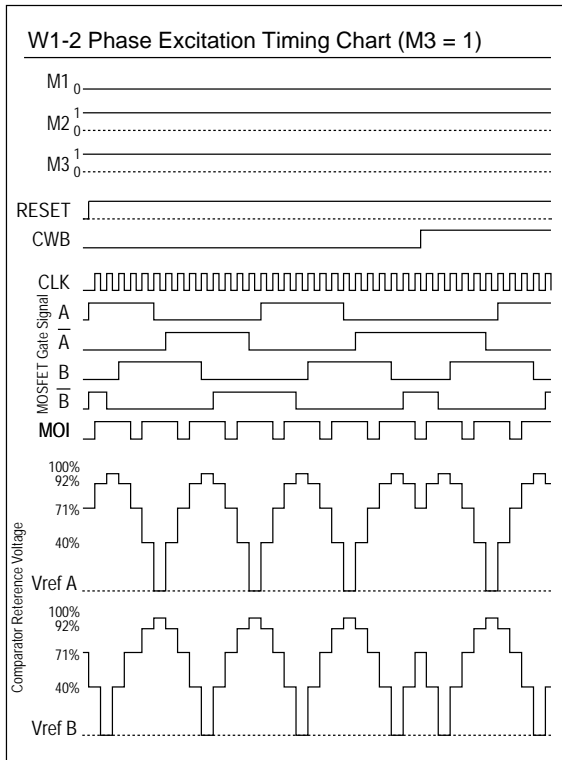
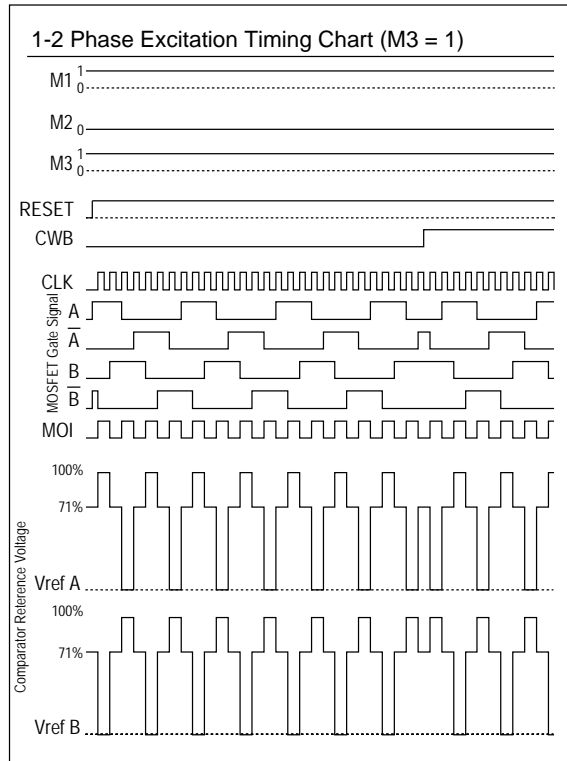
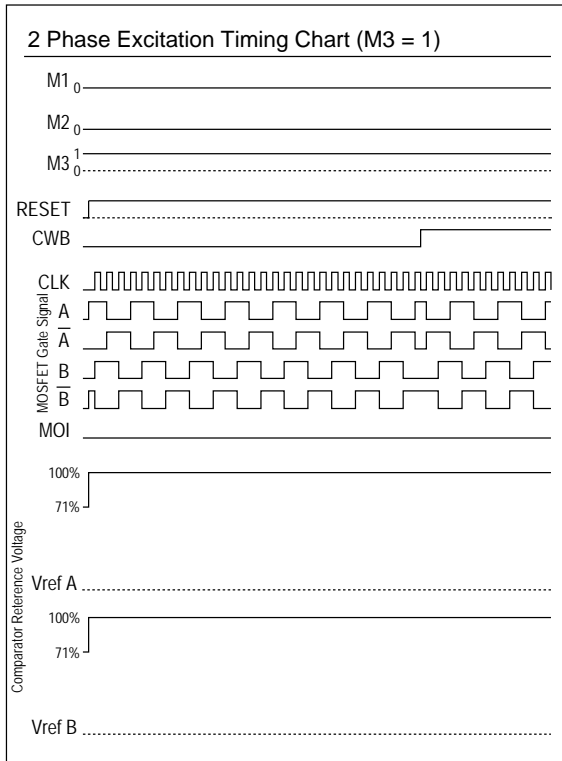
- Excitation phases before and after excitation mode switching <counterclockwise direction>



A13267

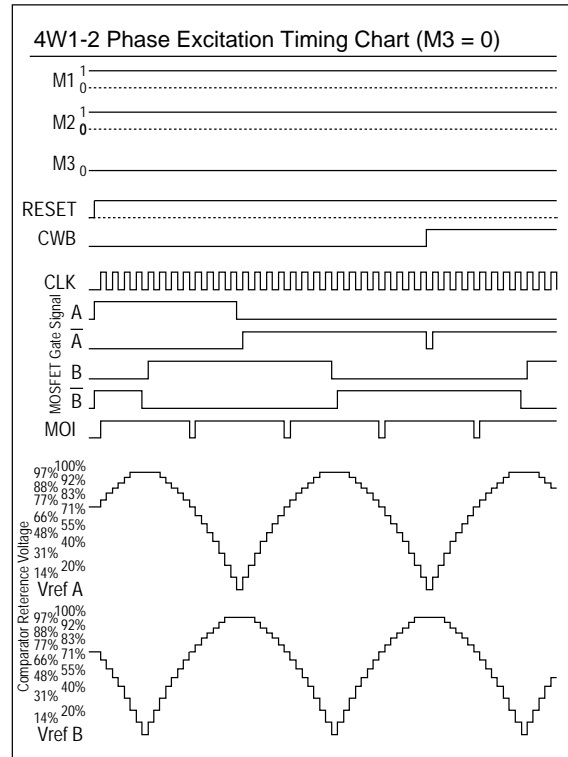
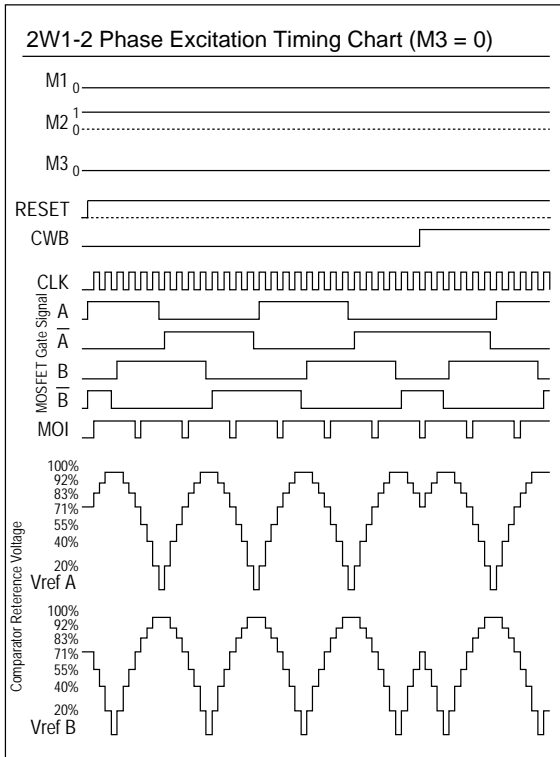
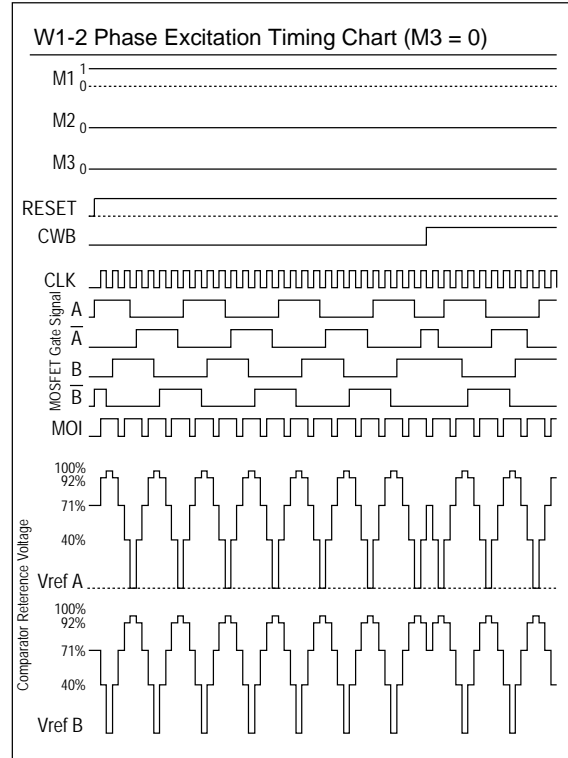
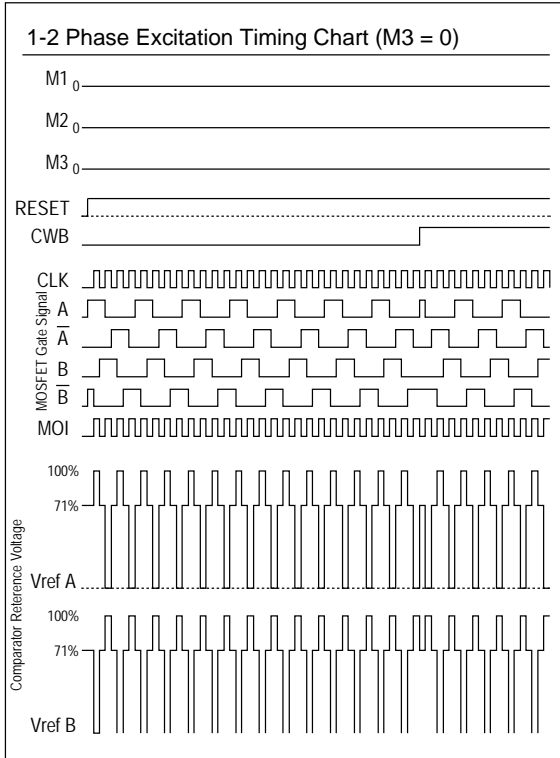
Excitation Time and Timing Charts

- CLK rising edge operation



A13268

• CLK rising and falling edge operation



A13269

Thermal Design

<Hybrid IC Average Internal Power Loss Pd>

The main elements internal to this hybrid IC with large average power losses are the current control devices, the regenerative current diodes, and the current detection resistor. Since sine wave drive is used, the average power loss during microstepping drive can be approximated by applying a waveform factor of 0.64 to the square wave loss during 2 phase excitation.

The losses in the various excitation modes are as follows.

2 phase excitation
$$Pd_{2EX} = (V_{sat}+V_{df}) \cdot \frac{f_{clock}}{2} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{2} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3)$$

1-2 phase excitation
$$Pd_{1-2EX} = 0.64 \cdot \left\{ (V_{sat}+V_{df}) \cdot \frac{f_{clock}}{4} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{4} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3) \right\}$$

W1-2 phase excitation
$$Pd_{W1-2EX} = 0.64 \cdot \left\{ (V_{sat}+V_{df}) \cdot \frac{f_{clock}}{8} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{8} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3) \right\}$$

2W1-2 phase excitation
$$Pd_{2W1-2EX} = 0.64 \cdot \left\{ (V_{sat}+V_{df}) \cdot \frac{f_{clock}}{16} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{16} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3) \right\}$$

4W1-2 phase excitation
$$Pd_{4W1-2EX} = 0.64 \cdot \left\{ (V_{sat}+V_{df}) \cdot \frac{f_{clock}}{16} \cdot I_{OH} \cdot t_2 + \frac{I_{OH} \cdot f_{clock}}{16} \cdot (V_{sat} \cdot t_1 + V_{df} \cdot t_3) \right\}$$

Here, t1 and t3 can be determined from the same formulas for all excitation methods.

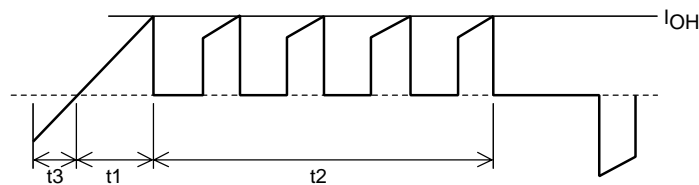
$$t_1 = \frac{-L}{R + 0.35} \cdot \ln \left(1 - \frac{R + 0.35}{V_{CC1}} \cdot I_{OH} \right) \qquad t_3 = \frac{-L}{R} \cdot \ln \left(\frac{V_{CC1} + 0.35}{I_{OH} \cdot R + V_{CC1} + 0.35} \right)$$

However, the formula for t2 differs with the excitation method.

2 phase excitation
$$t_2 = \frac{2}{f_{clock}} - (t_1 + t_3)$$
 1-2 phase excitation
$$t_2 = \frac{3}{f_{clock}} - t_1$$

W1-2 phase excitation
$$t_2 = \frac{7}{f_{clock}} - t_1$$
 2W1-2 phase excitation
$$t_2 = \frac{15}{f_{clock}} - t_1$$

 4W1-2 phase excitation



A13270

Motor Phase Current Model Figure (2 Phase Excitation)

- fclock : CLK input frequency (Hz)
- Vsat : The voltage drop of the power MOSFET and the current detection resistor (V)
- Vdf : The voltage drop of the body diode and the current detection resistor (V)
- I_{OH} : Phase current peak value (A)
- t1 : Phase current rise time (s)
- t2 : Constant-current operating time (s)
- t3 : Phase switching current regeneration time (s)
- V_{CC1} : Supply voltage applied to the motor (V)
- L : Motor inductance (H)
- R : Motor winding resistance (Ω)

<Determining the Size of the Hybrid IC Heat Sink>

Determine θ_{c-a} for the heat sink from the average power loss determined in the previous item.

$$\theta_{c-a} = \frac{T_{c \max} - T_a}{P_{dEX}} \text{ [}^\circ\text{C/W]}$$

$T_{c \max}$: Hybrid IC substrate temperature ($^\circ\text{C}$)

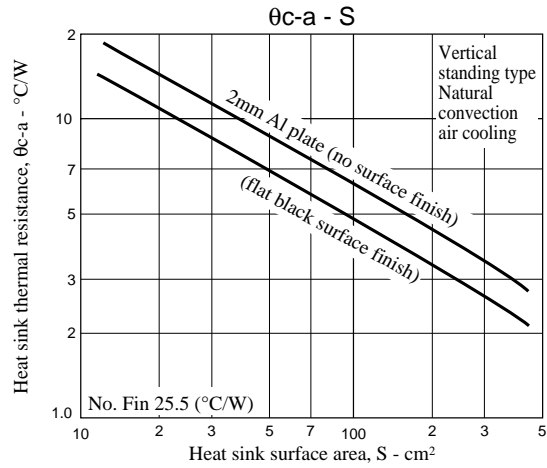
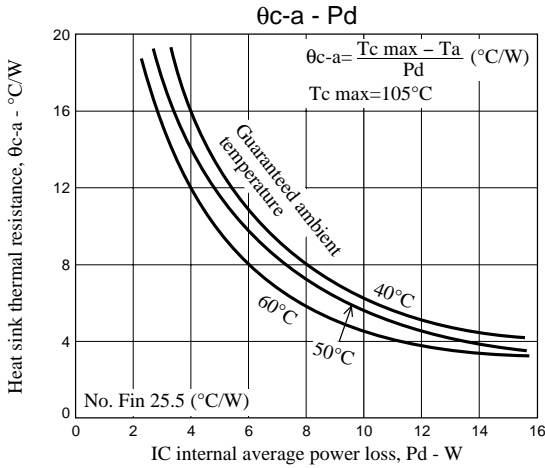
T_a : Application internal temperature ($^\circ\text{C}$)

P_{dEX} : Hybrid IC internal average loss (W)

Determine θ_{c-a} from the above formula and then size S (in cm^2) of the heat sink from the graphs shown below.

The ambient temperature of the device will vary greatly according to the air flow conditions within the application.

Therefore, always verify that the size of the heat sink is adequate to assure that the Hybrid IC back surface (the aluminum plate side) will never exceed a $T_{c \max}$ of 105°C , whatever the operating conditions are.



Next we determine the usage conditions with no heat sink by determining the allowable hybrid IC internal average loss from the thermal resistance of the hybrid IC substrate, namely 25.5°C/W .

For a $T_{c \max}$ of 105°C at an ambient temperature of 50°C

$$P_{dEX} = \frac{100 - 50}{25.5} = 2.15\text{W}$$

For a $T_{c \max}$ of 105°C at an ambient temperature of 40°C

$$P_{dEX} = \frac{100 - 40}{25.5} = 2.54\text{W}$$

This hybrid IC can be used with no heat sink as long as it is used at operating conditions below the losses listed above. (See $\Delta T_c - P_d$ curve in the graph on page 17.)

<Hybrid IC internal power element (MOSFET) junction temperature calculation>

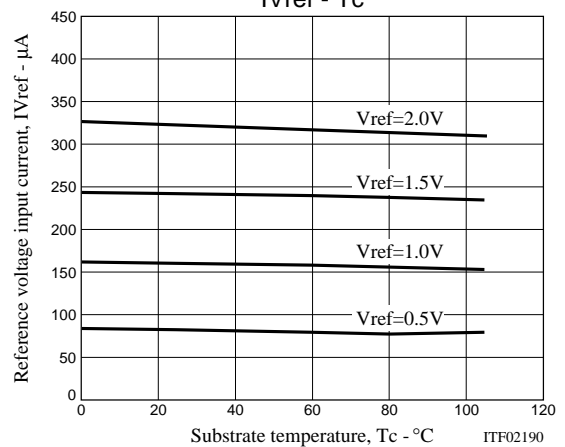
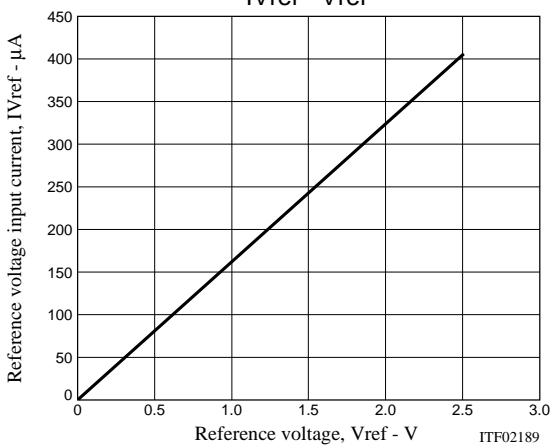
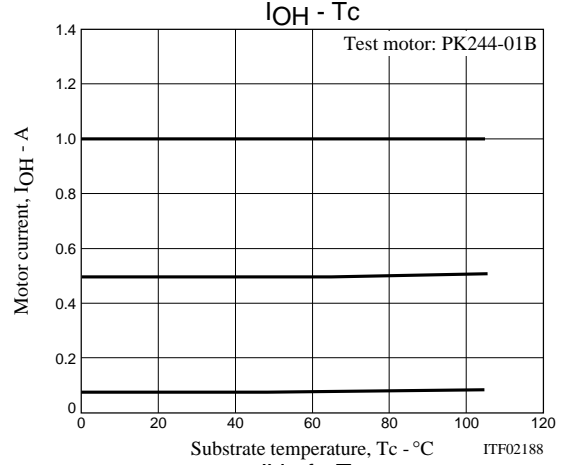
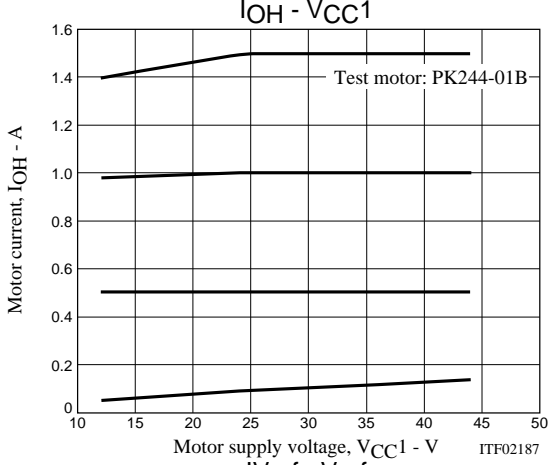
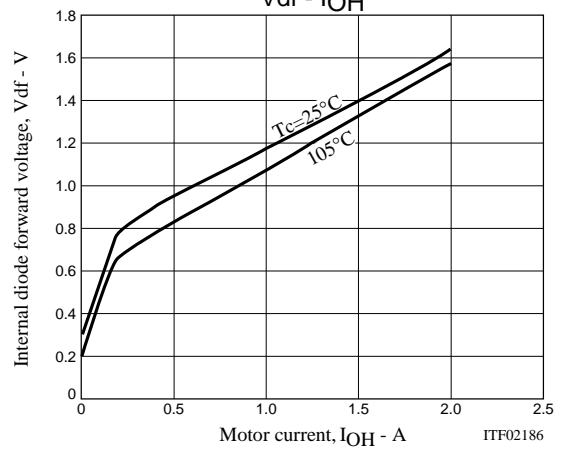
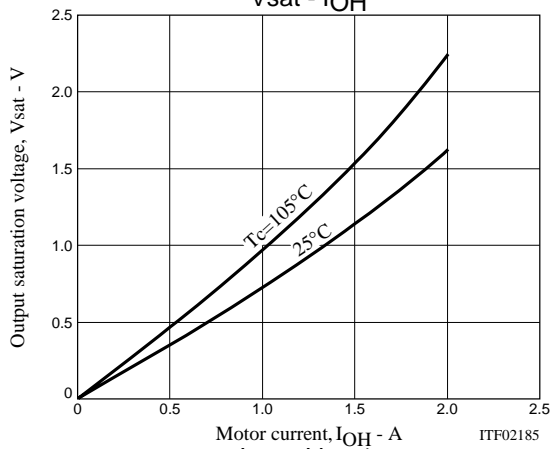
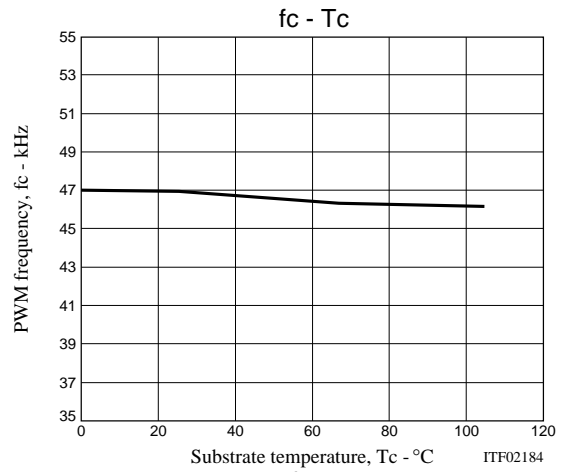
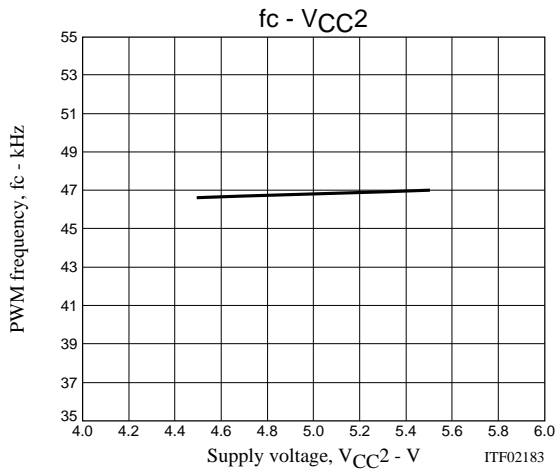
The junction temperature, T_j , of each device can be determined from the loss P_{ds} in each transistor and the thermal resistance θ_{j-c} .

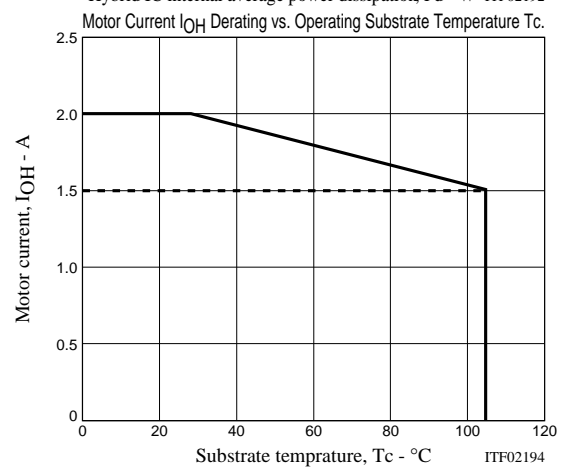
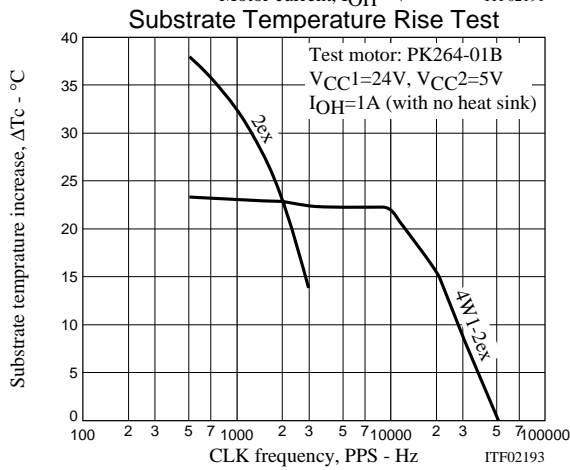
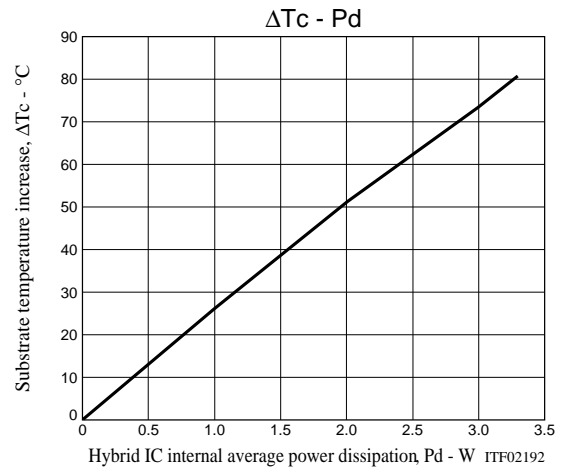
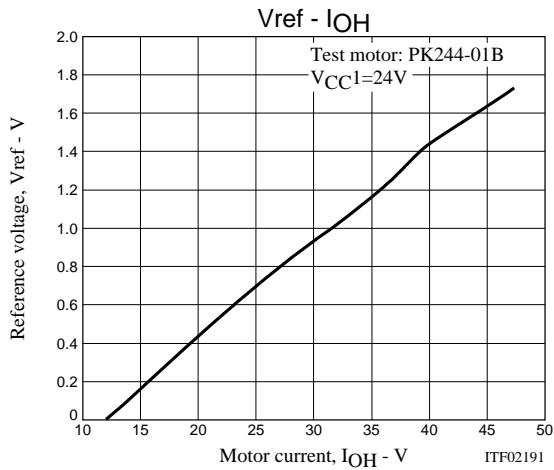
$$T_j = T_c + \theta_{j-c} \times P_{ds} \text{ (}^\circ\text{C)}$$

Here, we determine P_{ds} , the loss for each transistor, by determining P_{dEX} in each excitation mode.

$$P_{ds} = P_{dEX}/4$$

The steady-state thermal resistance θ_{j-c} of a power MOSFET is 19.2°C/W .





Notes

- The current ranges shown above apply when the output voltage is not in the avalanche range.
- The operating substrate temperature Tc values shown above are measured during motor operation. Since Tc varies with the ambient temperature Ta, the value of IOH, and whether IOH is continuous or intermittent, it must be measured in an actual operating system.

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of June, 2008. Specifications and information herein are subject to change without notice.