Description

The ACS8525A is a highly integrated, single-chip solution for “Hit-less” protection switching of SEC (SDH/SONET Equipment Clock) + Sync clock “Groups”, from Master and Slave SETS clock cards and a third (Stand-by) source, for Line Cards in a SONET or SDH Network Element. The ACS8525A has fast activity monitors on the SEC clock inputs and will implement automatic system protection switching against the Master clock failure. The selection of the Master/Slave input can be forced by a Force Fast Switch pin. If both the Master and Slave input clocks fail, the Stand-by “Group” is selected or, if no Stand-by is available, the device enters Digital Holdover mode.

The ACS8525A can perform frequency translation, converting, for example, an 8 kHz SEC input clock from a backplane into a 155.52 MHz clock for local line cards.

Master and Slave SEC inputs to the device support TTL/CMOS and PECL/LVDS. The Stand-by SEC and three Sync inputs are TTL/CMOS only.

The ACS8525A generates two SEC clock outputs, via one PECL/LVDS and one TTL/CMOS port, with spot frequencies from 2 kHz up to 311.04 MHz (up to 155.52 MHz on the TTL/CMOS port). It also provides an 8 kHz Frame Sync and a 2 kHz Multi-Frame Sync signal output with programmable pulse width and polarity.

The ACS8525 includes a Serial Port, which can be SPI compatible, providing access to the configuration and status registers for device setup.

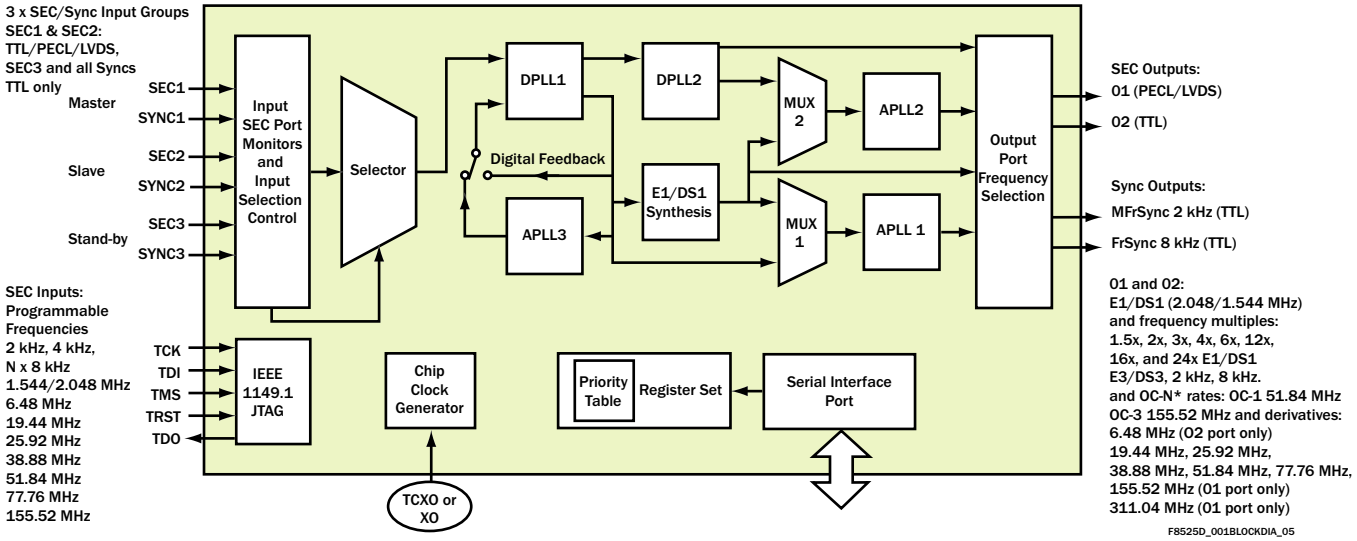
IEEE 1149.1 JTAG Boundary Scan is supported.

Features

- SONET/SDH applications up to OC-3/STM-1 bit rate.
- Switches between grouped inputs (SEC/Sync pairs).
- Inputs: three SECs at any of 2, 4, 8 kHz (and N x 8 kHz multiples up to 155.52 MHz), plus Frame Sync/Multi-Frame Sync.
- Outputs: two SEC clocks at any of several spot frequencies from 2 kHz up to 77.76 MHz via the TTL/CMOS port and up to 311.04 MHz via the PECL/LVDS port.
- Selectable clock I/O port technologies.
- Modes for E3/DS3 and multiple E1/DS1 rate output clocks.
- Frequency translation of SEC input clock to a different local line card clock.
- Robust input clock source activity monitoring on all inputs.
- Supports Free-run, Locked and Digital Holdover modes of operation.
- Automatic “Hit-less” source switchover on loss of input.
- External force fast switch between SEC1/SEC2 inputs.
- Phase Build-out for output clock phase continuity during input switchover.
- PLL “Locked” and “Acquisition” bandwidths individually selectable from 18, 35 or 70 Hz.
- Serial interface for device set-up.
- Single 3.3 V operation.
- Operating temperature (ambient) of 0 to +70°C.
- Available in LQFP 64 package.
- Lead (Pb)-free version available (ACS8525T), RoHS and WEEE compliant.

Block Diagram

Figure 1 Block Diagram of the ACS8525A LC/P



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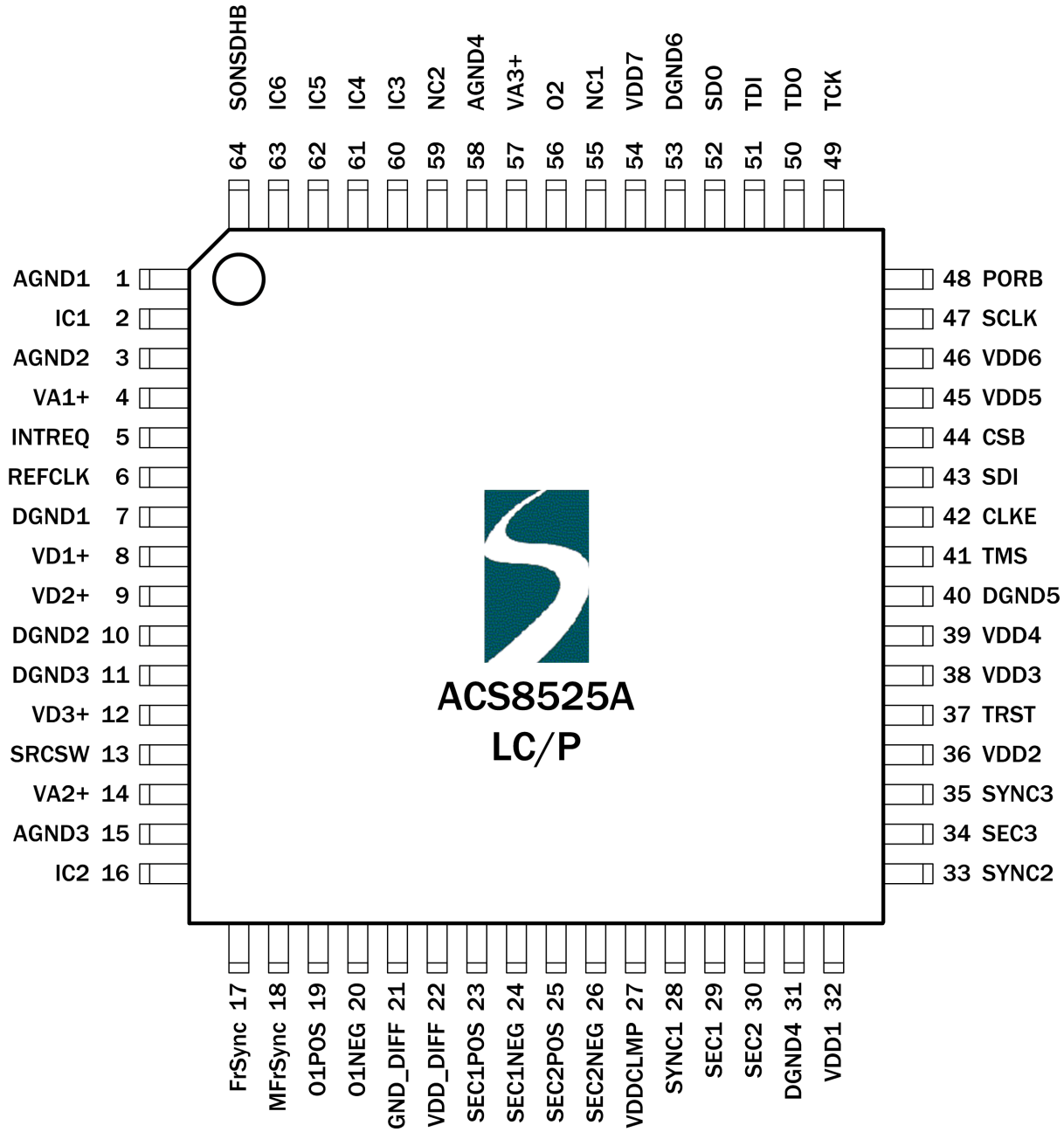
Pin Diagram

Figure 2 ACS8525A Pin Diagram Line Card Protection Switch for SONET/SDH Systems



Pin Description

Table 1 Power Pins

Pin Number	Symbol	I/O	Type	Description
8, 9, 12	VD1+, VD2+, VD3+	P	-	Supply Voltage: Digital supply to gates in analog section, +3.3 Volts ±5%.
22	VDD_DIFF	P	-	Supply Voltage: Digital supply for differential output pins 19 and 20, +3.3 Volts ±5%.
27	VDDCLMP	P	-	Digital Supply for input over-voltage clamping to +3.3 volts. Leave floating for no clamping.
32, 36, 38, 39, 45, 46, 54	VDD1, VDD2, VDD3, VDD4, VDD5, VDD6, VDD7	P	-	Supply Voltage: Digital supply to logic, +3.3 Volts ±5%.
4	VA1+	P	-	Supply Voltage: Analog supply to clock multiplying PLL, +3.3 Volts ±5%.
14, 57	VA2+, VA3+	P	-	Supply Voltage: Analog supply to output PLLs APLL2 and APPL1, +3.3 Volts ±5%.
15, 58	AGND3, AGND4		-	Supply Ground: Analog ground for output PLLs APLL2 and APPL1.
7, 10, 11	DGND1, DGND2, DGND3	P	-	Supply Ground: Digital ground for components in PLLs.
31, 40, 53	DGND4, DGND5, DGND6	P	-	Supply Ground: Digital ground for logic.
21	GND_DIFF	P	-	Supply Ground: Digital ground for differential ports.
1, 3	AGND1, AGND2	P	-	Supply Ground: Analog grounds.

Note...I = Input, O = Output, P = Power, TTL^U = TTL input with pull-up resistor, TTL_D = TTL input with pull-down resistor.

Table 2 Internally Connected

Pin Number	Symbol	I/O	Type	Description
2, 16, 60, 61, 62, 63	IC1, IC2, IC3, IC4, IC5, IC6,	-	-	Internally Connected: Leave to float.
55, 59	NC1, NC2	-	-	Not Connected: Leave to float.

Table 3 Other Pins

Pin Number	Symbol	I/O	Type	Description
5	INTREQ	O	TTL/CMOS	Interrupt Request: Active *High/Low* software Interrupt output.
6	REFCLK	I	TTL	Reference Clock: 12.800 MHz (refer to section headed Local Oscillator Clock).
13	SRCSW	I	TTL_D	Source Switching: Force Fast Source Switching on SEC1 and SEC2.
17	FrSync	O	TTL/CMOS	Output Reference: 8 kHz Frame Sync output.

Table 3 Other Pins (cont...)

Pin Number	Symbol	I/O	Type	Description
18	MFrSync	O	TTL/CMOS	Output Reference: 2 kHz Multi-Frame Sync output.
19, 20	O1POS, O1NEG	O	LVDS/PECL	Output Reference: Programmable, default 38.88 MHz, LVDS.
23, 24	SEC1_POS, SEC1_NEG	I	PECL/LVDS	Input Reference: Programmable, default 19.44 MHz, PECL.
25, 26	SEC2_POS, SEC2_NEG	I	PECL/LVDS	Input Reference: Programmable, default 19.44 MHz PECL.
28	SYNC1	I	TTL_D	(Master) Multi-Frame Sync 2kHz Input: Connect to 2 or 8 kHz Multi-Frame Sync output of Master SETS.
29	SEC1	I	TTL_D	(Master) Input Reference: Programmable, default 8 kHz.
30	SEC2	I	TTL_D	(Slave) Input Reference: Programmable, default 8 kHz.
33	SYNC2	I	TTL_D	(Slave) Multi-Frame Sync 2 kHz: Connect to 2 or 8 kHz Multi-Frame Sync output of Slave SETS.
34	SEC3	I	TTL_D	(Stand-by) Input Reference: External stand-by reference clock source, programmable, default 19.44MHz.
35	SYNC3	I	TTL_D	(Stand-by) Input Reference: External stand-by 2 or 8 kHz Multi-Frame Sync clock source.
37	TRST	I	TTL_D	JTAG Control Reset Input: TRST = 1 to enable JTAG Boundary Scan mode. TRST = 0 is Boundary Scan stand-by mode, still allowing normal device operation (JTAG logic transparent). NC if not used.
41	TMS	I	TTL_D	JTAG Test Mode Select: Boundary Scan enable. Sampled on rising edge of TCK. NC if not used.
42	CLKE	I	TTL_D	SCLK Edge Select: SCLK active edge select, CLKE = 1, selects falling edge of SCLK to be active.
43	SDI	I	TTL_D	Serial Interface Address: Serial Data Input.
44	CSB	I	TTL^U	Chip Select (Active *Low*): This pin is asserted *Low* by the microprocessor to enable the microprocessor interface.
47	SCLK	I	TTL_D	Serial Data Clock. When this pin goes *High* data is latched from SDI pin.
48	PORB	I	TTL^U	Power-On Reset: Master reset. If PORB is forced *Low*, all internal states are reset back to default values.
49	TCK	I	TTL_D	JTAG Clock: Boundary Scan clock input.
50	TDO	O	TTL/CMOS	JTAG Output: Serial test data output. Updated on falling edge of TCK.
51	TDI	I	TTL_D	JTAG Input: Serial test data Input. Sampled on rising edge of TCK.
52	SDO	O	TTL_D	Interface Address: SPI compatible Serial Data Output.
56	O2	O	TTL/CMOS	Output Reference: Programmable, default 19.44 MHz.
64	SONSDHB	I	TTL_D	SONET or SDH Frequency Select: Sets the initial power-up state (or state after a PORB) of the SONET/SDH frequency selection registers, Reg. 34, Bit 2 and Reg. 38, Bit 5, Bit 6 and Reg. 64 Bit 4. When set *Low*, SDH rates are selected (2.048 MHz etc.) and when set *High*, SONET rates are selected (1.544 MHz etc.) The register states can be changed after power-up by software.

Introduction

The ACS8525A is a highly integrated, single-chip solution for “Hit-less” protection switching of SEC + Sync clock “Groups”, from Master and Slave SETS clock cards and a third (Stand-by) source, for Line Cards in a SONET or SDH Network Element. The ACS8525A has fast activity monitors on the SEC clock inputs and will implement automatic system protection switching against failure of the selected clock. The selection of the Master/Slave input can be forced by a Force Fast Switch pin. The Stand-by “Group” is selected if both the Master and Slave input clocks fail, or, if not available, the device enters a Digital Holdover mode.

Digital Phase Locked Loop (DPLL) and Direct Digital Synthesis (DDS) methods are used in the device so that the overall PLL characteristics are very stable and consistent compared to traditional analog PLLs.

The ACS8525A has three SEC/SYNC input groups from which it can select any group as input. It generates independent clocks on outputs 01 and 02, with a total of 53 possible output frequencies, and generates two Sync outputs on outputs FrSync and MFrSync: 8 kHz Frame Synchronization (FrSync) signal and 2 kHz Multi-Frame Synchronization (MFrSync) signal.

The device has three main operating modes (states); Free-run, Locked, or Digital Holdover. In Free-Run mode, the ACS8525A generates a stable, low-noise clock signal at a frequency to the same accuracy as the external oscillator, or it can be made more accurate via software calibration to within ±0.02 ppm. In Locked mode, the ACS8525A selects the most appropriate of the three input SECs and generates a stable, low-noise clock signal locked to the selected reference. In Digital Holdover mode, the ACS8525A generates a stable, low-noise clock signal, adjusted to match the frequency of the last selected SEC.

One key architectural advantage that the ACS8525A has over traditional solutions is in the use of DPLL technology for precise and repeatable performance over temperature or voltage variations and between parts. The overall PLL bandwidth, loop damping, pull-in range and frequency accuracy are all determined by digital parameters that provide a consistent level of performance. An Analog PLL (APLL) takes the signal from the DPLL output and provides a lower jitter output. The APLL bandwidth is set four orders of magnitude higher than the DPLL bandwidth. This ensures that the overall system performance still maintains the advantage of consistent behavior provided by the digital approach.

The DPLLs are clocked by the external Oscillator module (TCXO or XO) so that the Free-run or Digital Holdover frequency stability is only determined by the stability of the external oscillator module. This second key advantage confines all temperature critical components to one well defined and pre-calibrated module, whose performance can be chosen to match the application.

All performance parameters of the DPLLs are programmable without the need to understand detailed PLL equations. Bandwidth, damping factor and lock range can all be set directly.

The ACS8525A includes an SPI compatible serial interface port, providing access to the configuration and status registers for device setup, external control and monitoring. The device is primarily controlled according to values in this Register block.

Each register (8-bit wide data field) is identified and referred to by its two-digit hexadecimal address and name, e.g. Reg. 7D *cnfg_interrupt*. The “Register Map” on page 38 summarizes the content of all of the registers, and each register is individually described in the subsequent Register Tables, organized in order of ascending Address (hexadecimal), in the “Register Descriptions” from page 42 onwards.

An Evaluation Board and intuitive GUI-based software package is available for this device to help designers learn how to use the ACS8525A and rapidly configure the device for particular applications. This has its own documentation: “ACS8525-EVB”.

General Description

The following description refers to the Block Diagram (Figure 1 on page 1).

Inputs

The ACS8525A SETS device has input ports for input clock groups from three sources, typically Master, Slave and Stand-by, where each clock group comprises one SEC and optionally one Sync signal. This is so that when any SEC input changeover is made, the corresponding Sync signal changeover is also made.

TTL/CMOS and PECL/LVDS ports are provided for the Master and Slave SEC inputs to the device. The Stand-by SEC input and three Frame Sync/Multi-frame Sync inputs to the device are via TTL Ports. All the TTL/CMOS parts are 3 V compatible (with clamping if required by connecting the VDDCLMP pin). Refer to the “Electrical Specifications”

on page 98 for more information on electrical compatibility.

Input frequencies supported range from 2 kHz to 155.52 MHz. Common E1, DS1, OC-3 and sub-divisions are supported as spot frequencies that the DPLLs will directly lock to. Any input frequency, up to 100 MHz, that is a multiple of 8 kHz can also be locked to via an inbuilt programmable divider.

Preconfiguring Inputs

Each input device has to be preconfigured with:

- Expected input frequency *cnfg_ref_source_frequency* register (Reg. 22 to 25 and 28)
- Technology (TTL or PECL/LVDS) where applicable, via *cnfg_differential_inputs* (Reg. 36)
- Selection Priority (Reg. 19, 1A and 1C).

Table 4 gives details of the input reference ports, showing the input technologies and the range of frequencies supported on each port; the default spot frequencies and default priorities assigned to each port on power-up or by reset are also shown.

SDH and SONET networks use different default frequencies; the network type is selectable using the *cnfg_input_mode* Reg. 34 Bit 2, *ip_sonsdhb*.

- For SONET, *ip_sonsdhb* = 1
- For SDH, *ip_sonsdhb* = 0

On power-up or by reset, the default will be set by the state of the SONSDHB pin (pin 64). Specific frequencies and priorities are set by configuration.

The frequency selection is programmed via the *cnfg_ref_source_frequency* register (Reg. 22 - Reg. 28).

Table 4 Input Reference Source Selection and Priority Table

Port Name	Channel Number (Bin)	Input Port Technology	Frequencies Supported	Default Priority
SEC1 TTL	0011	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	2
SEC2 TTL	0100	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 8 kHz Default (SDH): 8 kHz	3
SEC1 DIFF	0101	PECL/LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	0
SEC2 DIFF	0110	PECL/LVDS PECL default	Up to 155.52 MHz (see Note (ii)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	0
SYNC1	0111	TTL/CMOS	2/4/8 kHz auto-sensing	n/a
SYNC2	1000	TTL/CMOS	2/4/8 kHz auto-sensing	n/a
SEC3	1001	TTL/CMOS	Up to 100 MHz (see Note (i)) Default (SONET): 19.44 MHz Default (SDH): 19.44 MHz	4
SYNC3	1010	TTL/CMOS	2/4/8 kHz auto-sensing	n/a

Notes: (i) TTL ports (compatible also with CMOS signals) support clock speeds up to 100 MHz, with the highest spot frequency being 77.76 MHz. The actual spot frequencies are: 2 kHz, 4 kHz, 8 kHz (and N x 8 kHz), 1.544 MHz (SONET)/2.048 MHz (SDH), 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz. SONET or SDH input rate is selected via Reg. 34 Bit 2, ip_sonsdhb).

(ii) PECL and LVDS ports support the spot clock frequencies listed above plus 155.52 MHz (and 311.04 MHz for Output O1 only).

(iii) SEC1 TTL and SEC2 TTL ports are on pins SEC1 and SEC2. SEC1 DIFF (Differential) port uses pins SEC1POS and SEC1NEG, similarly SEC2DIFF uses pins SEC2POS and SEC2NEG.

PECL/LVDS Input Port Selection

The choice of PECL or LVDS compatibility is programmed via the *cnfg_differential_inputs* register. Unused PECL differential inputs should be fixed with one input *High* (VDD) and the other input *Low* (GND), or set in LVDS mode and left floating, in which case one input is internally pulled *High* and the other *Low*.

Input Locking Frequency Modes

Each input port has to be configured to receive the expected input frequency. To achieve this, three Input Locking Frequency modes are provided: Direct Lock, Lock8K and DivN.

Direct Lock Mode

In Direct Lock mode, DPLL1 can lock to the selected input at the spot frequency of the input, for example 19.44 MHz performs the DPLL phase comparisons at 19.44 MHz.

In Lock8K and DivN modes (and for the special case of 155 MHz), an internal divider is used prior to DPLL1 to divide the input frequency before it is used for phase comparisons.

Direct Lock Mode 155 MHz.

The max frequency allowed for phase comparison is 77.76 MHz, so for the special case of a 155 MHz input set to Direct Lock mode, there is a divide-by-two function automatically selected to bring the frequency down to within the limits of operation.

Lock8K Mode

Lock8K mode automatically sets the divider parameters to divide the input frequency down to 8 kHz. Lock8K can only be used on the supported spot frequencies (see Table 4 Note(i)). Lock8k mode is enabled by setting the *Lock8k* bit (Bit 6) in the appropriate *cnfg_ref_source_frequency* register location. Using lower frequencies for phase comparisons in the DPLL results in a greater tolerance to input jitter. It is possible to choose which edge of the input reference clock to lock to, by setting *8K Edge Polarity (*Bit 2 of Reg. 03, *test_register1*).

DivN Mode

In DivN mode, the divider parameters are set manually by configuration (Bit 7 of the *cnfg_ref_source_frequency* register), but must be set so that the frequency after division is 8 kHz.

The DivN function is defined as:

DivN = “Divide by N + 1”, i.e. it is the dividing factor used for the division of the input frequency, and has a value of (N + 1) where N is an integer from 1 to 15624 inclusive.

Therefore, in DivN mode the input frequency can be divided by any integer value between 2 to 15625. Consequently, any input frequency which is a multiple of 8 kHz, between 8 kHz and 125 MHz, can be supported by using DivN mode.

Note...Any reference input can be set to use DivN independently of the frequencies and configurations of the other inputs. However only one value of N is allowed, so all inputs with DivN selected must be running at the same frequency.

DivN Examples

(a) To lock to 2.000 MHz:

(i) Set the *cnfg_ref_source_frequency* register to 10XX0000 (binary) to enable DivN, and set the frequency to 8 kHz - the frequency required after division. (XX = “Leaky Bucket” ID for this input).

(ii) To achieve 8 kHz, the 2 MHz input must be divided by 250. So, if DivN = 250 = (N + 1) then N must be set to 249. This is done by writing F9 hex (249 decimal) to the DivN register pair Reg. 46/47.

(b) To lock to 10.000 MHz:

(i) The *cnfg_ref_source_frequency* register is set to 10XX0000 (binary) to set the DivN and the frequency to 8 kHz, the post-division frequency. (XX = “Leaky Bucket” ID for this input).

(ii) To achieve 8 kHz, the 10 MHz input must be divided by 1,250. So, if DivN, = 250 = (N+1) then N must be set to 1,249. This is done by writing 4E1 hex (1,249 decimal) to the DivN register pair Reg. 46/47.

Input SEC Activity Monitors

An input reference activity monitor is assigned to each of the three SEC inputs. The monitors operate continuously such that at all times the activity status of each SEC input is known.

SEC activity monitoring is used to declare whether or not an input is valid. Any SEC that suffers a loss-of-activity will be declared as invalid and unavailable for selection.

SEC activity monitoring is a continuous process which is used to identify clock problems. There is a difference in

dynamics between the selected clock and the other reference clocks. Anomalies occurring on non-selected SECs affect only that source's suitability for selection, whereas anomalies occurring on the selected clock could have a detrimental impact on the accuracy of the output clock.

Leaky Bucket Accumulator

Anomalies detected by the Activity Monitor are integrated in a Leaky Bucket Accumulator. There is one Leaky Bucket Accumulator per SEC input. Each Leaky Bucket can be programmed with a Bucket ID (0 to 3) which assigns to the Leaky Bucket the corresponding Leaky Bucket Configuration (from four available Configurations). Each Leaky Bucket Configuration comprises the following programmable parameters (See Reg. 50 to Reg. 5F):

- Bucket size
- Alarm trigger (set threshold)
- Alarm clear (reset threshold)
- Leak rate (decay rate)

There are occasional anomalies that do not cause the Accumulator to cross the alarm setting threshold, so the selected SEC is retained. Persistent anomalies cause the alarm setting threshold to be crossed and result in the selected SEC being rejected.

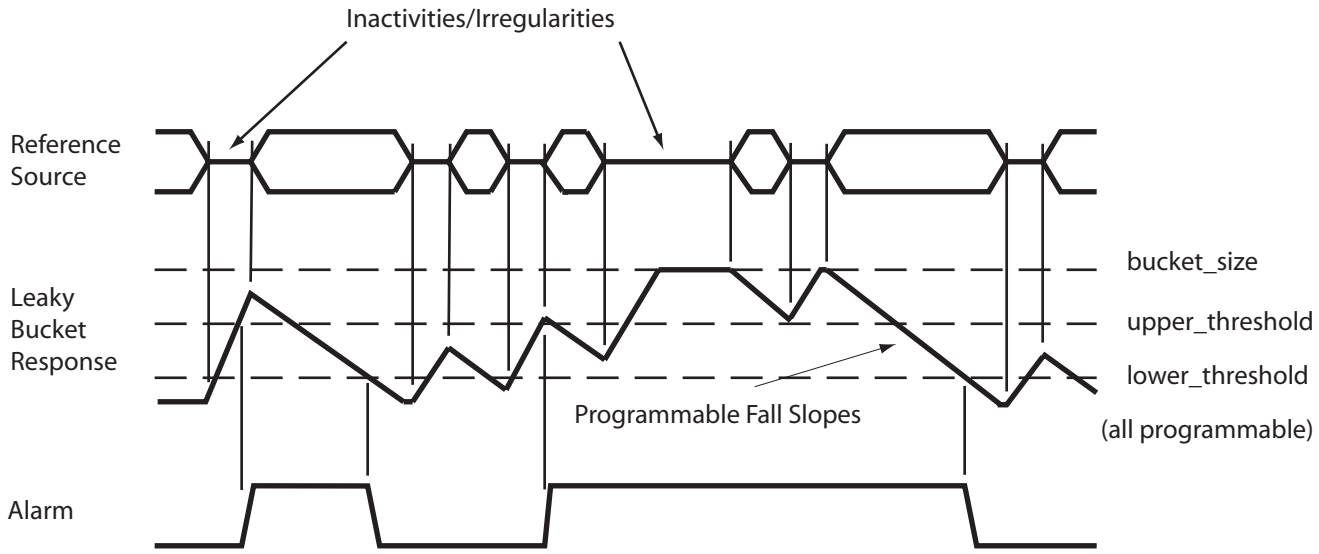
Each Leaky Bucket Accumulator is a digital circuit which mimics the operation of an analog integrator. If several events occur close together, each event adds to the amplitude and the alarm will be triggered quickly; if events occur over a greater time period but still sufficiently close together to overcome the decay, the alarm will be triggered eventually. If events occur at a rate which is not sufficient to overcome the decay, the alarm will not be triggered. Similarly, if no defect events occur for a sufficient time, the amplitude will decay gradually and the alarm will be cleared when the amplitude falls below the alarm clearing threshold. The ability to decay the amplitude over time allows the importance of defect events to be reduced as time passes by. This means that, in the case of isolated events, the alarm will not be set, whereas, once the alarm becomes set, it will be held on until normal operation has persisted for a suitable time (but if the operation is still erratic, the alarm will remain set).

Figure 3 illustrates the behavior of the Leaky Bucket Accumulator.

Each SEC input is monitored over a 128 ms period. If, within a 128 ms period, an irregularity occurs that is not deemed to be due to allowable jitter/wander, then the accumulator is incremented.

The Accumulator will continue to increment up to the point that it reaches the programmed Bucket size. The “fill rate” of the Leaky Bucket is, therefore, 8 units/second. The “leak rate” of the Leaky Bucket is programmable to be in multiples of the fill rate (x 1, x 0.5, x 0.25 and x 0.125) to give a programmable leak rate from 8 units/sec down to 1 unit/sec. A conflict between trying to “leak” at the same time as a “fill” is avoided by preventing a leak when a fill event occurs.

Figure 3 Inactivity and Irregularity Monitoring



Disqualification of a non-selected SEC is based on inactivity noted by the Activity Monitors. The currently selected SEC can be disqualified for being out-of phase, inactive, or if the source is outside the DPLL lock range.

If the currently selected SEC is disqualified, the next highest priority qualified SEC is selected.

Interrupts for Activity Monitors

The loss of the currently selected SEC will eventually cause the input to be considered invalid, triggering an interrupt. The time taken to raise this interrupt is dependant on the Leaky Bucket Configuration of the activity monitors. The fastest Leaky Bucket setting will still take up to 128 ms to trigger the interrupt. The interrupt caused by the brief loss of the currently selected SEC is provided to facilitate very fast source failure detection if desired. It is triggered after missing just a couple of cycles of the SEC. Some applications require the facility to switch downstream devices based on the status of the SECs. In order to provide extra flexibility, it is possible to flag the *main_ref_failed* interrupt (Reg. 06 Bit 6) on the pin TDO. This is simply a copy of the status bit in the interrupt register and is independent of the mask register settings. The bit is reset by writing to the interrupt status register in the normal way. This feature can be enabled and disabled by writing to Reg. 48 Bit 6.

Leaky Bucket Timing

The time taken (in seconds) to raise an inactivity alarm on an SEC that has previously been fully active (Leaky Bucket empty) will be:

$$(cnfg\_upper\_threshold\_n) / 8$$

where n is the number of the Leaky Bucket Configuration. If an input is intermittently inactive then this time can be longer. The default setting of *cnfg_upper_threshold_n* is 6, therefore the default time is 0.75 s.

The time taken (in seconds) to cancel the activity alarm on a previously completely inactive SEC is calculated, for a particular Leaky Bucket, as:

$$[2^{(a)} \times (b - c)] / 8$$

where:

a = cnfg_decay_rate_n
b = cnfg_Bucket_size_n
c = cnfg_lower_threshold_n
(where n = the number of the relevant Leaky Bucket Configuration in each case).

The default setting is shown in the following:

$$[2^{1} \times (8 - 4)] / 8 = 1.0 \text{ secs}$$

Fast Activity Monitor

Anomalies on the selected clock have to be detected as they occur and the PLL must be temporarily isolated until the clock is once again pure. The SEC activity monitoring process cannot be used for this because the high degree of accuracy required dictates that the process be slow. To achieve the immediacy required, the PLL requires an alternative mechanism. The phase locked loop itself contains a fast activity detector such that within approximately two missing input clock cycles, a no-activity flag is raised and the DPLL is frozen in Digital Holdover mode. This flag can also be read as the *DPLL1 main_ref_failed* bit (from Reg. 06 *sts_interrupts*, Bit 6) and can be set to indicate a phase lost state by enabling Reg. 73, Bit 6. With the DPLL in Digital Holdover mode it is isolated from further disturbances. If the input becomes available again before the activity monitor rejection alarm has been raised, then the DPLL will continue to lock to the input, with little disturbance. In this scenario, with the DPLL in the “locked” state, the DPLL uses “nearest edge locking” mode (±180° capture) avoiding cycle slips or glitches caused by trying to lock to an edge 360° away, as would happen with traditional PLLs.

Selector

This block has two main functions:

- Selection of the Input reference clock source via Reg. 33 *force_select_reference_source*
- Forcing of the Operating mode of the device, via Reg. 32 *cnfg_operating_mode*

Selection of Input SECs

Under normal operation, the input SECs are selected automatically by an order of priority given in the Priority Table. For special circumstances however, such as chip or board testing, the selection may be forced by configuration.

Automatic operation selects an SEC based on its predefined priority and its current validity. A table is maintained which lists all valid SECs in the order of priority. This is initially downloaded into the ACS8525A via the Serial interface by the Network Manager, and is subsequently modified by the results of the ongoing quality monitoring. In this way, when all the defined

sources are active and valid, the source with the highest programmed priority is selected, but if this source fails, the next-highest source is selected, and so on.

Restoration of repaired SECs is handled carefully to avoid inadvertent disturbance of the output clock. For this, the ACS8525A has two modes of operation; Revertive and Non-revertive.

In Revertive mode, if a re-validated (or newly validated) source has a higher priority than the SEC which is currently selected, a switchover will take place. Many applications prefer to minimize the clock switching events and choose Non-revertive mode.

In Non-revertive mode, when a re-validated (or newly validated) source has a higher priority, then the selected source will be maintained. The re-validation of the SEC will be flagged in the *sts_sources_valid* register (Reg. 0E and 0F) and, if not masked, will generate an interrupt. Selection of the re-validated source can take place under software control or if the currently selected source fails.

To enable software control, the software should briefly enable Revertive mode to effect a switch-over to the higher priority source. When there is a reference available with higher priority than the selected reference, there will be NO change of SEC as long as the Non-revertive mode remains on, and the currently selected source is valid. A failure of the selected reference will always trigger a switch-over regardless of whether Revertive or Non-revertive mode has been chosen.

Forced Control Selection

A configuration register, *force_select_reference_source* Reg. 33, controls both the choice of automatic or forced selection and the selection itself (when forced selection is required). For Automatic choice of source selection, the 4 LSB bit value *force_select_SEC_input* is set to all zeros or all ones (default). To force a particular input, the bit value is set according to the description for Reg. 33. Forced selection is not the normal mode of operation, and *force_select_SEC_input* defaults to the all-ones value on reset, thereby adopting the automatic selection of the SEC.

Automatic Control Selection - Priority Table

When an automatic selection is required, the *force_select_reference_source* register LSB 4 bits (*force_select_SEC_input*) must be set to all zeros or all ones.

The Priority Table register *cnfg_ref_selection_priority*, occupying three 8-bit register addresses (Reg. 19, 1A and 1C), is organized as one 4-bit word per input SEC port. Each 4 bit word represents the desired priority of that particular port. Unused ports should be given the value 0000 in the relevant register to indicate they are not to be included in the priority table. On power-up, or following a reset, the input priority configuration is set to the default values defined by Table 4. The selection priority values are all relative to each other, with lower-valued numbers taking higher priorities. Each SEC should be given a unique number; the valid values are 1 to 15 (dec). A value of 0 disables the SEC. However if two or more inputs are given the same priority number those inputs will be selected on a first in, first out basis. If the first of two same priority number sources goes invalid the second will be switched in. If the first then becomes valid again, it becomes the second source on the first in, first out basis, and there will not be a switch. If a third source with the same priority number as the other two becomes valid, it joins the priority list on the same first in, first out basis. There is no implied priority based on the channel numbers. Revertive/Non-revertive mode has no effect on sources with the same priority value.

The priority of Sync inputs is determined by the priority of their associated SEC inputs. The Sync inputs do not have their own separate priority table.

Ultra Fast Switching

An SEC is normally disqualified after the Leaky Bucket monitor thresholds have been crossed. An option for a faster disqualification has been implemented, whereby if Reg. 48 Bit 5 (*ultra_fast_switch*) is set, then a loss of activity of just two or three reference clock cycles causes a reference switch, and sets the *DPLL1_main_ref_failed* bit *(*see Reg. 06 Bit 6) which raises an interrupt (if not masked).

The *sts_interrupts* register Reg. 06 Bit 6 (*DPLL1_main_ref_failed*) is used to flag inactivity on the reference that the device is locked to much faster than the activity monitors can support. If Reg. 48 Bit 6 of the *cnfg_monitors* register (*los_flag_on_TDO*) is set, then the state of this bit is driven onto the TDO pin of the device.

Note...The flagging of the loss of the main reference failure on TDO is simply allowing the status of the sts_interrupts bit DPLL1_main_ref_failed to be reflected in the state of the TDO output pin. The pin will, therefore, remain High until the interrupt is cleared. This functionality is not enabled by default so the usual JTAG functions can be used. When the TDO output from the ACS8525A is connected to the TDI pin of the next

device in the JTAG scan chain, the implementation should be such that a logic change caused by the action of the interrupt on the TDI input should not effect the operation when JTAG is not active.

External Protection Switching Mode-SRCSW pin

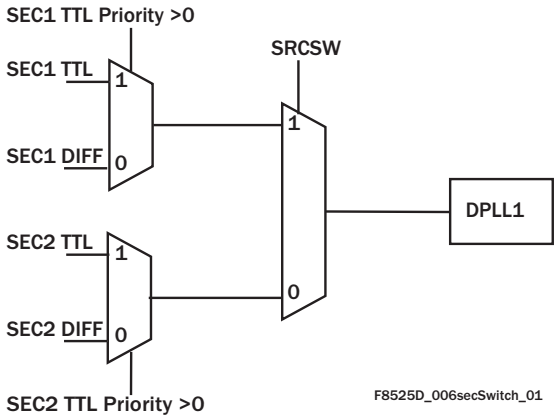
External Protection Switching mode, for fast switching between inputs SEC1 or SEC2, can be triggered directly from the dedicated pin SRCSW, once the mode has been initialized.

The mode is initialized by either holding SRCSW pin *High* during reset (SRCSW must remain *High* for at least a further 251 ms after PORB has gone *High* - see following Note), or by writing to Reg. 48 Bit 4. After External Protection Switching mode has been initialized, the value on this pin directly selects either SEC1 (SRCSW *High*) or SEC2 (SRCSW *Low*). If this mode is activated at reset by pulling the SRCSW pin *High*, then it configures the default frequency tolerance of SEC1 and SEC2 to ±80 ppm (Reg. 41 and 42), as opposed to the normal frequency tolerance of ±9.2 ppm. These registers can be subsequently set by external software, if required.

Note...The 251 ms comprises 250 ms allowance for the internal reset to be removed plus 1 ms allowance for APLLs to start-up and become stable.

The control of TTL or DIFF selection for inputs SEC1 and SEC2 is independently determined by the priority values of the TTL inputs; if the programmed priority of SEC1 TTL is 0, then SEC1 DIFF is available for selection by SRCSW pin; similarly, if SEC2 TTL is 0 priority, SEC2 DIFF is available for selection by SRCSW pin (See Reg. 19 and 1A *cnfg_ref_selection_priority* and Figure 4).

Figure 4 SEC1 and SEC2 Switching



When external protection switching is enabled, the device will operate as a simple switch. All clock monitoring is disabled and the DPLL will simply be forced to try to lock on to the indicated reference source. Consequently the device will always indicate “Locked” state in the operating mode register (Reg. 09, Bits 2:0).

Output Clock Phase Continuity on Source Switchover

If either PBO is selected on (default), or, if DPLL frequency limit set to less than ±30 ppm (±9.2 ppm default), the device will always comply with GR-1244-CORE[13] specifications for Stratum 3 (max rate of phase change of 81 ns/1.326 ms), for all input frequencies.

A well designed system would have Master and Slave clock from the clock sync cards aligned to within a few nanoseconds. In which case a complete system using the Semtech SETS clock card parts (ACS8530, ACS8520 or ACS8510) and this Line Card part would be fully compliant to GR-1244-CORE[13] specifications under all conditions due to the low frequency range and bandwidth set at the clock card end. These parts and the ACS8525A LC/P also allow easy frame sync (8 kHz) alignment both at the clock card and at the Line Card end through the use of dedicated frame sync (8 kHz) inputs, in addition to the main clock inputs.

Forcing of the Operating Mode of the Device

The Selector can force the following Operating modes, (*cnfg_operating_mode*, Reg. 32):

- Auto
- Free-run
- Holdover
- Locked
- Lost-phase
- Pre-locked
- Pre-locked2

See “Operating Modes (States) of the Device” on page 30.

Phase Locked Loops (PLLs)

PLL Overview

Figure 1 shows the PLL circuitry to comprise two Digital PLLs (DPLL1 and DPLL2), two output multiplying and filtering Analog PLLs (APLL1 and APLL2), output frequency dividers in an Output Port Frequency Selection block, a synthesis block, multiplexers MUX1 and MUX2, and a feedback Analog PLL (APLL3). These functional blocks, and their interconnections are highly configurable,

via register control, which provides a range of output frequencies and levels of jitter performance.

The DPLLs give a stable and consistent level of performance that can be easily programmed for different dynamic behavior or operating range. They are not affected by operating conditions or silicon process variations. Digital Synthesis is used to generate all required SONET/SDH output frequencies. The digital logic operates at 204.8 MHz that is multiplied up from the external 12.800 MHz oscillator module. Hence the best resolution of the output signals from the DPLLs is one 204.8 MHz cycle or 4.9 ns.

Additional resolution and lower final output jitter is provided by a de-jittering APLL that reduces the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps RMS as typical final outputs measured broadband (from 10 Hz to 1 GHz).

This arrangement combines the advantages of the flexibility and repeatability of a DPLL with the low jitter of an APLL. The DPLLs in the ACS8525A are programmable for PLL parameters of bandwidth (18, 35 and 70 Hz), damping factor (from 1.2 to 20), frequency acceptance and output range (from 0 to 80 ppm, typically 9.2 ppm), input frequency (12 common SONET/SDH spot frequencies) and input-to-output phase offset (in 6 ps steps up to 200 ns). There is no requirement to understand the loop filter equations or detailed gain parameters since all high level factors such as overall bandwidth can be set directly via registers in the microprocessor interface. No external critical components are required for either the internal DPLLs or APLLs, providing another key advantage over traditional discrete designs.

Either the software or an internal state machine controls the operation of DPLL1. The state machine for DPLL2 is very simple and cannot be manually/externally controlled. One additional feature of DPLL2 is the ability to measure a phase difference between two inputs.

DPLL1 always produces an output at 77.76 MHz to feed the APLL, regardless of the frequency selected at the output pins or the locking frequency (frequency at the input of the Phase and Frequency Detector- PFD).

DPLL2 can be operated at a number of frequencies. This is to enable the generation of extra output frequencies, which cannot be easily related to 77.76 MHz. If DPLL2 is enabled, it locks to the 8 kHz from DPLL1. This is because all of the frequencies of operation of DPLL2 can be divided to 8 kHz and this will ensure synchronization of frequencies, from 8kHz upwards, within the two DPLLs.

Both of the DPLLs' outputs can be connected to multiplying and filtering APLLs. The outputs of these APLLs are divided making a number of frequencies simultaneously available for selection at the output clock ports. The various combinations of DPLL, APLL and divider configurations allow for generation of a comprehensive set of frequencies, as listed in Table 7, "Output Frequency Selection," on page 22.

A function is provided to synchronize the lower output frequencies when DPLL1 is locked to a high frequency reference input. The dividers that generate the 2 kHz and 8 kHz outputs are reset such that the output 2/8 kHz clocks are lined up with the input 2 kHz.

The ACS8525A also supports Sync pulse references of 4 kHz or 8 kHz although in these cases frequencies lower than the Sync pulse reference may not necessarily be in phase.

The PLL configurations for particular output frequencies is described in "Output Frequency Selection and PLL Configuration" on page 22.

PLL Architecture

Figure 5 shows the PLL arrangement in more detail. Each DPLL comprises a generic Phase and Frequency Detector (PFD), a Digital Loop filter, and a Digital Timed Oscillator (DTO- not shown); together with Forward, Feedback, and Low Frequency (LF) (DPLL1 only) Digital Frequency Synthesis (DFS) blocks. The DPLL architecture for DPLL1.

is actually more complex than that of DPLL2, and provides greater functionality.

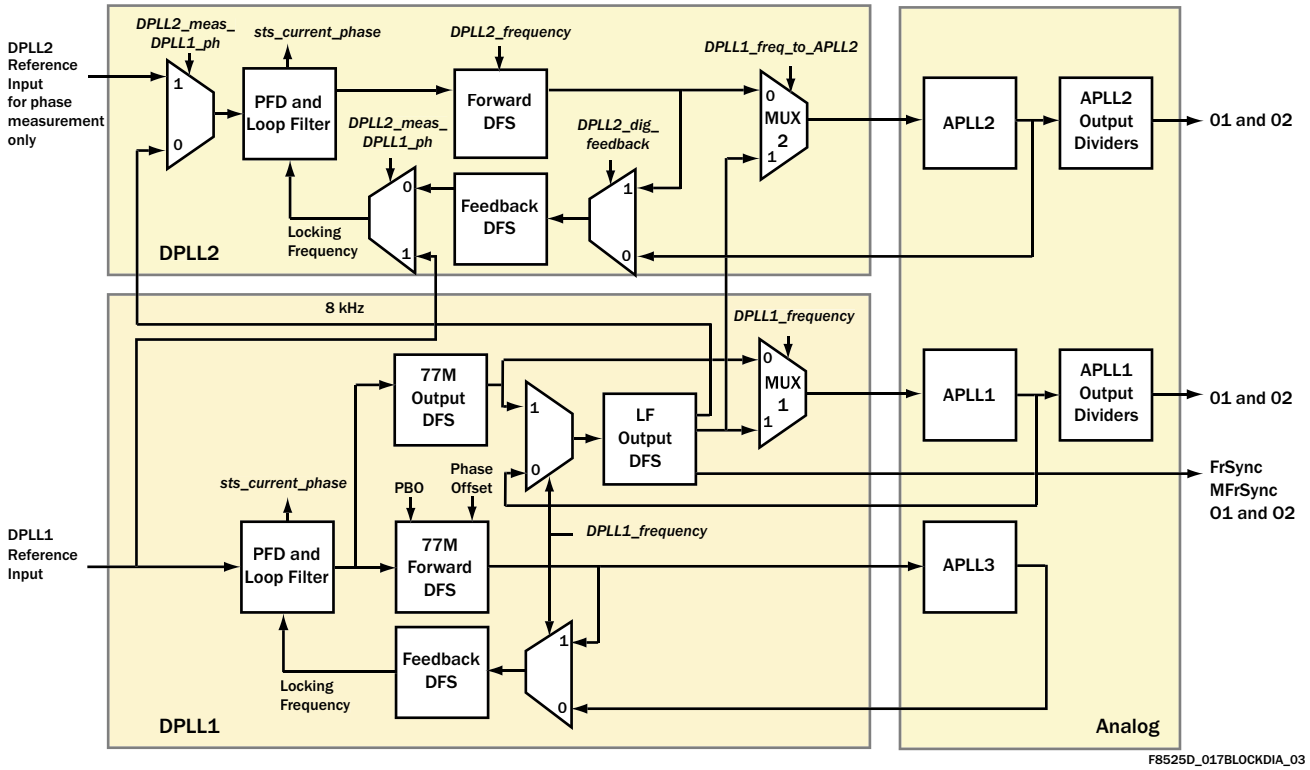
The selected SEC input is always supplied to DPLL1. DPLL1 may use either digital feedback or analog feedback (via APLL3).

DPLL2 always takes its feed from DPLL1 and cannot be used to select a different input to that of DPLL1, except in the case where the device is being used to measure phase difference between input sources. In this case, the PFD of DPLL2 is used for phase measurement and the DPLL2 normal output is rendered unusable.

DPLL1 and APLLs

DPLL1 always produces 77.76 MHz regardless of either the reference frequency (frequency at the input pin of the device) or the locking frequency (frequency at the input of the DPLL PFD).

Figure 5 PLL Block Diagram



The input reference is either passed directly to the PFD or via a pre-divider (not shown) to produce the reference input. The feedback 77.76 MHz is either divided or synthesized to generate the locking frequency.

Any Digital Frequency Synthesis (DFS) generated clock will inherently have jitter on it equivalent to one period of the generating clock (p-p). The DPLL1 77M Forward DFS block uses DFS clocked by the 204.8 MHz system clock to synthesize the 77.76 MHz and, therefore, has an inherent 4.9 ns of p-p jitter. There is an option to use a feedback APLL (APLL3) to filter out this jitter before the 77.76 MHz is used to generate the feedback locking frequency in the DPLL1 feedback DFS block. This analog feedback option allows a lower jitter (<1 ns) feedback signal to give maximum performance.

The DPLL1 77M Forward DFS block is also the block that handles Phase Build-out and any phase offset programmed into the device. Hence, the DPLL1 77M Forward DFS and the DPLL1 77M Output DFS blocks are locked in frequency but may be offset in phase.

The DPLL1 77M Output DFS block also uses the 204.8 MHz system clock and always generates 77.76 MHz for the output clocks (with inherent 4.9 ns of jitter). This is fed to DPLL1 LF Output DFS block and to APLL1. The low frequency DPLL1 LF Output DFS block is used to produce three frequencies; two of them, Digital1 and Digital2, are available for selection to be produced at outputs 01 and 02, and the third frequency can produce multiple E1/DS1 rates via the filtering APLLs. The input clock to the DPLL1 LF Output DFS block is either 77.76 MHz from APLL1 (post jitter filtering) or 77.76 MHz direct from the DPLL1 77M Output DFS.

Utilizing the clock from APLL1 will result in lower jitter outputs from the DPLL1 LF Output DFS block. However, when the input to the APLL1 is taken from the DPLL1 LF Output DFS block, the input to that block comes directly from the DPLL1 77M Output DFS block so that a “loop” is not created.

APLL1 is for multiplying and filtering. The input to APLL1 can be either 77.76 MHz from the DPLL1 77M Output DFS block or an alternative frequency from the DPLL1 LF

Output DFS block (offering 77.76 MHz, 12E1, 16E1, 24DS1 or 16DS1). The frequency from APLL1 is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. APLL1 is subsequently divided by 1, 2, 4, 6, 8, 12, 16 and 48 and these are available at the 01 and 02 Outputs.

DPLL2 & APLLs

DPLL2 is simpler than DPLL1. DPLL2 offers no PBO or phase offset. The DPLL2 input can only be used to lock to DPLL1. Unlike DPLL1, the DPLL2 Forward DFS block does not always generate 77.76 MHz. The possible frequencies are listed in Table 10, "APLL2 Frequencies," on page 27. Similar to DPLL1, the output of the DPLL2 Forward DFS block is generated using DFS clocked by the 204.8 MHz system clock and will have an inherent jitter of 4.9 ns.

The DPLL2 feedback DFS also has the facility to be able to use the post APLL2 (jitter-filtered) clock to generate the feedback locking frequency. Again, this will give the maximum performance by using a low jitter feedback.

APLL2 block is also for multiplying and filtering. The input to APLL2 can come either from the DPLL2 Forward DFS block or from DPLL1. The input to APLL2 can be programmed to be one of the following:

(a) Output from the DPLL2 Forward DFS block (12E1, 24DS1, 16E1, 16DS1, E3, DS3, OC-N),

(b) 12E1 from DPLL1,

(c) 16E1 from DPLL1,

(d) 24DS1 from DPLL1,

(e) 16DS1 from DPLL1.

The frequency generated from the APLL2 is four times its input frequency i.e. 311.04 MHz when used with a 77.76 MHz input. APLL2 is subsequently divided by 2, 4, 8, 12, 16, 48 and 64 and these are available at the 01 and 02 Outputs.

"Digital" Frequencies

The DPLL1 LF Output DFS block shown in the diagram, clocked either by the DPLL1 77M Output DFS block or via the APLL1, generates the single frequencies Digital1 and Digital2 (see Table 11 and Table 12). The input clock frequency of the DFS is always 77.76 MHz and as such has a period of approximately 12 ns. The jitter generated on the Digital outputs is relatively high, because they do not pass through an APLL for jitter filtering. The minimum level of jitter is when DPLL1 is in analog feedback mode, when the p-p jitter will be approximately 13 ns (equivalent to a period of the DFS clock). The maximum jitter is generated when in digital feedback mode, when the total is approximately 18 ns.

The E1/DS1 Synthesis block generates the E1/DS1 rates for the APLLs, using the output from DPLL1. It can generate 12E1, 16E1, 16DS1 or 24DS1, for selection by the multiplexers.

FrSync, MFrSync, 2 kHz and 8 kHz Clock Outputs

Whilst the FrSync and MFrSync Outputs are always supplied from DPLL1, the 2 kHz and 8 kHz options available from the 01 and 02 Outputs can be supplied from either DPLL1 or DPLL2 (Reg. 7A Bit 7).

Multiplexers

Multiplexers MUX1 and MUX2 are used to select the appropriate inputs to the Analog PLLs. The function they represent is controlled by Reg. 65 *cnfg_DPLL1_frequency.*

APLL2 Input Selection using MUX 2

- DPLL2 selected for input to APLL2 (Reg. 65 Bit 6 = 0) The input frequency is selected from the operating frequency of DPLL2 (Reg. 64 Bits [2:0])
- DPLL1 + LF Output DFS selected for Input to APLL2
  - 12E1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 00)
  - 16E1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 01)
  - 24DS1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 10)
  - 16DS1 (Reg. 65 Bit 6 = 1 and Bits [5:4] set to 11)

APLL1 Input Selection using MUX 1

- DPLL1 (77.76 MHz) output fed to input of APLL1. Analog feedback used in DPLL1 (Reg. 65 Bits [2:0] set to 000)
- DPLL1 (77.76 MHz) output fed to input of APLL1. Digital feedback used in DPLL1 (Reg. 65 Bits [2:0] set to 001)
- DPLL1 + LF Output DFS selected for input to APLL1
  - 12E1 (Reg. 65 Bits [2:0] set to 010)
  - 16E1 (Reg. 65 Bits [2:0] set to 011)
  - 24DS1 (Reg. 65 Bits [2:0] set to 100)
  - 16DS1 (Reg. 65 Bits [2:0] set to 101)

Notes: (i) DPLL2 output cannot be selected for input to APLL1

(ii) If both multiplexers select LF Output DFS, the same frequency value must be selected in Reg. 65 Bits [2:0] and Reg. 65 Bits [5:4].

APLLs

There are three main APLLs. APLL1 and APLL2 provide a lower final output jitter reducing the 4.9 ns p-p jitter from the digital down to 500 ps p-p and 60 ps rms as typical final outputs measured broadband (from 10 Hz to 1 GHz). The feedback APLL (APLL3) is selected by default; it provides improved performance over the digital feedback.

APLL Output Dividers

Each APLL has its own divider. Each divider simultaneously outputs a series of fixed ratios of its APLL input. Any of these divided outputs may be selected as the output on Output Ports 01 or 02 by configuring Reg. 61 and Reg. 62, with the following exceptions: (APLL1)/2 and (APLL1)/1 only available for Output 01 (differential port), and (APLL1)/48 only available for Output 02.

PFD and Loop Filters

The PFD compares the input reference with that of the locking frequency (feedback) giving a phase error which is then filtered by a 100 Hz low pass filter, to give the average phase error for input into a loop filter. The PFD is quite complex and has several programmable options to determine what phase error value is fed to the loop (see "Phase and Frequency Detectors" on page 18) depending on the type of jitter/wander expected.

The loop filter bandwidth and damping is programmable to optimize the locking time/ability to track the input. See "Damping Factor Programmability" on page 18 and Figure 6 on page 18.

PLL Operational Controls

The main factors controlling the operation of the PLL are:

1. The operating mode of the device. See "Operating Modes (States) of the Device" on page 30.
2. Input reference and feedback frequency selection. See "PLL Architecture" on page 14 and "Input Locking Frequency Modes" on page 9.
3. Loop Bandwidth (Input Acquisition/Locked Bandwidth) and Damping factor of the DPLLs - these determine how fast the device can to lock to the selected input, or how tightly it can track the input. See from "Input Acquisition Bandwidth" to "Damping Factor Programmability" next.
4. PFD settings - these affect the input phase error to the Loop filter and relate to jitter and wander tolerance. See "Phase/Frequency/Lock Detection" on page 18.
5. Phase compensation functions - See "Phase Compensation Functions" on page 19.

Input Acquisition Bandwidth

DPLL1 has programmable acquisition bandwidth of 18, 35 or 70 Hz. The default is set to 70 Hz.

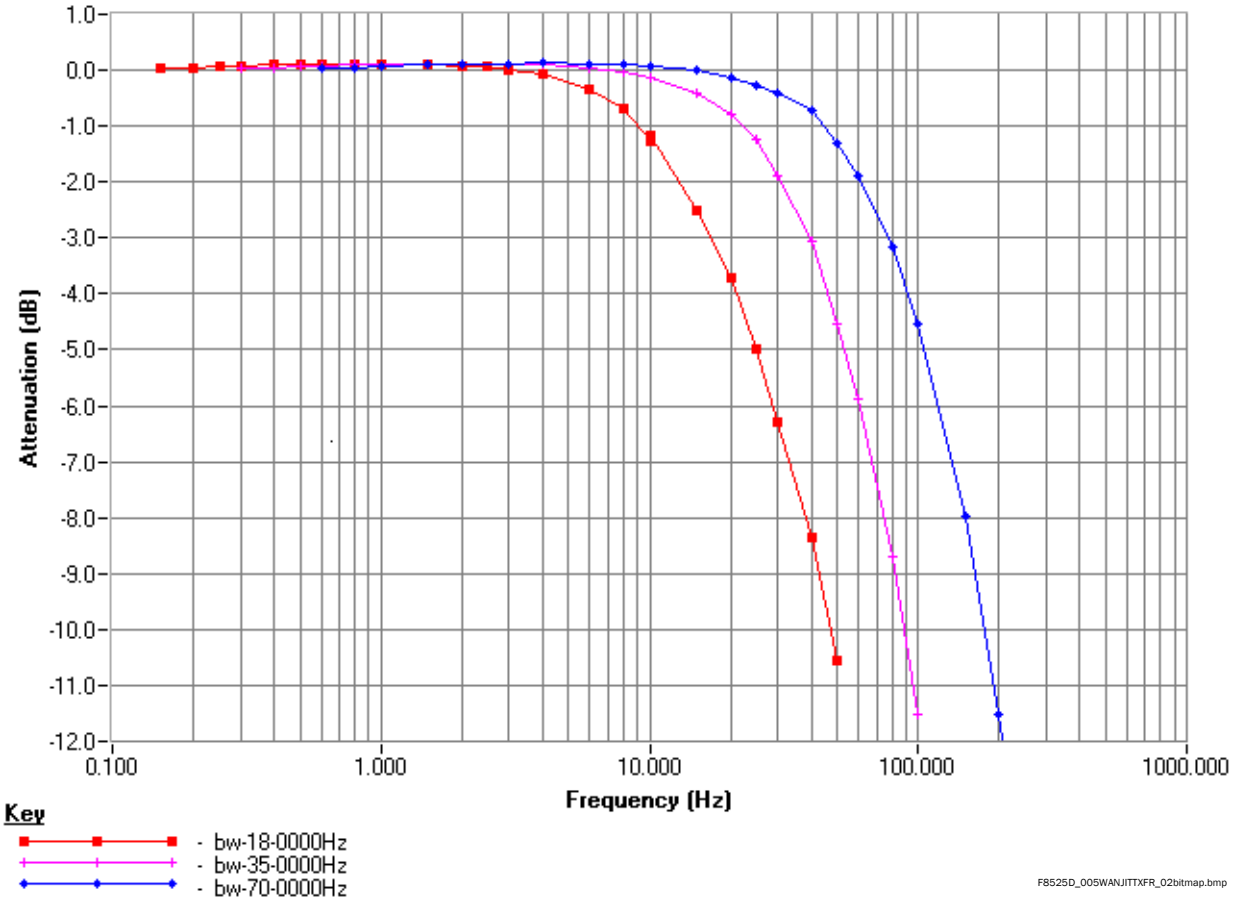
Input Locked Bandwidth

The ACS8525A has programmable Locked Bandwidth of 18, 35 or 70 Hz. These bandwidth settings correspond to the -3 dB jitter attenuation point on the ACS8525A's jitter transfer characteristic shown in Figure 6. If the ACS8525A is used with only DPLL1, the highest bandwidth setting is recommended to ensure the closest tracking of the input SEC. If DPLL2 is also to be used, DPLL1 should be set to a lower bandwidth setting than DPLL2. The lowest bandwidth setting will provide the highest jitter attenuation although this is not the main function of the ACS8525A device.

Table 5 Available Damping Factors for different DPLL Bandwidths, and Associated Gain Peak Values

Bandwidth/Hz	Reg. 6B [2:0]	Damping Factor selected	Gain Peak/dB
18	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

Figure 6 DPLL1 Jitter Transfer Characteristic, (Freq = 1.544 MHz, Jitter = 0.2 UI p-p, Damping Factor = 5)



Damping Factor Programmability

The DPLL damping factor is set by default to provide a maximum wander gain peak of around 0.1 dB. Many of the specifications (e.g. GR-1244-CORE [13], G.812[7] and G.813[8]) specify a wander transfer gain of less than 0.2 dB. GR-253[11] specifies jitter (not wander) transfer of less than 0.1 dB. To accommodate the required levels of transfer gain, the ACS8525A provides a choice of damping factors, with more choice given as the bandwidth setting increases into the frequency regions classified as jitter. Table 5 shows which damping factors are available for selection at the different bandwidth settings, and what the corresponding jitter transfer approximate gain peak will be.

Phase/Frequency/Lock Detection

Two main types of detector are used in the ACS8525A:

- Phase and frequency detectors, and
- Phase Loss/Lock detectors.

Phase and Frequency Detectors

There are two multi-phase and frequency detectors, one for each DPLL. The multi-phase and frequency detectors are used to compare input and feedback clocks. They operate at input frequencies up to 77.76 MHz. DPLL1 can lock to input spot frequencies from 2 kHz up to 77.76 MHz (155.52 MHz is internally divided down to 77.76 MHz). A common arrangement however is to use Lock8k mode (See Bit 6 of Reg. 22 to Reg. 28), where all input frequencies are divided down to 8 kHz internally. Marginally better MTIE figures may be possible in direct lock mode due to more regular phase updates. This direct locking capability is one of the unique features of the ACS8525A.

A patented multi-phase detector is used in order to give an infinitesimally small input phase resolution combined with large jitter tolerance. A multi-phase detector comprises the following phase detectors:

- Phase and frequency detector (±360° or ±180° range)

- An Early/Late phase detector for fine resolution
- A multi-cycle phase detector for large input jitter tolerance (up to 8191 UI), which captures and remembers phase differences of many cycles between input and feedback clocks.

The phase detectors can be configured to be immune to occasional missing input clock pulses by using nearest edge detection (±180° capture) or the normal ± 360° phase capture range which gives frequency locking. The device will automatically switch to nearest edge locking when the multi-UI phase detector is not enabled, and the other phase detectors have detected that phase lock has been achieved. It is possible to disable the selection of nearest edge locking via Reg. 03 Bit 6 (set to 1). In this setting, frequency locking will always be enabled.

The balance between the first two types of phase detector employed can be adjusted via Reg. 6A to 6D. The default settings should be sufficient for all modes. Adjustment of these settings affects only small signal overshoot and bandwidth.

The multi-cycle phase detector (wide-range) is enabled via Reg. 74, Bit 6 set to 1 and the range is set in exponentially increasing steps from ±1 UI up to 8191 UI via Reg. 74, Bits [3:0].

When this detector is enabled it keeps a track of the correct phase position over many cycles of phase difference to give excellent jitter tolerance. This provides an alternative to switching to Lock8k mode as a method of achieving high jitter tolerance.

An additional control (Reg. 74 Bit 5) enables the multi-phase detector value to be used in the final phase value as part of the DPLL loop. When enabled by setting *High*, the multi cycle phase value will be used in the loop and gives faster pull-in (but more overshoot). The characteristics of the loop will be similar to Lock8k mode where again large input phase differences contribute to the loop dynamics. Setting the bit *Low* only uses a max figure of 360° in the loop and will give slower pull-in but gives less overshoot. The final phase position that the loop has to pull in to is still tracked and remembered by the multi-cycle phase detector in either case.

Phase Lock/Loss Detectors

Phase lock detection is handled in several ways. Phase loss can be triggered from:

- The fine phase lock detector, which measures the phase between input and feedback clock
- The coarse phase lock detector, which monitors whole cycle slips
- Detection that the DPLL is at min. or max. frequency
- Detection of no activity on the input

Each of these sources of phase loss indication is individually enabled via register bits (see Reg. 73 and 74). Phase lock or lost is used to determine whether to switch to nearest edge locking and whether to use acquisition or normal bandwidth settings for the DPLL. Acquisition bandwidth is used for faster pull-in from an unlocked state.

The coarse phase lock detector detects phase differences of n cycles between input and feedback clocks, where n is set by Reg. 74 Bits [3:0]; the same register that is used for the coarse phase detector range, since these functions go hand in hand. This detector may be used in the case where it is required that a phase loss indication is not given for reasonable amounts of input jitter and so the fine phase loss detector is disabled and the coarse detector is used instead.

Phase Compensation Functions

The ACS8525A has the following phase compensation functions and controls:

- Phase Build-out (PBO)
- PBO Phase Offset
- Input-to-Output Phase Adjustment

Phase Build-out

Phase Build-out (PBO) is the function to minimize phase transients on the output SEC clock during input reference switching. If the currently selected input reference clock source is lost (due to a short interruption or complete loss of reference), the next highest priority SEC will be selected, and a PBO event triggered. When a PBO event is triggered, the device enters a temporary Holdover state. When in this temporary state, the phase of the input reference is measured, relative to the output. The device then automatically accounts for any measured phase difference and adds the appropriate phase offset into the DPLL to compensate.

Following a PBO event, whatever the phase difference on change of input, the output phase transient is minimized to be typically less than ±2.5 ns (in digital feedback mode).

On the ACS8525A, PBO can be enabled, disabled or frozen using the Serial interface. By default, it is enabled.

When PBO is enabled, PBO can also be frozen (at the current offset setting). The device will then ignore any further PBO events occurring on any subsequent reference switch, and maintain the current phase offset. If PBO is disabled while the device is in the Locked mode, there may be a phase shift on the output SEC clocks as the DPLL locks back to 0° phase error. The rate of phase shift will depend on the programmed bandwidth. Enabling PBO whilst in the Locked stated will also trigger a PBO event.

PBO Phase Offset

In order to minimize the systematic (average) phase error for PBO, a PBO Phase Offset can be programmed in 0.101 ns steps in the *cnfg_PBO_phase_offset* register, Reg. 72. The range of the programmable PBO phase offset is restricted to ±1.4 ns. This can be used to eliminate an accumulation of phase shifts in one direction.

Input to Output Phase Adjustment

When PBO is off such that the system always tries to align the outputs to the inputs at the 0° position, there is a mechanism provided in the ACS8525A for precise fine tuning of the output phase position with respect to the input. This can be used to compensate for circuit and board wiring delays. The output phase can be adjusted in 6 ps steps up to 200 ns in a positive or negative direction. The phase adjustment actually changes the phase position of the feedback clock so that the DPLL adjusts the output clock phases to compensate. The rate of change of phase is therefore related to the DPLL bandwidth. For the DPLL to track large instant changes in phase, either Lock8k mode should be on, or the coarse phase detector should be enabled. Register *cnfg_phase_offset* at Reg. 70 and 71 controls the output phase, which is only used when Phase Build-out is off (Reg. 48, Bit 2 = 0, and Reg. 76, Bit 4 = 0).

DPLL Feature Summary

DPLL1 is the more feature rich of the two DPLLs. The features of the two DPLLs are summarized here. Refer to the Register Descriptions for more information.

DPLL1 Main Features

- Multiple E1 and DS1 outputs supported
- Low jitter MFrSync (2 kHz) and FrSync (8 kHz) outputs
- Multiple phase loss and multiple phase detectors (see “DPLL1 Advanced Features” on page 20”)
- Direct PLL locking to common SONET/SDH input frequencies or any multiple of 8 kHz
- Automatic mode switching between Free-run, Locked and Digital Holdover states (see “Operating Modes (States) of the Device” on page 30)
- Fast detection on input failure and entry into Digital Holdover mode (holds at the last good frequency value)
- Frequency translation between input and output rates via direct digital synthesis
- High accuracy digital architecture for stable PLL dynamics combined with an APLL for low jitter final output clocks
- Non-revertive mode
- Frame Sync pulse alignment
- Selectable Automatic DPLL bandwidth control (auto selects either Locked bandwidth, or Acquisition bandwidth), or Locked DPLL bandwidth (Reg. 3B Bit 7)
- Two programmable bandwidth controls:
  - Locked bandwidth: 18, 35 or 70 Hz (Reg. 67)
  - Acquisition bandwidth: 18, 35 or 70 Hz (Reg. 69)
- Programmable damping factor (for optional faster locking and peaking control). Factors = 1.2, 2.5, 5, 10 or 20. (Reg. 6B, Bits [2:0])
- Programmable DPLL pull-in frequency range (Reg. 41, Reg. 42)
- Phase Build-out on source switching (hit-less source switching), on/off (Reg. 48 Bit 3)
- Freeze Phase Build-out, on/off (Reg. 48 Bit 2)

DPLL1 Advanced Features

Phase Loss Indicators

- Phase loss fine limit. on/off (Reg. 73 Bit 7) and programmable range 0 to 7 dec (Reg. 73 Bits [2:0])
- Multi-cycle phase loss course limit, on/off (Reg. 74 Bit 7) and selectable range from ±1 to 8191 UI in 13 steps (Reg. 74 Bits [3:0])

Output Phase Adjustment

- Programmable Input to Output phase offset adjustment, ±200 ns, 6 ps resolution step size (Reg. 70 and 71)
- Programmable mean offset on Phase Build-out event (PBO phase offset on source switching) - disturbance down to ±5 ns. (Reg. 72 Bits [5:0]). Requires PBO to be on (Reg. 48 Bit 3)

Phase Detector Controls

- Multi-cycle phase detection - Coarse phase lock & capture range on/off (Reg. 74 Bit 6) and selectable range from ±1 to 8191 UI in 13 steps (Reg. 74 Bits [3:0]). If selected, this feature increases jitter and wander tolerance to a maximum of 8192 UI (normally limited to ±0.5 UI)
- Use of coarse phase detector result in DPLL algorithm, on/off (Reg. 74 Bit 6) - speeds up phase locking
- Limit DPLL1 Integral when at DPLL frequency limit, on/off (Reg. 3B Bit 3) - reduces overshoot
- Anti-noise filter for low frequency inputs, on/off (Reg. 76 Bit 7)

Advanced Phase Detector Controls

The phase detector actually comprises two different phase detector types, PD1 and PD2. Their interworking and selection algorithms are beyond the scope of this datasheet, however it should be noted the gain of only PD2 is adjustable by configuration, in the following feature:

- DPLL1 PD2 gain control enable, on/off (Reg. 6D Bit 7)
  If on, this allows automatic gain selection according to the type of feedback to the DPLL (For the digital feedback setting, the gain used for PD2 is given by Reg. 6D Bits [2:0]). If off, PD2 is not used.
- Adjustable gain settings for PD2 (with auto switching enabled), for the following feedback cases:
  - Digital feedback (Reg. 6D Bits [2:0])
  - Analog feedback (all frequencies above 8 kHz) (Reg. 6D Bits [6:4])
  - Analog 8k (or less) feedback (Reg. 6B Bits [2:0])

Phase Monitors

- Input phase measured at DPLL1 or DPLL2. DPLL select (Reg. 4B Bit 4), 16-bit phase status (Reg. 77/78)
- Phase measured between two inputs (uses DPLL2's PFD (Reg. 65 Bit 7))

DPLL2 Main Features

The main features of DPLL2 are:

- Always locked to DPLL1
- A single programmable bandwidth control: 18, 35 or 70 Hz
- Damping factor, (For optional faster locking and peaking control) Factors = 1.2, 2.5, 5, 10 or 20.
- Digital feedback, on/off (Reg. 35 Bit 6)
- Output frequency selection (Reg. 64)
  - DS3/E3 support (44.736 MHz / 34.368 MHz) independent of rates from DPLL1
  - Low jitter E1/DS1 options independent of rates from DPLL1
  - Frequencies of n x E1/DS1 including 16 and 12 x E1, and 16 and 24 x DS1 supported
  - Squelched (clock off)
- Can provide the source for the 2 kHz and 8 kHz outputs available at Outputs 01 and 02 (Reg. 74 Bit 7)
- Can use the phase detector in DPLL2 to measure the input phase difference between two inputs
- Selectable DPLL2 digital feedback, on/off (Reg. 64 Bit 6)

DPLL2 Advanced Features

The advanced features are the same as those for DPLL1, with DPLL2 using the configuration values for DPLL1, with the following exceptions:

Advanced Phase Detector Controls

- PD2 gain control enable, on/off (Reg. 6C, Bit 7)
  If on, this allows automatic gain selection according to the type of feedback to the DPLL (For the digital feedback setting, the gain used for PD2 is given by (Reg. 6C Bits [2:0]). If off, PD2 is not used.
- Adjustable gain settings for PD2 (with auto switching enabled), for the following feedback cases:
  - Digital feedback (Reg. 6C Bits [2:0])
  - Analog feedback (all frequencies above 8K) (Reg. 6C Bits [6:4])
  - Analog 8k (or less) feedback (Reg. 6A Bits [2:0])

Outputs

The ACS8525A delivers four output signals on the following ports: Two clocks, one each on ports Output 01 and Output 02; and two Sync signals, on ports FrSync and MFrSync. Output 01 and Output 02 are independent of each other and are individually selectable. Output 01 is a differential port (pins 01POS and 01NEG), and can be selected PECL or LVDS. Output 02 (pin 02) and the Sync outputs are TTL/CMOS.

The two Sync outputs, FrSync (8 kHz) and MFrSync (2 kHz), are derived from DPLL1.

PECL/LVDS Output Port Selection

The choice of PECL or LVDS compatibility for Output 01 is programmed via the *cnfg_differential_output* register, Reg. 3A.

Output Frequency Selection and PLL Configuration

The output frequency at many of the outputs is controlled by a number of inter-dependent parameters (refer to "PLL Architecture" on page 14). The frequencies of the output clocks are selectable from a range of pre-defined spot frequencies/port technologies, as defined in Tables 6 and 7.

Outputs 01 & 02 Frequency Configuration Steps

The output frequency selection is performed in the following steps:

6. Refer to Table 8, Frequency Divider Look-up, to choose a set of output frequencies.
7. Refer to the Table 8 to determine the required APLL frequency to support the frequency set.
8. Refer to Table 9, APLL1 Frequencies, and Table 10, APLL2 Frequencies, to determine in what mode DPLL1 and DPLL2 need to be configured, considering the output jitter level.
9. Refer to Table 11, 01 and 02 Output Frequency Selection, and the column headings in Table 8, Frequency Divider Look-up, to select the appropriate frequency from either of the APLLs on each output as required.

Table 6 Output Reference Source Selection Table

Port Name	Output Port Technology	Frequencies Supported
Output 01	LVDS/PECL (LVDS default)	Frequency selection as per Table 7 and Table 11
Output 02	TTL/CMOS	
FrSync	TTL/CMOS	FrSync, 8 kHz programmable pulse width and polarity, see Reg. 7A.
MFrSync	TTL/CMOS	MFrSync, 2 kHz programmable pulse width and polarity, see Reg. 7A.

Note...1.544 MHz/2.048 MHz are shown for SONET/SDH respectively. Pin SONSDHB controls default, when High SONET is default

Table 7 Output Frequency Selection

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
				rms (ps)	p-p (ns)
2 kHz	77.76 MHz Analog	-	-	60	0.6
2 kHz	Any digital feedback mode	-	-	1400	5
8 kHz	77.76 MHz Analog	-	-	60	0.6
8 kHz	Any digital feedback mode	-	-	1400	5

Table 7 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)		DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
					rms (ps)	p-p (ns)
1.536		-	12E1 mode	Select DPLL2	500	2.3
1.536		-	-	Select DPLL1 12E1	250	1.5
1.544		-	16DS1 mode	Select DPLL2	200	1.2
1.544		-	-	Select DPLL1 16DS1	150	1.0
1.544	via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
1.544	via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
2.048		-	12E1 mode	Select DPLL2	500	2.3
2.048		-	-	Select DPLL1 12E1	250	1.5
2.048		-	16E1 mode	Select DPLL2	400	2.0
2.048		-	-	Select DPLL1 16E1	220	1.2
2.048	(not Output 01)	12E1 mode	-	-	900	4.5
2.048	via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
2.048	via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
2.059		-	16DS1 mode	Select DPLL2	200	1.2
2.059		-	-	Select DPLL1 16DS1	150	1.0
2.059	(not Output 01)	16DS1 mode	-	-	760	2.6
2.316		-	24DS1 mode	Select DPLL2	110	0.75
2.316		-	-	Select DPLL1 24DS1	110	0.75
2.731		-	16E1 mode	Select DPLL2	400	1.5
2.731		-	-	Select DPLL1 16E1	220	1.2
2.731	(not Output 01)	16E1 mode	-	-	250	1.6
2.796		-	DS3 mode	Select DPLL2	110	1.0
3.088		-	24DS1 mode	Select DPLL2	110	0.75
3.088		-	-	Select DPLL1 24DS1	110	0.75
3.088	(not Output 01)	24DS1 mode	-	-	110	0.75
3.088	via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
3.088	via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
3.728		-	DS3 mode	Select DPLL2	110	1.0
4.096	via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
4.096	via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
4.296		-	E3 mode	Select DPLL2	120	1.0

Table 7 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)		DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
					rms (ps)	p-p (ns)
4.86		-	77.76 MHz mode	Select DPLL2	60	0.6
5.728		-	E3 mode	Select DPLL2	120	1.0
6.144		12E1 mode	-	-	900	4.5
6.144		-	12E1 mode	Select DPLL2	500	2.3
6.144		-	-	Select DPLL1 12E1	250	1.5
6.176		16DS1 mode	-	-	760	2.6
6.176		-	16DS1 mode	Select DPLL2	200	1.2
6.176		-	-	Select DPLL1 16DS1	150	1.0
6.176	via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
6.176	via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
6.48		-	77.76 MHz mode	Select DPLL2	60	0.6
6.48	(not Output 01)	77.76 MHz analog	-	-	60	0.6
6.48	(not Output 01)	77.76 MHz digital	-	-	60	0.6
8.192		12E1 mode	-	-	900	4.5
8.192		16E1 mode	-	-	250	1.6
8.192		-	16E1 mode	Select DPLL2	400	2.0
8.192		-	-	Select DPLL1 16E1	220	1.2
8.192	via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
8.192	via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
8.235		16DS1 mode	-	-	760	2.6
9.264		24DS1 mode	-	-	110	0.75
9.264		-	24DS1 mode	Select DPLL2	110	0.75
9.264		-	-	Select DPLL1 24DS1	110	0.75
10.923		16E1 mode	-	-	250	1.6
11.184		-	DS3 mode	Select DPLL2	110	1.0
12.288		12E1 mode	-	-	900	4.5
12.288		-	12E1 mode	Select DPLL2	500	2.3
12.288		-	-	Select DPLL1 12E1	250	1.5
12.352		24DS1 mode	-	-	110	0.75
12.352		16DS1 mode	-	-	760	2.6
12.352		-	16DS1 mode	Select DPLL2	200	1.2

Table 7 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
				rms (ps)	p-p (ns)
12.352	-	-	Select DPLL1 16DS1	150	1.0
12.352 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
12.352 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
16.384	12E1 mode	-	-	900	4.5
16.384	16E1 mode	-	-	250	1.6
16.384	-	16E1 mode	Select DPLL2	400	2.0
16.384	-	-	Select DPLL1 16E1	220	1.2
16.384 via Digital1 or Digital2 (not Output 01)	77.76 MHz Analog	-	-	3800	13
16.384 via Digital1 or Digital2 (not Output 01)	Any digital feedback mode	-	-	3800	18
16.469	16DS1 mode	-	-	760	2.6
17.184	-	E3 mode	Select DPLL2	120	1.0
18.528	24DS1 mode	-	-	110	0.75
18.528	-	24DS1 mode	Select DPLL2	110	0.75
18.528	-	-	Select DPLL1 24DS1	110	0.75
19.44	77.76 MHz analog	-	-	60	0.6
19.44	77.76 MHz digital	-	-	60	0.6
19.44	-	77.76MHz mode	Select DPLL2	60	0.6
21.845	16E1 mode	-	-	250	1.6
22.368	-	DS3 mode	Select DPLL2	110	1.0
24.576	12E1 mode	-	-	900	4.5
24.576	-	12E1 mode	Select DPLL2	500	2.3
24.576	-	-	Select DPLL1 12E1	250	1.5
24.704	24DS1 mode	-	-	110	0.75
24.704	16DS1 mode	-	-	760	2.6
24.704	-	16DS1 mode	Select DPLL2	200	1.2
24.704	-	-	Select DPLL1 16DS1	150	1.0
25.92	77.76 MHz analog	-	-	60	0.6
25.92	77.76 MHz digital	-	-	60	0.6
32.768	16E1 mode	-	-	250	1.6
32.768	-	16E1 mode	Select DPLL2	400	2.0
32.768	-	-	Select DPLL1 16E1	220	1.2

Table 7 Output Frequency Selection (cont...)

Frequency (MHz, unless stated otherwise)	DPLL1 Mode	DPLL2 Mode	APLL2 Input Mux	Jitter Level (Typ)	
				rms (ps)	p-p (ns)
34.368	-	E3 mode	Select DPLL2	120	1.0
37.056	24DS1 mode	-	-	110	0.75
37.056	-	24DS1 mode	Select DPLL2	110	0.75
37.056	-	-	Select DPLL1 24DS1	110	0.75
38.88	77.76 MHz analog	-	-	60	0.6
38.88	77.76 MHz digital	-	-	60	0.6
38.88	-	77.76 MHz mode	Select DPLL2	60	0.6
44.736	-	DS3 mode	Select DPLL2	110	1.0
49.152 (Output 01 only)	12E1 mode	-	-	900	4.5
49.408 (Output 01 only)	16DS1 mode	-	-	760	2.6
51.84	77.76 MHz analog	-	-	60	0.6
51.84	77.76 MHz digital	-	-	60	0.6
65.536 (Output 01 only)	16E1 mode	-	-	250	1.6
68.736	-	E3 mode	Select DPLL2	120	1.0
74.112 (Output 01 only)	24DS1 mode	-	-	110	0.75
77.76	77.76 MHz analog	-	-	60	0.6
77.76	77.76 MHz digital	-	-	60	0.6
77.76	-	77.76 MHz mode	Select DPLL2	60	0.6
98.304 (Output 01 only)	12E1 mode	-	-	900	4.5
98.816 (Output 01 only)	16DS1 mode	-	-	760	2.6
131.07 (Output 01 only)	16E1 mode	-	-	250	1.6
148.22 (Output 01 only)	24DS1 mode	-	-	110	0.75
155.52 (Output 01 only)	77.76 MHz analog	-	-	60	0.6
155.52 (Output 01 only)	77.76 MHz digital	-	-	60	0.6
311.04 (Output 01 only)	77.76 MHz analog	-	-	60	0.6
311.04 (Output 01 only)	77.76 MHz digital	-	-	60	0.6

Table 8 Frequency Divider Look-up

Transmission Rate	APLL Frequency	APLL/2	APLL/4	APLL/6	APLL/8	APLL/12	APLL/16	APLL/48	APLL/64
OC-N Rates	311.04	155.52	77.76	51.84	38.88	25.92	19.44	6.48	4.86
E3	274.944	137.472	68.376	-	34.368	-	17.184	5.728	4.296
DS3	178.944	89.472	44.736	-	22.368	-	11.184	3.728	2.796
24DS1	148.224	74.112	37.056	24,704	18.528	12.352	9.264	3.088	2.316
16E1	131.072	65.536	32.768	21.84533	16.384	10.92267	8.192	2.730667	2.048
16DS1	98.816	49.408	24.704	16.46933	12.352	8.234667	6.176	2.058667	1.544
12E1	98.304	49.152	24.576	16.384	12.288	8.192	6.144	2.048	1.536

Note...All frequencies in MHz

Table 9 APLL1 Frequencies

APLL1 Frequency	Synthesis/MUX setting for APLL1 Input	DPLL1 Frequency Control Register Bits Reg. 65 Bits[2:0]	Output Jitter Level ns (p-p)
311.04	Normal (digital feedback)	000	<0.5
311.04 MHz	Normal (analog feedback)	001	<0.5
98.304 MHz	12E1 (digital feedback)	010	<2
131.072 MHz	16E1 (digital feedback)	011	<2
148.224 MHz	24DS1 (digital feedback)	100	<2
98.816 MHz	16DS1 (digital feedback)	101	<2
-	Do not use	110	-
-	Do not use	111	-

Note...If using Synthesis for inputs to both APLL1 and APLL2, then they must both use the same synthesis settings.

Table 10 APLL2 Frequencies

APLL2 Frequency	DPLL Mode	DPLL2 Forward DFS Frequency (MHz)	DPLL2 Freq Control Register Bits Reg. 64 Bits [2:0]	APLL2 Input from DPLL1 or 2. Reg. 65 Bit 6	DPLL1 + Synthesis Freq to APLL2 Register Bits Reg. 65 Bits [5:4]	Output Jitter Level ns (p-p)
311.04 MHz	DPLL2-Squelched	77.76	000	0 (DPLL2 enabled)	XX	<0.5
311.04 MHz	DPLL2-Normal	77.76	001	0 (DPLL2 enabled)	XX	<0.5
98.304 MHz	DPLL2-12E1	24.576	010	0 (DPLL2 enabled)	XX	<0.5
131.072 MHz	DPLL2-16E1	32.768	011	0 (DPLL2 enabled)	XX	<0.5
148.224 MHz	DPLL2-24DS1	37.056 (2*18.528)	100	0 (DPLL2 enabled)	XX	<0.5

Table 10 APLL2 Frequencies (cont...)

APLL2 Frequency	DPLL Mode	DPLL2 Forward DFS Frequency (MHz)	DPLL2 Freq Control Register Bits Reg. 64 Bits [2:0]	APLL2 Input from DPLL1 or 2. Reg. 65 Bit 6	DPLL1 + Synthesis Freq to APLL2 Register Bits Reg. 65 Bits [5:4]	Output Jitter Level ns (p-p)
98.816 MHz	DPLL2-16DS1	24.704	101	0 (DPLL2 enabled)	XX	<0.5
274.944 MHz	DPLL2-E3	68.736 (2*34.368)	110	0 (DPLL2 enabled)	XX	<0.5
178.944 MHz	DPLL2-DS3	44.736	111	0 (DPLL2 enabled)	XX	<0.5
98.304 MHz	DPLL1-12E1	-	XXX	1 (DPLL1 enabled)	00	<2
131.072 MHz	DPLL1-16E1	-	XXX	1 (DPLL1 enabled)	01	<2
148.224 MHz	DPLL1-24DS1	-	XXX	1 (DPLL1 enabled)	10	<2
98.816 MHz	DPLL1-16DS1	-	XXX	1 (DPLL1 enabled)	11	<2

Table 11 O1 and O2 Output Frequency Selection

Value in Register	Output Frequency for given "Value in Register" for each Output Port's *Cnf_output_frequency* Register	
	Output O2 Reg. 61 Bits [3:0]	Output O1 Reg. 62 Bits [7:4]
0000	Off	Off
0001	2 kHz	2 kHz
0010	8 kHz	8 kHz
0011	Digital2	APLL1/2
0100	Digital1	Digital1
0101	APLL1/48	APLL1/1
0110	APLL1/16	APLL1/16
0111	APLL1/12	APLL1/12
1000	APLL1/8	APLL1/8
1001	APLL1/6	APLL1/6
1010	APLL1/4	APLL1/4
1011	APLL2/64	APLL2/64
1100	APLL2/48	APLL2/48
1101	APLL2/16	APLL2/16
1110	APLL2/8	APLL2/8
1111	APLL2/4	APLL2/4

"Digital" Frequencies

Table 11, "O1 and O2 Output Frequency Selection," lists Digital1 and Digital2 as available for selection. Digital1 is a single frequency selected from the range shown in Table 12. Digital2 is another single frequency selected from the same range.

Using Output O2 to Control Pulse Width of 2/8 kHz on FrSync, MFrSync and O1 Outputs

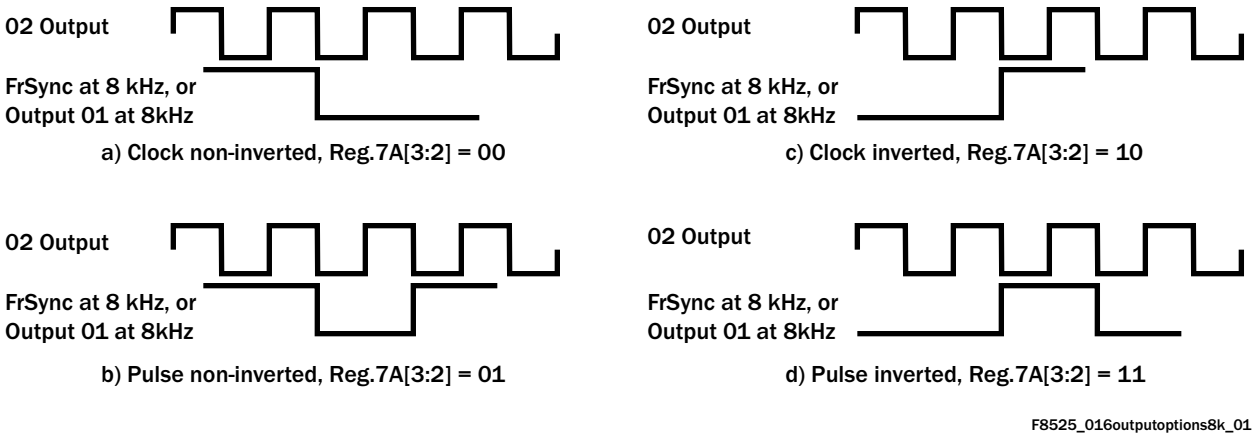
It can be seen from Table 11 (O1 and O2 Output Frequency Selection) that frequencies listed as 2 kHz and 8 kHz can be selected. Whilst the FrSync and MFrSync outputs are always supplied from DPLL1, the 2 kHz and 8 kHz options available from the O1 and O2 outputs are all supplied via DPLL1 or DPLL2 (Reg. 7A Bit 7).

The outputs can be either clocks (50:50 mark-space) or pulses, and can be inverted. When pulse configuration is used, the pulse width will be one cycle of the rate selected on Output O2 (Output O2 must be configured to generate at least 1,544 kHz to ensure that pulses are generated correctly). Figure 7 shows the various options with the 8 kHz controls in Reg. 7A. There is an identical arrangement with Reg. 7A Bits [1:0] for the 2 kHz O1 and MFrSync outputs. Outputs FrSync and MFrSync can be disabled via Reg. 63 Bits [7:6].

Table 12 Digital Frequency Selections

Digital1 Control Reg. 39 Bits [5:4]	Digital1 SONET/ SDH Reg. 38 Bit5	Digital1 Freq. (MHz)	Digital2 Control Reg. 39 Bits[7:6]	Digital2 SONET/SDH Reg. 38 Bit6	Digital2 Freq. (MHz)
00	0	2.048	00	0	2.048
01	0	4.096	01	0	4.096
10	0	8.192	10	0	8.192
11	0	16.384	11	0	16.384
00	1	1.544	00	1	1.544
01	1	3.088	01	1	3.088
10	1	6.176	10	1	6.176
11	1	12.352	11	1	12.352

Figure 7 Control of 8k Options.



Operating Modes (States) of the Device

The ACS8525A has three primary modes of operation, or operating states: Free-Run, Locked and Digital Holdover. These are supported by three secondary, temporary modes (Pre-Locked, Lost-Phase and Pre-Locked2). Refer to the State Transition Diagram for DPLL1, Figure 8.

The ACS8525A can operate in Forced or Automatic control. On reset, the ACS8525A reverts to Automatic Control, where transitions between states are controlled completely automatically. Forced Control can be invoked by configuration, allowing transitions to be performed under external control. This is not the normal mode of operation, but is provided for special occasions such as testing, or where a high degree of hands-on control is required.

Free-run Mode

The Free-run mode is typically used following a power-on-reset or a device reset before network synchronization has been achieved. In the Free-run mode, the timing and synchronization signals generated from the ACS8525A are based on the 12.800 MHz clock frequency provided from the external oscillator and are not synchronized to an input SEC. By default, the frequency of the output clock is a fixed multiple of the frequency of the external oscillator, and the accuracy of the output clock is equal to the accuracy of the oscillator. However the external oscillator frequency can be calibrated to improve its accuracy by a software calibration routine using register *cnfg_nominal_frequency* (Reg. 3C and 3D). For example a 500 ppm offset crystal could be made to look like one accurate to 0.02 ppm.

The transition from Free-run to Pre-locked occurs when the ACS8525A selects an SEC.

Pre-locked Mode

The ACS8525A will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE[13] specification, if the selected SEC is of good quality. If the device cannot achieve lock within 100 seconds, it reverts to Free-Run mode and another SEC is selected.

Locked Mode

The Locked mode is entered from Pre-locked, Pre-locked2 or Phase-lost mode when an input reference source has been selected and the DPLL has locked. The DPLL is considered to be locked when the phase loss/lock detectors (See“Phase Lock/Loss Detectors” on page 19) indicate that the DPLL has remained in phase lock continuously for at least one second. When the ACS8525A is in Locked mode, the output frequency and phase tracks that of the selected input reference source.

Lost-phase Mode

Lost-phase mode is used whenever the phase loss/lock detectors (See“Phase Lock/Loss Detectors” on page 19) indicate that the DPLL has lost phase lock. The DPLL will still be trying to lock to the input clock reference, if it exists. If the Leaky Bucket Accumulator calculates that the anomaly is serious, the device disqualifies the reference source. If the device spends more than 100 seconds in Lost-phase mode, the reference is disqualified and a phase alarm is raised on it. If the reference is disqualified, one of the following transitions takes place:

1. Go to Pre-locked2;
   - If a known good stand-by source is available.

2. Go to Holdover;
   - If no stand-by sources are available.

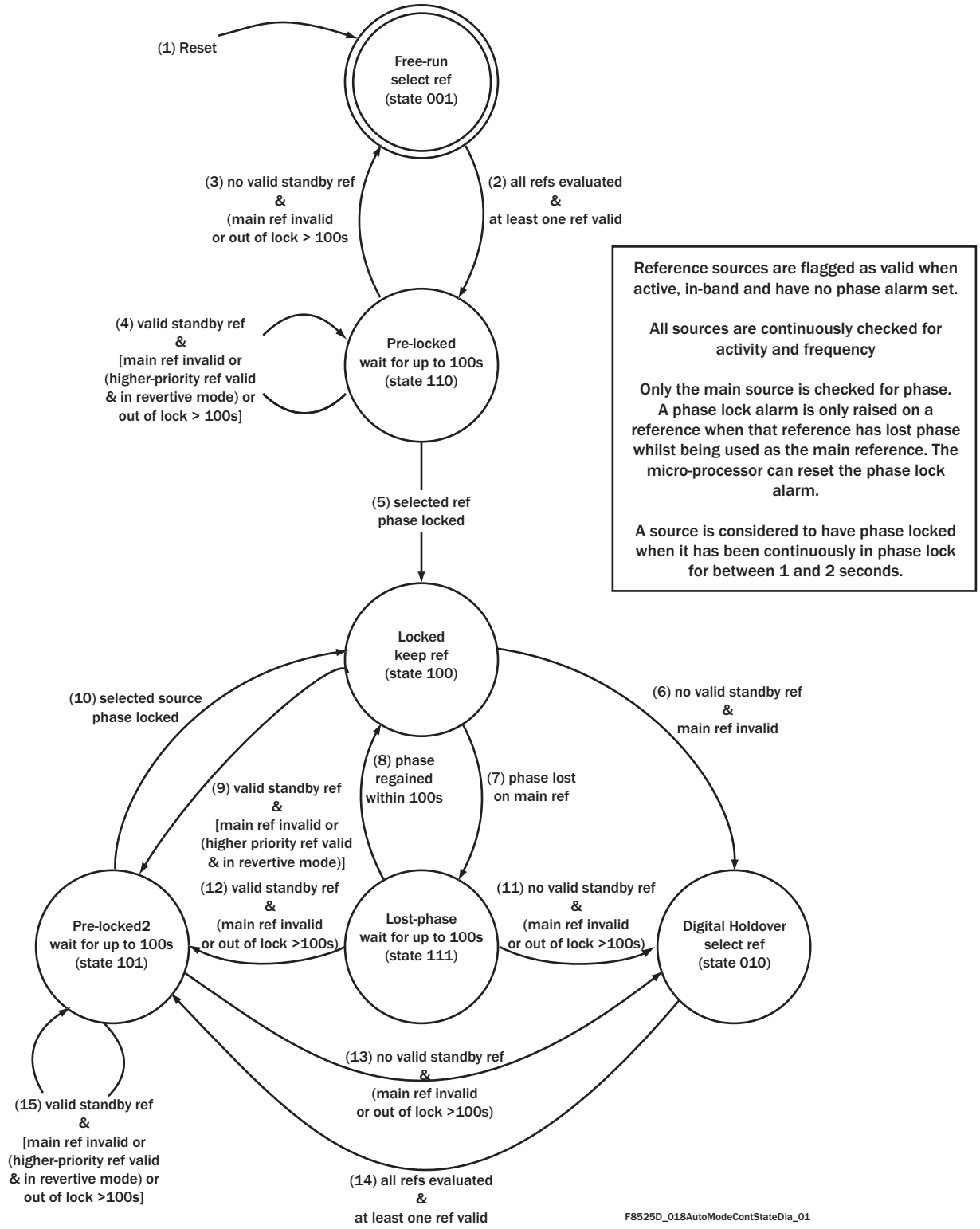
Digital Holdover Mode

Digital Holdover mode is the operating condition the device enters when its currently selected input source becomes invalid, and no other valid replacement source is available.

In Digital Holdover mode, the ACS8525A provides the timing signals to maintain the Line Card but is not phase locked to an input SEC.

Digital Holdover operates Instantaneously, which means the DPLL freezes at the frequency it was operating at the time of entering Digital Holdover mode. This determines the output frequency accuracy.

Figure 8 Automatic Mode Control State Diagram (DPLL1)



Note...The state diagram above is for DPLL1 only, and the 3-bit state value refers to the register sts_operating Reg. 09 Bits [2:0] DPLL1_operating _mode. By contrast, the DPLL2 has only automatic operation and can be in one of only two possible states: "Instantaneous Automatic Holdover" with zero frequency offset (its start-up state), or "Locked". The states of DPLL2 are not configurable by the User and there is no "Free-run" state.

Pre-locked2 Mode

This state is very similar to the Pre-locked state. It is entered from the Digital Holdover state when an input SEC has been selected and applied to the phase locked loop. It is also entered if the device is operating in Revertive mode and a higher-priority SEC is restored.

Upon applying a SEC to the phase locked loop, the ACS8525A will enter the Locked state in a maximum of 100 seconds, as defined by GR-1244-CORE[13] specification, if the selected SEC is of good quality. If the device cannot achieve lock within 100 seconds, it reverts to Digital Holdover mode and another SEC is selected.

Local Oscillator Clock

The Master system clock on the ACS8525A should be provided by an external clock oscillator of frequency 12.800 MHz. Wander on the local oscillator clock will not have a significant effect on the output clock whilst in Locked mode. In Free-Run or Holdover mode wander on the crystal is more significant. Variation in crystal temperature or supply voltage both cause drifts in operating frequency, as does ageing. These effects must be limited by careful selection of a suitable component for the local oscillator. Please contact Semtech for information on crystal oscillator suppliers.

Crystal Frequency Calibration

The absolute crystal frequency accuracy is less important than the stability since any frequency offset can be compensated by adjustment of register values in the IC. This allows for calibration and compensation of any crystal frequency variation away from its nominal value. ± 50 ppm adjustment would be sufficient to cope with most crystals, in fact the range is an order of magnitude larger due to the use of two 8-bit register locations. The setting of the *cnfg_nominal_frequency* register allows for this adjustment. An increase in the register value increases the output frequencies by 0.0196229 ppm for each LSB step.

Note...The default register value (in decimal) = 39321 (9999 hex) = 0 ppm offset. The minimum to maximum offset range of the register is 0 to 65535 (dec), giving an adjustment range of -771 ppm to +514 ppm of the output frequencies, in 0.0196229 ppm steps.
Example: If the crystal was oscillating at 12.800 MHz + 5 ppm, then the calibration value in the register to give a - 5 ppm adjustment in output frequencies to compensate for the crystal inaccuracy, would be:
39321 - (5 / 0.0196229) = 39066 (dec) = 989A (hex).

Status Reporting and Phase Measurement

Input Status Interrupts

Status interrupts are provided for the following events:

- Changed status on SEC input (one interrupt per input) (Reg. 05)
- Change of Operating mode (Reg. 06)
- DPLL1 Main reference Failure (Reg. 06)
- Frame Sync alarm limit reached (Reg. 08)

These interrupts are flagged on pin INTREQ.

Input Status Information

Status information can be read from the following Status Registers:

*sts_operating_mode (*Reg. 09*)*

*sts_priority_table (*Reg. 0A *and* 0B*)*

*sts_current_DPLL_frequency (*Reg. 0C*,* 0D*, and* 07*)*

*sts_sources_valid (*Reg. 0E *and* 0F*)*

*sts_reference_sources (*Reg. 11*,* 12 *and* 14*)*

Refer to “Register Map” on page 38 and associated Register Descriptions for more details.

DPLL Frequency Reporting

The registers *sts_current_DPLL_frequency* (Reg. 0C, 0D and 07) report the frequency of DPLL1 or DPLL2 with respect to the external crystal XO frequency (after calibration via Reg. 3C, 3D if used). The selection of DPLL2 or DPLL1 reporting is made via Reg. 4B, Bit 4. The value is a 19-bit signed number with one LSB representing 0.0003068 ppm (range of ±80 ppm). This value is actually the integral path value in the DPLL, and as such corresponds to an averaged measurement of the input frequency, with an averaging time inversely proportional to the DPLL bandwidth setting. Reading this regularly can show how the currently locked source is varying in value e.g. due to frequency wander on its input.

The input phase, as seen at the DPLL phase detector, can be read back from register *sts_current_phase*, Reg. 77 and 78. DPLL1 or DPLL2 phase detector reporting is again controlled by Reg. 4B, Bit 4. One LSB corresponds to 0.707° phase difference. For DPLL1 this will be reporting the phase difference between the input and the internal feedback clock. The phase result is internally

averaged or filtered with a -3 dB attenuation point at approximately 100 Hz.

Measuring Phase Between Master and Slave/Stand-by SEC Sources

The phase can be measured between the selected SEC input to DPLL1 and either of the other two SEC inputs by a using the Phase and Frequency detector of DPLL2. This special configuration requires manual selection of DPLL2's selected source (by altering the Priorities).

The DPLL2 PFD compares two inputs (usually the feedback and reference input) with each other and performs some filtering. This filtering has a bandwidth of approx. 100 Hz. This will result in a digital number representing the filtered phase difference between these two signals being available (normally used for the digital synthesis).

Under normal circumstances the frequency of the inputs to the PFD are determined by the input frequency selection and the pre-divider settings such as lock8k and DivN. The appropriate feedback frequency is automatically selected from the supported spot frequencies to match the input reference frequency (post division if necessary).

The phase difference is reported in units of 0.707 degrees of the actual locking frequency. When direct locking to high frequency input, the actual time is then scaled down and will give resolution down to e.g. 110 ps at 19.44 MHz in direct locking mode compared with 245 ns with Lock8K mode enabled with the same 19.44 MHz input. The two inputs to the PFD have to be very close in frequency to give an accurate phase measurement.

Reg. 65, Bit 7 is used to switch one input to the DPLL2 phase detector over to the current DPLL1 input. The other phase detector input becomes connected to a second input source. The second input source can be changed via the DPLL2 priority (Reg. 19 to 1C), when Reg. 4B, Bit 4 = 1).

The phase difference measurement is held in the 16-bit register, *sts_current_phase* Reg. 77 and 78. The register is updated on a 204.8 MHz cycle.

When measuring the relative phase error between the selected inputs, the user must ensure that the settings and frequency are the same for the two inputs to be measured. Enabling this phase measurement feature replaces the DPLL2 feedback signal to the DPLL2 PFD with the DPLL1 PFD input reference signal. Reading the current phase register from DPLL2 will yield the filtered phase difference between the two inputs. If there is jitter or wander present on either or both inputs, then this will have an effect on the measured phase. The extent of this effect will depend on the frequency of the jitter/wander compared to the 100 Hz bandwidth of the phase filter.

With the input selections in the examples below, a meaningful result for phase measurement will be obtained from Example 1 only.

Example 1

SEC1 19.44 MHz input, direct locking

SEC2 19.44 MHz input, direct locking

Example 2

SEC1 19.44 MHz input, direct locking

SEC2 19.44 MHz input, Lock8K

The phase reported in degrees of the locking frequency.

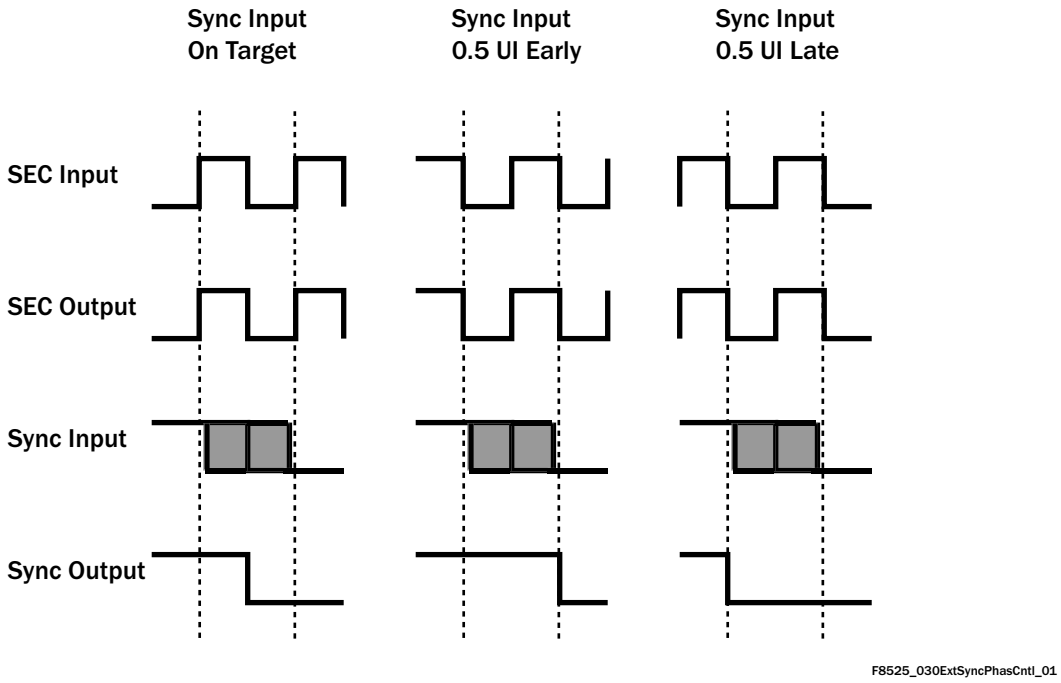
Direct locking to the highest frequency gives the most meaningful result, as the actual time is scaled down and will give a resolution in picoseconds, for example: 101 ps @19.44 MHz, Direct locking on SEC1 and SEC2. With Lock8K enabled instead of direct locking, a result can be measured but the phase error will have a much lower resolution of 245 nanoseconds.

Sync Reference Sources

The ACS8525A provides the facility to have a Sync reference source associated with each SEC. The Sync inputs (SYNC1, SYNC2 and SYNC3) are used for Frame Sync output alignment and can be 2, 4 or 8 kHz (automatically detected frequency). In the ACS8525A device, the Sync is treated as an additional part of the SEC clock. The failure of a Sync input will never cause a source disqualification. The Sync input is used to internally align the generation of the output 2 kHz and 8 kHz Sync pulses.

On the ACS8525A, the presence of a Sync input associated with any particular SEC input is optional. If a Sync input is not present, or it fails, the 2 kHz and 8 kHz outputs will simply continue to be generated with the same relationship to the SEC output. This also applies to a source switch from a reference with a Sync input to a reference without a Sync input. The Sync outputs are always divided from the SEC outputs and will never free-run.

Figure 9 External Sync Input Phase Control (Reg.7B Bits [1:0])



As with all frequencies generated at the outputs of the ACS8525A, the Sync outputs are falling edge aligned. However, the Sync outputs can be inverted. They can also be selected to have a number of different pulse widths. In addition to these controls on the outputs, the input Sync phases with respect to their associated SEC can be configured (separately for each Sync). Nominally, the Sync input is expected to be falling edge aligned with the SEC. Therefore it is sampled on the rising edge of the SEC. This gives a tolerance to offset between the SEC and the Sync input of ±0.5 UI of the SEC clock. If the Sync is delayed or advanced with respect to the SEC the expected position of the edge can be moved by 0.5 UI early or late. The tolerance is always ±0.5 UI of the SEC from the expected position. Figure 9 summarizes these points and *Sync_phase_SYNC1* (Reg. 7B, Bits [1:0]) provides the controlling configuration.

Aligning Phase of MFrSync and FrSync Outputs to Phase of Sync Inputs

The selected Sync input (which is selected by SEC selection) is monitored by the ACS8525A for consistent phase and correct frequency compared with the SEC input, and if it does not pass these quality checks, an alarm flag is raised (Reg. 08, Bit 7 and Reg. 09, Bit 7). The check for consistent phase involves checking that each input edge is within an expected timing window. The window size is set by Reg. 7C, Bits [6:4]. An internal detector senses that a correct Sync signal is present and only then allows the signal to resynchronize the internal dividers that generate the 8 kHz FrSync and 2 kHz MFrSync outputs. This sequence avoids spurious resynchronizations that may otherwise occur with connections and disconnections of the Sync input.

The Sync input will normally be a 2 kHz frequency, only its falling edge is used. It can however be at a frequencies of 4 kHz or 8 kHz without any change to the register setups. However the 2 kHz Sync output alignment can only be achieved when aligning to a 2 kHz SEC.

Safe sampling of the selected Sync input is achieved by using the “locked-to” SEC, with which it is paired, to do the input sampling. Phase Build-out mode should be off (Reg. 48, Bit 2 = 0). The Sync input is normally sampled on the rising edge of the current input reference clock, in order to provide the most margin. As mentioned earlier, modification of the expected timing of the selected Sync input with respect to its SEC can be achieved via Reg. 7B, Bits [1:0].

A different sampling resolution is used depending on the input reference frequency and the setting of Reg. 7B Bit 6, *cnfg_sync_phase*. With this bit *Low*, the Sync input sampling has a 6.48 MHz resolution. When Bit 6 is *High* the selected Sync can have a sampling resolution of

either 19.44 MHz (when the current locked to reference is 19.44 MHz) or 38.88 MHz (all other frequencies). This would allow, for instance, a 19.44 MHz and 2 kHz pair to be used for Line Card synchronization.

Reg. 7B Bit 7, *Indep_FrSync/MFrSync* controls whether the 2 kHz MFrSync and 8 kHz FrSync outputs keep their precise alignment with the other output clocks. When *Indep_FrSync/MFrSync* Reg. 7B Bit 7 is *Low* the FrSyncs and the other higher rate clocks are not independent and their alignment on the falling 8kHz edge is maintained. This means that when bit *Sync_OC-N_rates* is *High*, the OC-N rate dividers and clocks are also synchronized by the Sync input. On a change of phase position of the Sync, this could result in a shift in phase of the 6.48 MHz output clock when a 19.44 MHz precision is used for the Sync input. To avoid disturbing any of the output clocks and only align the MFrSync and FrSync outputs, at the chosen level of precision, Independent Frame Sync mode can be used (Reg. 7B, Bit 7 = 1). Edge alignment of the FrSync output with other clocks outputs may then change depending on the selected Sync sampling precision used. For example with a 19.44 MHz reference input clock and Reg. 7B Bits 6 & 7 both *High* (independent mode and Sync OC-N rates), then the FrSync output will still align with the 19.44 MHz output but not with the 6.48 MHz output clock.

The FrSync and MFrSync outputs always come from DPLL1. 2 kHz and 8 kHz outputs can also be produced at the O1 to O2 outputs. These can come from either the DPLL1 or from the DPLL2, controlled by Reg. 7A, Bit 7.

Power-On Reset

The Power-On Reset (PORB) pin resets the device if forced *Low*. The reset is asynchronous, the minimum *Low* pulse width is 5 ns. Reset is needed to initialize all of the register values to their defaults. Reset must be asserted at power on, and may be re-asserted at any time to restore defaults. This is implemented simply using an external capacitor to GND along with the internal pull-up resistor. The ACS8525A is held in a reset state for 250 ms after the PORB pin has been pulled *High*. In normal operation PORB should be held *High*.

Serial Interface

The ACS8525A device has a serial interface which can be SPI compatible. The Motorola SPI Convention is such that address and data is transmitted and received MSB first. On the ACS8525A address and data are transmitted and received LSB first. Address, read/write control and data on the SDI pin are latched into the device on the rising edge of the SCLK. During a read operation, serial data output on the SDO pin can be read out of the device on either the rising or falling edge of the SCLK depending on the logic level of CLKE. For standard Motorola SPI compliance, data should be clocked out of the SDO pin on the rising edge of the SCLK so that it may be latched into the microprocessor on the falling edge of the SCLK. Figure 10 and Figure 11 show the timing diagrams of read and write accesses for this interface.

The serial interface clock (SCLK) is not required to run between accesses (i.e., when CSB = 1).

Figure 10 Read Access Timing for SERIAL Interface

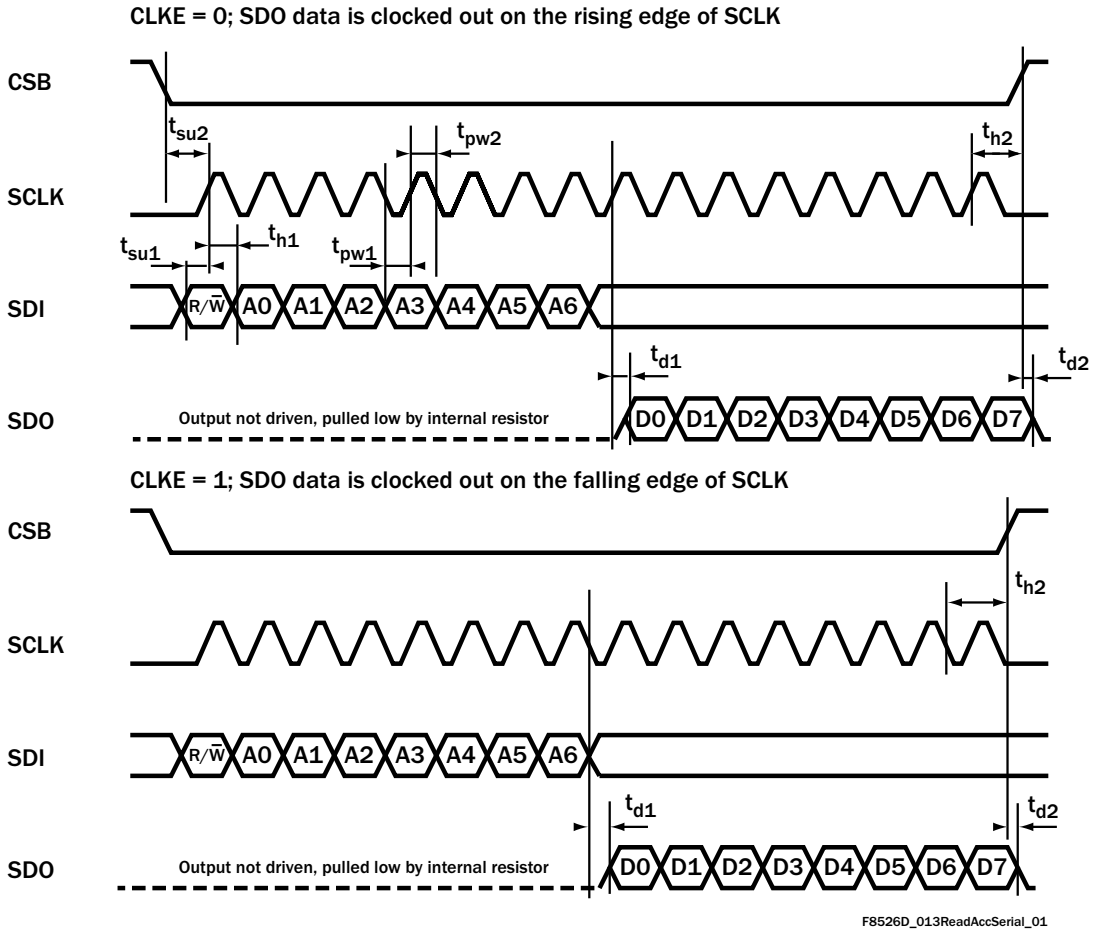


Table 13 Read Access Timing for SERIAL Interface (For use with Figure 10)

Symbol	Parameter	MIN	TYP	MAX
t_{SU1}	Setup SDI valid to $SCLK_{rising\ edge}$	4 ns	-	-
t_{SU2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	14 ns	-	-
t_{d1}	Delay $SCLK_{rising\ edge}$ ($SCLK_{falling\ edge}$ for CLKE = 1) to SDO valid	-	-	18 ns
t_{d2}	Delay $CSB_{rising\ edge}$ to SDO high-Z	-	-	16 ns
t_{pw1}	SCLK *Low* time	22 ns	-	-
t_{pw2}	SCLK *High* time	22 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	6 ns	-	-
t_{h2}	Hold CSB *Low* after $SCLK_{rising\ edge}$, for CLKE = 0 Hold CSB *Low* after $SCLK_{falling\ edge}$, for CLKE = 1	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	10 ns	-	-

Figure 11 Write Access Timing for SERIAL Interface

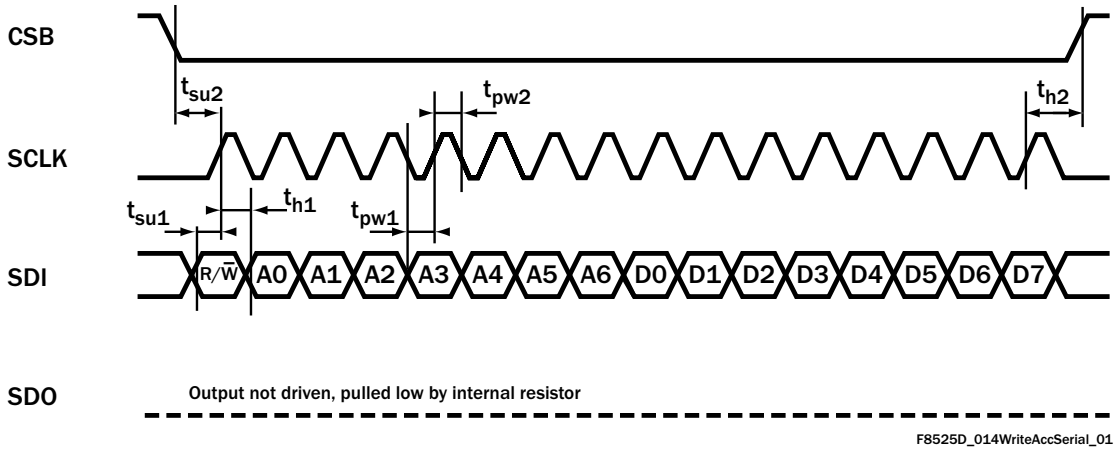


Table 14 Write Access Timing for SERIAL Interface (For use with Figure 11)

Symbol	Parameter	MIN	TYP	MAX
t_{su1}	Setup SDI valid to $SCLK_{rising\ edge}$	4 ns	-	-
t_{su2}	Setup $CSB_{falling\ edge}$ to $SCLK_{rising\ edge}$	14 ns	-	-
t_{pw1}	SCLK *Low* time	22 ns	-	-
t_{pw2}	SCLK *High* time	22 ns	-	-
t_{h1}	Hold SDI valid after $SCLK_{rising\ edge}$	6 ns	-	-
t_{h2}	Hold CSB *Low* after $SCLK_{rising\ edge}$	5 ns	-	-
t_p	Time between consecutive accesses ($CSB_{rising\ edge}$ to $CSB_{falling\ edge}$)	10 ns	-	-

Register Map

Each Register, or register group, is described in the following Register Map (Table 15) and subsequent Register Description Tables.

Register Organization

The ACS8525A LC/P uses a total of 91 eight-bit register locations, identified by a Register Name and corresponding hexadecimal Register Address. They are presented here in ascending order of Reg. address and each Register is organized with the most-significant bit positioned in the left-most bit, with bit significance decreasing towards the right-most bit. Some registers carry several individual data fields of various sizes, from single-bit values (e.g. flags) upwards. Several data fields are spread across multiple registers, as shown in the Register Map,
Table 15. Shaded areas in the map are “don’t care” and writing either 0 or 1 will not affect any function of the device. Bits labelled “Set to 0” or “Set to 1” must be set as stated during initialization of the device, either following power- up, or after a power-on reset (POR). Failure to correctly set these bits may result in the device operating in an unexpected way.

CAUTION! Do not write to any undefined register addresses as this may cause the device to operate in a test mode. If an undefined register has been inadvertently addressed, the device should be reset to ensure the undefined registers are at default values.

Multi-word Registers

For Multi-word Registers (e.g. Reg. 0C and 0D), all the words have to be written to their separate addresses, and without any other access taking place, before their combined value can take effect. If the sequence is interrupted, the sequence of writes will be ignored. Reading a multi-word address freezes the other address words of a multi-word address so that the bytes all correspond to the same complete word.

Register Access

Most registers are of one of two types, configuration registers or status registers, the exceptions being the *chip_id* and *chip_revision* registers. Configuration registers may be written to or read from at any time (the complete 8-bit register must be written, even if only one bit is being modified). All status registers may be read at any time and, in some status registers (such as the *sts_interrupts* register), any individual data field may be cleared by writing a 1 into each bit of the field (writing a 0 value into a bit will not affect the value of the bit).

Configuration Registers

Each configuration register reverts to a default value on power-up or following a reset. Most default values are fixed, but some can be pin-set. All configuration registers can be read out over the microprocessor port.

Status Registers

The Status Registers contain readable registers. They may all be read from outside the chip but are not writeable from outside the chip (except for a clearing operation). All status registers are read via shadow registers to avoid data hits due to dynamic operation. Each individual status register has a unique location.

Interrupt Enable and Clear

Interrupt requests are flagged on pin INTREQ; the active state (*High* or *Low*) is programmable and the pin can either be driven, or set to high impedance when non-active (Reg 7D refers).

Bits in the interrupt status register are set (*High*) by the following conditions;

1. Any SEC becoming valid or going invalid.
2. A change in the operating state e.g. Locked, Holdover.
3. A brief loss of the currently selected SEC.

All interrupt sources, see Reg. 05, Reg. 06 and Reg. 08, are maskable via the mask register, each one being enabled by writing a 1 to the appropriate bit. Any unmasked bit set in the interrupt status register will cause the interrupt request pin to be asserted. All interrupts are cleared by writing a 1 to the bit(s) to be cleared in the status register. When all pending unmasked interrupts are cleared the interrupt pin will go inactive.

Defaults

Each Register is given a defined default value at reset and these are listed in the Map and Description Tables. However, some read-only status registers may not necessarily show the same default values after reset as those given in the tables. This is because they reflect the status of the device which may have changed in the time it takes to carry out the read, or through reasons of configuration. In the same way, the default values given for shaded areas could also take different values to those stated.

Table 15 Register Map

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
chip_id (RO)	00	4D	chip_id[7:0], 8 LSBs of Chip ID							
	01	21	chip_id[15:8], 8 MSBs of Chip ID							
chip_revision (RO)	02	02	chip_revision[7:0]							
test_register1 (R/W)	03	14	Phase_alarm	Disable_180		Resync_ analog	Set to 0	8K Edge Polarity	Set to 0	Set to 0
test_register2 (R/W)	04	12	Do not use							
sts_interrupts (R/W)	05	FF			status_SEC2_ DIFF	status_SEC1_ DIFF	status_SEC2_ TTL	status_SEC1_ TTL		
	06	3F	operating_ mode	DPLL1_main_ ref_failed						status_SEC3
sts_current_DPLL_frequency, see OC/OD	07	00						Bits [18:16] of sts_current_DPLL_frequency		
sts_interrupts (R/W)	08	10	Sync_alarm_ int							
sts_operating_mode (RO)	09	01	Sync_alarm	DPLL2_Lock	DPLL1_freq_ soft_alarm	DPLL2_freq_ soft_alarm		DPLL1_operating_mode		
sts_priority_table (RO)	0A	00	Highest priority validated source				Currently selected source			
	0B	00	3rd highest priority validated source				2nd highest priority validated source			
sts_current_DPLL_frequency[7:0]	0C	00	Bits [7:0] of sts_current_DPLL_frequency							
(RO) [15:8]	0D	00	Bits [15:8] of sts_current_DPLL_frequencyy							
[18:16]	07	00						Bits [18:16] of sts_current_DPLL_frequency		
sts_sources_valid (RO)	0E	00			SEC2 DIFF	SEC1 DIFF	SEC2 TTL	SEC1 TTL		
	0F	00								SEC3
sts_reference_sources (RO) Alarm Status on inputs: SEC1 & SEC2 TTL	11	22			No Activity SEC2 TTL	Phase Lock SEC2 TTL			No Activity SEC1 TTL	Phase Lock SEC1 TTL
SEC1 & SEC2 DIFF	12	22			No Activity SEC2 DIFF	Phase Lock SEC2 DIFF			No Activity SEC1 DIFF	Phase Lock SEC1 DIFF
SEC3	14	22							No Activity SEC3	Phase Lock SEC3
cnfg_ref_selection_priority (R/W) SEC1 & SEC2 TTL	19	32	programmed_priority_SEC2_TTL				programmed_priority_SEC1_TTL			
SEC1 & SEC2 DIFF	1A	00	programmed_priority_SEC2_DIFF				programmed_priority_SEC1_DIFF			
SEC3	1C	04					programmed_priority_SEC3			
cnfg_ref_source_frequency_ <input> (R/W), where <input> = SEC1 TTL	22	00	divn_SEC1 TTL	lock8k_SEC1 TTL	Bucket_id_SEC1 TTL		reference_source_frequency_SEC1 TTL			
SEC2 TTL	23	00	divn_SEC2 TTL	lock8k_SEC2 TTL	Bucket_id_SEC2 TTL		reference_source_frequency_SEC2 TTL			
SEC1 DIFF	24	03	divn_SEC1 DIFF	lock8k_SEC1 DIFF	Bucket_id_SEC1 DIFF		reference_source_frequency_SEC1 DIFF			
SEC2 DIFF	25	03	divn_SEC2 DIFF	lock8k_SEC2 DIFF	Bucket_id_SEC2 DIFF		reference_source_frequency_SEC2 DIFF			
SEC3	28	03	divn_SEC3	lock8k_SEC3	Bucket_id_SEC3		reference_source_frequency_SEC3			
cnfg_operating_mode (R/W)	32	00						DPLL1_operating_mode		
force_select_reference_source (R/W)	33	0F					forced_select_SEC_input			
cnfg_input_mode (R/W)	34	CA	auto_extsync_ en	phalarm_ timeout	XO_ edge		extsync_en	ip_sonsdhb		reversion_ mode
cnfg_DPLL2_path (R/W)	35	A0		DPLL2_dig_ feedback						
cnfg_differential_inputs (R/W)	36	03							SEC2_DIFF_ PECL	SEC1_DIFF_ PECL
cnfg_dig_outputs_sonsdh (R/W)	38	04		dig2_sonsdh	dig1_sonsdh					
cnfg_digtial_frequencies (R/W)	39	08	digital2_frequency		digital1_frequency					
cnfg_differential_output (R/W)	3A	C2							Output 01 _LVDS_PECL	
cnfg_auto_bw_sel	3B	98	auto_BW_sel				DPLL1_lim_int			
cnfg_nominal_frequency [7:0]	3C	99	Bits[7:0] of cnfg_nominal_frequency							
(R/W) [15:8]	3D	99	Bits[15:8] of cnfg_nominal_frequency							
cnfg_DPLL_freq_limit (R/W) [7:0]	41	76	Bits[7:0] of cnfg_DPLL_freq_limit							

Table 15 Register Map (cont...)

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_DPLL_freq_limit (R/W) [9:8]	42	00							Bits[9:8] of cnfg_DPLL_freq_limit	
cnfg_interrupt_mask (R/W) [7:0]	43	00	Set to 0	Set to 0	SEC2 DIFF	SEC1 DIFF	SEC2 TTL	SEC1 TTL		
[15:8]	44	00	operating_ mode	main_ref_ failed				Set to 0		SEC3
[23:16]	45	00	Sync_ip_alarm							
cnfg_freq_divn (R/W) [7:0].	46	FF	divn_value [7:0] (divide Input frequency by n)							
[13:8]	47	3F		divn_value [13:8] (divide Input frequency by n)						
cnfg_monitors (R/W)	48	04		los_flag_on_ TDO	ultra_fast_ switch	ext_switch	PBO_freeze	PBO_en		
cnfg_registers_source_select (R/W)	4B	00				DPLL1_DPLL2 _select				
cnfg_freq_lim_ph_loss	4D		freq_lim_ph_ loss							
cnfg_upper_threshold_0 (R/W)	50	06	upper_threshold_0_value (Activity alarm, Config. 0, Leaky Bucket - set threshold)							
cnfg_lower_threshold_0 (R/W)	51	04	lower_threshold_0_value (Activity alarm, Config. 0, Leaky Bucket - reset threshold)							
cnfg_bucket_size_0 (R/W)	52	08	Bucket_size_0_value (Activity alarm, Config. 0, Leaky Bucket - size)							
cnfg_decay_rate_0 (R/W)	53	01							decay_rate_0_value (Activity alarm, Config. 0, Leaky Bucket - leak rate)	
cnfg_upper_threshold_1 (R/W)	54	06	upper_threshold_1_value (Activity alarm, Config. 1, Leaky Bucket - set threshold)							
cnfg_lower_threshold_1 (R/W)	55	04	lower_threshold_1_value (Activity alarm, Config. 1, Leaky Bucket - reset threshold)							
cnfg_bucket_size_1 (R/W)	56	08	Bucket_size_1_value (Activity alarm, Config. 1, Leaky Bucket - size)							
cnfg_decay_rate_1 (R/W)	57	01							decay_rate_1_value (Activity alarm, Config. 1, Leaky Bucket - leak rate)	
cnfg_upper_threshold_2 (R/W)	58	06	upper_threshold_2_value (Activity alarm, Config. 2, Leaky Bucket - set threshold)							
cnfg_lower_threshold_2 (R/W)	59	04	lower_threshold_2_value (Activity alarm, Config. 2, Leaky Bucket - reset threshold)							
cnfg_bucket_size_2 (R/W)	5A	08	Bucket_size_2_value (Activity alarm, Config. 2, Leaky Bucket - size)							
cnfg_decay_rate_2 (R/W)	5B	01							decay_rate_2_value (Activity alarm, Config. 2, Leaky Bucket - leak rate)	
cnfg_upper_threshold_3 (R/W)	5C	06	upper_threshold_3_value (Activity alarm, Config. 3, Leaky Bucket - set threshold)							
cnfg_lower_threshold_3 (R/W)	5D	04	lower_threshold_3_value (Activity alarm, Config. 3, Leaky Bucket - reset threshold)							
cnfg_bucket_size_3 (R/W)	5E	08	Bucket_size_3_value (Activity alarm, Config. 3, Leaky Bucket - size)							
cnfg_decay_rate_3 (R/W)	5F	01							decay_rate_3_value (Activity alarm, Config. 3, Leaky Bucket - leak rate)	
cnfg_output_frequency (R/W) (Output O2)	61	06					output_freq_O2			
(Output O1)	62	80	output_freq_O1							
(MFrSync/FrSync)	63	C0	MFrSync_en	FrSync_en						
cnfg_DPLL2_frequency (R/W)	64	00						DPLL2_frequency		
cnfg_DPLL1_frequency (R/W)	65	01	DPLL2_meas_ DPLL1_ph	APLL2_for_ DPLL1_E1/ DS1	DPLL1_freq_to_APLL2			DPLL1_frequency		
cnfg_DPLL2_bw (R/W)	66	00							DPLL2_bandwidth	
cnfg_DPLL1_locked_bw (R/W)	67	10							DPLL1_locked_bandwidth	
cnfg_DPLL1_acq_bw (R/W)	69	11							DPLL1_acquisition_bandwidth	
cnfg_DPLL2_damping (R/W)	6A	13		DPLL2_PD2_gain_alog_8k				DPLL2_damping		
cnfg_DPLL1_damping (R/W)	6B	13		DPLL1_PD2_gain_alog_8k				DPLL1_damping		
cnfg_DPLL2_PD2_gain (R/W)	6C	C2	DPLL2_PD2_ gain_enable	DPLL2_PD2_gain_alog				DPLL2_PD2_gain_digital		
cnfg_DPLL1_PD2_gain (R/W)	6D	C2	DPLL1_PD2_ gain_enable	DPLL1_PD2_gain_alog				DPLL1_PD2_gain_digital		
cnfg_phase_offset (R/W) [7:0]	70	00	phase_offset_value [7:0]							
[15:8]	71	00	phase_offset_value[15:8]							
cnfg_PBO_phase_offset (R/W)	72	00			PBO_phase_offset					
cnfg_phase_loss_fine_limit (R/W)	73	A2	fine_limit_en	noact_ph_loss	narrow_en			phase_loss_fine_limit		

Table 15 Register Map (cont...)

Register Name RO = Read Only R/W = Read/Write	Address (hex)	Default (hex)	Data Bit 7 (MSB)	6	5	4	3	2	1	0 (LSB)
cnfg_phase_loss_coarse_limit (R/W)	74	85	coarse_lim_ phaseloss_en	wide_range_ en	multi_ph_resp		phase_loss_coarse_limit			
cnfg_ip_noise_window (R/W)	76	06	ip_noise_ window_en							
sts_current_phase (RO) [7:0]	77	00	current_phase[7:0]							
[15:8]	78	00	current_phase[15:8]							
cnfg_phase_alarm_timeout (R/W)	79	32			timeout_value (in two-second intervals)					
cnfg_sync_pulses (R/W)	7A	00	2k_8k_from_ DPLL2				8k_invert	8k_pulse	2k_invert	2k_pulse
cnfg_sync_phase (R/W)	7B	00	Indep_FrSync/ MFrSync	Sync_OC-N_ rates	Sync_phase_SYNC3		Sync_phase_SYNC2		Sync_phase_SYNC1	
cnfg_sync_monitor (R/W)	7C	2B	ph_offset_ ramp	Sync_monitor_limit						
cnfg_interrupt (R/W)	7D	02						Interrupt GPO_en	Interrupt tristate_en	Interrupt int_polarity
cnfg_protection(R/W)	7E	85	protection_value							

Register Descriptions

Address (hex): 00

Register Name	*chip_id*	Description	(RO) 8 least significant bits of the chip ID.	Default Value	0100 1101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_id[7:0], 8 LSBs of Chip ID							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_id* Least significant byte of the 2-byte device ID.	48 (hex)	

Address (hex): 01

Register Name	*chip_id*	Description	(RO) 8 most significant bits of the chip ID.	Default Value	0010 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_id[15:8], 8 MSBs of Chip ID							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_id* Most significant byte of the 2-byte device ID.	21 (hex)	

Address (hex): 02

Register Name	*chip_revision*	Description	(RO) Silicon revision of the device.	Default Value	0000 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
chip_revision[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*chip_revision* Silicon revision of the device.	02(hex)	

Address (hex): 03

Register Name	*test_register1*	**Description**	(R/W) Register containing various test controls (not normally used).	**Default Value**	0001 0100

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
phase_alarm	*disable_180*		*resync_analog*	Set to 0	*8k Edge Polarity*	Set to 0	Set to 0

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*phase_alarm (*phase alarm (R/O)) Instantaneous result from DPLL1.	0 1	DPLL1 reporting phase locked. DPLL1 reporting phase lost.
6	*disable_180* Normally the DPLL will try to lock to the nearest edge (±180°) for the first 2 seconds when locking to a new reference. If the DPLL does not determine that it is phase locked after this time, then the capture range reverts to ±360°, which corresponds to frequency and phase locking. Forcing the DPLL into frequency locking mode may reduce the time to frequency lock to a new reference by up to two seconds. However, this may cause an unnecessary phase shift of up to 360° when the new and old references are very close in frequency and phase.	0 1	DPLL1 automatically determines frequency lock enable. DPLL1 forced to always frequency and phase lock.
5	Not used.	-	-
4	*resync_analog* (analog dividers re-synchronization) The analog output dividers include a synchronization mechanism to ensure phase lock at low frequencies between the input and the output.	0 1	Analog divider only synchronized during first 2 seconds after power-up. Analog dividers always synchronized.This keeps the clocks divided down from the APLL output, in sync with equivalent frequency digital clocks in the DPLL. Hence ensuring that 6.48 MHz output clocks, and above, are in sync with the DPLL even though only a 77.76 MHz clock drives the APLL.
3	*Set to 0* Test Control. Leave unchanged or set to 0.	0	-
2	*8k Edge Polarity* When lock 8k mode is selected for the current input SEC, this bit allows the system to lock on either the rising or the falling edge of the input clock.	0 1	Lock to falling clock edge. Lock to rising clock edge.
1	*Set to 0* Test Control. Leave unchanged or set to 0.	0	-
0	*Set to 0* Test Control. Leave unchanged or set to 0.	0	-

Address (hex): 04 *test_register2* Do not use. Only zero should be written to this address.

Address (hex): 05

Register Name	*sts_interrupts*	Description	(R/W) Bits [7:0] of the interrupt status register.	Default Value	1111 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		status_SEC2_DIFF	*status_SEC1_DIFF*	*status_SEC2_TTL*	*status_SEC1_TTL*		

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
5	*status_SEC2_DIFF* Interrupt indicating that input SEC2 DIFF has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input SEC2 DIFF has not changed status (valid/invalid). Input SEC2 DIFF has changed status (valid/invalid). Writing 1 resets the interrupt to 0.
4	*status_SEC1_DIFF* Interrupt indicating that input SEC1 DIFF has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input SEC1 DIFF has not changed status (valid/invalid). Input SEC1 DIFF has changed status (valid/invalid). Writing 1 resets the interrupt to 0.
3	*status_SEC2_TTL* Interrupt indicating that input SEC2 TTL has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input SEC2 TTL has not changed status (valid/invalid). Input SEC2 TTL has changed status (valid/invalid). Writing 1 resets the interrupt to 0.
2	*status_SEC1_TTL* Interrupt indicating that input SEC1 TTL has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input SEC1 TTL has not changed status (valid/invalid). Input SEC1 TTL has changed status (valid/invalid). Writing 1 resets the interrupt to 0.
[1:0]	Not used.	-	-

Address (hex): 06

Register Name	*sts_interrupts*	Description	(R/W) Bits [15:8] of the interrupt status register.	Default Value	0011 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
operating_mode	*DPLL1_main_ref_failed*						*status_SEC3*

Bit No.	Description	Bit Value	Value Description
7	*operating_mode* Interrupt indicating that the operating mode has changed. Latched until reset by software writing a 1 to this bit.	0 1	Operating mode has not changed. Operating mode has changed. Writing 1 resets the interrupt to 0.

Address (hex): 06 (cont...)

Register Name	*sts_interrupts*	Description	(R/W) Bits [15:8] of the interrupt status register.	Default Value	0011 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
operating_ mode	*DPLL1_ main_ref_failed*						*status_SEC3*

Bit No.	Description	Bit Value	Value Description
6	*DPLL1_main_ref_failed* Interrupt indicating that input to the DPLL1 has failed. This interrupt will be raised after 2 missing input cycles. This is much quicker than waiting for the input to become invalid. This input is not generated in *Free-run* or *Holdover* modes. Latched until reset by software writing a 1 to this bit.	0 1	Input to DPLL1 is valid. Input to DPLL1 has failed. Writing 1 resets the interrupt to 0.
[5:1]	Not used.	-	-
0	*status_SEC3* Interrupt indicating that input SEC3 has become valid (if it was invalid), or invalid (if it was valid). Latched until reset by software writing a 1 to this bit.	0 1	Input SEC3 has not changed status (valid/invalid). Input SEC3 has changed status (valid/invalid). Writing 1 resets the interrupt to 0.

Address (hex): 07

Register Name	*sts_current_DPLL_frequency [18:16]*	Description	(RO) Bits [18:16] of the current DPLL frequency.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					Bits [18:16] of *sts_current_DPLL_frequency*		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-
[2:0]	Bits [18:16] of *sts_current_DPLL_frequency* When Bit 4 (*DPLL1_DPLL2_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for DPLL1 is reported. When this Bit 4 = 1 the frequency for DPLL2 is reported.	-	See register description of *sts_current_DPLL_frequency* at Reg. 0D.

Address (hex): 08

Register Name	*sts_interrupts*	Description	(R/W) Bits [23:16] of the interrupt status register.	Default Value	0001 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sync_alarm_ int							

Bit No.	Description	Bit Value	Value Description
7	*Sync_alarm_int* Interrupt indicating that the selected Sync input monitor has hit its alarm limit. Latched until reset by software writing a 1 to this bit.	0 1	Input Sync alarm has not occurred. Input Sync alarm has occurred. Writing 1 resets the input to 0.
[6:0]	Not used.	-	-

Address (hex): 09

Register Name	*sts_operating_mode*	Description	(RO) Current operating state of the device's internal state machine.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sync_alarm	*DPLL2_Lock*	*DPLL1_freq_ soft_alarm*	*DPLL2_freq_ soft_alarm*		*DPLL1_operating_mode*		

Bit No.	Description	Bit Value	Value Description
7	*Sync_alarm* Reports current interrupt status of the selected Sync input monitor.	0 1	External Sync. monitor not in alarm condition. External Sync. monitor in alarm condition.

Address (hex): 09 (cont...)

Register Name	*sts_operating_mode*	Description	(RO) Current operating state of the device's internal state machine.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sync_alarm	*DPLL2_Lock*	*DPLL1_freq_ soft_alarm*	*DPLL2_freq_ soft_alarm*		*DPLL1_operating_mode*		

Bit No.	Description	Bit Value	Value Description
6	*DPLL2_Lock* Reports current phase lock status of DPLL2. DPLL2 does not have the same state machine as DPLL1, as it does not support all the features of DPLL1. It can only report its state as locked or unlocked. The bit indicates that the DPLL2 is locked by monitoring the DPLL2 phase loss indicators, which potentially come from four sources. The four phase loss indicators are enabled by the same registers that enable them for the DPLL1, as follows: the fine phase loss detector enabled by Reg. 73 Bit 7, the coarse phase loss detector enabled by Reg. 74 Bit 7, the phase loss indication from no activity on the input enabled by Reg. 73 Bit 6 and phase loss from the DPLL being at its minimum or maximum frequency limits enabled by Reg. 4D Bit 7. For the DPLL2 lock indicator (at Reg. 09 Bit 6) the bit will latch an indication of phase lost from the coarse phase lock detector such that when an indication of phase lost (or not locked) is set it stays in that phase lost or not locked state (so Reg. 09 Bit 6 =0). For this bit to give a correct current reading of the DPLL2 locked state, then the coarse phase loss detector should be temporarily disabled (set Reg. 74 Bit 7 = 0), then the DPLL2 locked bit can be read (Reg. 09 Bit 6), then the coarse phase loss detector should be re-enabled again (set Reg. 74 Bit 7 = 1). Once the bit is indicating "locked" (Reg. 09 Bit 6=1), it is always a correct indication and no change to the coarse phase loss detector enable is required. If at any time any cycle slips occur that trigger the coarse phase loss detector (which monitors cycle slips) then this information is latched so that the lock bit (Reg. 09 Bit 6) will go low and stay low, indicating that a problem has occurred. It is then a requirement that the coarse phase loss detector's disable/re-enable sequence is performed during a read of the DPLL2 locked bit, in order to get a current indication of whether the DPLL2 is locked.	0 1	DPLL2 not phase locked to SEC. DPLL2 phase locked to SEC.

Address (hex): 09 (cont...)

Register Name	*sts_operating_mode*	**Description**	(RO) Current operating state of the device's internal state machine.	**Default Value**	0000 0001

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Sync_alarm	*DPLL2_Lock*	*DPLL1_freq_ soft_alarm*	*DPLL2_freq_ soft_alarm*		*DPLL1_operating_mode*		

Bit No.	**Description**	**Bit Value**	**Value Description**
5	*DPLL1_freq_soft_alarm* DPLL1 has a programmable frequency limit and "soft" alarm limit. The frequency limit is the extent to which it will track a reference before limiting. The "soft" limit is the point beyond which the DPLL tracking a reference will cause an alarm. This bit reports the status of the "soft" alarm.	0 1	DPLL1 tracking its reference within the limits of the programmed "soft" alarm. DPLL1 tracking its reference beyond the limits of the programmed "soft" alarm.
4	*DPLL2_freq_soft_alarm* DPLL2 has a programmable frequency limit and "soft" alarm limit. The frequency limit is the extent to which it will track a reference before limiting. The "soft" limit is the point beyond which the DPLL tracking a reference will cause an alarm. This bit reports the status of the "soft" alarm.	0 1	DPLL2 tracking its reference within the limits of the programmed "soft" alarm. DPLL2 tracking its reference beyond the limits of the programmed "soft" alarm.
3	Not used.	-	-
[2:0]	*DPLL1_operating_mode* This field is used to report the state of the internal finite state machine controlling DPLL1.	000 001 010 011 100 101 110 111	Not used. Free Run. Holdover. Not used. Locked. Pre-locked2. Pre-locked. Phase Lost.

Address (hex): 0A

Register Name	*sts_priority_table*	**Description**	(RO) Bits [7:0] of the validated priority table.	**Default Value**	0000 0000

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Highest priority validated source				*Currently selected source*			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:4]	*Highest priority validated source* Reports the input channel number of the highest priority validated source.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 to 1111	No valid source available. Not used. Not used. Input SEC1 TTL is the highest priority valid source. Input SEC2 TTL is the highest priority valid source. Input SEC1 DIFF is the highest priority valid source. Input SEC2 DIFF is the highest priority valid source. Not used. Not used. Input SEC3 is the highest priority valid source. Not used.
[3:0]	*Currently selected source* Reports the input channel number of the currently selected source. When in Non-revertive mode, this is not necessarily the same as the highest priority validated source.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010-1111	No source currently selected. Not used. Not used. Input SEC1 TTL is the currently selected source. Input SEC2 TTL is the currently selected source. Input SEC1 DIFF is the currently selected source. Input SEC2 DIFF is the currently selected source. Not used. Not used. Input SEC3 is the currently selected source. Not used.

Address (hex): 0B

Register Name	*sts_priority_table*	**Description**	(R0) Bits [15:8] of the validated priority table.	**Default Value**	0000 0000

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
3rd highest priority validated source				*2nd highest priority validated source*			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:4]	*3rd highest priority validated source* Reports the input channel number of the 3rd highest priority validated source.	0000	Less than 3 valid sources available.
		0001	Not used.
		0010	Not used.
		0011	Input SEC1 TTL is the 3rd highest priority valid source.
		0100	Input SEC2 TTL is the 3rd highest priority valid source.
		0101	Input SEC1 DIFF is the 3rd highest priority valid source.
		0110	Input SEC2 DIFF is the 3rd highest priority valid source.
		0111	Not used.
		1000	Not used.
		1001	Input SEC3 is the 3rd highest priority valid source.
		1010-1111	Not used.
[3:0]	*2nd highest priority validated* Reports the input channel number of the 2nd highest priority validated source.	0000	Less than 2 valid sources available.
		0001	Not used.
		0010	Not used.
		0011	Input SEC1 TTL is the 2nd highest priority valid source.
		0100	Input SEC2 TTL is the 2nd highest priority valid source.
		0101	Input SEC1 DIFF is the 2nd highest priority valid source.
		0110	Input SEC2 DIFF is the 2nd highest priority valid source.
		0111	Not used.
		1000	Not used.
		1001	Input SEC3 is the 2nd highest priority valid source.
		1010-1111	Not used.

Address (hex): 0C

Register Name	*sts_current_DPLL_frequency [7:0]*	Description	(RO) Bits [7:0] of the current DPLL frequency.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bits [7:0] of *sts_current_DPLL_frequency*							

Bit No.	Description	Bit Value	Value Description
[7:0]	Bits [7:0] of *sts_current_DPLL_frequency* *When Bit 4 (*DPLL1_DPLL2_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for DPLL1 is reported. When this Bit 4 = 1 the frequency for DPLL2 is reported.	-	See register description of *sts_current_DPLL_frequency* at Reg. 0D.

Address (hex): 0D

Register Name	*sts_current_DPLL_frequency [15:8]*	Description	(RO) Bits [15:8] of the current DPLL frequency.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bits [15:8] of *sts_current_DPLL_frequency*							

Bit No.	Description	Bit Value	Value Description
[7:0]	Bits [15:8] of *sts_current_DPLL_frequency* The value in this register is combined with the value in Reg. 0C and Reg. 07 to represent the current frequency offset of the DPLL. *When Bit 4 (*DPLL1_DPLL2_select*) of Reg. 4B (*cnfg_registers_source_select*) = 0 the frequency for DPLL1 is reported. When this Bit 4 = 1 the frequency for DPLL2 is reported.	-	In order to calculate the ppm offset of the DPLL with respect to the crystal oscillator frequency, the value in Reg. 07, Reg. 0D and Reg. 0C need to be concatenated. This value is a 2's complement signed integer. The value multiplied by 0.0003068 dec will give the value in ppm offset with respect to the XO frequency, allowing for any crystal calibration that has been performed, via *cnfg_nominal_frequency*, Reg. 3C and 3D. The value is actually the DPLL integral path value so it can be viewed as an average frequency, where the rate of change is related to the DPLL bandwidth. If Bit 3 of Reg. 3B is *High* then this value will freeze if the DPLL has been pulled to its min or max frequency.

Address (hex): 0E

Register Name	*sts_sources_valid*	Description	(R0) 8 least significant bits of the *sts_sources_valid* register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		SEC2 DIFF	*SEC1 DIFF*	*SEC2 TTL*	*SEC1 TTL*		

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
5	*SEC2 DIFF* Bit indicating if SEC2 DIFF is valid. The input is valid if it has no outstanding alarms.	0 1	Input SEC2 DIFF is invalid. Input SEC2 DIFF is valid.
4	*SEC1 DIFF* Bit indicating if SEC1 DIFF is valid. The input is valid if it has no outstanding alarms.	0 1	Input SEC1 DIFF is invalid. Input SEC1 DIFF is valid.
3	*SEC2 TTL* Bit indicating if SEC2 TTL is valid. The input is valid if it has no outstanding alarms.	0 1	Input SEC2 TTL is invalid. Input SEC2 TTL is valid.
2	*SEC1 TTL* Bit indicating if SEC1 TTL is valid. The input is valid if it has no outstanding alarms.	0 1	Input SEC1 TTL is invalid. Input SEC1 TTL is valid.
[1:0]	Not used.	-	-

Address (hex): 0F

Register Name	*sts_sources_valid*	Description	(R0) 8 most significant bits of the sts_sources_valid register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							SEC3

Bit No.	Description	Bit Value	Value Description
[7:1]	Not used.	-	-
0	*SEC3* Bit indicating if SEC3 is valid. The input is valid if it has no outstanding alarms.	0 1	Input SEC3 is invalid. Input SEC3 is valid.

Address (hex): 11

Register Name	*sts_reference_sources SEC1 & SEC2 TTL*	Description	(RO except for test when R/W) Reports any alarms active on inputs.	Default Value	0010 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reg. 11: Status of SEC2 TTL Input				*Reg. 11: Status of SEC1 TTL Input*	
		Reg. 12: Status of SEC2 DIFF Input				*Reg. 12: Status of SEC1 DIFF Input*	
						Reg. 14: Status of SEC3 Input	

Bit No.	Description	Bit Value	Value Description
[7:6] & [3:2]	Not Used	-	-
5 & 1	*Input Activity Alarm* Alarm indication from the activity monitors.	0 1	No alarm. Input has an active “no activity” alarm.
4 & 0	*Phase Lock Alarm* If the DPLL cannot indicate that it is phase locked onto the current source within 100 seconds this alarm will be raised.	0 1	No alarm. Phase lock alarm.

Address (hex): 12 As Reg. 11, but for *sts_reference_sources,* Inputs: *SEC1 & SEC2 DIFF*

Address (hex): 14 As Reg. 11, but for *sts_reference_sources,* Input: *SEC3*

Address (hex): 19

Register Name	*cnfg_ref_selection_priority SEC1 & SEC2 TTL*	Description	(R/W) Configures the relative priority of input sources SEC1 TTL and SEC2 TTL.	Default Value	0011 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
programmed_priority_SEC2 TTL				*programmed_priority_SEC1 TTL*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*programmed_priority_SEC2 TTL* This 4-bit value represents the relative priority of input SEC2 TTL. The smaller the number, the higher the priority; zero disables the input. *When the priority of this input is set to >0, the priority of SEC2 DIFF is set to 0 (disabled).	0000 0001-1111	Input SEC2 TTL unavailable for automatic selection. Input SEC2 TTL priority value.

Address (hex): 19 (cont...)

Register Name	*cnfg_ref_selection_priority SEC1 & SEC2 TTL*	Description	(R/W) Configures the relative priority of input sources SEC1 TTL and SEC2 TTL.	Default Value	0011 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
programmed_priority_SEC2 TTL				*programmed_priority_SEC1 TTL*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*programmed_priority_SEC1 TTL* This 4-bit value represents the relative priority of input SEC1 TTL. The smaller the number, the higher the priority; zero disables the input. *When the priority of this input is set to >0, the priority of SEC1 DIFF is set to 0 (disabled).	0000 0001-1111	Input SEC1 TTL unavailable for automatic selection. Input SEC1 TTL priority value.

Address (hex): 1A

Register Name	*cnfg_ref_selection_priority SEC1 & SEC2 DIFF*	Description	(R/W) Configures the relative priority of input sources SEC1 DIFF and SEC2 DIFF.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
programmed_priority_SEC2 DIFF				*programmed_priority_SEC1 DIFF*			

Bit No.	Description	Bit Value	Value Description
[7:4]	*programmed_priority_SEC2 DIFF* This 4-bit value represents the relative priority of input SEC2 DIFF. The smaller the number, the higher the priority; zero disables the input. *When the priority of this input is set to >0, the priority of SEC2 TTL is set to 0 (disabled).	0000 0001-1111	Input SEC2 DIFF unavailable for automatic selection. Input SEC2 DIFF priority value.
[3:0]	*programmed_priority_SEC1 DIFF* This 4-bit value represents the relative priority of input SEC1 DIFF. The smaller the number, the higher the priority; zero disables the input. *When the priority of this input is set to >0, the priority of SEC1 TTL is set to 0 (disabled).	0000 0001-1111	Input SEC1 DIFF unavailable for automatic selection. Input SEC1 DIFF priority value.

Address (hex): 1C

Register Name	*cnfg_ref_selection_priority SEC3*	Description	(R/W) Configures the relative priority of input source SEC3.	Default Value	0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				programmed_priority_SEC3			

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-
[3:0]	*cnfg_ref_selection_priority_9* This 4-bit value represents the relative priority of input SEC3. The smaller the number, the higher the priority; zero disables the input.	0000 0001-1111	Input SEC3 unavailable for automatic selection. Input SEC3 priority value.

Address (hex): 22

Register Name	*cnfg_ref_source_frequency <input>* *For Reg. 22, <input> = SEC1 TTL*	Description	(R/W) Configuration of the frequency and input monitoring for input <input>.	Default Value	SEC1 TTL= 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
divn_<input>	*lock8k_<input>*	*Bucket_id_<input>*		*reference_source_frequency_<input>*			

Bit No.	Description	Bit Value	Value Description
7	*divn_<input>* This bit selects whether or not input SEC1 TTL is divided in the programmable pre-divider prior to being input to the DPLL and frequency monitor- see Reg. 46 and Reg. 47 (*cnfg_freq_divn*).	0 1	Input <input> fed directly to DPLL and monitor. Input <input> fed to DPLL and monitor via pre-divider.
6	*lock8k_<input>* This bit selects whether or not input SEC1 TTL is divided in the preset pre-divider prior to being input to the DPLL. This results in the DPLL locking to the reference after it has been divided to 8 kHz. This bit is ignored when *divn_<input>* is set (bit =1).	0 1	Input <input> fed directly to DPLL. Input <input> fed to DPLL via preset pre-divider.
[5:4]	*Bucket_id_<input>* Every input has its own Leaky Bucket used for activity monitoring. There are four possible configurations for each Leaky Bucket- see Reg. 50 to Reg. 5F. This 2-bit field selects the configuration used for input <input>.	00 01 10 11	Input <input> activity monitor uses Leaky Bucket Configuration 0. Input <input> activity monitor uses Leaky Bucket Configuration 1. Input <input> activity monitor uses Leaky Bucket Configuration 2. Input <input> activity monitor uses Leaky Bucket Configuration 3.

Address (hex): 22 (cont...)

Register Name	*cnfg_ref_source_frequency <input>* *For Reg. 22, <input> = SEC1 TTL*	Description	(R/W) Configuration of the frequency and input monitoring for input <input>.	Default Value	SEC1 TTL= 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
divn_<input>	*lock8k_<input>*	*Bucket_id_<input>*		*reference_source_frequency_<input>*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*reference_source_frequency_<input>* Programs the frequency of the SEC connected to input <input>. If *divn_<input>* is set, then this value should be set to 0000 (8 kHz).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011-1111	8 kHz. 1544/2048 kHz (dependant on Bit 2 (*ip_sonsdhb*) in Reg. 34). 6.48 MHz. 19.44 MHz. 25.92 MHz. 38.88 MHz. 51.84 MHz. 77.76 MHz. 155.52 MHz. 2 kHz. 4 kHz. Not used.

Address (hex): 23 Use description for Reg. 22, but use <input> = *SEC2 TTL* Default = 0000 0000

Address (hex): 24 Use description for Reg. 22, but use <input> = *SEC1 DIFF* Default = 0000 0011

Address (hex): 25 Use description for Reg. 22, but use <input> = *SEC2 DIFF* Default = 0000 0011

Address (hex): 28 Use description for Reg. 22, but use <input> = *SEC3* Default = 0000 0011

Address (hex): 32

Register Name	*cnfg_operating_mode*	Description	(R/W) Register to force the state of DPLL1 controlling state machine.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					DPLL1_operating_mode		

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-

Address (hex): 32 (cont...)

Register Name	*cnfg_operating_mode*	Description	(R/W) Register to force the state of DPLL1 controlling state machine.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					DPLL1_operating_mode		

Bit No.	Description	Bit Value	Value Description
[2:0]	*DPLL1_operating_mode* This field is used to control the state of the internal finite state machine controlling DPLL1. A value of zero is used to allow the finite state machine to control itself. Any other value will force the state machine to jump into that state. Care should be taken when forcing the state machine. Whilst it is forced, the internal monitoring functions cannot affect the internal state machine, therefore, the user is responsible for all monitoring and control functions required to achieve the desired functionality.	000 001 010 011 100 101 110 111	Automatic (internal state machine controlled). Free Run. Holdover. Not used. Locked. Pre-locked2. Pre-locked. Phase Lost.

Address (hex): 33

Register Name	*force_select_reference_source*	Description	(R/W) Register used to force the selection of a particular SEC for DPLL1.	Default Value	0000 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				forced_select_SEC_input			

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-
[3:0]	*forced_select_SEC_input* Value representing the SEC to be selected by DPLL1. Value of 0 hex will leave the selection to the automatic control mechanism within the device. Using this mechanism will bypass all the monitoring functions assuming the selected input to be valid. If the device is not in state “Locked” then it will progress to state locked in the usual manner. If the input fails, the device will not change state to Holdover, as it is not allowed to disqualify the source. The effect of this register is simply to raise the priority of the selected input to “1” (highest). To ensure selection of the programmed input reference under all circumstances, revertive mode should be enabled (Reg. 34 bit 0 set to “1”).	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010-1111	Automatic state machine source selection Not used. Not used. DPLL1 forced to select input SEC1 TTL. DPLL1 forced to select input SEC2 TTL. DPLL1 forced to select input SEC1 DIFF. DPLL1 forced to select input SEC2 DIFF. Not used. Not used. DPLL1 forced to select input SEC3. Not used.

Address (hex): 34

Register Name	*cnfg_input_mode*	**Description**	(R/W) Register controlling various input modes of the device.	**Default Value**	1100 1010*

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
auto_extsync_en	*phalarm_time-out*	*XO_edge*		*extsync_en*	*ip_sonsdhb*		*reversion_mode*

Bit No.	**Description**	**Bit Value**	**Value Description**
7	*auto_extsync_en* Bit to automatically disable the external Frame Sync input following a source switch.	0 1	External Frame Sync enabled/disabled according to *extsync_en*. External Frame Sync enabled if *extsync_en* = 1 until a source switch. After this it is only re-enabled by writing "1" to *extsync_en* again.
6	*phalarm_timeout* Bit to enable the automatic timeout facility on phase alarms. When enabled, any source with a phase alarm set will have its phase alarm cancelled after 128 seconds.	0 1	Phase alarms on sources only cancelled by software. Phase alarms on sources automatically time out.
5	*XO_edge* If the 12.800 MHz oscillator module connected to REFCLK has one edge faster than the other, then for jitter performance reasons, the faster edge should be selected. This bit allows either the rising edge or the falling edge to be selected.	0 1	Device uses the rising edge of the external oscillator. Device uses the falling edge of the external oscillator.
4	Not used.	-	-
3	*extsync_en* Bit to select whether or not DPLL1 will look for a reference Sync pulse on the *SYNC1/2/3* input pins. Even though this bit may enable the external Sync reference, it may be disabled according to *auto_extsync_en*.	0 1	No External Frame Sync signal on selected Sync input- *SYNC1/2/3* pins ignored. External Sync derived from selected Sync input- *SYNC1/2/3* pin- according to *auto_extsync_en*.
2	*ip_sonsdhb* Bit to configure input frequencies to be either SONET or SDH derived. This applies only to selections of 0001 (bin) in the *cnfg_ref_source_frequency* registers when the input frequency is either 1544 kHz or 2048 kHz. *The default value of this bit is taken from the value of the SONSDHB pin at power-up.	0 1	SDH- inputs set to 0001 expected to be 2048 kHz. SONET- inputs set to 0001 expected to be 1544 kHz.
1	Not used.	-	-
0	*reversion_mode* Bit to select Revertive/Non-revertive mode. When in Non-revertive mode, the device will not automatically switch to a higher priority source, unless the current source fails. When in Revertive mode the device will always select the highest priority source.	0 1	Non-revertive mode. Revertive mode.

Address (hex): 35

Register Name	*cnfg_DPLL2_path*	Description	(R/W) Register to configure the feedback mode of DPLL2.	Default Value	1010 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL2_dig_ feedback						

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
6	*DPLL2_dig_feedback* Bit to select digital feedback mode for DPLL2.	0 1	DPLL2 in analog feedback mode. DPLL2 in digital feedback mode.
[5:0]	Not used.	-	-

Address (hex): 36

Register Name	*cnfg_differential_inputs*	Description	(R/W) Configures the differential inputs to be PECL or LVDS type inputs.	Default Value	0000 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						SEC2_DIFF_ PECL	*SEC1_DIFF_ PECL*

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
1	*SEC2_DIFF_PECL* Configures the SEC2 DIFF input to be compatible with either 3 V LVDS or 3 V PECL electrical levels.	0 1	SEC2 DIFF input LVDS compatible. SEC2 DIFF input PECL compatible (Default).
0	*SEC1_DIFF_PECL* Configures the SEC1 DIFF input to be compatible with either 3 V LVDS or 3 V PECL electrical levels.	0 1	SEC1 DIFF input LVDS compatible. SEC1 DIFF input PECL compatible (Default).

Address (hex): 38

Register Name	*cnfg_dig_outputs_sonsdh*	**Description**	Configures *Digital1* and *Digital2* output frequencies to be SONET or SDH compatible frequencies.	**Default Value**	0000 0100*

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	dig2_sonsdh	*dig1_sonsdh*					

Bit No.	**Description**	**Bit Value**	**Value Description**
7	Not used.	-	-
6	*dig2_sonsdh* Selects whether the frequencies generated by the *Digital2* frequency generator are SONET derived or SDH. *Default value of this bit is set by the SONSDHB pin at power-up.	1 0	*Digital2* can be selected from 1,544/3,088/6,176/12,352 kHz. *Digital2* can be selected from 2,048/4,096/8,192/16,384 kHz.
5	*dig1_sonsdh* Selects whether the frequencies generated by the *Digital1* frequency generator are SONET derived or SDH. *Default value of this bit is set by the SONSDHB pin at power-up.	1 0	*Digital1* can be selected from 1,544/3,088/6,176/12,352 kHz. *Digital1* can be selected from 2,048/4,096/8,192/16,384 kHz.
[4:0]	Not used.	-	-

Address (hex): 39

Register Name	*cnfg_digtial_frequencies*	**Description**	(R/W) Configures the actual frequencies of *Digital1* & *Digital2.*	**Default Value**	0000 1000

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
digital2_frequency		*digital1_frequency*					

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:6]	*digital2_frequency* Configures the frequency of *Digital2*. Whether this is SONET or SDH based is configured by Bit 6 (*dig2_sonsdh*) of Reg. 38.	00 01 10 11	*Digital2* set to 1,544 kHz or 2,048 kHz. *Digital2* set to 3,088 kHz or 4,096 kHz. *Digital2* set to 6,176 kHz or 8,192 kHz. *Digital2* set to 12,353 kHz or 16,384 kHz.
[5:4]	*digital1_frequency* Configures the frequency of *Digital1*. Whether this is SONET or SDH based is configured by Bit 5 (*dig1_sonsdh*) of Reg. 38.	00 01 10 11	*Digital1* set to 1,544 kHz or 2,048 kHz. *Digital1* set to 3,088 kHz or 4,096 kHz. *Digital1* set to 6,176 kHz or 8,192 kHz. *Digital1* set to 12,353 kHz or 16,384 kHz.
[3:0]	Not used.		

Address (hex): 3A

Register Name	*cnfg_differential_output*	Description	(R/W) Configures the electrical compatibility of the differential output driver to be 3 V PECL or 3 V LVDS.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						Output O1_LVDS_PECL	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*Output O1_LVDS_PECL* Selection of the electrical compatibility of Output O1 between 3 V PECL and 3 V LVDS.	00 01 10 11	Output O1 disabled. Output O1 3 V PECL compatible. Output O1 3 V LVDS compatible. Not used.

Address (hex): 3B

Register Name	*cnfg_auto_bw_sel*	Description	(R/W) Register to select automatic BW selection for DPLL1 path.	Default Value	1001 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
auto_BW_sel				DPLL1_lim_int			

Bit No.	Description	Bit Value	Value Description
7	*auto_BW_sel* Bit to select locked bandwidth (Reg. 67) or acquisition bandwidth (Reg. 69) for DPLL1.	1 0	Automatically selects either locked or acquisition bandwidth as appropriate. Always selects locked bandwidth.
[6:4]	Not used.	-	-
3	DPLL1_lim_int When set to 1 the integral path value of DPLL1 is limited or frozen when DPLL1 reaches either min. or max. frequency. This can be used to minimise subsequent overshoot when the DPLL is pulling in. Note that when this happens, the reported frequency value, via *current_DPLL_freq* (Reg. 0C, 0D and 07) is also frozen.	1 0	DPLL value frozen. DPLL not frozen.
[2:0]	Not used.	-	-

Address (hex): 3C

Register Name	*cnfg_nominal_frequency [7:0]*	Description	(R/W) Bits [7:0] of the register used to calibrate the crystal oscillator used to clock the device.	Default Value	1001 1001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_nominal_frequency_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*cnfg_nominal_frequency_value[7:0].*	-	See register description of Reg. 3D (*cnfg_nominal_frequency_value[15:8]*).

Address (hex): 3D

Register Name	*cnfg_nominal_frequency [15:8]*	Description	(R/W) Bits [15:8] of the register used to calibrate the crystal oscillator used to clock the device.	Default Value	1001 1001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
cnfg_nominal_frequency_value[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*cnfg_nominal_frequency_value[15:8]* This register is used in conjunction with Reg. 3C (*cnfg_nominal_frequency_value[7:0].*) to be able to offset the frequency of the crystal oscillator by up to +514 ppm and –771 ppm. The default value represents 0 ppm offset from 12.800 MHz. This value is an unsigned integer. The value in Reg. 3C/3D is used within the DPLL to offset the frequency value used in the DPLL only. This means that the value programmed will affect the value reported in the *sts_current_DPLL_frequency* (Reg. 07/0D/0C). Ilt will also affect the value programmed into the DPLL frequency offset limit .	-	In order to program the ppm offset of the crystal oscillator frequency, the value in Reg. 3C and Reg. 3D need to be concatenated. This value is an unsigned integer. The value multiplied by 0.0196229 dec will give the value in ppm. To calculate the absolute value, the default 39321 (9999 hex) needs to be subtracted.

Address (hex): 41

Register Name	*cnfg_DPLL_freq_limit [7:0]*	Description	(R/W) Bits [7:0] of the DPLL frequency limit register.	Default Value	0111 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bits[7:0] of *cnfg_DPLL_freq_limit*							

Bit No.	Description	Bit Value	Value Description
[7:0]	Bits [7:0] of *cnfg_DPLL_freq_limit* This register defines the extent of frequency offset to which either the DPLL1 or DPLL2 will track a source before limiting- i.e. it represents the pull-in range of the DPLLs. The offset of the device is determined by the frequency offset of the DPLL when compared to the offset of the external crystal oscillator clocking the device. If the oscillator is calibrated using *cnfg_nominal_frequency* Reg. 3C and 3D, then this calibration is automatically taken into account. The DPLL frequency limit limits the offset of the DPLL when compared to the calibrated oscillator frequency.	-	In order to calculate the frequency limit in ppm, Bits [1:0] of Reg. 42 and Bits [7:0] of Reg. 41 need to be concatenated. This value is a unsigned integer and represents limit *both* positive and negative in ppm. The value multiplied by 0.078 will give the value in ppm.

Address (hex): 42

Register Name	*cnfg_DPLL_freq_limit [9:8]*	Description	(R/W) Bits [9:8] of the DPLL frequency limit register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						Bits [9:8] of *cnfg_DPLL_freq_limit*	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	Bits [9:8] of *cnfg_DPLL_freq_limit*.	-	See Reg. 41 (*cnfg_DPLL_freq_limit*) for details.

Address (hex): 43

Register Name	*cnfg_interrupt_mask [7:0]*	Description	(R/W) Bits [7:0] of the interrupt mask register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		SEC2 DIFF	*SEC1 DIFF*	*SEC2 TTL*	*SEC1 TTL*	Set to 0	Set to 0

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-
5	*SEC2 DIFF* Mask bit for input SEC2 DIFF interrupt.	0 1	Input SEC2 DIFF cannot generate interrupts. Input SEC2 DIFF can generate interrupts.
4	*SEC1 DIFF* Mask bit for input SEC1 DIFF interrupt.	0 1	Input SEC1 DIFF cannot generate interrupts. Input SEC1 DIFF can generate interrupts.
3	*SEC2 TTL* Mask bit for input SEC2 TTL interrupt.	0 1	Input SEC2 TTL cannot generate interrupts. Input SEC2 TTL can generate interrupts.
2	*SEC1 TTL* Mask bit for input SEC1 TTL interrupt.	0 1	Input SEC1 TTL cannot generate interrupts. Input SEC1 TTL can generate interrupts.
[1:0]	Set to 0.	0	Set to 0.

Address (hex): 44

Register Name	*cnfg_interrupt_mask [15:8]*	Description	(R/W) Bits [15:8] of the interrupt mask register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
operating_ mode	*main_ref_failed*				Set to 0		*SEC3*

Bit No.	Description	Bit Value	Value Description
7	*operating_mode* Mask bit for *operating_mode* interrupt.	0 1	Operating mode cannot generate interrupts. Operating mode can generate interrupts.
6	*main_ref_failed* Mask bit for *main_ref_failed* interrupt.	0 1	Main reference failure cannot generate interrupts. Main reference failure can generate interrupts.
[5:3]	Not used.	-	-
2	Set to 0.	0	Set to 0.
1	Not used.	-	-
0	*SEC3* Mask bit for input SEC3 interrupt.	0 1	Input SEC3 cannot generate interrupts. Input SEC3 can generate interrupts.

Address (hex): 45

Register Name	*cnfg_interrupt_mask [23:16]*	Description	(R/W) Bits [23:16] of the interrupt mask register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sync_ip_alarm							

Bit No.	Description	Bit Value	Value Description
7	*Sync_ip_alarm* Mask bit for *Sync_ip_alarm* interrupt.	0 1	The external Sync input cannot generate interrupts. The external Sync input can generate interrupts.
[6:0]	Not used.	-	-

Address (hex): 46

Register Name	*cnfg_freq_divn [7:0].*	Description	(R/W) Bits [7:0] of the division factor for inputs using the DivN feature.	Default Value	1111 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
divn_value [7:0] (divide Input frequency by n)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*divn_value[7:0].*	-	See Reg. 47 (*cnfg_freq_divn {13:8]*) for details.

Address (hex): 47

Register Name	*cnfg_freq_divn [13:8]*	Description	(R/W) Bits [13:8] of the division factor for inputs using the DivN feature.	Default Value	0011 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		divn_value [13:8] (divide input frequency by n)					

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-

Address (hex): 47 (cont...)

Register Name	*cnfg_freq_divn [13:8]*	Description	(R/W) Bits [13:8] of the division factor for inputs using the DivN feature.	Default Value	0011 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	divn_value [13:8] (divide input frequency by n)						

Bit No.	Description	Bit Value	Value Description
[5:0]	*divn_value[13:8]* This register, in conjunction with Reg. 46 (*cnfg_freq_divn*) represents the integer value by which to divide inputs that use the DivN pre-divider. The DivN feature supports input frequencies up to a maximum of 100 MHz; therefore, the maximum value that should be written to this register is 30D3 hex (12499 dec). Use of higher DivN values may result in unreliable behaviour.	-	The input frequency will be divided by the value in this register plus 1. i.e. to divide by 8, program a value of 7.

Address (hex): 48

Register Name	*cnfg_monitors*	Description	(R/W) Configuration register controlling several input monitoring and switching options.	Default Value	0000 0100*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	los_flag_on_TDO	*ultra_fast_switch*	*ext_switch*	*PBO_freeze*	*PBO_en*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
6	*los_flag_on_TDO* Bit to select whether the *main_ref_fail* interrupt from DPLL1 is flagged on the TDO pin. If enabled this will not strictly conform to the IEEE 1149.1 JTAG standard for the function of the TDO pin. When enabled the TDO pin will simply mimic the state of the *main_ref_fail* interrupt status bit.	0 1	Normal mode, TDO complies with IEEE 1149.1. TDO pin used to indicate the state of the *main_ref_fail* interrupt status. This allows a system to have a hardware indication of a source failure very rapidly.
5	*ultra_fast_switch* Bit to enable ultra-fast switching mode. When in this mode, the device will disqualify a locked-to source as soon as it detects a few missing input cycles.	0 1	Currently selected source only disqualified by Leaky Bucket or frequency monitors. Currently selected source disqualified after less than 3 missing input cycles.

Address (hex): 48 (cont...)

Register Name	*cnfg_monitors*	Description	(R/W) Configuration register controlling several input monitoring and switching options.	Default Value	0000 0100*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	los_flag_on_TDO	*ultra_fast_switch*	*ext_switch*	*PBO_freeze*	*PBO_en*		

Bit No.	Description	Bit Value	Value Description
4	*ext_switch* Bit to enable external switching mode. When in external switching mode, the device is only allowed to lock to a pair of sources. If the programmed priority of input SEC1 TTL is non-zero, then when the SRCSW pin is *High*, the device will be forced to lock to input SEC1 TTL regardless of the signal present on that input. If the programmed priority of input SEC1 TTL is zero, then it will be forced to lock to input SEC1 DIFF instead. If the programmed priority of input SEC2 TTL is non-zero, then when the SRCSW pin is *Low*, the device will be forced to lock to input SEC2 TTL regardless of the signal present on that input. If the programmed priority of input SEC2 TTL is zero, then it will be forced to lock to input SEC2 DIFF instead. * The default value of this bit is dependent on the value of the SRCSW pin at power-up.	0 1	Normal operation mode. External source switching mode enabled. Operating mode of the device is always forced to be “locked” when in this mode.
3	*PBO_freeze* Bit to control the freezing of Phase Build-out operation. If Phase Build-out has been enabled and there have been some source switches, then the input-output phase relationship of DPLL1 is unknown. If Phase Build-out is no longer required, then it can be frozen. This will maintain the current input-output phase relationship, but not allow further Phase Build-out events to take place. Simply disabling Phase Build-out could cause a phase shift in the output, as DPLL1 re-locks the phase to zero degrees.	0 1	Phase Build-out not frozen. Phase Build-out frozen, no further Phase Build-out events will occur.
2	*PBO_en* Bit to enable Phase Build-out events on source switching. When enabled a Phase Build-out event is triggered every time DPLL1 selects a new source- this includes exiting the Holdover or Free-run states.	0 1	Phase Build-out not enabled. DPLL1 locks to zero degrees phase. Phase Build-out enabled on source switching.
1	Not used.	-	-

Address (hex): 4B

Register Name	*cnfg_registers_source_select*	Description	(R/W) Register to select the source of many of the registers.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			DPLL1_DPLL2_ select				

Bit No.	Description	Bit Value	Value Description
[7:5]	Not used.	-	-
4	*DPLL1_DPLL2_select* Bit to select between many of the registers associated with DPLL1 or DPLL2 e.g. frequency registers.	0 1	DPLL1 registers selected. DPLL2 registers selected.
[3:0]	Not used.	-	-

Address (hex): 4D

Register Name	*cnfg_freq_lim_ph_loss*	Description	(R/W) Register to enable the phase lost indication when DPLL hits its hard frequency limit.	Default Value	1000 1110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
freq_lim_ph_ loss							

Bit No.	Description	Bit Value	Value Description
7	*freq_lim_ph_loss* Bit to enable the phase lost indication when the DPLL hits its *hard* frequency limit as programmed in Reg. 41 and Reg. 42 (*cnfg_DPLL_freq_limit*). This results in the DPLL entering the phase lost state any time the DPLL tracks to the extent of its hard limit.	0 1	Phase lost/locked determined normally. Phase lost forced when DPLL tracks to hard limit.
[6:0]	Not used.	-	-

Address (hex): 50

Register Name	*cnfg_upper_threshold_0*	Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 0.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
upper_threshold_0_value (Activity alarm, Config. 0, Leaky Bucket - set threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_0_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate_0*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_0_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 51

Register Name	*cnfg_lower_threshold_0*	Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 0.	Default Value	0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_0_value (Activity alarm, Config. 0, Leaky Bucket - reset threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_0_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate_0*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_0_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 52

Register Name	*cnfg_bucket_size_0*	Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 0.	Default Value	0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_0_value (Activity alarm, Config. 0, Leaky Bucket - size)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_0_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 53 (*cnfg_decay_rate_0*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 53

Register Name	*cnfg_decay_rate_0*	Description	(R/W) Register to program the "decay" or "leak" rate for Leaky Bucket Configuration 0.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_0_value (Activity alarm, Config. 0, Leaky Bucket - leak rate)	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_0_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1,024 ms.

Address (hex): 54

Register Name	*cnfg_upper_threshold_1*	Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 1.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
upper_threshold_1_value (Activity alarm, Config. 1, Leaky Bucket - set threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_1_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 57 (*cnfg_decay_rate_1*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_1_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 55

Register Name	*cnfg_lower_threshold_1*	Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 1.	Default Value	0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_1_value (Activity alarm, Config. 1, Leaky Bucket - reset threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_1_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 57 (*cnfg_decay_rate_1*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_1_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 56

Register Name	*cnfg_bucket_size_1*	Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 1.	Default Value	0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_1_value (Activity alarm, Config. 1, Leaky Bucket - size)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_1_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 57 (*cnfg_decay_rate_1*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 57

Register Name	*cnfg_decay_rate_1*	Description	(R/W) Register to program the "decay" or "leak" rate for Leaky Bucket Configuration 1.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_1_value (Activity alarm, Config. 1, Leaky Bucket - leak rate)	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_1_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1,024 ms.

Address (hex): 58

Register Name	*cnfg_upper_threshold_2*	Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 2.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
upper_threshold_2_value (Activity alarm, Config. 2, Leaky Bucket - set threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_2_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5B (*cnfg_decay_rate_2*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_2_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 59

Register Name	*cnfg_lower_threshold_2*	Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 2.	Default Value	0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_2_value (Activity alarm, Config. 2, Leaky Bucket - reset threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_2_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5B (*cnfg_decay_rate_2*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_2_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 5A

Register Name	*cnfg_bucket_size_2*	Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 2.	Default Value	0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_2_value (Activity alarm, Config. 2, Leaky Bucket - size)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_2_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5B (*cnfg_decay_rate_2*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 5B

Register Name	*cnfg_decay_rate_2*	Description	(R/W) Register to program the "decay" or "leak" rate for Leaky Bucket Configuration 2.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_2_value (Activity alarm, Config. 2, Leaky Bucket - leak rate)	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_2_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1,024 ms.

Address (hex): 5C

Register Name	*cnfg_upper_threshold_3*	Description	(R/W) Register to program the activity alarm setting limit for Leaky Bucket Configuration 3.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
upper_threshold_3_value (Activity alarm, Config. 3, Leaky Bucket - set threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*upper_threshold_3_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5F (*cnfg_decay_rate_3*), in which this does not occur, the accumulator is decremented by 1. When the accumulator count reaches the value programmed as the *upper_threshold_3_value,* the Leaky Bucket raises an input inactivity alarm.	-	Value at which the Leaky Bucket will raise an inactivity alarm.

Address (hex): 5D

Register Name	*cnfg_lower_threshold_3*	Description	(R/W) Register to program the activity alarm resetting limit for Leaky Bucket Configuration 3.	Default Value	0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
lower_threshold_3_value (Activity alarm, Config. 3, Leaky Bucket - reset threshold)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*lower_threshold_3_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5F (*cnfg_decay_rate_3*), in which this does not occur, the accumulator is decremented by 1. The *lower_threshold_3_value* is the value at which the Leaky Bucket will reset an inactivity alarm.	-	Value at which the Leaky Bucket will reset an inactivity alarm.

Address (hex): 5E

Register Name	*cnfg_bucket_size_3*	Description	(R/W) Register to program the maximum size limit for Leaky Bucket Configuration 3.	Default Value	0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
bucket_size_3_value (Activity alarm, Config. 3, Leaky Bucket - size)							

Bit No.	Description	Bit Value	Value Description
[7:0]	*bucket_size_3_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in Reg. 5F (*cnfg_decay_rate_3*), in which this does not occur, the accumulator is decremented by 1. The number in the Bucket cannot exceed the value programmed into this register.	-	Value at which the Leaky Bucket will stop incrementing, even with further inactive periods.

Address (hex): 5F

Register Name	*cnfg_decay_rate_3*	Description	(R/W) Register to program the "decay" or "leak" rate for Leaky Bucket Configuration 3.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						decay_rate_3_value (Activity alarm, Config. 3, Leaky Bucket - leak rate)	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*decay_rate_3_value* The Leaky Bucket operates on a 128 ms cycle. If, during a cycle, it detects that an input has either failed or has been erratic, then for each cycle in which this occurs, the accumulator is incremented by 1, and for each period of 1, 2, 4, or 8 cycles, as programmed in this register, in which this does not occur, the accumulator is decremented by 1. The Leaky Bucket can be programmed to "leak" or "decay" at the same rate as the "fill" cycle, or effectively at one half, one quarter, or one eighth of the fill rate.	00 01 10 11	Bucket decay rate of 1 every 128 ms. Bucket decay rate of 1 every 256 ms. Bucket decay rate of 1 every 512 ms. Bucket decay rate of 1 every 1024 ms.

Address (hex): 61

Register Name	*cnfg_output_frequency (Output 02)*	**Description**	(R/W) Register to configure and enable the frequencies available on Output 02.	**Default Value**	0000 0110

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
				output_freq_02			

Bit No.	**Description**	**Bit Value**	**Value Description**
[7:4]	Not used.	-	-
[3:0]	*output_freq_02* Configuration of the output frequency available at Output 02. Many of the frequencies available are dependent on the frequencies of the APLL1 and the APLL2. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Output disabled. 2 kHz. 8 kHz. Digital2 (Reg. 39 *cnfg_digital_frequencies*). Digital1 (Reg. 39 *cnfg_digital_frequencies*). APLL1 frequency/48. APLL1 frequency/16. APLL1 frequency/12. APLL1 frequency/8. APLL1 frequency/6. APLL1 frequency/4. APLL2 frequency/64. APLL2 frequency/48. APLL2 frequency/16. APLL2 frequency/8. APLL2 frequency/4.

Address (hex): 62

Register Name	*cnfg_output_frequency (Output O1)*	Description	(R/W) Register to configure and enable the frequencies available on Output O1.	Default Value	1000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
output_freq_O1							

Bit No.	Description	Bit Value	Value Description
[7:4]	*output_freq_O1* Configuration of the output frequency available at Output O1. Many of the frequencies available are dependent on the frequencies of the APLL1 and the APLL2. These are configured in Reg. 64 and Reg. 65. For more detail see the detailed section on configuring the output frequencies.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Output disabled. 2 kHz. 8 kHz. APLL1 frequency/2. Digital1 (Reg. 39 *cnfg_digital_frequencies*). APLL1 frequency. APLL1 frequency/16. APLL1 frequency/12. APLL1 frequency/8. APLL1 frequency/6. APLL1 frequency/4. APLL2 frequency/64. APLL2 frequency/48. APLL2 frequency/16. APLL2 frequency/8. APLL2 frequency/4.
[3:0]	Not used.	-	-

Address (hex): 63

Register Name	*cnfg_output_frequency (MFrSync/FrSync)*	Description	(R/W) Register to configure and enable the frequencies available on outputs MFrSync and FrSync.	Default Value	1100 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MFrSync_en	*FrSync_en*						

Bit No.	Description	Bit Value	Value Description
7	*MFrSync_en* Register bit to enable the 2 kHz Sync output (MFrSync).	0 1	Output MFrSync disabled. Output MFrSync enabled.
6	*FrSync_en* Register bit to enable the 8 kHz Sync output (FrSync).	0 1	Output FrSync disabled. Output FrSync enabled.
[5:0]	Not used.	-	-

Address (hex): 64

Register Name	*cnfg_DPLL2_frequency*	Description	(R/W) Register to configure DPLL2 Frequency.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					DPLL2_frequency		

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-
[2:0]	*DPLL2_frequency* Register to configure the frequency of operation of DPLL2. The frequency of DPLL2 will also affect the frequency of the APLL2 which, in turn, affects the frequencies available at outputs 01 and 02 see Reg. 61 - Reg. 63. It is also possible to not use DPLL2 at all, but use the APLL2 to run directly from DPLL1 output, see Reg. 65 (*cnfg_DPLL1_frequency*). If any frequencies are required from the APLL2 then DPLL2 should not be squelched, as the APLL2 input is squelched and the APLL2 will free run.	000 001 010 011 100 101 110 111	DPLL2 mode = squelched (clock off). DPLL2 mode = 77.76 MHz (OC-N rates), giving APLL2 frequency = 311.04 MHz. DPLL2 mode = 12E1, giving APLL2 output frequency (before dividers) = 98.304 MHz. DPLL2 mode = 16E1, giving APLL2 output frequency (before dividers) = 131.072 MHz. DPLL2 mode = 24DS1, giving APLL2 output frequency (before dividers) = 148.224 MHz. DPLL2 mode = 16DS1, giving APLL2 output frequency (before dividers) = 98.816 MHz. DPLL2 mode = E3, giving APLL2 output frequency (before dividers) = 274.944 MHz. DPLL2 mode = DS3, giving APLL2 output frequency (before dividers) = 178.944 MHz.

Address (hex): 65

Register Name	*cnfg_DPLL1_frequency*	Description	(R/W) Register to configure DPLL1 and several other parameters.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPLL2_meas_ DPLL1_ph	*APLL2_for_ DPLL1_E1/DS1*	*DPLL1_freq_to_APLL2*			*DPLL1_frequency*		

Bit No.	Description	Bit Value	Value Description
7	*DPLL2_meas_DPLL1_ph* Register bit to control the feature where DPLL2 is used to measure phase offset between the SEC input selected by DPLL1 and either of the other two SEC Inputs. Refer to the Section “Measuring Phase Between Master and Slave/Stand-by SEC Sources” on page 33.	0 1	Normal- DPLL2 normal operation. DPLL2 disabled, DPLL2 phase detector used to measure phase between selected DPLL1 input and selected DPLL2 input.
6	*APLL2_for_DPLL1_E1/DS1* Register bit to select whether the APLL2 takes its input from DPLL2 or DPLL1. If DPLL1 is selected then the frequency is controlled by Bits [5:4], *DPLL1_freq_to_APLL2*.	0 1	APLL2 takes its input from DPLL2. APLL2 takes its input from DPLL1.

Address (hex): 65 (cont...)

Register Name	*cnfg_DPLL1_frequency*	Description	(R/W) Register to configure DPLL1 and several other parameters.	Default Value	0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPLL2_meas_ DPLL1_ph	*APLL2_for_ DPLL1_E1/DS1*	*DPLL1_freq_to_APLL2*			*DPLL1_frequency*		

Bit No.	Description	Bit Value	Value Description
[5:4]	*DPLL1_freq_to_APLL2* Register to select the frequency/mode of DPLL1 which is driven to the APLL2 when selected by Bit 6, *APLL2_for_DPLL1_E1/DS1*. Register to select DPLL1's frequency driven to the APLL2 (DPLL1 mode*) when selected by Bit 6, *APLL2_for_DPLL1_E1/DS1 ; and consequently the APLL output frequency in the T4 path.* *Note that this is not the operating frequency of DPLL1 itself - which is fixed at outputting 77.76 MHz - but is the multiplied output from the LF Output DFS block. See Figure 5 "PLL Block Diagram" on page 15.	00 01 10 11	DPLL1 mode = 12E1, giving APLL2 output frequency (before dividers) = 98.304 MHz. DPLL1 mode = 16E1, giving APLL2 output frequency (before dividers) = 131.072 MHz. DPLL1 mode = 24DS1, giving APLL2 output frequency (before dividers) = 148.224 MHz. DPLL1 mode = 16DS1, giving APLL2 output frequency (before dividers) = 98.816 MHz.
3	Not used.	-	-
[2:0]	*DPLL1_frequency* Register to configure the frequency driven to APLL1 (DPLL1 mode*) and consequently the APLL output frequency in the T0 path. This register affects the frequencies available at outputs 01 and 02, see Reg. 61 - Reg. 63. *Note that this is not the operating frequency of the DPLL1 itself - which is fixed at outputting 77.76 MHz - but is the multiplied output from the LF Output DFS block. See Figure 5 "PLL Block Diagram" on page 15. Note...001 is the only selection that does not bypass APLL3. All other selections use digital feedback.	000 001 010 011 100 101 110 111	DPLL1 mode = 77.76 MHz, digital feedback, APLL1 output frequency (before dividers) = 311.04 MHz. DPLL1 mode = 77.76 MHz, analog feedback, APLL1 output frequency (before dividers) = 311.04 MHz. DPLL1 mode = 12E1, giving APLL1 output frequency (before dividers) = 98.304 MHz. DPLL1 mode = 16E1, giving APLL1 output frequency (before dividers) = 131.072 MHz. DPLL1 mode = 24DS1, giving APLL1 output frequency (before dividers) = 148.224 MHz. DPLL1 mode = 16DS1, giving APLL1 output frequency (before dividers) = 98.816 MHz. Not used. Not used.

Address (hex): 66

Register Name	*cnfg_DPLL2_bw*	Description	(R/W) Register to configure the bandwidth of DPLL2.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL2_bandwidth	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	*DPLL2_bandwidth* Register to configure the bandwidth of DPLL2.	00 01 10 11	DPLL2 18 Hz bandwidth. DPLL2 35 Hz bandwidth. DPLL2 70 Hz bandwidth. Not used.

Address (hex): 67

Register Name	*cnfg_DPLL1_locked_bw*	Description	(R/W) Register to configure the bandwidth of DPLL1, when phase locked to an input.	Default Value	0001 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL1_locked_bandwidth	

Bit No.	Description	Bit Value	Value Description
[7:2]	Not used.	-	-
[1:0]	DPLL1_*locked_bandwidth* Register to configure the bandwidth of DPLL1 when locked to an input reference. Reg. 3B Bit 7 is used to control whether this bandwidth is used all of the time or automatically switched to when phase locked.	11 00 01 10	DPLL1, 18 Hz locked bandwidth. DPLL1, 35 Hz locked bandwidth. DPLL1, 70 Hz locked bandwidth. Not used.

Address (hex): 69

Register Name	*cnfg_DPLL1_acq_bw*	Description	(R/W) Register to configure the bandwidth of DPLL1, when not phase locked to an input.	Default Value	0001 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL1_acquisition_bandwidth	

Bit No.	Description	Bit Value	Value Description
[7:4]	Not used.	-	-

Address (hex): 69 (cont...)

Register Name	*cnfg_DPLL1_acq_bw*	Description	(R/W) Register to configure the bandwidth of DPLL1, when not phase locked to an input.	Default Value	0001 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						DPLL1_acquisition_bandwidth	

Bit No.	Description	Bit Value	Value Description
[3:0]	*DPLL1_acquisition_bandwidth* Register to configure the bandwidth of DPLL1 when acquiring phase lock on an input reference. Reg. 3B Bit 7 is used to control whether this bandwidth is not used or automatically switched to when not phase locked.	11 00 01 10	DPLL1, 18 Hz acquisition bandwidth. DPLL1, 35 Hz acquisition bandwidth. DPLL1, 70 Hz acquisition bandwidth. Not used.

Address (hex): 6A

Register Name	*cnfg_DPLL2_damping*	Description	(R/W) Register to configure the damping factor of DPLL2, along with the gain of Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL2_PD2_gain_alog_8k				*DPLL2_damping*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
[6:4]	*DPLL2_PD2_gain_alog_8k* Register to control the gain of the Phase Detector 2 when locking to a reference of 8 kHz or less in analog feedback mode. This setting is only used if automatic gain selection is enabled in Reg. 6C Bit 7, *cnfg_DPLL2_PD2_gain*.	-	Gain value of the Phase Detector 2 when locking to an 8 kHz reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6A (cont...)

Register Name	*cnfg_DPLL2_damping*	Description	(R/W) Register to configure the damping factor of DPLL2, along with the gain of Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL2_PD2_gain_alog_8k				*DPLL2_damping*		

Bit No.	Description	Bit Value	Value Description		
[2:0]	*DPLL2_damping* Register to configure the damping factor of DPLL2. The bit values correspond to different damping factors, depending on the bandwidth selected. The Gain Peak for the Damping Factors given in the Value Description (right) are tabulated below:		**Damping Factor for Bandwidth of 18 Hz:**	**Damping Factor for Bandwidth of 35 Hz:**	**Damping Factor for Bandwidth of 70 Hz:**
		001	1.2	1.2	1.2
		010	2.5	2.5	2.5
		011	5	5	5
		100	5	10	10
		101	5	10	20

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

Address (hex): 6B

Register Name	*cnfg_DPLL1_damping*	Description	(R/W) Register to configure the damping factor of DPLL1, along with the gain of the Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL1_PD2_gain_alog_8k				*DPLL1_damping*		

Bit No.	Description	Bit Value	Value Description
7	Not used.	-	-
[6:4]	*DPLL1_PD2_gain_alog_8k* Register to control the gain of the Phase Detector 2 when locking to a reference of 8 kHz or less in analog feedback mode. This setting is only used if automatic gain selection is enabled in Reg. 6D Bit 7, *cnfg_DPLL1_PD2_gain*.	-	Gain value of the Phase Detector 2 when locking to an 8 kHz reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6B (cont...)

Register Name	*cnfg_DPLL1_damping*	Description	(R/W) Register to configure the damping factor of DPLL1, along with the gain of the Phase Detector 2 in some modes.	Default Value	0001 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	DPLL1_PD2_gain_alog_8k				*DPLL1_damping*		

Bit No.	Description	Bit Value	Value Description		
[2:0]	*DPLL1_damping* Register to configure the damping factor of DPLL1. The bit values correspond to different damping factors, depending on the bandwidth selected. The Gain Peak for the Damping Factors given in the Value Description (right) are the same as those tabulated in the description for Reg. 6A.		**Damping Factor for Bandwidth of 18 Hz:**	**Damping Factor for Bandwidth of 35 Hz:**	**Damping Factor for Bandwidth of 70 Hz:**
		001	1.2	1.2	1.2
		010	2.5	2.5	2.5
		011	5	5	5
		100	5	10	10
		101	5	10	20

Address (hex): 6C

Register Name	*cnfg_DPLL2_PD2_gain*	Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for DPLL2.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPLL2_PD2_gain_enable	*DPLL2_PD2_gain_alog*				*DPLL2_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
7	*DPLL2_PD2_gain_enable*	0 1	DPLL2 Phase Detector 2 not used. DPLL2 Phase Detector 2 gain enabled and choice of gain determined according to the locking mode: - digital feedback mode - analog feedback mode - analog feedback at 8 kHz.
[6:4]	*DPLL2_PD2_gain_alog* Register to control the gain of Phase Detector 2 when locking to a reference, higher than 8 kHz, in analog feedback mode. This setting is not used if automatic gain selection is disabled in Bit 7, *DPLL2_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking to a high frequency reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6C (cont...)

Register Name	*cnfg_DPLL2_PD2_gain*	Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for DPLL2.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPLL2_PD2_gain_enable	*DPLL2_PD2_gain_alog*				*DPLL2_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
[2:0]	*DPLL2_PD2_gain_digital* Register to control the gain of Phase Detector 2 when locking to a reference in digital feedback mode. This setting is always used if automatic gain selection is disabled in Bit 7, *DPLL2_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking to any reference in digital feedback mode.

Address (hex): 6D

Register Name	*cnfg_DPLL1_PD2_gain*	Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for DPLL1.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPLL1_PD2_gain_enable	*DPLL1_PD2_gain_alog*				*DPLL1_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
7	*DPLL1_PD2_gain_enable*	0	DPLL2 Phase Detector 2 not used.
		1	DPLL2 Phase Detector 2 gain enabled and choice of gain determined according to the locking mode: - digital feedback mode - analog feedback mode - analog feedback at 8 kHz
[6:4]	*DPLL1_PD2_gain_alog* Register to control the gain of Phase Detector 2 when locking to a reference, higher than 8 kHz, in analog feedback mode. This setting is not used if automatic gain selection is disabled in Bit 7, *DPLL1_PD2_gain_enable*.	-	Gain value of Phase Detector 2 when locking to a high frequency reference in analog feedback mode.
3	Not used.	-	-

Address (hex): 6D (cont...)

Register Name	*cnfg_DPLL1_PD2_gain*	Description	(R/W) Register to configure the gain of Phase Detector 2 in some modes for DPLL1.	Default Value	1100 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPLL1_PD2_gain_enable	*DPLL1_PD2_gain_alog*				*DPLL1_PD2_gain_digital*		

Bit No.	Description	Bit Value	Value Description
[2:0]	*DPLL1_PD2_gain_digital* Register to control the gain of Phase Detector 2 when locking to a reference in digital feedback mode. Automatic gain selection must be enabled (Bit 7, *DPLL1_PD2_gain_enable*), for *DPLL1_PD2_gain_digital* to have any effect.	-	Gain value of Phase Detector 2 when locking to any reference in digital feedback mode.

Address (hex): 70

Register Name	*cnfg_phase_offset [7:0]*	Description	(R/W) Bits [7:0] of the phase offset control register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
phase_offset_value[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*phase_offset_value[7:0]* Register forming part of the phase offset control.	-	See Reg. 71, *cnfg_phase_offset[15:8]* for more details.

Address (hex): 71

Register Name	*cnfg_phase_offset [15:8]*	Description	(R/W) Bits [15:8] of the phase offset control register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
phase_offset_value[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*phase_offset_value[15:8]* Register forming part of the phase offset control. If the phase offset register is written to when the DPLL is locked to an input, then it is possible that some internal signals become out of synchronisation. In order to avoid this, the phase offset is automatically "ramped" to the new value. If the phase offset is only ever adjusted when the device is in Holdover, then this is not necessary, and this automatic "ramping" can be disabled, see Reg. 7C, *cnfg_sync_monitor*. This register is ignored and has no affect when Phase Build-out is enabled in either Reg. 48 or Reg. 76.	-	The value in this register is to be concatenated with the contents of Reg. 70 *cnfg_phase_offset[7:0]*. This value is a 16-bit 2's complement signed number. The value multiplied by 6.279 represents the extent of the applied phase offset in picoseconds. The phase offset register is not a control to a "traditional" delay line. This number 6.279 actually represents a fractional portion of the period of an internal 77.76 MHz cycle and can, therefore, be represented more accurately as follows. Each bit value of the register represents the period of the internal 77.76 MHz clock divided by 2^{11}. If, for example, the DPLL is locked to a reference that is +1 ppm in frequency with respect to a perfect oscillator, then the period, and hence the phase offset, will be decreased by 1 ppm. Programming a value of 1024 into the phase offset register will produce a complete inversion of the 77.76 MHz output clock. *Note...The exact period of the internal 77.76 MHz clock is determined by the current state of the DPLL i.e. in Locked mode its accuracy depends on that of the locked to input, in Holdover or Free-run it depends on the accuracy of the external oscillator.*

Address (hex): 72

Register Name	*cnfg_PBO_phase_offset*	Description	(R/W) Register to offset the mean time error of Phase Build-out events.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PBO_phase_offset					

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-

Address (hex): 72 (cont...)

Register Name	*cnfg_PBO_phase_offset*	Description	(R/W) Register to offset the mean time error of Phase Build-out events.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		PBO_phase_offset					

Bit No.	Description	Bit Value	Value Description
[5:0]	*PBO_phase_offset* Each time a Phase Build-out event is triggered, there is an uncertainty of up to 5 ns introduced which translates to a phase hit on the output. The mean error over a large number of events is designed to be zero. This register can be used to introduce a fixed offset into each PBO event. This will have the effect of moving the mean error positive or negative in time.	-	The value in this register is a 6-bit 2's complement number. The value multiplied by 0.101 gives the programmed offset in nanoseconds. Values greater than +1.4 ns or less than -1.4 ns should NOT be used as they may cause internal mathematical errors.

Address (hex): 73

Register Name	*cnfg_phase_loss_fine_limit*	Description	(R/W) Register to configure some of the parameters of the DPLL phase detectors.	Default Value	1010 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
fine_limit_en	*noact_ph_loss*	*narrow_en*			*phase_loss_fine_limit*		

Bit No.	Description	Bit Value	Value Description
7	*fine_limit_en* Register bit to enable the *phase_loss_fine_limit* Bits [2:0]. When disabled, phase lock/loss is determined by the other means within the device. This must be disabled when multi-UI jitter tolerance is required, see Reg. 74, *cnfg_phase_loss_course_limit*.	0 1	Phase loss indication only triggered by other means. Phase loss triggered when phase error exceeds the limit programmed in *phase_loss_fine_limit*, Bits [2:0].
6	*noact_ph_loss* The DPLL detects that an input has failed very rapidly. Normally, when the DPLL detects this condition, it does not consider phase lock to be lost and will phase lock to the nearest edge (±180°) when a source becomes available again, hence giving tolerance to missing cycles. If phase loss is indicated, then frequency and phase locking is instigated (±360° locking). This bit can be used to force the DPLL to indicate phase loss immediately when no activity is detected.	0 1	No activity on reference does not trigger phase lost indication. No activity triggers phase lost indication.

Address (hex): 73 (cont...)

Register Name	*cnfg_phase_loss_fine_limit*	Description	(R/W) Register to configure some of the parameters of the DPLL phase detectors.	Default Value	1010 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
fine_limit_en	*noact_ph_loss*	*narrow_en*			*phase_loss_fine_limit*		

Bit No.	Description	Bit Value	Value Description
5	*narrow_en* (test control bit) Set to 1 (default value).	0 1	 Set to 1.
[4:3]	Not used.	-	-
[2:0]	*phase_loss_fine_limit* When enabled by Bit 7, this register coarsely sets the phase limit at which the device indicates phase lost or locked. The default value of 2 (010) gives a window size of around ±90 - 180°. The phase position of the inputs to the DPLL has to be within the window limit for 1 – 2 seconds before the device indicates phase lock. If it is outside the window for any time then phase loss is immediately indicated. For most cases the default value of 2 (010) is satisfactory. The window size changes in proportion to the value, so a value of 1 (001) will give a narrow phase acceptance or lock window of approximately ±45 - 90°.	000 001 010 011 100 101 110 111	Do not use. Indicates phase loss continuously. Small phase window for phase lock indication. Recommended value.))) Larger phase window for phase lock indication.))

Address (hex): 74

Register Name	*cnfg_phase_loss_coarse_limit*	Description	(R/W) Register to configure some of the parameters of DPLL phase detectors.	Default Value	1000 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
coarse_lim_ phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	Description	Bit Value	Value Description
7	*coarse_lim_phaseloss_en* Register bit to enable the coarse phase detector, whose range is determined by *phase_loss_coarse_limit* Bits [3:0]. This register sets the limit in the number of input clock cycles (UI) that the input phase can move by before the DPLL indicates phase lost.	0 1	Phase loss not triggered by the coarse phase lock detector. Phase loss triggered when phase error exceeds the limit programmed in *phase_loss_coarse_limit*, Bits [3:0].

Address (hex): 74 (cont...)

Register Name	*cnfg_phase_loss_coarse_limit*	**Description**	(R/W) Register to configure some of the parameters of DPLL phase detectors.	**Default Value**	1000 0101

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
coarse_lim_ phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	**Description**	**Bit Value**	**Value Description**
6	*wide_range_en* To enable the device to be tolerant to large amounts of applied jitter and still do direct phase locking at the input frequency rate (up to 77.76 MHz), a wide range phase detector and phase lock detector is employed. This bit enables the wide range phase detector. This allows the device to be tolerant to, and therefore keep track of, drifts in input phase of many cycles (UI). The range of the phase detector is set by the same register used for the phase loss coarse limit (Bits [3:0]).	0 1	Wide range phase detector off. Wide range phase detector on.
5	*multi_ph_resp* Enables the phase result from the coarse phase detector to be used in the DPLL algorithm. Bit 6 should also be set when this is activated. The coarse phase detector can measure and keep track over many thousands of input cycles, thus allowing excellent jitter and wander tolerance. This bit enables that phase result to be used in the DPLL algorithm, so that a large phase measurement gives a faster pull-in of the DPLL. If this bit is not set then the phase measurement is limited to ±360° which can give a slower pull-in rate at higher input frequencies, but could also be used to give less overshoot. Setting this bit in direct locking mode, for example with a 19.44 MHz input, would give the same dynamic response as a 19.44 MHz input used with 8 k locking mode, where the input is divided down internally to 8 kHz first.	0 1	DPLL phase detector limited to ±360° (±1 UI). However it will still remember its original phase position over many thousands of UI if Bit 6 is set. DPLL phase detector also uses the full coarse phase detector result. It can now measure up to: ±360° x 8191 UI = ±2,948,760°.
4	Not used.	-	-

Address (hex): 74 (cont...)

Register Name	*cnfg_phase_loss_coarse_limit*	Description	(R/W) Register to configure some of the parameters of DPLL phase detectors.	Default Value	1000 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
coarse_lim_ phaseloss_en	*wide_range_en*	*multi_ph_resp*		*phase_loss_coarse_limit*			

Bit No.	Description	Bit Value	Value Description
[3:0]	*phase_loss_coarse_limit* Sets the range of the coarse phase loss detector and the coarse phase detector. When locking to a high frequency signal, and jitter tolerance greater than 0.5 UI is required, then the DPLL can be configured to track phase errors over many input clock periods. This is particularly useful with very low bandwidths. This register configures how many UI over which the input phase can be tracked. It also sets the range of the coarse phase loss detector, which can be used with or without the multi-UI phase capture range capability. This register value is used by Bits 6 and 7.	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100-1111	Input phase error tracked over ±1 UI. Input phase error tracked over ±3 UI. Input phase error tracked over ±7 UI. Input phase error tracked over ±15 UI. Input phase error tracked over ±31 UI. Input phase error tracked over ±63 UI. Input phase error tracked over ±127 UI. Input phase error tracked over ±255 UI. Input phase error tracked over ±511 UI. Input phase error tracked over ±1023 UI. Input phase error tracked over ±2047 UI. Input phase error tracked over ±4095 UI. Input phase error tracked over ±8191 UI.

Address (hex): 76

Register Name	*cnfg_ip_noise_window*	Description	(R/W) Register to configure the noise rejection function for low frequency inputs.	Default Value	0000 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ip_noise_ window_en							

Bit No.	Description	Bit Value	Value Description
7	*ip_noise_window_en* Register bit to enable a window of 5% tolerance around low-frequency inputs (2, 4 and 8 kHz). This feature ensures that any edge caused by noise outside the 5% window where the edge is expected will not be considered within the DPLL. This reduces any possible phase hit when a low-frequency connection is removed and contact bounce is possible.	0 1	DPLL considers all edges for phase locking. DPLL ignores input edges outside a 95% to 105% window.
[6:0]	Not used.	-	-

Address (hex): 77

Register Name	*sts_current_phase [7:0]*	Description	(RO) Bits [7:0] of the current phase register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
current_phase[7:0]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*current_phase* Bits [7:0] of the current phase register. See Reg. 78 *sts_current_phase [15:8]* for details.	-	See Reg. 78 *sts_current_phase [15:8]* for details.

Address (hex): 78

Register Name	*sts_current_phase [15:8]*	Description	(RO) Bits [15:8] of the current phase register.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
current_phase[15:8]							

Bit No.	Description	Bit Value	Value Description
[7:0]	*current_phase* Bits [15:8] of the current phase register. This register is used to read either from the phase detector of either DPLL1 or DPLL2, according to Reg. 4B Bit 4 *DPLL2_DPLL1_select*. The value is averaged in the phase averager before being made available.	-	The value in this register should be concatenated with the value in Reg. 77 *sts_current_phase [7:0]*. This 16-bit value is a 2's complement signed integer. The value multiplied by 0.707 is the averaged value of the current phase error, in degrees, as measured at the DPLL's phase detector.

Address (hex): 79

Register Name	*cnfg_phase_alarm_timeout*	Description	(R/W) Register to configure how long before a phase alarm is raised on an input.	Default Value	0011 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		timeout_value (in two-second intervals)					

Bit No.	Description	Bit Value	Value Description
[7:6]	Not used.	-	-

Address (hex): 79 (cont...)

Register Name	*cnfg_phase_alarm_timeout*	Description	(R/W) Register to configure how long before a phase alarm is raised on an input.	Default Value	0011 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			timeout_value (in two-second intervals)				

Bit No.	Description	Bit Value	Value Description
[5:0]	*timeout_value* Phase alarms can only be raised on an input when DPLL1 is attempting to lock to it. Once an input has been rejected due to a phase alarm, there is no way to measure whether it is good again, because it is no longer selected by the DPLL. The phase alarms can either remain until reset by software, or timeout after 128 seconds, as selected in Reg. 34 Bit 6, *phalarm_timeout.*	-	This 6-bit unsigned integer represents the length of time before a phase alarm will be raised on an input. The value multiplied by 2 gives the time in seconds. This time value is the time that the controlling state machine will spend in Pre-locked, Pre-locked2 or Phase-lost modes before setting the phase alarm on the selected input.

Address (hex): 7A

Register Name	*cnfg_sync_pulses*	Description	(R/W) Register to configure the Sync outputs available from FrSync and MFrSync and select the source for the 2 kHz and 8 kHz outputs from 01 and 02.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2k_8k_from_ DPLL2				*8k_invert*	*8k_pulse*	*2k_invert*	*2k_pulse*

Bit No.	Description	Bit Value	Value Description
7	*2k_8k_from_DPLL2* Register to select the source (DPLL1 or DPLL2) for the 2 kHz and 8 kHz outputs available from 01 and 02.	0 1	2/8 kHz on 01 and 02 generated from DPLL1. 2/8 kHz on 01 and 02 generated from DPLL2.
[6:4]	Not used.	-	-
3	*8k_invert* Register bit to invert the 8 kHz output from FrSync.	0 1	8 kHz FrSync output not inverted. 8 kHz FrSync output inverted.
2	*8k_pulse* Register bit to enable the 8 kHz output from FrSync to be either pulsed or 50:50 duty cycle. Output 02 must be enabled to use “pulsed output” mode on the FrSync output, and then the pulse width on the FrSync output will be equal to the period of the output programmed on 02.	0 1	8 kHz FrSync output not pulsed. 8 kHz FrSync output pulsed.

Address (hex): 7A (cont...)

Register Name	*cnfg_sync_pulses*	Description	(R/W) Register to configure the Sync outputs available from FrSync and MFrSync and select the source for the 2 kHz and 8 kHz outputs from 01 and 02.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2k_8k_from_DPLL2				*8k_invert*	*8k_pulse*	*2k_invert*	*2k_pulse*

Bit No.	Description	Bit Value	Value Description
1	*2k_invert* Register bit to invert the 2 kHz output from MFrSync.	0 1	2 kHz MFrSync output not inverted. 2 kHz MFrSync output inverted.
0	*2k_pulse* Register bit to enable the 2 kHz output from MFrSync to be either pulsed or 50:50 duty cycle. Output 02 must be enabled to use “pulsed output” mode on the MFrSync output, and then the pulse width on the MFrSync output will be equal to the period of the output programmed on 02.	0 1	2 kHz MFrSync output not pulsed. 2 kHz MFrSync output pulsed.

Address (hex): 7B

Register Name	*cnfg_sync_phase*	Description	(R/W) Register to configure the behaviour of the synchronisation for the external frame reference.	Default Value	0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Indep_FrSync/MFrSync	*Sync_OC-N_rates*	*Sync_phase_SYNC3*		*Sync_phase_SYNC2*		*Sync_phase_SYNC1*	

Bit No.	Description	Bit Value	Value Description
7	*Indep_FrSync/MrSync* This allows the option of either maintaining alignment of FrSync and other clock outputs during synchronisation from the selected Sync input, or whether to not maintain alignment to all clocks and so not disturb any of the output clocks.	0 1	MFrSync & FrSync outputs are always aligned with other output clocks. MFrSync & FrSync outputs are independent of other output clocks.

Address (hex): 7B (cont...)

Register Name	*cnfg_sync_phase*	**Description**	(R/W) Register to configure the behaviour of the synchronisation for the external frame reference.	**Default Value**	0000 0000

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Indep_FrSync/ MFrSync	*Sync_OC-N_ rates*	*Sync_phase_SYNC3*		*Sync_phase_SYNC2*		*Sync_phase_SYNC1*	

Bit No.	**Description**	**Bit Value**	**Value Description**
6	Sync_OC-N_rates This allows the selected Sync input to synchronize the OC-3 derived clocks in order to maintain alignment between the FrSync output and output clocks and allow a finer sampling precision of the selected Sync input of either 19.44MHz or 38.88MHz.	0 1	The OC-N rate clocks are not affected by the selected Sync input. The selected Sync input is sampled with a 6.48 MHz precision. 6.48MHz should be provided as the input reference clock. Allows the selected Sync input to operate with a 19.44 MHz or 38.88 MHz input clock reference. Input sampling and output alignment to 19.44 MHz is used when the current clock input is 19.44 MHz, otherwise 38.88 MHz sampling precision is used.
[5:4]	*Sync_phase_SYNC3* Register to control the sampling of the external Sync input. Nominally the falling edge of the input is aligned with the falling edge of the reference clock. The margin is ±0.5 U.I. (Unit Interval).	00 01 10 11	On target. 0.5 U.I. early. 1 U.I. late. 0.5 U.I. late.
[3:2]	*Sync_phase_SYNC2* Register to control the sampling of the external Sync input. Nominally the falling edge of the input is aligned with the falling edge of the reference clock. The margin is ±0.5 U.I. (Unit Interval).	00 01 10 11	On target. 0.5 U.I. early. 1 U.I. late. 0.5 U.I. late.
[1:0]	*Sync_phase_SYNC1* Register to control the sampling of the external Sync input. Nominally the falling edge of the input is aligned with the falling edge of the reference clock. The margin is ±0.5 U.I. (Unit Interval).	00 01 10 11	On target. 0.5 U.I. early. 1 U.I. late. 0.5 U.I. late.

Address (hex): 7C

Register Name	*cnfg_sync_monitor*	Description	(R/W) Register to configure the external Sync input monitor. It also has a bit to control the phase offset automatic ramping feature.	Default Value	0010 1011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ph_offset_ramp	*Sync_monitor_limit*						

Bit No.	Description	Bit Value	Value Description
7	*ph_offset_ramp* Register bit to force an internal phase offset calibration routine. See also Reg. 71, *Cnfg_Phase_Offset*. The calibration routine puts the device into Holdover while it internally ramps the phase offset to zero, then resets all internal output and feedback dividers, then ramps the phase offset to the current value from Regs 70 and 71, and then turns Holdover off. The routine is transparent to the outside with no visible change in output phase offset.	0 1	Phase offset automatically ramped on from old value to new value when there is a change in Reg 70 or 71. Start phase offset internal phase offset calibration routine.
[6:4]	*Sync_monitor_limit* An alternative to allowing the external Sync input to synchronize the outputs, is to use the Sync monitor block to alarm when the external Sync input does not align with the output within a certain number of input clock cycles. This register defines the limit in UI of the selected SEC. If the external Sync does not occur within this limit, then Sync alarm will be raised, see Reg. 09 Bit 7.	000 001 010 011 100 101 110 111	Sync alarm raised beyond ±1 UI. Sync alarm raised beyond ±2 UI. Sync alarm raised beyond ±3 UI. Sync alarm raised beyond ±4 UI. Sync alarm raised beyond ±5 UI. Sync alarm raised beyond ±6 UI. Sync alarm raised beyond ±7 UI. Sync alarm raised beyond ±8 UI.
[3:0]	Not used.	-	-

Address (hex): 7D

Register Name	*cnfg_interrupt*	Description	(R/W) Register to configure interrupt output.	Default Value	0000 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					Interrupt *GPO_en*	Interrupt *tristate_en*	Interrupt *int_polarity*

Bit No.	Description	Bit Value	Value Description
[7:3]	Not used.	-	-

Address (hex): 7D (cont...)

Register Name	*cnfg_interrupt*	Description	(R/W) Register to configure interrupt output.	Default Value	0000 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					Interrupt *GPO_en*	Interrupt *tristate_en*	Interrupt *int_polarity*

Bit No.	Description	Bit Value	Value Description
2	Interrupt *GPO_en* (Interrupt General Purpose Output). If the interrupt output pin is not required, then setting this bit will allow the pin to be used as a general purpose output. The pin will be driven to the state of the polarity control bit, *int_polarity*.	0 1	Interrupt output pin used for interrupts. Interrupt output pin used for GPO purpose.
1	Interrupt *tristate_en* The interrupt can be configured to be either connected directly to a processor, or wired together with other sources.	0 1	Interrupt pin always driven when inactive. Interrupt pin only driven when active, high-impedance when inactive.
0	Interrupt *int_polarity* The interrupt pin can be configured to be active *High* or *Low*.	0 1	Active *Low* - pin driven *Low* to indicate active interrupt. Active *High* - pin driven *High* to indicate active interrupt.

Address (hex): 7E

Register Name	*cnfg_protection*	Description	(R/W) Protection register to protect against erroneous software writes.	Default Value	1000 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
protection_value							

Bit No.	Description	Bit Value	Value Description
[7:0]	*protection_value* This register can be used to ensure that the software writes a specific value to this register, before being able to modify any other register in the device. Three modes of protection are offered, (i) protected, (ii) fully unprotected, (iii) single unprotected. When protected, no other register in the device can be written to. When fully unprotected, any writeable register in the device can be written to. When single unprotected, only one register can be written before the device automatically re-protects itself. *Note...This register cannot be protected.*	0000 0000 – 1000 0100 1000 0101 1000 0110 1000 0111 – 1111 1111	Protected mode. Fully unprotected. Single unprotected. Protected mode.

JTAG

The JTAG connections on the ACS8525A allow a full boundary scan to be made. The JTAG implementation is fully compliant to IEEE 1149.1[4], with the following minor exceptions, and the user should refer to the standard for further information.

1. The output boundary scan cells do not capture data from the core, and so do not support INTEST. However this does not affect board testing.
2. In common with some other manufacturers, pin TRST is internally pulled *Low* to disable JTAG by default. The standard is to pull *High*. The polarity of TRST is as the standard: TRST *High* to enable JTAG boundary scan mode, TRST *Low* for normal operation.

The JTAG timing diagram is shown in Figure 12.

Over-voltage Protection

The ACS8525A may require Over-voltage Protection on input reference clock ports according to ITU recommendation K.41[10]. Semtech protection devices are recommended for this purpose (see separate Semtech data book).

ESD Protection

Suitable precautions should be taken to protect against electrostatic damage during handling and assembly. This device incorporates ESD protection structures that protect the device against ESD damage at ESD input levels up to at least +/2kV using the Human Body Model (HBD) MIL-STD-883D Method 3015.7, for all pins.

Latchup Protection

This device is protected against latchup for input current pulses of magnitude up to at least ±100 mA to JEDEC Standard No. 78 August 1997.

Figure 12 JTAG Timing

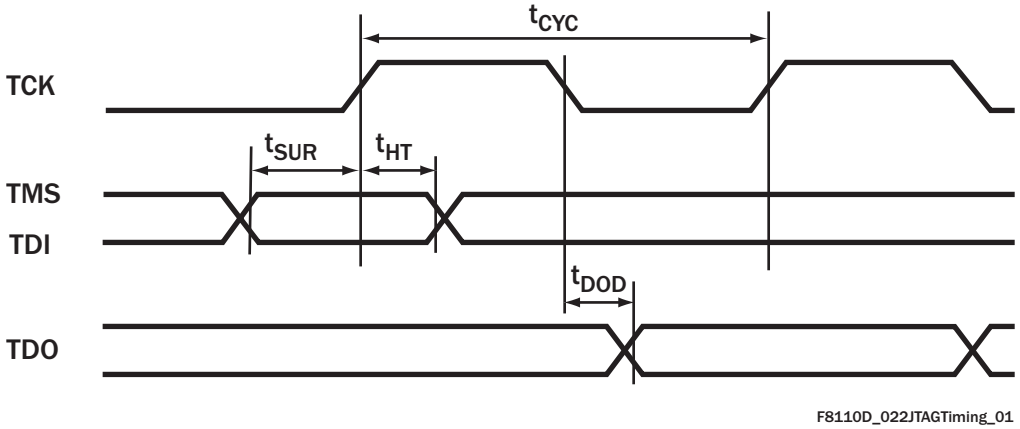


Table 16 JTAG Timing (for use with Figure 12)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Cycle Time	t_{CYC}	50	-	-	ns
TMS/TDI to TCK rising edge time	t_{SUR}	3	-	-	ns
TCK rising to TMS/TDI hold time	t_{HT}	23	-	-	ns
TCK falling to TDO valid	t_{DOD}	-	-	5	ns

Maximum Ratings

Important Note: The Absolute Maximum Ratings, Table 17, are stress ratings only, and functional operation of the device at conditions other than those indicated in the Operating Conditions sections of this specification are not implied. Exposure to the absolute maximum ratings for an extended period may reduce the reliability or useful lifetime of the product.

Table 17 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage VDD1, VDD2, VDD3, VDD4, VDD5, VDD6, VDD7, VD1+, VD2+,VD3+, VA1+, VA2+, VA3+, VDD_DIFF	V_{DD}	-0.5	3.6	V
Input Voltage (non-supply pins)	V_{IN}	-	3.6	V
Output Voltage (non-supply pins)	V_{OUT}	-	3.6	V
Ambient Operating Temperature Range	T_A	0	+70	^oC
Storage Temperature	T_{STOR}	-50	+150	^oC

Operating Conditions

Table 18 Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supply (DC Voltage) VDD1, VDD2, VDD3, VDD4, VDD5, VDD6, VDD7, VD1+, VD2+,VD3+, VA1+, VA2+, VA3+, VDD_DIF	V_{DD}	3.135	3.3	3.465	V
Ambient Temperature Range	T_A	0	-	+70	^oC
Supply Current (Typical - one 19 MHz output)	I_{DD}		110	200	mA
Total Power Dissipation	P_{TOT}		360	720	mW

DC Characteristics

Table 19 DC Characteristics: TTL Input Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Input Current	I_{IN}	-	-	10	µA

Table 20 DC Characteristics: TTL Input Port with Internal Pull-up

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-up Resistor	PU	25	-	95	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 21 DC Characteristics: TTL Input Port with Internal Pull-down

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{IN} *High*	V_{IH}	2	-	-	V
V_{IN} *Low*	V_{IL}	-	-	0.8	V
Pull-down Resistor (except TCK input)	PD	25	-	95	kΩ
Pull-down Resistor (TCK input only)	PD	12.5	-	47.5	kΩ
Input Current	I_{IN}	-	-	120	µA

Table 22 DC Characteristics: TTL Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{OUT} *Low* (I_{OL} = 4mA)	V_{OL}	0	-	0.4	V
V_{OUT} *High* (I_{OL} = 4mA)	V_{OH}	2.4	-	-	V
Drive Current	ID	-	-	4	mA

Table 23 DC Characteristics: PECL Input/Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
PECL Input *Low* Voltage Differential Inputs (Note ii)	V_{ILPECL}	V_{DD}-2.5	-	V_{DD}-0.5	V
PECL Input *High* Voltage Differential Inputs (Note ii)	V_{IHPECL}	V_{DD}-2.4	-	V_{DD}-0.4	V
Input Differential Voltage	V_{IDPECL}	0.1	-	1.4	V

Table 23 DC Characteristics: PECL Input/Output Port (cont...)

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
PECL Input *Low* Voltage Single-ended Input (Note iii)	V_{ILPECL_S}	V_{DD}-2.4	-	V_{DD}-1.5	V
PECL Input *High* Voltage Single-ended Input (Note iii)	V_{ILPECL_S}	V_{DD}-1.3	-	V_{DD}-0.5	V
Input *High* Current Input Differential Voltage V_{ID} = 1.4V	I_{IHPECL}	-10	-	+10	µA
Input *Low* Current Input Differential Voltage V_{ID} = 1.4V	I_{ILPECL}	-10	-	+10	µA
PECL Output *Low* Voltage (Note iv)	V_{OLPECL}	V_{DD}-2.10	-	V_{DD}-1.62	V
PECL Output *High* Voltage (Note iv)	V_{OHPECL}	V_{DD}-1.25	-	V_{DD}-0.88	V
PECL Output Differential Voltage (Note iv)	V_{ODPECL}	580	-	900	mV

Notes: (i) Unused differential input ports should be left floating and set in LVDS mode, or the positive and negative inputs tied to V_{DD} and GND respectively.

(ii) Assuming a differential input voltage of at least 100 mV.

(iii) Unused differential input terminated to V_{DD} - 1.4 V.

(iv) With 50 Ω load on each pin to V_{DD} - 2 V, i.e. 82 Ω to GND and 130 Ω to V_{DD}.

Figure 13 Recommended Line Termination for PECL Input/Output Ports

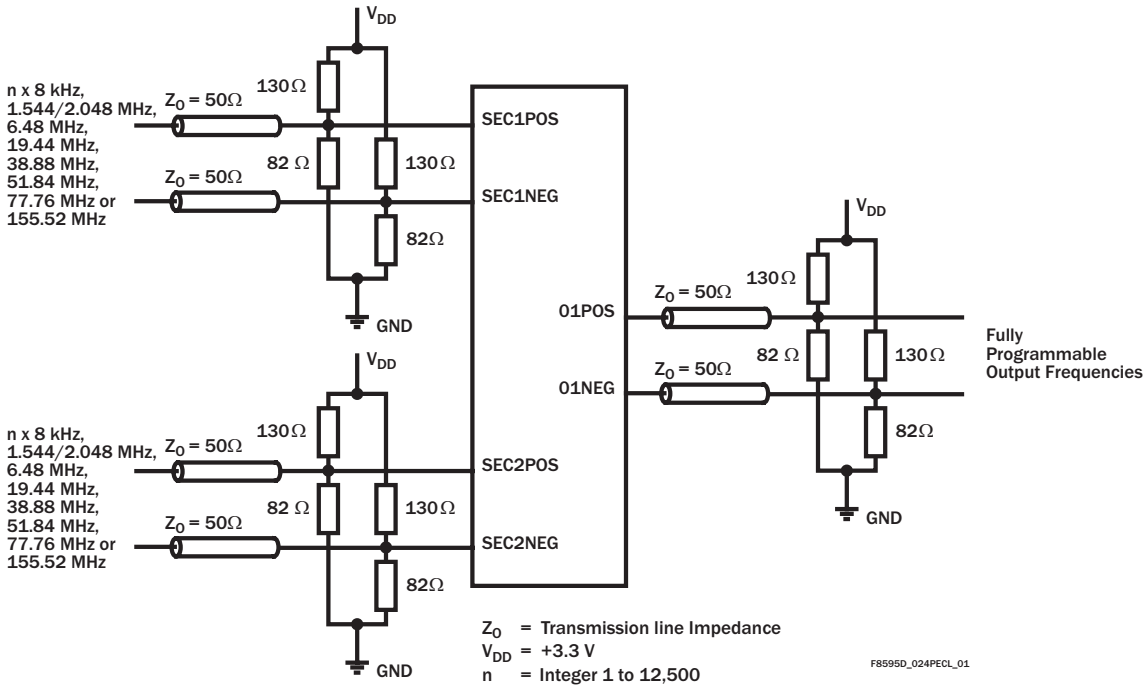


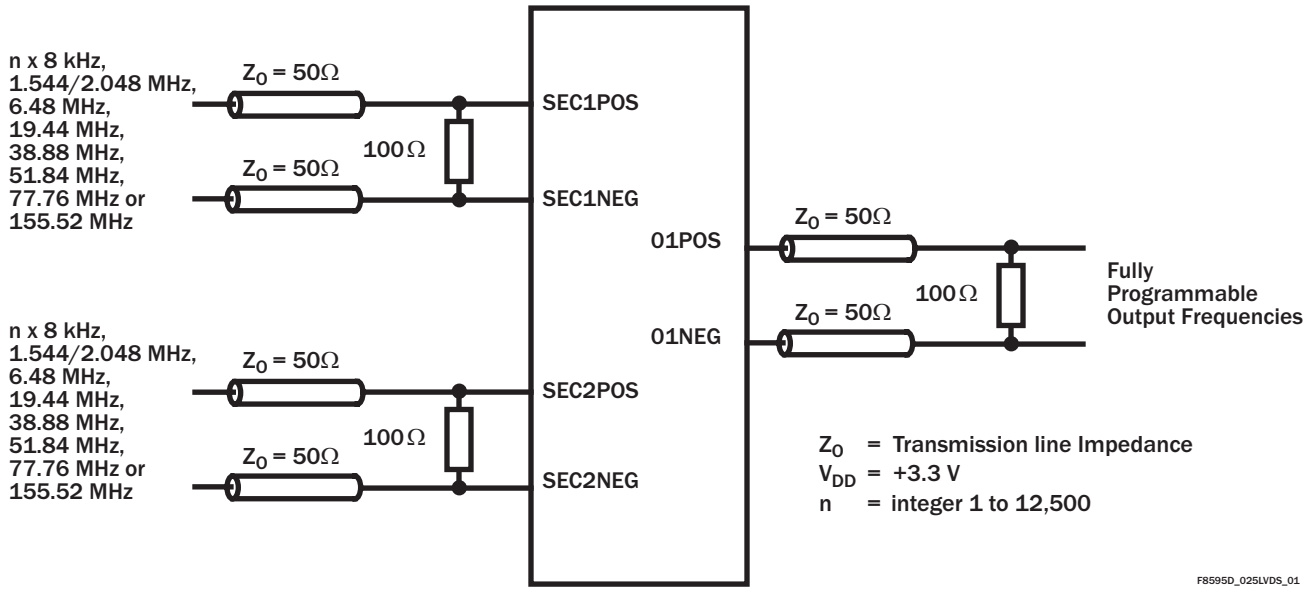
Table 24 DC Characteristics: LVDS Input/Output Port

Across all operating conditions, unless otherwise stated

Parameter	Symbol	Minimum	Typical	Maximum	Units
LVDS Input Voltage Range Differential Input Voltage = 100 mV	V_{VRLVDS}	0	-	2.40	V
LVDS Differential Input Threshold	V_{DITH}	-100	-	+100	mV
LVDS Input Differential Voltage	$V_{IDLVTSDS}$	0.1	-	1.4	V
LVDS Input Termination Resistance Must be placed externally across the LVDS ± input pins of ACS8525A. Resistor should be 100 Ω with 5% tolerance	R_{TERM}	95	100	105	Ω
LVDS Output *High* Voltage (Note (i))	V_{OHLVDS}	-	-	1.585	V
LVDS Output *Low* Voltage (Note (i))	V_{OLLVDS}	0.885	-	-	V
LVDS Differential Output Voltage	V_{ODLVDS}	250	-	450	mV
LVDS Change in Magnitude of Differential Output Voltage for complementary States (Note (i))	$V_{DOSLVDS}$	-	-	25	mV
LVDS Output Offset Voltage Temperature = 25°C (Note (i))	V_{OSLVDS}	1.125	-	1.275	V

Notes: (i) With 100 Ω load between the differential outputs.

Figure 14 Recommended Line Termination for LVDS Input/Output Ports



Jitter Performance

Output jitter generation measured over 60 second interval, UI p-p max measured using C-MAC E2747 12.800 MHz TCXO on ICT Flexacom tester.

Table 25 Output Jitter Generation at 35 Hz bandwidth and 8 kHz Input

Test Definition		Jitter Spec	ACS8525A Jitter
Specification	**Filter**	**UI**	**UI (TYP)**
G813[8] for 155 MHz o/p option 1	65 kHz - 1.3 MHz	0.1 p-p	0.073 p-p
G813[8] & G812[7] for 2.048 MHz option 1	20 Hz - 100 kHz	0.05 p-p	0.012 p-p
G813[8] for 155 MHz o/p option 2	12 kHz - 1.3 MHz	0.1 p-p	0.069 p-p
G812[7] for 1.544 MHz o/p	10 Hz - 40 kHz	0.05 p-p	0.011 p-p
G812[7] for 155 MHz electrical	500 Hz - 1.3 MHz	0.5 p-p	0.083 p-p
G812[7] for 155 MHz electrical	65 kHz - 1.3 MHz	0.075 p-p	0.073p-p
ETS-300-462-3[2] for 2.048 MHz SEC o/p	20 Hz - 100 kHz	0.5 p-p	0.012 p-p
ETS-300-462-3[2] for 2.048 MHz SEC o/p	49 Hz - 100 kHz	0.2 p-p	0.012 p-p
ETS-300-462-3[2] for 2.048 MHz SSU o/p	20 Hz - 100 kHz	0.05 p-p	0.012 p-p
ETS-300-462-5[3] for 155 MHz o/p	500 Hz - 1.3 MHz	0.5 p-p	0.083 p-p
ETS-300-462-5[3] for 155 MHz o/p	65 kHz - 1.3 MHz	0.1 p-p	0.073 p-p
GR-253-CORE[11] net i/f, 51.84 MHz o/p	100 Hz - 0.4 MHz	1.5 p-p	0.038 p-p
GR-253-CORE[11] net i/f, 51.84 MHz o/p	20 kHz to 0.4 MHz	0.15 p-p	0.019 p-p
GR-253-CORE[11] net i/f, 155 MHz o/p	500 Hz - 1.3 MHz	1.5 p-p	0.083 p-p
GR-253-CORE[11] net i/f, 155 MHz o/p	65 kHz - 1.3 MHz	0.15 p-p	0.073 p-p
GR-253-CORE[11] cat II elect i/f, 155 MHz	12 kHz - 1.3 MHz	0.1 p-p	0.069 p-p
		0.01 rms	0.009 rms
GR-253-CORE[11] cat II elect i/f, 51.84 MHz	12 kHz - 400 kHz	0.1 p-p	0.008 p-p
		0.01 rms	0.004 rms
GR-253-CORE[11] DS1 i/f, 1.544 MHz	10 Hz - 40 kHz	0.1 p-p	0.001 p-p
		0.01 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	10 Hz - 8 kHz	0.02 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	8 Hz - 40 kHz	0.025 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	10 Hz - 40 kHz	0.025 rms	<0.001 rms
AT&T 62411[1] for 1.544 MHz	Broadband	0.05 rms	<0.001 rms
G-742[6] for 2.048 MHz	DC - 100 kHz	0.25 rms	0.012 rms
G-742[6] for 2.048 MHz	18 kHz - 100 kHz	0.05 p-p	0.012 p-p
G-736[5] for 2.048 MHz	20 Hz - 100 kHz	0.05 p-p	0.012 p-p

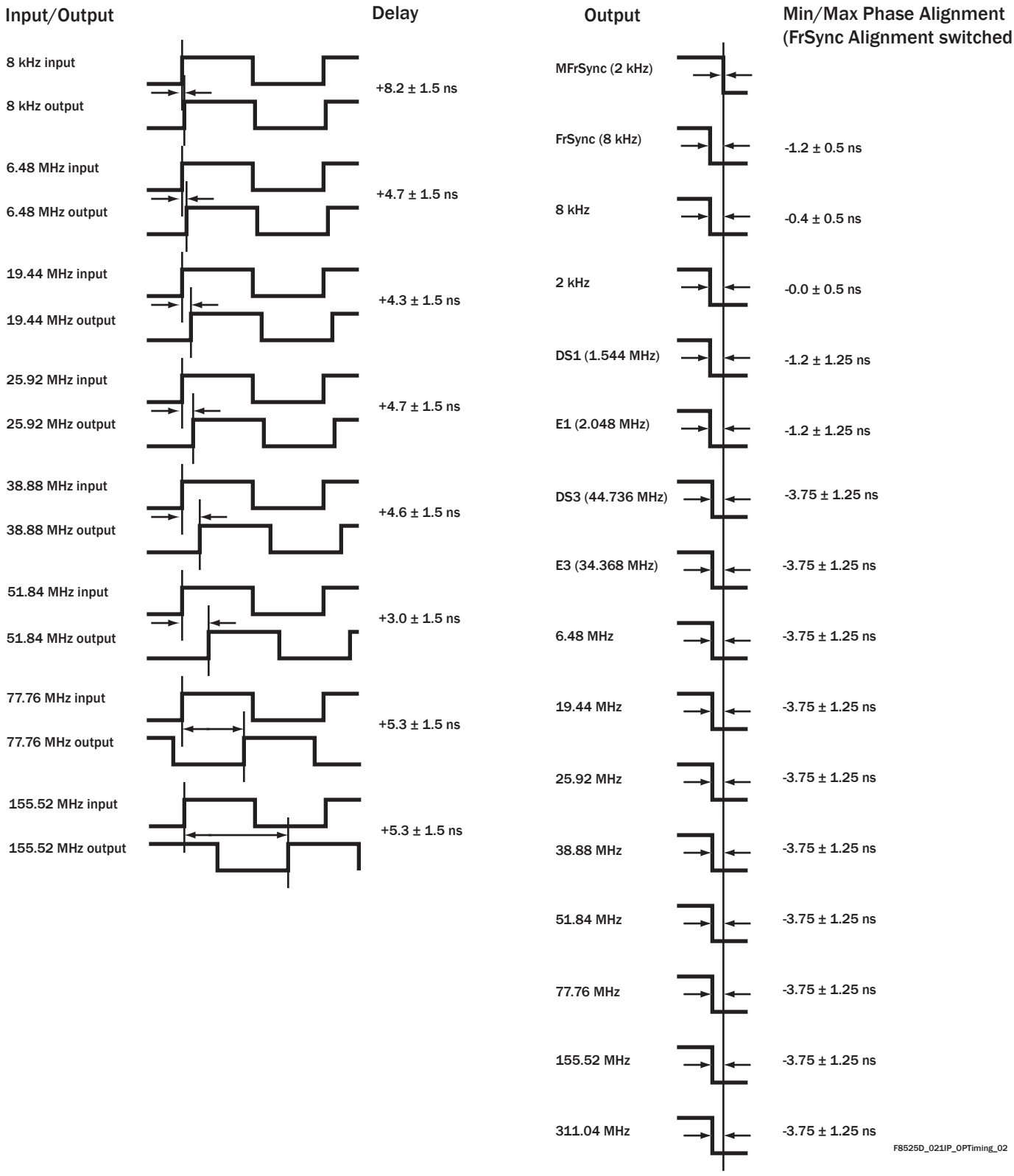
Table 25 Output Jitter Generation at 35 Hz bandwidth and 8 kHz Input (cont...)

Test Definition		Jitter Spec	ACS8525A Jitter
Specification	**Filter**	**UI**	**UI (TYP)**
GR-499-CORE[12] & G824[9] for 1.544 MHz	10 Hz - 40kHz	5.0 p-p	0.001 p-p
GR-499-CORE[12] & G824[9] for 1.544 MHz	8 kHz - 40kHz	0.1 p-p	0.001 p-p
GR-1244-CORE[13] for 1.544 MHz	> 10 Hz	0.05 p-p	0.001 p-p

Note...This table is only for comparing the ACS8525A output jitter performance against values and quoted in various specifications for given conditions. It should not be used to infer compliance to any other aspects of these specifications.

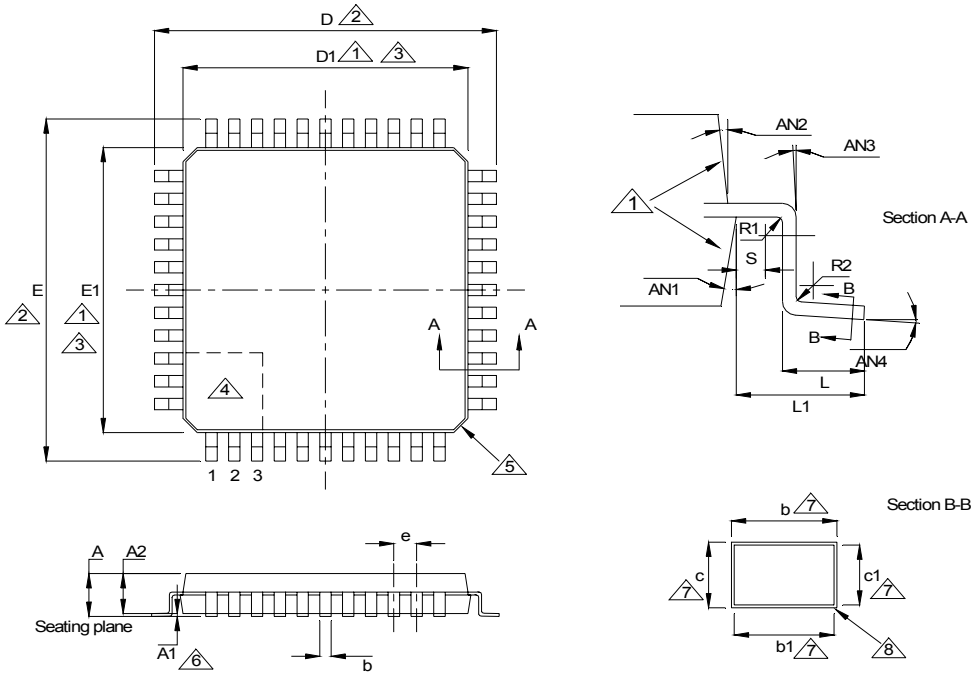
Input/Output Timing

Figure 15 Input/Output Timing with Phase Build-out Off (Typical Conditions)



Package Information

Figure 16 LQFP Package



Notes

1. The top package body may be smaller than the bottom package body by as much as 0.15 mm.
2. To be determined at seating plane.
3. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Details of pin 1 identifier are optional but will be located within the zone indicated.
5. Exact shape of corners can vary.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
8. Shows plating.

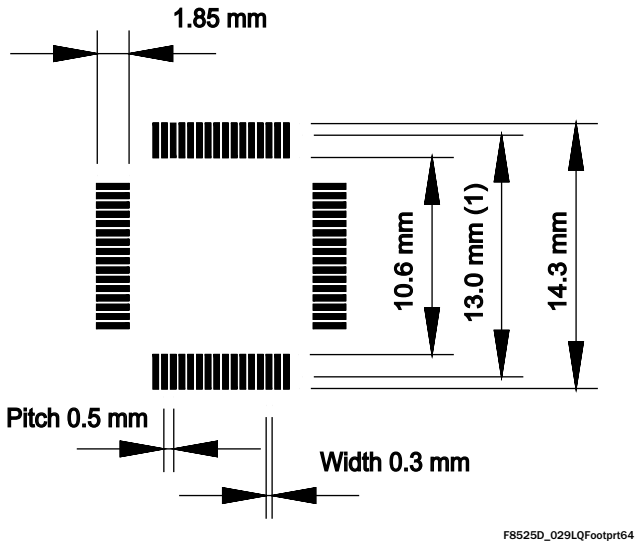
Table 26 64 Pin LQFP Package Dimension Data (for use with Figure 16)

Dimensions in mm	D/E	D1/ E1	A	A1	A2	e	AN1	AN2	AN3	AN4	R1	R2	L	L1	S	b	b1	c	c1
Min.	-	-	1.40	0.05	1.35	-	11°	11°	0°	0°	0.08	0.08	0.45	-	0.20	0.17	0.17	0.09	0.09
Nom.	12.00	10.00	1.50	0.10	1.40	0.50	12°	12°	-	3.5°	-	-	0.60	1.00 (ref)	-	0.22	0.20	-	-
Max.	-	-	1.60	0.15	1.45	-	13°	13°	-	7°	-	0.20	0.75	-	-	0.27	0.23	0.20	0.16

Thermal Conditions

The device is rated for full temperature range when this package is used with a 4 layer or more PCB. Copper coverage must exceed 50%. All pins must be soldered to the PCB. Maximum operating temperature must be reduced when the device is used with a PCB with less than these requirements.

Figure 17 Typical 64-Pin LQFP Package Landing Pattern



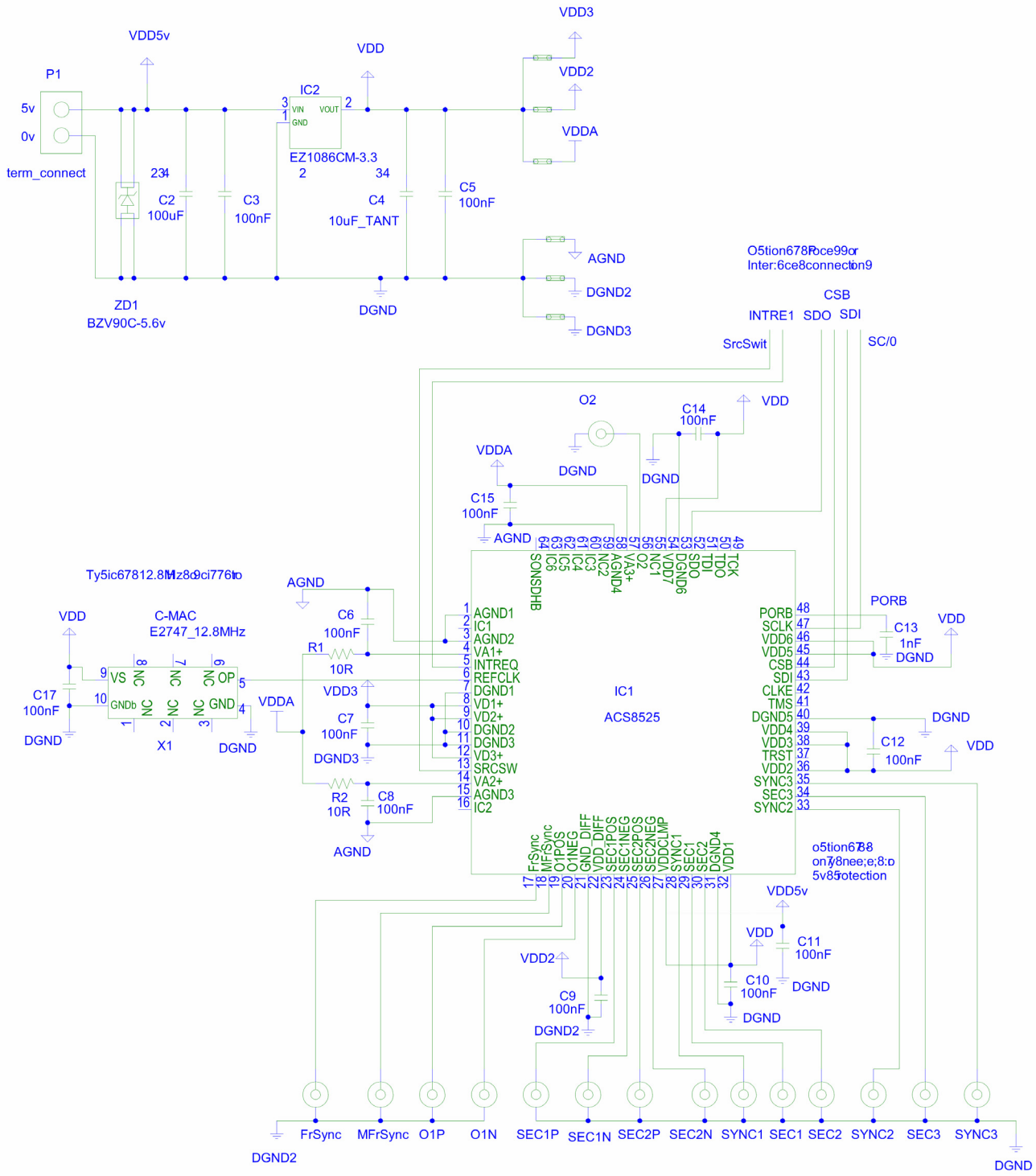
Notes: (i) Solderable to this limit.

(ii) Square package - dimensions apply in both X and Y directions.

(iii) Typical example. The user is responsible for ensuring compatibility with PCB manufacturing process, etc.

Application Information

Figure 18 Simplified Application Schematic



Abbreviations

APLL	Analogue Phase Locked Loop
BITS	Building Integrated Timing Supply
DFS	Digital Frequency Synthesis
DPLL	Digital Phase Locked Loop
DS1	1544 kbit/s interface rate
DTO	Discrete Time Oscillator
E1	2048 kbit/s interface rate
I/O	Input - Output
LQFP	Low profile Quad Flat Pack
LVDS	Low Voltage Differential Signal
MTIE	Maximum Time Interval Error
PBO	Phase Build-out
PD2	Phase Detector 2
PECL	Positive Emitter Coupled Logic
PFD	Phase and Frequency Detector
PLL	Phase Locked Loop
POR	Power-On Reset
ppb	parts per billion
ppm	parts per million
p-p	peak-to-peak
R/W	Read/Write
RO	Read Only
RoHS	Restrictive Use of Certain Hazardous Substances (directive)
rms	root-mean-square
SDH	Synchronous Digital Hierarchy
SEC	SDH/SONET Equipment Clock
SETS	Synchronous Equipment Timing source
SONET	Synchronous Optical Network
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
TDEV	Time Deviation
TCXO	Temperature Compensated Crystal Oscillator
UI	Unit Interval
WEEE	Waste Electrical and Electronic Equipment (directive)
XO	Crystal Oscillator

References

[1] AT & T 62411 (12/1990)
ACCUNET® T1.5 Service description and Interface Specification

[2] ETSI ETS 300 462-3, (01/1997)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3: The control of jitter and wander within synchronization networks

[3] ETSI ETS 300 462-5 (09/1996)
Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment

[4] IEEE 1149.1 (1990)
Standard Test Access Port and Boundary-Scan Architecture

[5] ITU-T G.736 (03/1993)
Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s

[6] ITU-T G.742 (1988)
Second order digital multiplex equipment operating at 8448 kbit/s, and using positive justification

[7] ITU-T G.812 (06/1998)
Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

[8] ITU-T G.813 (08/1996)
Timing characteristics of SDH equipment slave clocks (SEC)

[9] ITU-T G.824 (03/2000)
The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

[10] ITU-T K.41 (05/1998)
Resistibility of internal interfaces of telecommunication centres to surge overvoltages

[11] Telcordia GR-253-CORE, Issue 3 (09/ 2000)
Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria

[12] Telcordia GR-499-CORE, Issue 2 (12/1998)
Transport Systems Generic Requirements (TSGR) Common requirements

[13] Telcordia GR-1244-CORE, Issue 2 (12/2000)
Clocks for the Synchronized Network: Common Generic Criteria

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Notes

Revision Status/History

The Revision Status of the datasheet, as shown in the center of the datasheet header bar, may be TARGET, PRELIMINARY, or FINAL, and refers to the status of the Device (not the datasheet) within the design cycle. TARGET status is used when the design is being realized but is not yet physically available, and the datasheet content reflects the intention of the design. The datasheet is raised to PRELIMINARY status when initial prototype devices are physically available, and the datasheet content more accurately represents the realization of the design.

The datasheet is only raised to FINAL status after the device has been fully characterized, and the datasheet content updated with measured, rather than simulated parameter values.

This is a FINAL release (Revision 1.00) of the ACS8525A datasheet. Changes made for this document revision are given in Table 27, together with a summary of previous revisions. For specific changes between earlier revisions, refer (where available) to those earlier revisions. Always use the current version of the datasheet.

Table 27 Revision History

Revision	Reference	Description of Changes
1.00/September 2007	Page 99	Table 17 & 18 updated to revised specification.

Notes

Ordering Information

Table 28 Parts List

Part Number	Description
ACS8525A	Line Card Protection Switch for SONET/SDH Systems.
ACS8525AT	Lead (Pb)-free packaged version of ACS8525A; RoHS and WEEE compliant.

Disclaimers

Life support- This product is not designed or intended for use in life support equipment, devices or systems, or other critical applications, and is not authorized or warranted for such use.

Right to change- Changes may be made to this product without notice. Customers are advised to obtain the latest version of the relevant information before placing orders.

Compliance to relevant standards- Operation of this device is subject to the User's implementation and design practices. It is the responsibility of the User to ensure equipment using this device is compliant to any relevant standards.

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