<u>TOSHIBA</u>

TENTATIVE

TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

T C D 1 5 0 1 C

The TCD1501C which includes sample-and-hold circuit is a high sensitive and low dark current 5000 elements CCD image sensor.

The sensor is designed for facsimile, imagescanner and OCR.

The device contains a row of 5000 elements photodiodes which provide a 16 lines / mm (400DPl) across a A3 size paper. The device is operated by 5V (pulse), and 12V power supply.

FEATURES

- Number of Image Sensing Elements : 5000 elements
- Image Sensing Element Size

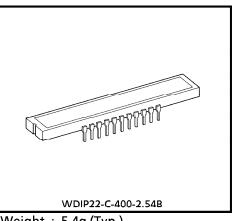
: $7\mu m$ by $7\mu m$ on $7\mu m$ centers

- Photo Sensing Region : High sensitive and low voltage dark signal pn photodiode
- Clock : 2 Phase (5V)
- Internal Circuit : S/H circuit
- Package : 22pin DIP

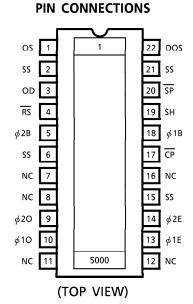
MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	Vø		v
Shift Pulse Voltage	V _{SH}		
Reset Pulse Voltage	VRS	-0.3~8	
Clamp Pulse Voltage	VCP		
Sample and Hold Pulse Voltage	VSP		
Power Supply Voltage	V _{OD}	-0.3~15	
Operating Temperature	T _{opr}	- 25~60	°C
Storage Temperature	T _{stg}	- 40~100	°C

(Note 1) All voltage are with respect to SS terminals (Ground).



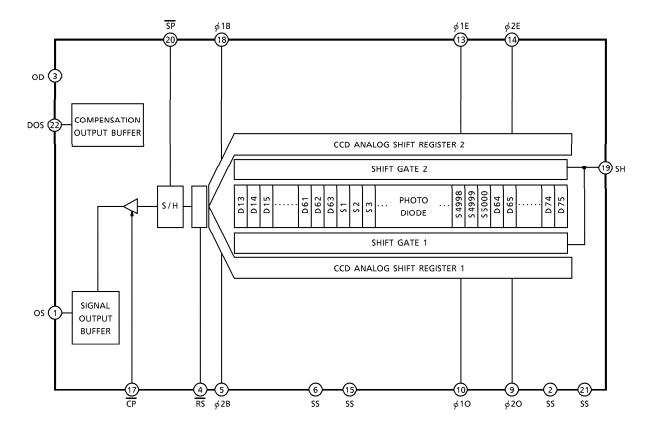
Weight : 5.4g (Typ.)



961001EBA2

TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

CIRCUIT DIAGRAM



PIN NAME

∳1E, O	Clock (Phase 1)
φ2Ε, Ο	Clock (Phase 2)
φIB	Final Stage Clock (Phase 1)
φ2B	Final Stage Clock (Phase 2)
SH	Shift Gate
RS	Reset Gate
SP	Sample and Hold Gate
CP	Clamp Gate
OS	Signal Output
DOS	Compensation Output
OD	Power
SS	Ground
NC	Non Connection

961001EBA2'

The products described in this document are subject to foreign exchange and foreign trade control laws. The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others. The information contained herein is subject to change without notice. 8 •

TOSHIBA

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{OD} = 12V, V ϕ = V_{RS} = V_{SP} = V_{SP} = V_{CP} = 5V, f ϕ = 0.5MHz, f_{RS} = 1MHz, t_{INT} (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP, LOAD RESISTANCE = 100k Ω)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R	10.4	13	15.6	V / Ix•s	
	PRNU	—	_	10	%	(Note 2)
Photo Response Non Uniformity	PRNU (3)	_	6	10	mV	(Note 9)
Register Imbalance	RI	_		3	%	(Note 3)
Saturation Output Voltage	VSAT	2	3	_	V	(Note 4)
Saturation Exposure	SE	0.13	0.23		lx∙s	(Note 5)
Dark Signal Voltage	VDRK	_	1	2	mV	(Note 6)
Dark Signal Non Uniformity	DSNU	_	2	3	mV	(Note 6)
DC Power Dissipation	PD	—	240	325	mW	
Total Transfer Efficiency	TTE	92	_		%	
Output Impedance	Zo		0.5	1	kΩ	
Dynamic Range	DR	_	3000		_	(Note 7)
DC Signal Output Voltage	Vos	4	5	6.5	V	(Note 8)
DC Compensation Output Voltage	V _{DOS}	4	5	6.5	V	(Note 8)
DC Differential Error Voltage	VOS-VDOS	—	_	400	mV	

(Note 2) Measured at 50% of SE (Typ.)

Definition of PRNU : PRNU =
$$\frac{\Delta \chi}{\overline{\chi}} \times 100$$
 (%)

Where \overline{x} is average of total signal output and Δx is the maximum deviation from \overline{x} under uniform illumination.

(Note 3) Measured at 50% of SE (Typ.) RI is defined as follows:

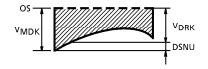
$$RI = \frac{\frac{4999}{\sum |xn - xn + 1|}}{\frac{4999 \times \overline{x}}{2}} \times 100 \,(\%)$$

Where xn and xn + 1 are signal output of each pixel. \overline{x} is average of total signal output.

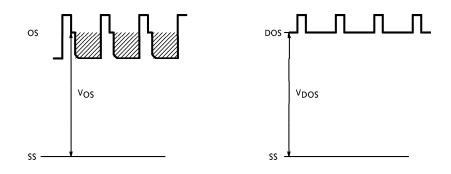
(Note 4) V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

TOSHIBA

- (Note 5) Definition of SE : SE = $\frac{V_{SAT}}{R}$ (I x·s)
- (Note 6) V_{DRK} is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



- (Note 7) Definition of DR : DR = $\frac{V_{SAT}}{V_{DRK}}$ V_{DRK} is proportional to t_{INT} (Integration Time). So the shorter t_{INT} condition makes wider DR values.
- (Note 8) DC signal output voltage and DC compensation output voltage are defined as follows:



(Note 9) PRUN (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.).

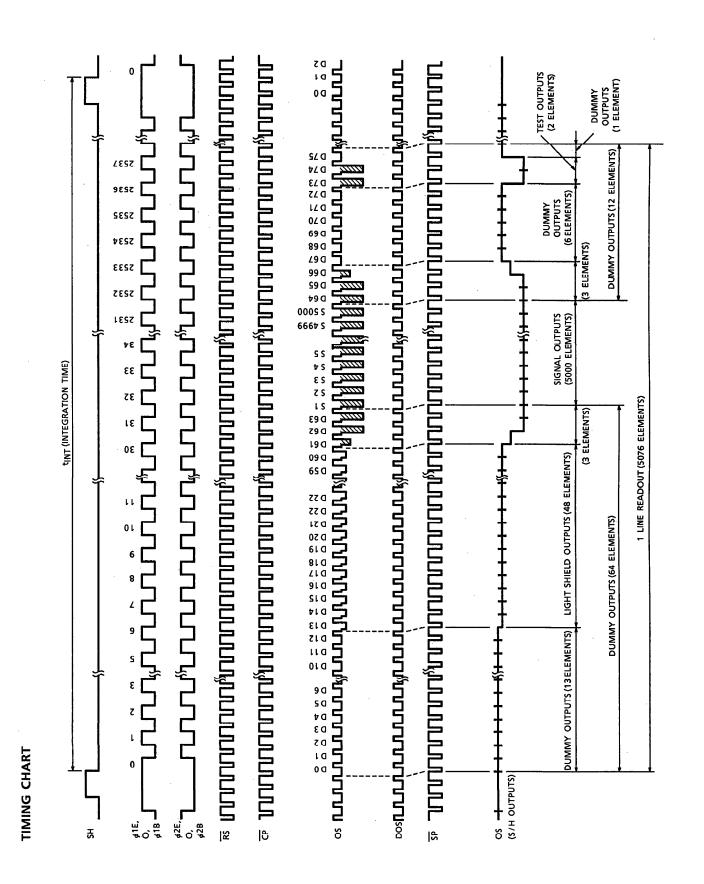
OPERATING CONDITION

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT	
Clock Pulse Voltage	"H" Level	V¢1E, O	4.5	5	5.5	V	
	"L" Level	V ∳2E, O	0	_	0.5	v	
Final Stage Clock Voltage	"H" Level	V∳1B	4.5	5	5.5	v	
	"L" Level	V∳2B	0	_	0.5	v	
Shift Pulse Voltage	"H" Level	V _{SH}	4.5	5	5.5	V	
	"L" Level		0	_	0.5		
Devel D. Jac Malance	"H" Level	V _{RS}		4.5	5	5.5	v
Reset Pulse Voltage	"L" Level			0	_	0.5	v
Clamp Bulsa Valtaga	"H" Level	V _{CP}	4.5	5	5.5	V	
Clamp Pulse Voltage	"L" Level		0	—	0.5		
Sample and Hold Pulse Voltage *	"H" Level	V _{SP}	4.5	5	5.5	V	
	"L" Level		0	_	0.5	V	
Power Supply Voltage		V _{OD}	11.4	12.0	13.0	V	

* Supply "L" level to SP terminal when sample-and-hold circuitry is not used.

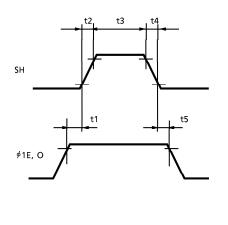
CLOCK CHARACTERISTICS (Ta = 25°C)

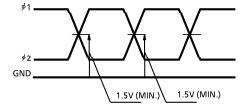
	1	1	1		
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	fø	—	0.5	6.0	MHz
Reset Pulse Frequency	fRS	_	1.0	12.0	MHz
Sample and Hold Pulse Frequency	f <u>SP</u>	—	1.0	2.0	MHz
Clark Canaditanaa	CφE	—	350	450	рF
Clock Capacitance	CφO	—	350	450	
Final Stage Clock Capacitance	C∳B	_	10	20	рF
Shift Gate Capacitance	C _{SH}	—	10	20	рF
Reset Gate Capacitance	CRS	_	10	20	pF
Clamp Gate Capacitance	CCP	_	10	20	pF
Sample and Hold Gate Capacitance	CSP	_	10	20	рF



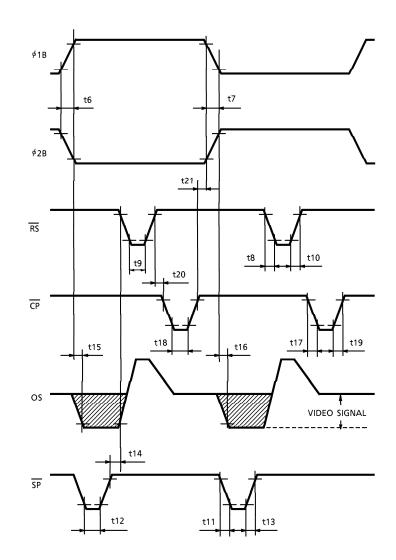
TIMING REQUIREMENTS

SH, ø1 TIMING





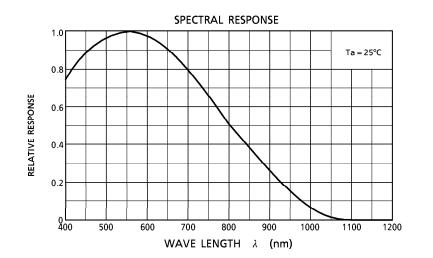
 ϕ 1, ϕ 2, \overline{RS} , \overline{CP} , OS, \overline{SP} TIMING

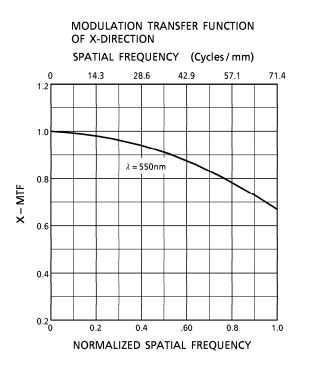


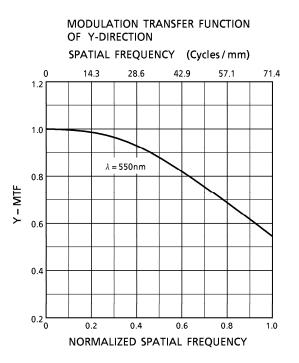
CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 10)	MAX.	UNIT
Pulse Timing of SH and ϕ 10, E	t1, t5	100	300	—	ns
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	500	1000	_	ns
φ1, φ2 Pulse Rise Time, Fall Time	t6, t7	0	100	_	ns
RS Pulse Rise Time, Fall Time	t8, t10	0	20	_	ns
RS Pulse Width	t9	20	250		ns
SP Pulse Rise Time, Fall Time	t11, t13	0	20	_	ns
SP Pulse Width	t12	20	—	_	ns
Pulse Timing of SP and RS	t14	0	50	_	ns
Video Data Delay Time (Note 11)	t15, t16	_	30	_	ns
CP Pulse Rise Time, Fall Time	t17, t19	0	20	_	ns
CP Pulse Width	t18	20	—	—	ns
Pulse Timing of RS and CP	t20	0		_	ns
Pulse Timing of ϕ 1B, ϕ 2B and \overline{CP}	t21	0	—	—	ns

(Note 10) TYP. is the case of f_{RS} = 1.0MHz (Note 11) Load Resistance is $100k\Omega$

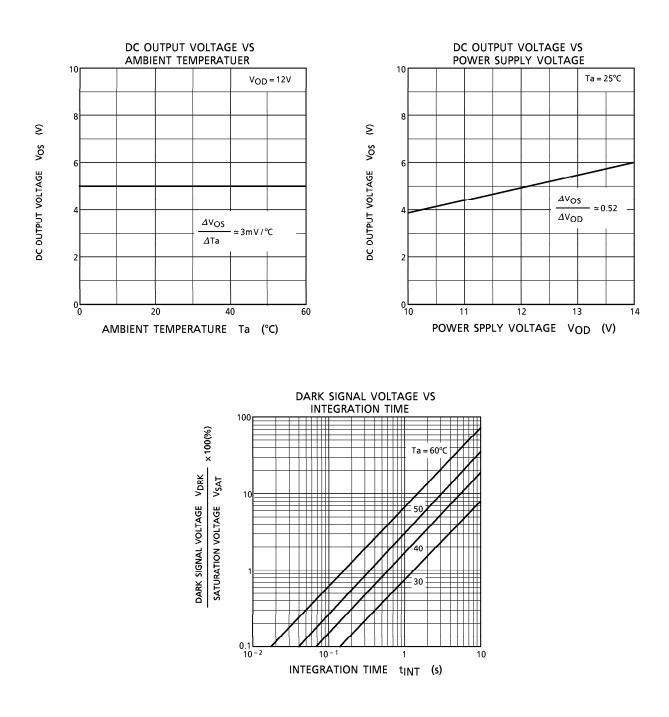
TYPICAL PERFORMANCE CURVES







TYPICAL PERFORMANCE CURVES (Cont'd)



CAUTION

1. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂.

Care should be taken to avoid mechanical or thermal shock because the glass window iseasily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

Unit in mm

PACKAGE OUTLINE WDIP22-C-400-2.54B (A)

0.7±0.1^(Note 3) 11.5±0.8^(Note 1) 35(7 µ m×5000) 22 12 10.03±0.3 0.25 ± 0.1 10.4±0.3 5.02 ± 0.3 1 11 1.7 ± 0.3 (Note 2) 53.6±0.5 3.22±0.5 4.19±0.5 3.0±0.3 0.67MIN 0.51±0.15 14.1TYP 2.54 1.02±0.1

- (Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
- (Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
- (Note 3) GLASS THICKNES (n = 1.5)

Weight : 5.4g (Typ.)