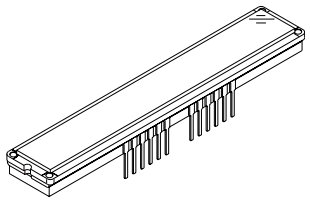
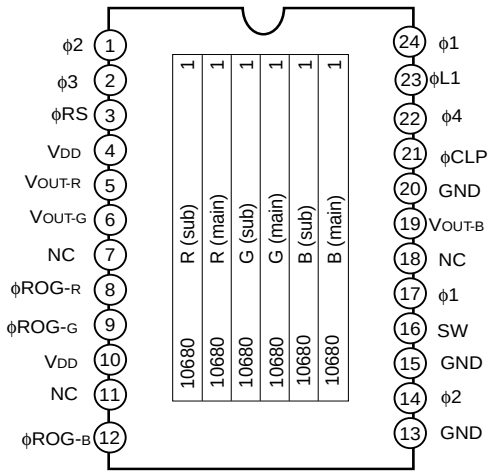
SONY

ILX585K

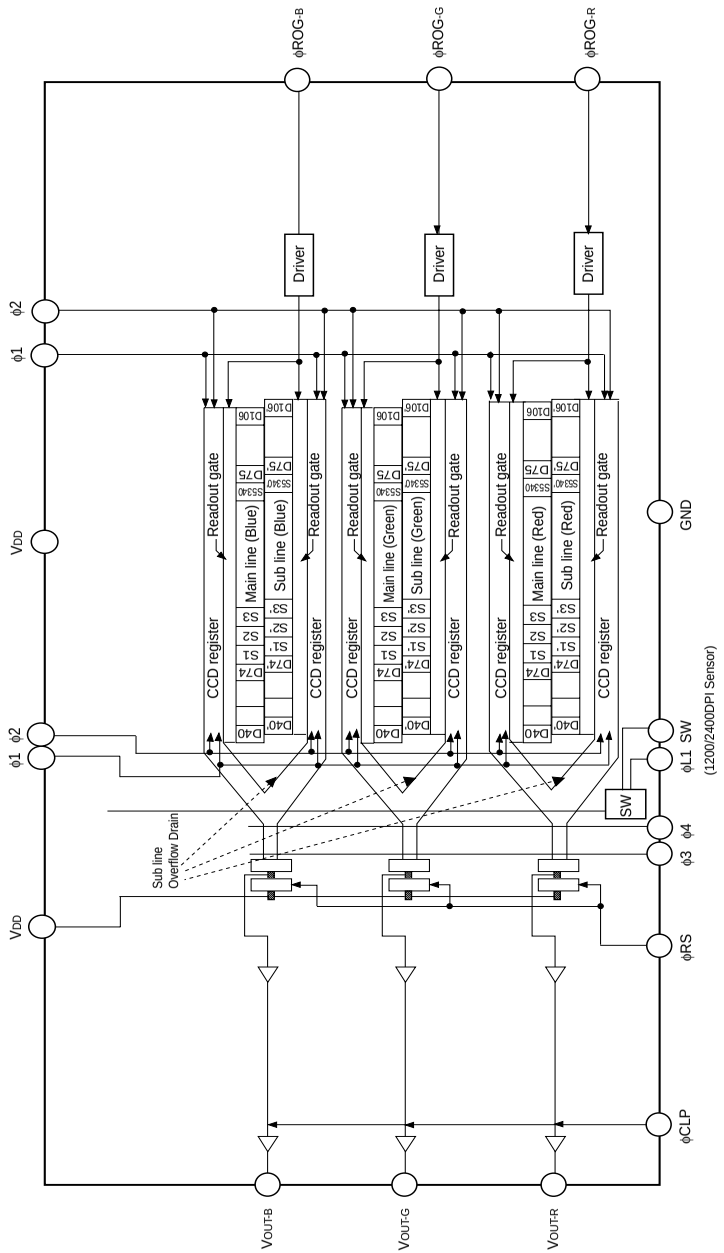
24 pin DIP (Plastic)





02.07.30

Block Diagram



Pin Description

Recommended Supply Voltage

Clock Characteristics

Clock Frequency

2400 DPI Staggered

4;	3	fD	1	12(	5
ϕ1 ϕ ϕ1	−ϕ1− ϕ− ϕ1	7	1	e	A
ϕ ϕ ϕ	−ϕ− ϕ− ϕ	7	1	1	A

Input Clock Pulse Voltage Condition

4;		fD	1	12(	5
ϕ1 ϕ ϕ ϕ	3	1	1	1	
ϕ1 ϕ	3			1	

SW mode

	1

Electrooptical Characteristics (Note 1, 2)

(Ta=25c,VDD=12V, ffRS=1MHz, Input clock=5Vp-p, Light source=3200K, IR cut filter CM500S (t = 1.0mm)

	σ				4	

Notes:

1. In accordance with the given electrooptical characteristics, the black level is defined as the average value of D40, D41 to D73.
2. For the sensitivity test light is applied with a uniform intensity of illumination.
3. PRNU us defubed as indicated below. Ray iincidence conditions are the same as for Note 2.
   Vout=500mV(typ.)

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100 \ [\%]$$

4. Use below the minimum value of the saturation output voltage.

5. Saturation exposure is defined as follows.

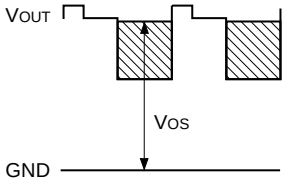
   $SE = \frac{\quad}{\quad}$

   Where R indicates R_R, R_G, R_B and SE indicates SE_R, SE_G, SE_B.

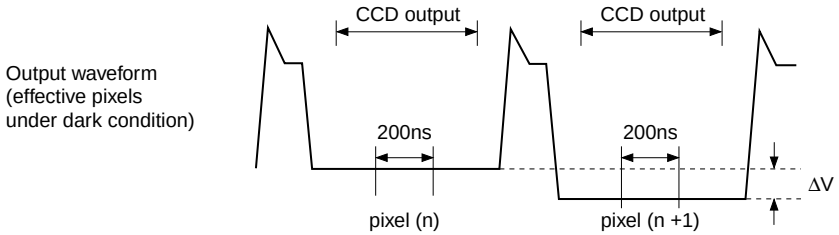
6. Optical signal accumulated time τ_{int} stands at 4ms.

7. Supply current means the total current of this device.

8. Vos is defined as indicated bellow.
   V_{OUT} indicates V_{OUT-R}, V_{OUT-G}, and V_{OUT-B}.



9. Random noise is defined on the output waveform with the external clamp and is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e.dark conditions) calculated by the following procedure.



a) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
b) Each of the output level at video output periods is averaged over 200ns period to get V (n) and V (n + 1).
c) V (n + 1) is subtracted from V (n) to get ƒ¢V.

   ƒ¢V = Vn •|V (n + 1)

d) The standard deviation of ƒ¢V is calculated after procedure b) and c) are repeated 30 times (30 readings).

$$\Delta\overline{V} = \frac{1}{30}\sum_{i=1}^{30} |\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30} (|\Delta Vi| \bullet |\Delta V)^2}$$

e) Procedure b), c) and d) are repeated 10 times to get sigma value.

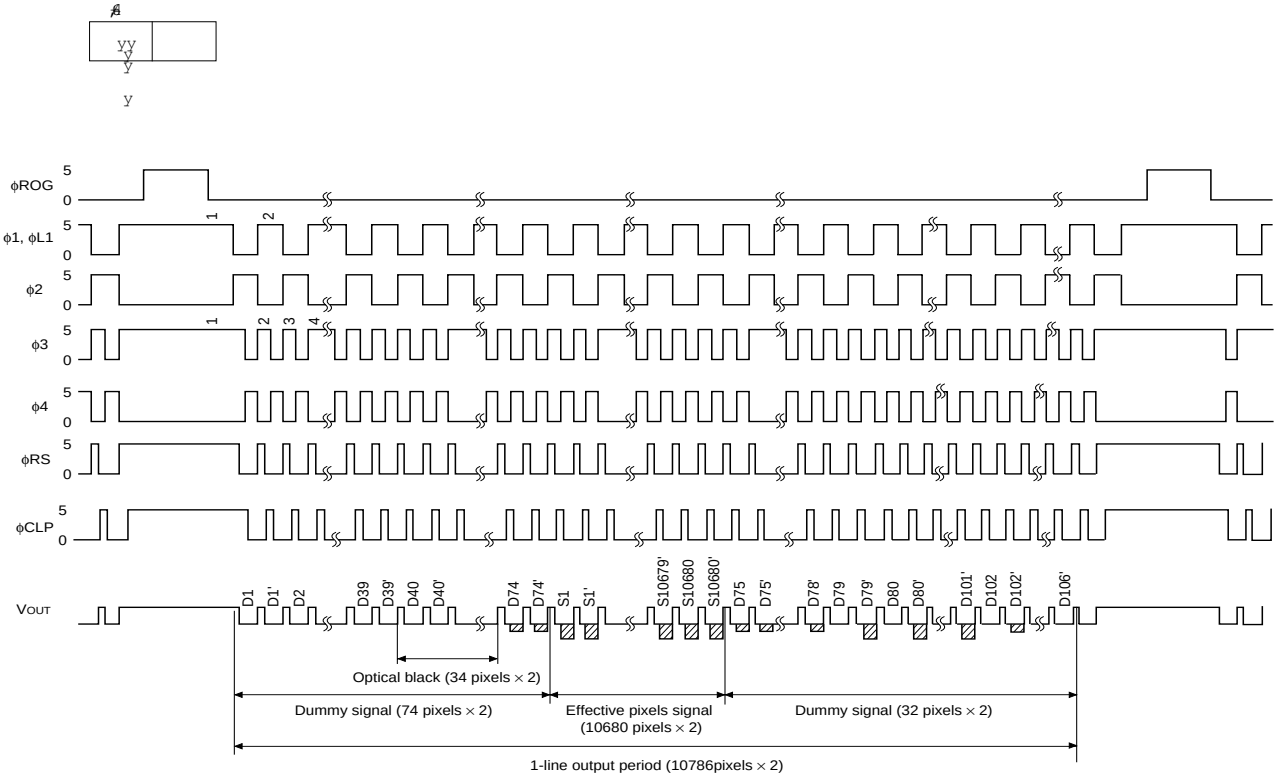
f) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10}\sum_{i=1}^{10} \sigma j$$

g) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify random noise as follows.

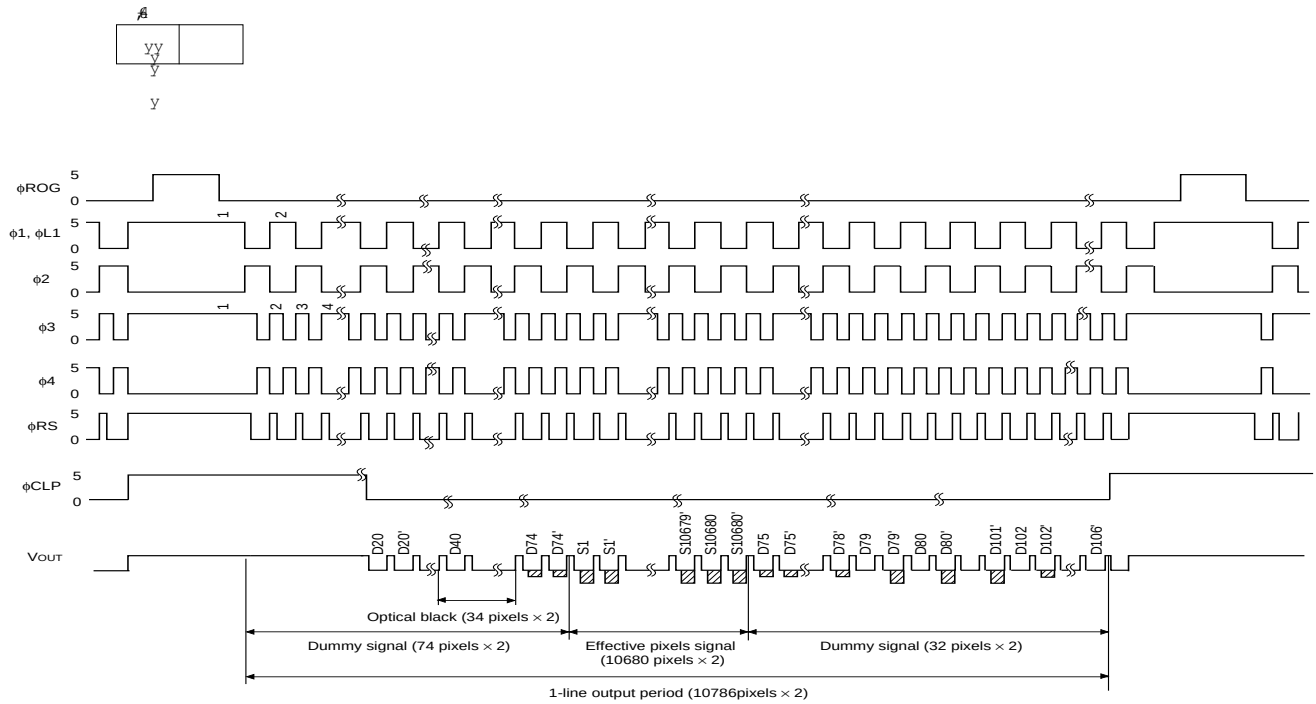
$$NDσ = \frac{1}{\sqrt{2}}\overline{\sigma}$$

Clock Timing Chart 1 2400 DPI Staggered(pixel clamp mode)



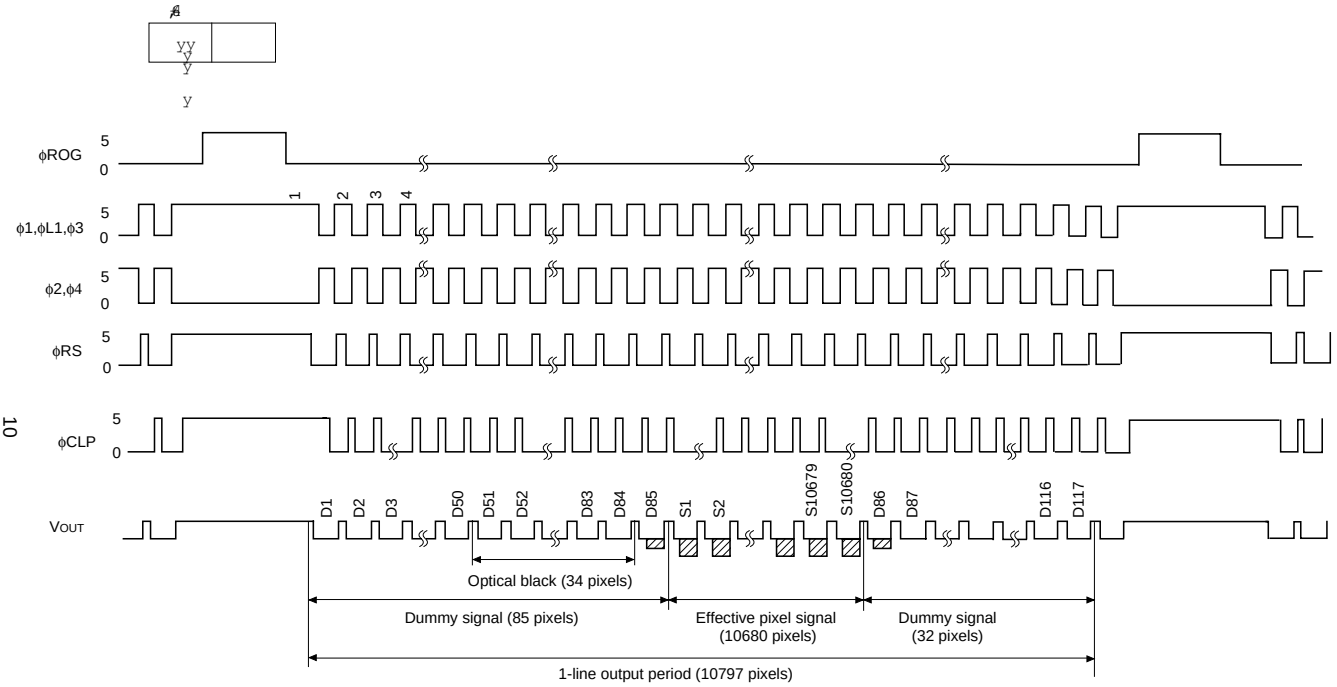
Note) The transfer pulses (φ1, φ2) must have more than 10786 cycles.
The transfer pulses (φ3, φ4) must have more than 21572 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

Clock Timing Chart 2 2400 DPI Staggered(line clamp mode)



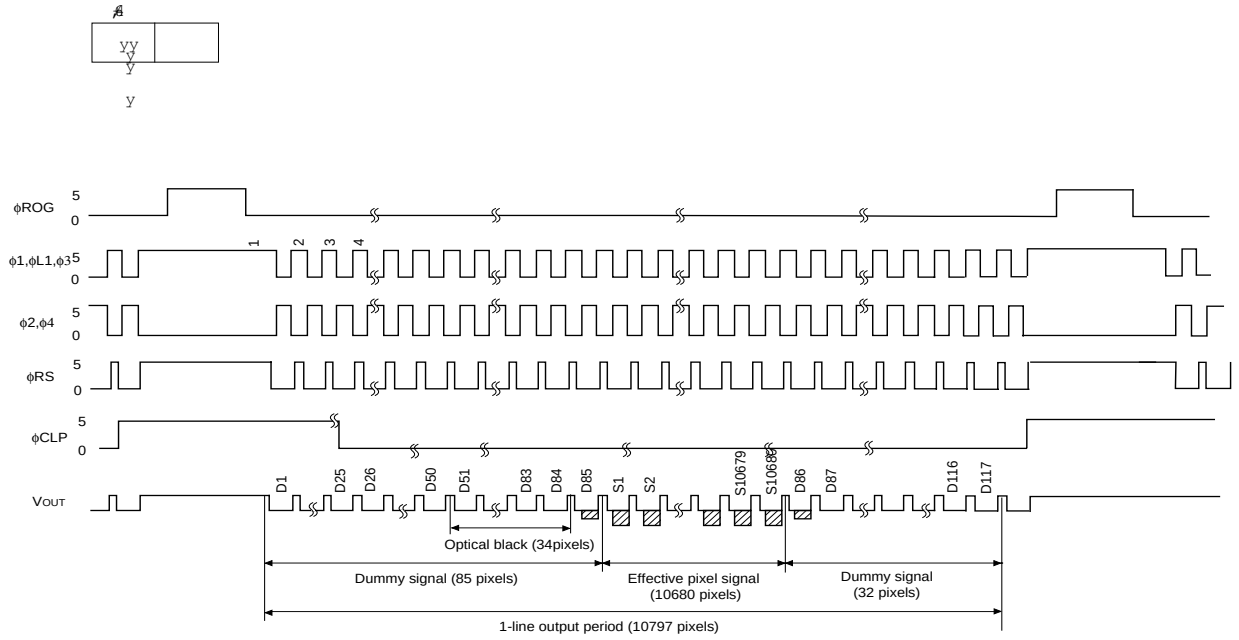
Note) The transfer pulses (φ1, φ2) must have more than 10786 cycles.
The transfer pulses (φ3, φ4) must have more than 21572 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

Clock Timing Chart 3 1200 DPI Linear(pixel clamp mode)



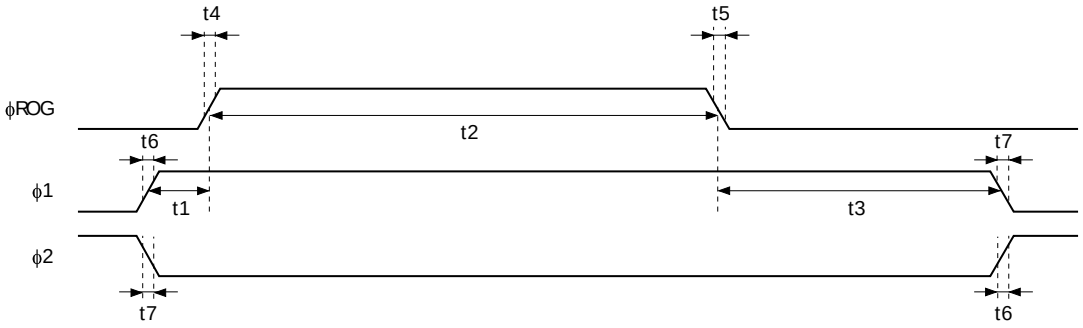
Note) The transfer pulses (φ1, φ2) must have more than 10797 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

Clock Timing Chart 4 1200 DPI Linear(line clamp mode)

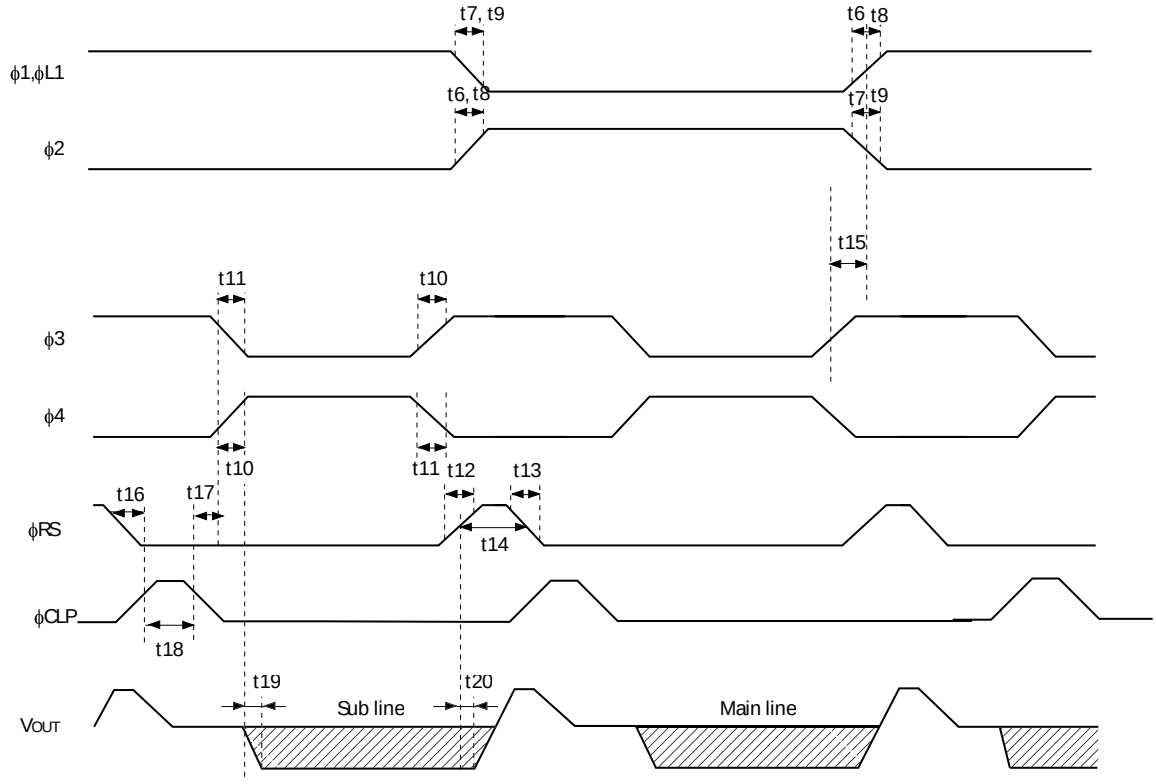


Note) The transfer pulses (φ1, φ2) must have more than 10797 cycles.
VOUT indicates VOUT-R, VOUT-G, VOUT-B.

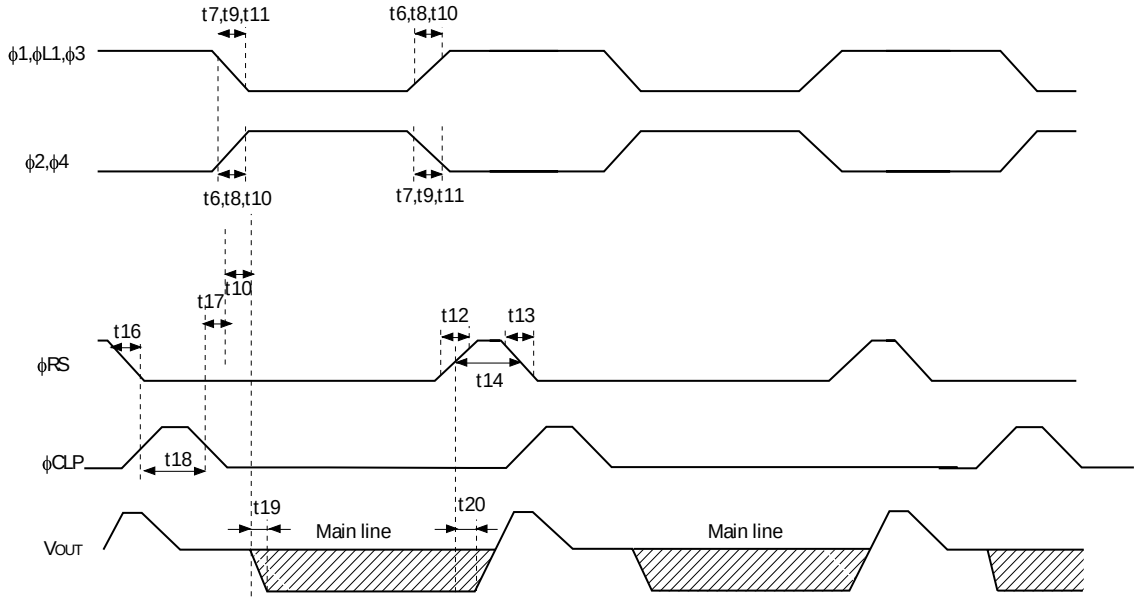
Clock Timing Chart5 2400 DPI Staggered



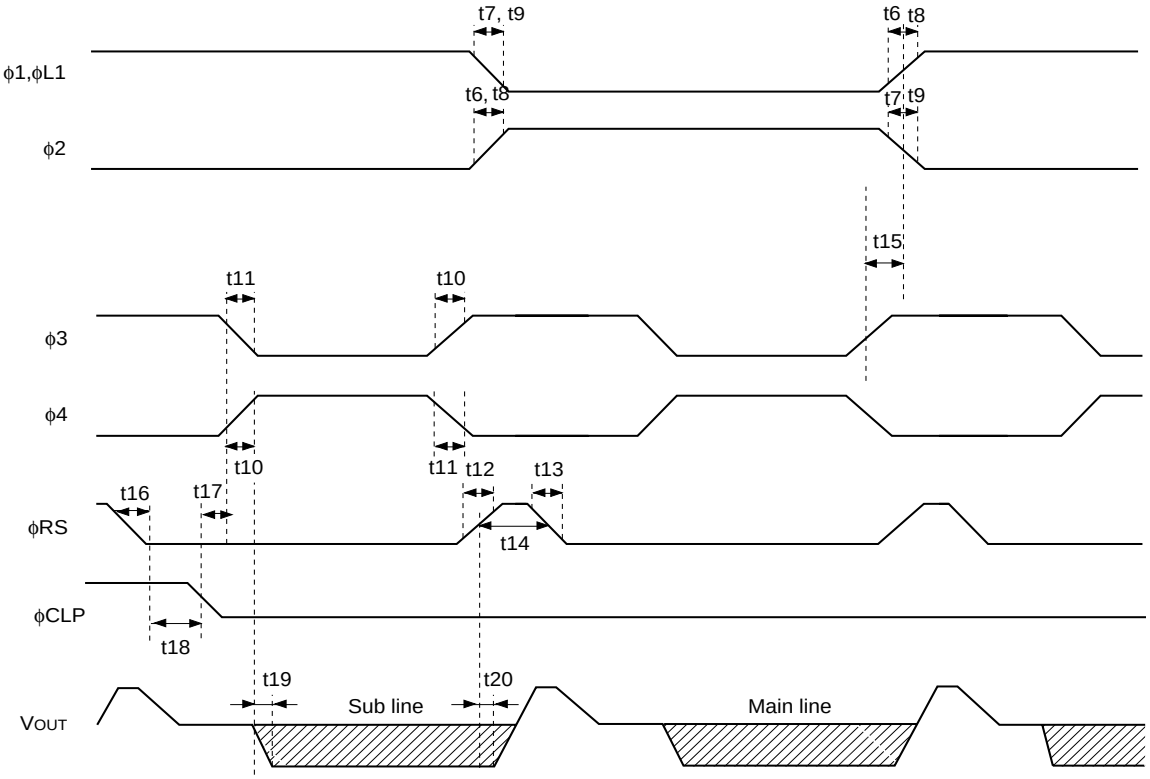
ClockTiming Chart 6
(2400 DPI pixel clamp mode)



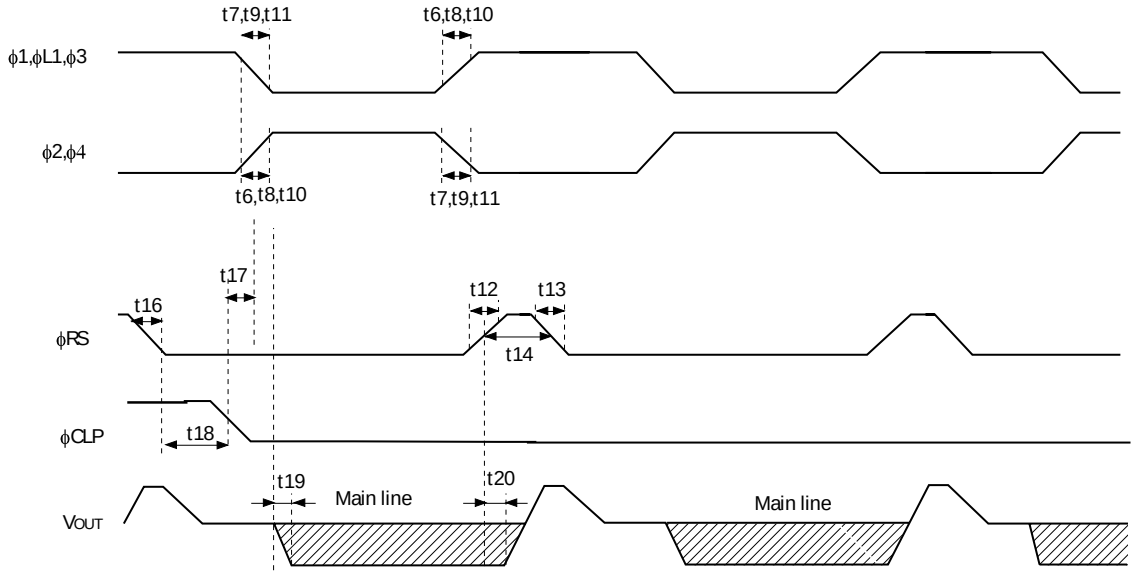
ClockTiming Chart 7
(1200 DPI pixel clamp mode)



ClockTiming Chart 8
(2400 DPI line clamp mode)



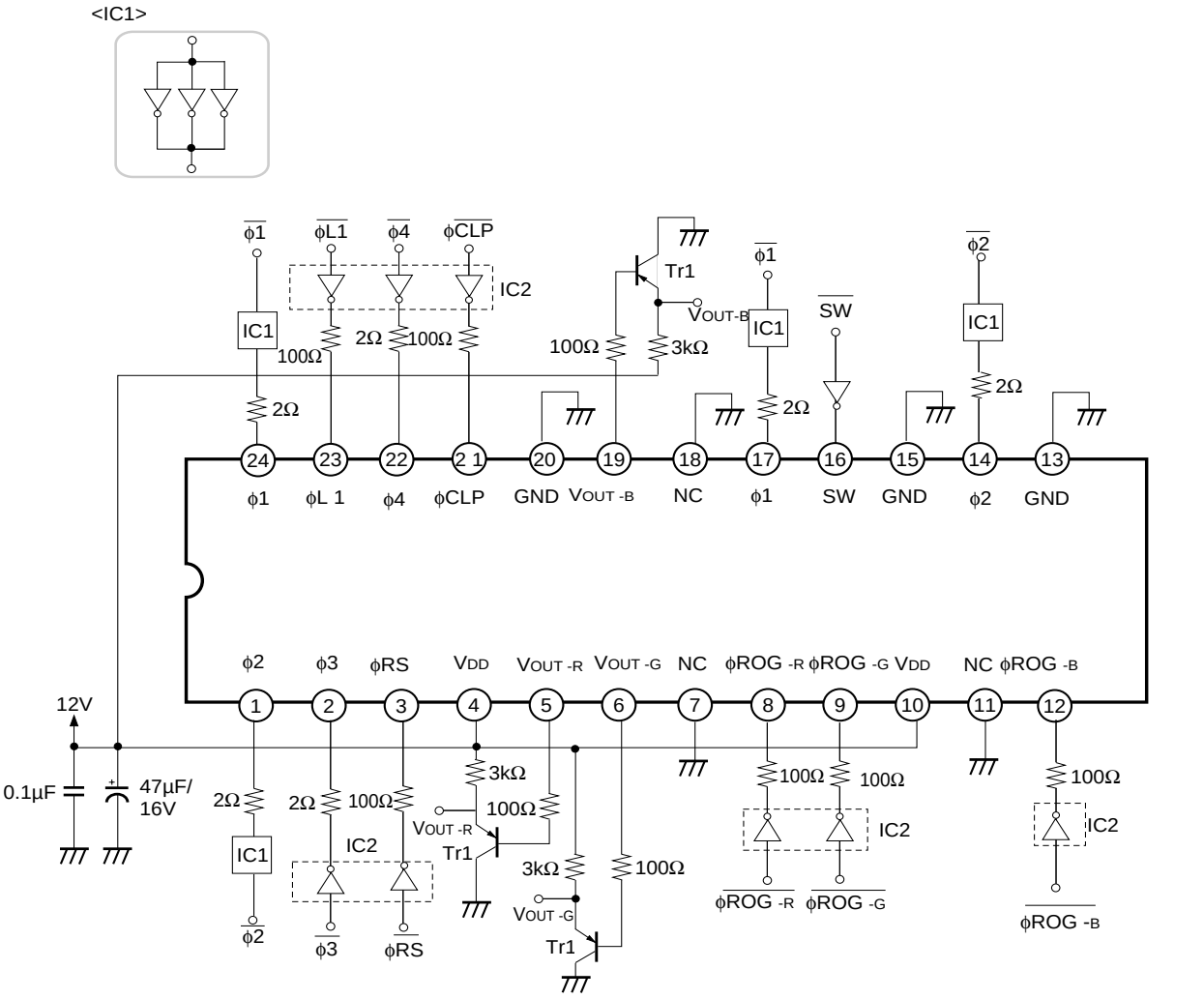
ClockTiming Chart 9
(1200 DPI line clamp mode)



Clock Pulse Recommended Timing

*1 These timing is the recommended condition under $f_{\phi RS}$ = 1MHz.

Application Circuit*



* Data rate $f_{\phi RS}$ = 1MHz

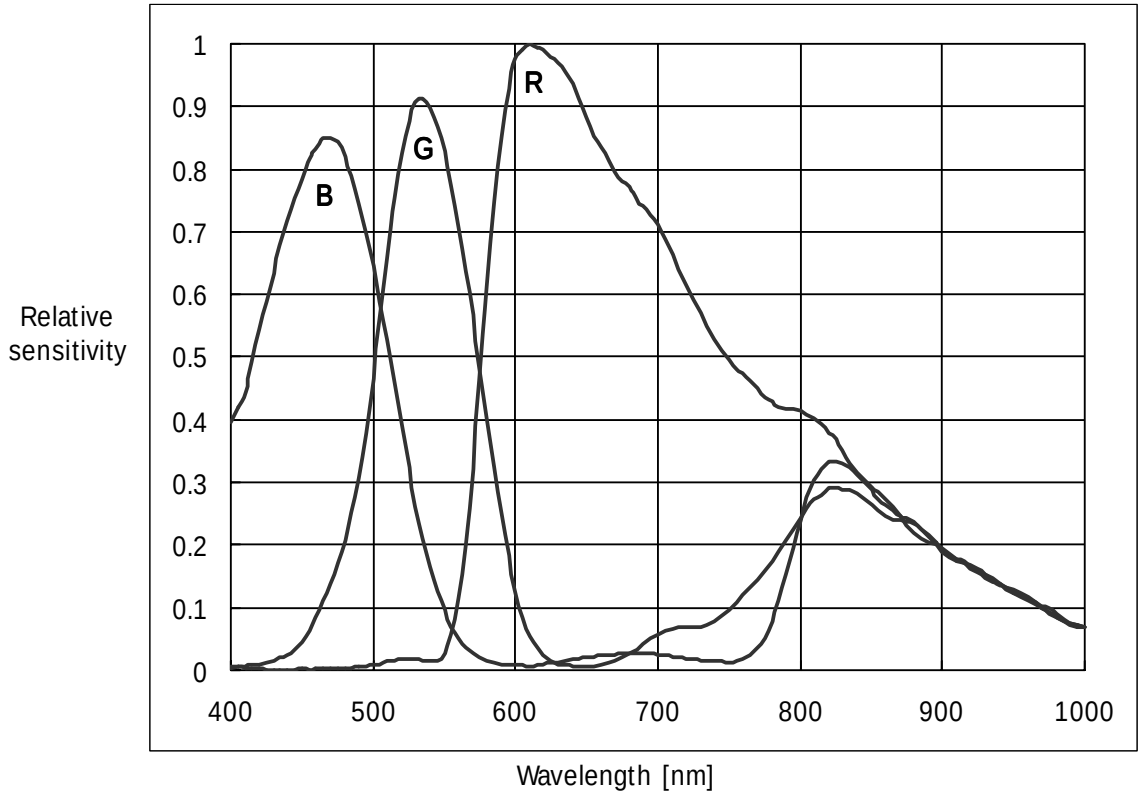
IC1: 74AC04 ×3pcs
IC2: 74HC04
Tr1: 2SA1175

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

<2400DPI>

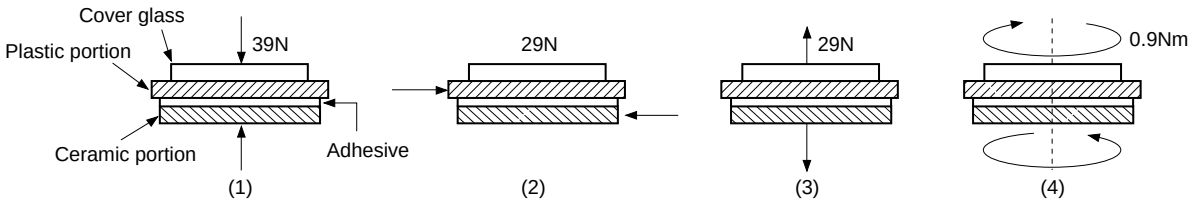
Spectral sensitivity characteristics (Standard characteristics)



Notes of Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Packages
   The following points should be observed when handling and installing packages.
   a) Remain within the following limits when applying static load to the package:
      (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
      (2) Shearing strength: 29N/surface
      (3) Tensile strength: 29N/surface
      (4) Torsional strength: 0.9Nm



   b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
   c) Be aware that any of the following can cause the package to crack or dust to be generated.
      (1) Applying repetitive bending stress to the external leads.
      (2) Applying heat to the external leads for an extended period of time with soldering iron.
      (3) Rapid cooling or heating.
      (4) Prying the plastic portion and ceramic portion away at a support point of the adhesive layer.
      (5) Applying the metal a crash or a rub against the plastic portion.
      Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.
   d) The notch of the plastic portion is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch or ceramic may overlap with the notch of the plastic portion.

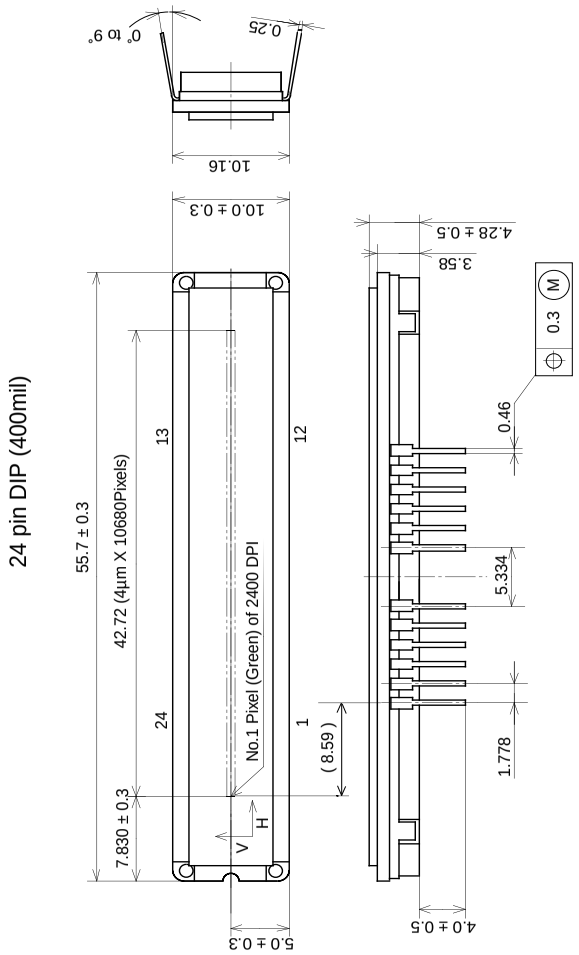
3) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm



1. The height from the bottom to the sensor surface is 2.38 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic, Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.43g
DRAWING NUMBER	LS-B41(E)

02.07.30