Low Frequency EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Provides up to 15dB of EMI suppression.
- Generates a 1X or ½X low EMI spread spectrum clock of the input frequency.
- Input frequency range: 8MHz to 32MHz.
- Internal loop filter minimizes external components and board space.
- Frequency deviation:
  - P2005A: ± 1% to ± 3%
  - P2005S: ± 0.6% to ± 1.8%
- SSON# control pin for spread spectrum enable and disable options.
- Low cycle-to-cycle jitter.
- 3.3V or 5V operating voltage range.
- Ultra-low power CMOS design.
- Available in 8-pin SOIC and TSSOP.

Product Description

The P2005A/S is a versatile spread spectrum frequency modulator designed specifically for input clock frequencies from 8MHz to 32MHz. *Refer Output Frequency Selection Table.* The P2005A/S can generate an EMI reduced clock from crystal, ceramic resonator, or system clock. The P2005A/S offers various percentage deviations ranging form ±0.6% to ±3.0%. *Refer Frequency Deviation Selections Table.* The P2005A/S reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P2005A/S allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

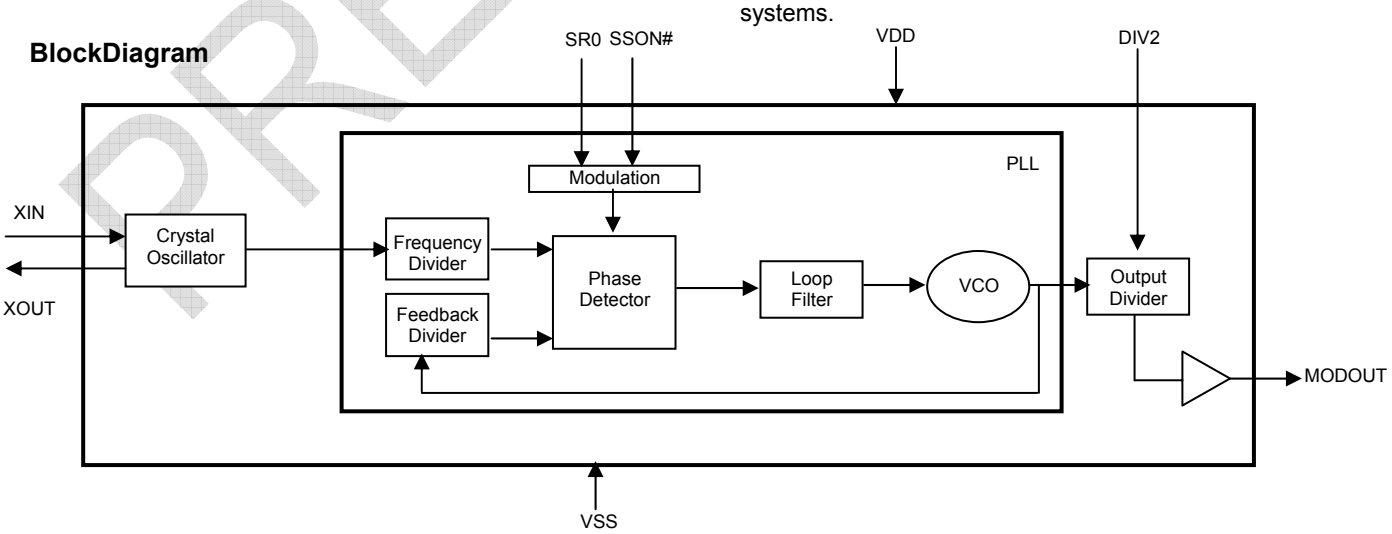
The P2005A/S uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The P2005A/S modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

Applications

The P2005A/S is targeted towards EMI management for high-speed digital applications such as PC peripheral devices, consumer electronics and embedded controller systems.

BlockDiagram



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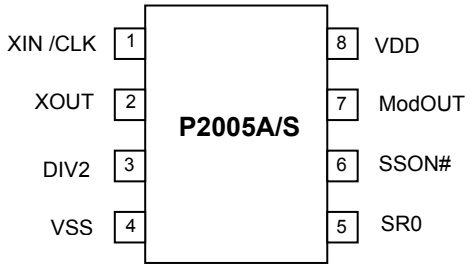
Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN/CLK	I	Connect to crystal or clock.
2	XOUT	O	Crystal output.
3	DIV2	I	Digital logic input used to select normal output mode or divide-by-two output mode. When this pin is HIGH, the frequency of the output clock is the same as the input clock frequency. When it is tied low, the output frequency is half the input clock frequency. This pin has an internal pull-up resistor.
4	VSS	P	Ground to entire chip. Connect to system ground.
5	SR0	I	Digital logic input used to select Spreading Range *Refer Modulation Output and Spreading Range Selection Table*. This pin has an internal pull-up resistor.
6	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull-low resistor.
7	ModOUT	O	Spread spectrum clock output.
8	VDD	P	Power supply for the entire chip (+3.3V or 5.0V)

Output Frequency Selections

Input Frequency		8MHz	12MHz	16MHz	20MHz	24MHz	28MHz	32MHz	
DIV2	0 (1/2 X)	4MHz	6MHz	8MHz	10MHz	12MHz	14MHz	16MHz	Output Frequency
	1 (1X)	8MHz	12MHz	16MHz	20MHz	24MHz	28MHz	32MHz	

Frequency Deviation Selections as a Function of Input Frequency

P/N	SR0	Input Frequency Range							Modulation Rate (KHz)
		8MHz	12MHz	16MHz	20MHz	24MHz	28MHz	32MHz	
P2005A	0	± 3.0%	± 2.5%	± 2.0%	± 1.8%	± 1.5%	± 1.5%	± 1.3%	$(X_{IN}/20) * 62.5$
	1	± 2.5%	± 2.0%	± 1.8%	± 1.5%	± 1.3%	± 1.3%	± 1.0%	
P2005S	0	± 1.8%	± 1.5%	± 1.2%	± 1.1%	± 0.9%	± 0.9%	± 0.8%	
	1	± 1.5%	± 1.2%	± 1.1%	± 0.9%	± 0.8%	± 0.8%	± 0.6%	

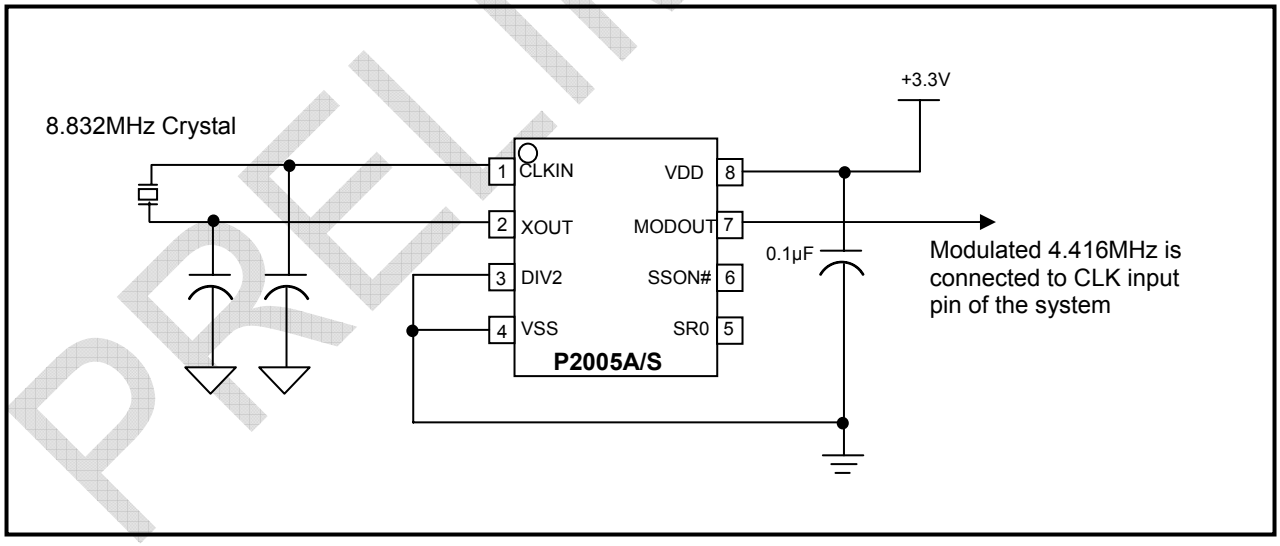
Spread Spectrum

The *Output Frequency Selection Table and the Frequency Deviations Selections Table* illustrate the two possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency (Note: The center frequency is the frequency of the external reference input on CLKIN, Pin1).

Example:
The P2005A/S is designed for communications, digital video and imaging applications. It is not only optimized for operation in the 8MHz – 32MHz range, but its output frequency can be extended down to one half of the input clock frequency using the divide-by-two feature. This feature extends low frequency as low as to 4MHz. Setting Pin 3 low (DIV2 = 0; Divide-by-two mode) sets the output frequency (ModOUT) to half the frequency of the input clock (CLKIN). This is a simple way to generate a spread spectrum modulated low frequency clock when only a higher frequency signal is available. If you want the output frequency to be the same as the input, you can either set DIV2=1 or leave it unconnected.

Selecting the P2005A/S's spread options is a matter of either setting SR0=1 or SR0=0. Setting SR0=0 set as a lower modulation spread, while setting it to 1 introduces a wider spectral spread in the output clock. *Refer Modulation output and Spreading Selections Tables.* The example given in the figure below shows the device set to the divide-by-two mode (DIV2=0) with a lower spectrum range (SR0=0). The versatility provided by allowing both clock division and spread spectrum on one chip is already proving to be a popular solution among leading system manufacturers.

P2005A/S Application Schematic



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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to 70	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND – 0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	VDD + 0.3	V
I_{IL}	Input low current (pull-up resistors on inputs SR0, SR1, CP0 and CP1)	-	-	-35	µA
I_{IH}	Input high current (pull-down resistor on input SSON#)	-	-	35	µA
I_{XOL}	XOUT Output Low Current (@ 0.4V, VDD = 3.3V)	-	3	-	mA
I_{XOH}	XOUT Output High Current (@ 2.5V, VDD = 3.3V)		3		
V_{OL}	Output low voltage (VDD = 3.3V, I_{OL} = 20mA)	-	-	0.4	V
V_{OH}	Output high voltage (VDD = 3.3V, I_{OH} = 20mA)	2.5	-	-	V
I_{CC}	Dynamic supply current normal mode (3.3V, and 15pF loading)	6.0	7.0	8.3	mA
I_{DD}	Static supply current standby mode	-	0.6	-	mA
VDD	Operating voltage	3.1	3.3	5.5	V
t_{ON}	Power up time (first locked clock cycle after power up)	-	0.18	-	mS
Z_{OUT}	Clock output impedance	-	50	-	Ω

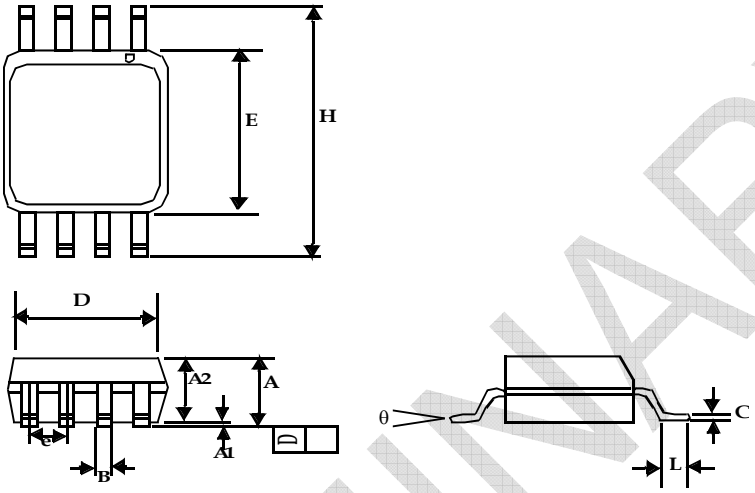
AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input frequency		8	-	32	MHz
f_{OUT}	Output frequency	1X Option	8	-	32	MHz
		1/2X Option	4	-	16	
t_{LH}*	Output rise time (measured at 0.8V to 2.0V)		0.7	0.9	1.1	nS
t_{HL}*	Output fall time (measured at 2.0V to 0.8V)		0.6	0.8	1.0	nS
t_{JC}	Jitter (cycle to cycle)		-	-	360	pS
t_D	Output duty cycle		45	50	55	%

*t_{LH} and t_{HL} are measured into a capacitive load of 15pF

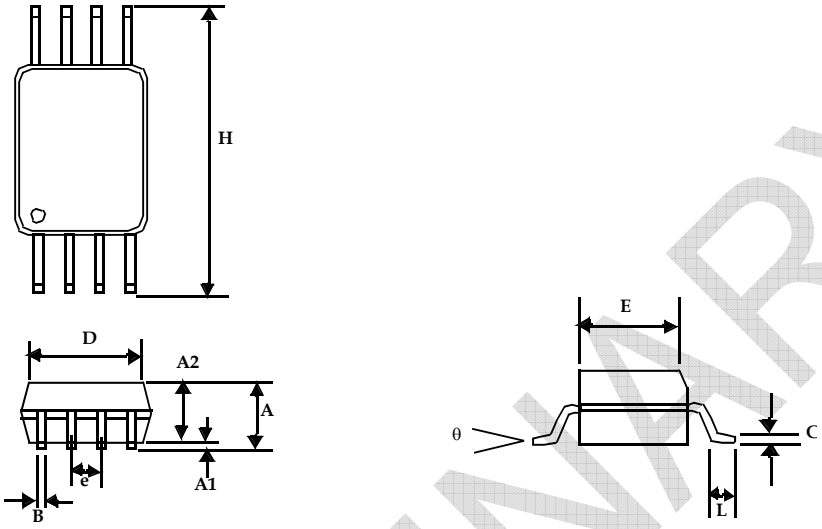
Package Information

8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

8-lead TSSOP (4.40-MM Body)



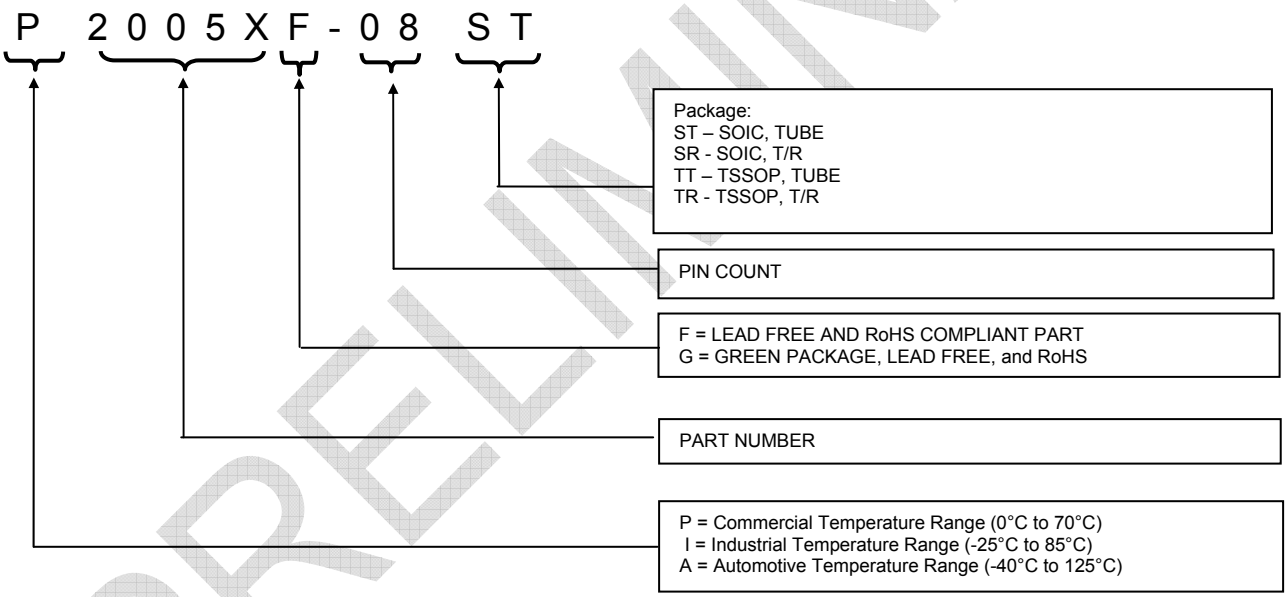
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

Ordering Codes

Part Number	Marking	Package type	Temperature
P2005XF-08ST	P2005XF	8 PIN SOIC, TUBE, Pb Free	Commercial
P2005XF-08SR	P2005XF	8 PIN SOIC, TAPE AND REEL, Pb Free	Commercial
P2005XF-08TT	P2005XF	8 PIN TSSOP, TUBE, Pb Free	Commercial
P2005XF-08TR	P2005XF	8 PIN TSSOP, TAPE AND REEL, Pb Free	Commercial
P2005XG-08ST	P2005XG	8 PIN SOIC, TUBE, Green	Commercial
P2005XG-08SR	P2005XG	8 PIN SOIC, TAPE AND REEL, Green	Commercial
P2005XG-08TT	P2005XG	8 PIN TSSOP, TUBE, Green	Commercial
P2005XG-08TR	P2005XG	8 PIN TSSOP, TAPE AND REEL, Green	Commercial

Note: X=A or S

Device Ordering Information



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Document Version: v1.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003