



LC7874E

CD Graphics Decoder



Overview

The LC7874E is a CMOS LSI that provides the signal processing needed for compact disc graphics (CD-G) on a single chip. The LC7874E accepts subcode R to W signals output from a CD player DSP LC786X Series, LC7862XE Series, or LC7863XE Series device, and performs de-interleaving, error detection and correction, graphic instruction processing, and image processing.

Features

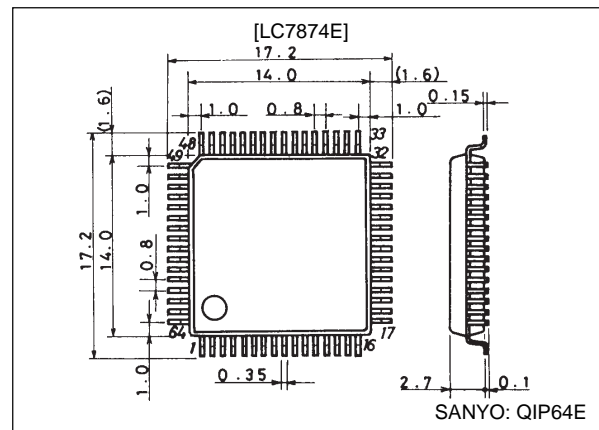
- A CD-G decoder can be configured using a three-chip combination of this LSI—the LC7874E—with external RAM (64K × 4 bits) and an LC78010E digital RGB encoder.
- Performs insertion and protection of CD subcode R to W sync signals and detection of R to W signal de-interleave error signals.
- Has two crystal oscillators, for NTSC and PAL, with simple switchover by means of a control pin. Connecting a crystal resonator of 14.31818 MHz for NTSC and 17.734476 MHz for PAL enables the standard clock and other necessary timings to be generated internally.
- Performs CD graphics instruction processing and drawing functions, and controls image display.

- Has microcomputer interface functions, allowing set upgrading.
- Provides superimposition support.
- Has a color bar signal output function.
- DRAM interface and RGB output and sync signal output are 3-state outputs.

Package Dimensions

unit: mm

3159-QFP64E



- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Specifications

Electrical Characteristics at $T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	V_{DD}	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Input voltage	V_{IN}	S1, S2, SFSY, PW, SBSY, CE, DI, CL, MUTE, DB0 to 3, CB, CE1, CE2, CE3, LINE, HRESET, VRESET, INIT, RESET, N/P, SON, XIN1, XIN2	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Output voltage	V_{OUT}	SBCK, DO, CDGM, WE, RAS, A0 to 7, DB0 to 3, CAS, OE, ROUT0 to 3, GOUT0 to 3, BOUT0 to 3, HSYNC, CSYNC, BLANK, YS, 4FSCO, EFLG, FSCO, XOUT1, XOUT2	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d \text{ max}$	$T_a = 25^\circ\text{C}$	500	mW
Operating temperature	T_{opr}		-30 to $+85$	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to $+125$	$^\circ\text{C}$

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Allowable Operating Ranges at Ta = -30°C to +85°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply voltage	V _{DD}	V _{DD}	3.0	5.0	5.5	V
Input high-level voltage	V _{IH1}	S1, S2, CB LINE, N/P, SON	0.7 V _{DD}		V _{DD} + 0.3	V
	V _{IH2}	INIT, RESET	0.8 V _{DD}		V _{DD} + 0.3	V
	V _{IH3}	CL	0.8 V _{DD}		5.8	V
	V _{IH4}	DB0 to DB3, HRESET, VRESET	2.2		V _{DD} + 0.3	V
	V _{IH5}	SFSY, PW, SBSY, CE, DI, MUTE, CE1 to CE3	2.2		5.8	V
Input low-level voltage	V _{IL1}	S1, S2, CB, LINE, N/P, SON	V _{SS} - 0.3		0.3V _{DD}	V
	V _{IL2}	CL, INIT, RESET	V _{SS} - 0.3		0.2V _{DD}	V
	V _{IL3}	SFSY, PW, SBSY, CE, DI, MUTE, DB0 to DB3, CE1 to CE3, HRESET, VRESET	V _{SS} - 0.3		0.8	V
Input frequency	F _{SCIN1}	XIN1	14.31818			MHz
	F _{SCIN2}	XIN2	17.734476			MHz
Input amplitude	V _{IN}	XIN1, XIN2	0.5		V _{DD}	Vp-p

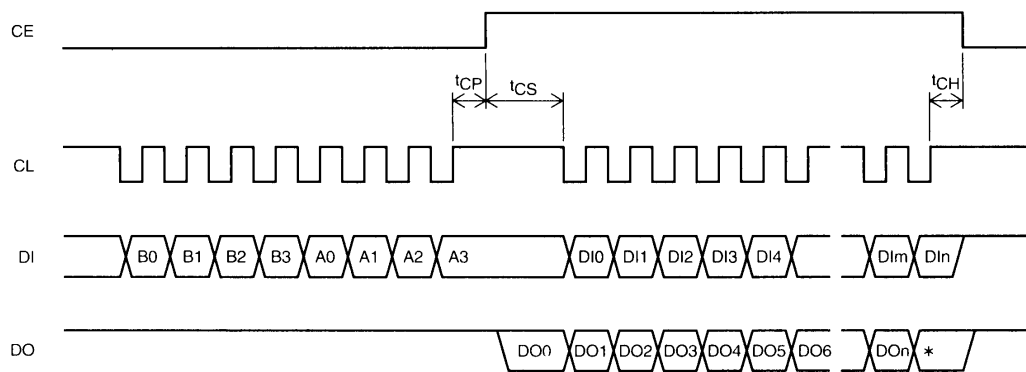
Electrical Characteristics at Ta = -30 to +85°C, V_{DD} = 5 V unless otherwise specified

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	I _{IH1}	S1, S2, SFSY, PW, SBSY, CE, DI, CL, MUTE, DB0 to DB3, LINE, HRESET, VRESET, CE1 to 3, INIT, RESET, N/P, SON : V _{IN} = V _{DD}			5	μA
	I _{IH2}	CB : V _{IN} = V _{DD}	30	100	200	μA
Input low-level current	I _{IL1}	S1, S2, SFSY, PW, SBSY, CE, DI, CL, MUTE, DB0 to DB3, CB, LINE, HRESET, VRESET, CE1 to 3, INIT, RESET, N/P, SON : V _{IN} = V _{SS}	-5			μA
Output high-level voltage	V _{OH}	SBCK, WE, RAS, A0 to 7, CAS, OE, DB0 to 3, CDGM, ROUT0 to 3, GOUT0 to 3, BOUT0 to 3, FSCO, 4FSCO, HSYNC, YS, CSYNC, BLANK, EFLG : I _{OH} = -0.5 mA	V _{DD} - 1		V _{DD}	V
Output low-level voltage	V _{OL}	SBCK, WE, RAS, A0 to 7, CAS, OE, DB0 to 3, CDGM, ROUT0 to 3, GOUT0 to 3, BOUT0 to 3, FSCO, 4FSCO, HSYNC, YS, CSYNC, BLANK, EFLG : I _{OL} = 2.0 mA	V _{SS}		0.4	V
Output off leakage current	I _{OFF}	A0 to A7, RAS, CAS, OE, WE, DB0 to DB3, HSYNC, ROUT0 to 3, GOUT0 to 3, BOUT0 to 3, CSYNC, BLANK, FSCO, 4FSCO	-5		+5	μA
Built-in feedback resistance	R _X	XIN1, XIN2		1		MΩ
Clock frequency	f _O	SBCK		220		kHz
Operating current drain	I _{DD}	V _{DD}		26	40	mA

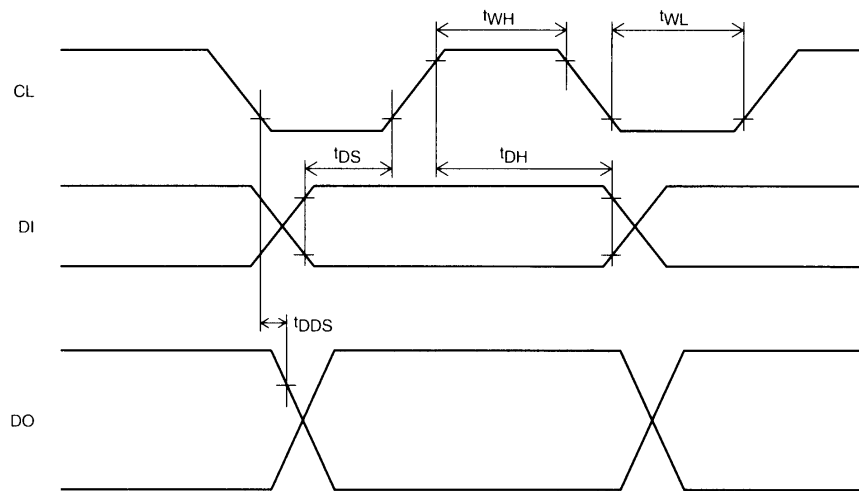
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Timing Characteristics (Microcontroller Interface Timing) at $T_a = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input minimum pulse width	t_{WH}	CL, high pulse width	400			ns
	t_{WL}	CL, low pulse width	400			ns
Data setup time	t_{DS}	DI, CL	200			ns
Data hold time	t_{DH}	DI, CL	200			ns
Data hold time	t_{DOH}	DO, CL	130		300	ns
CE wait time	t_{CP}	CE, CL	400			ns
CE setup time	t_{CS}	CE, CL	400			ns
CE hold time	t_{CH}	CE, CL	400			ns



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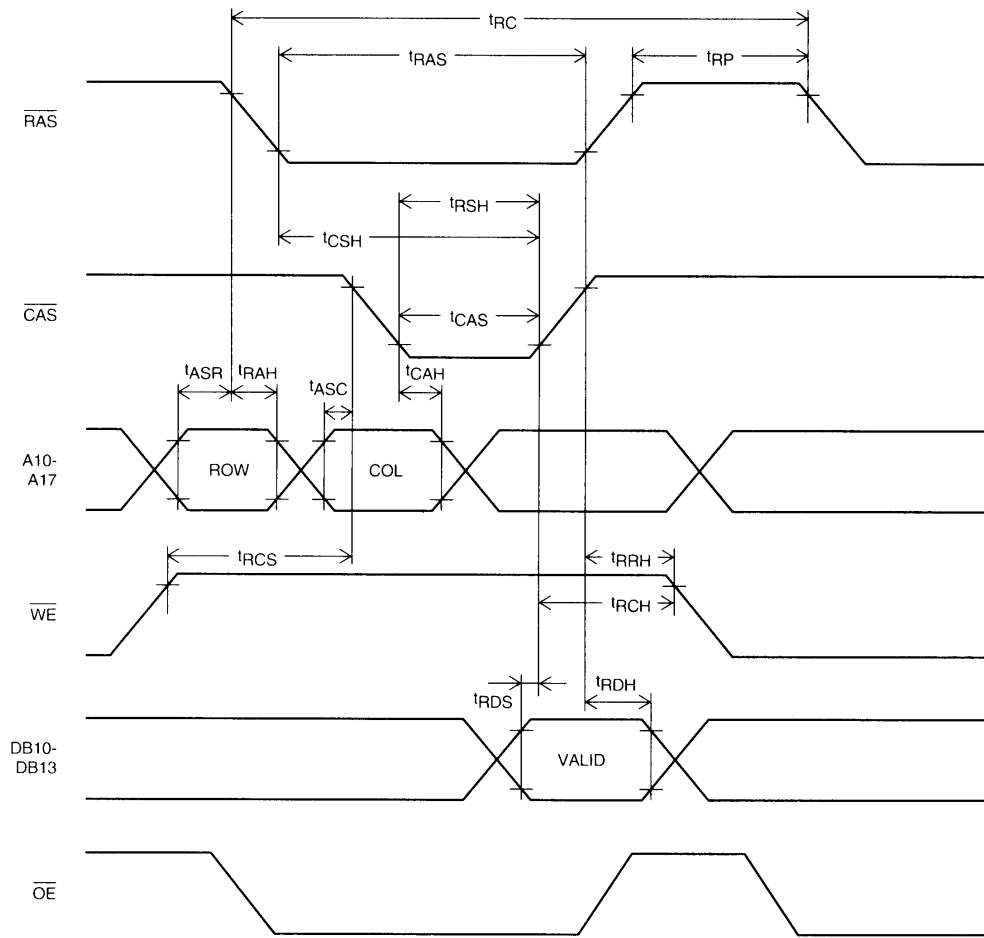
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Timing Characteristics (DRAM Access Timing) at $T_a = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$

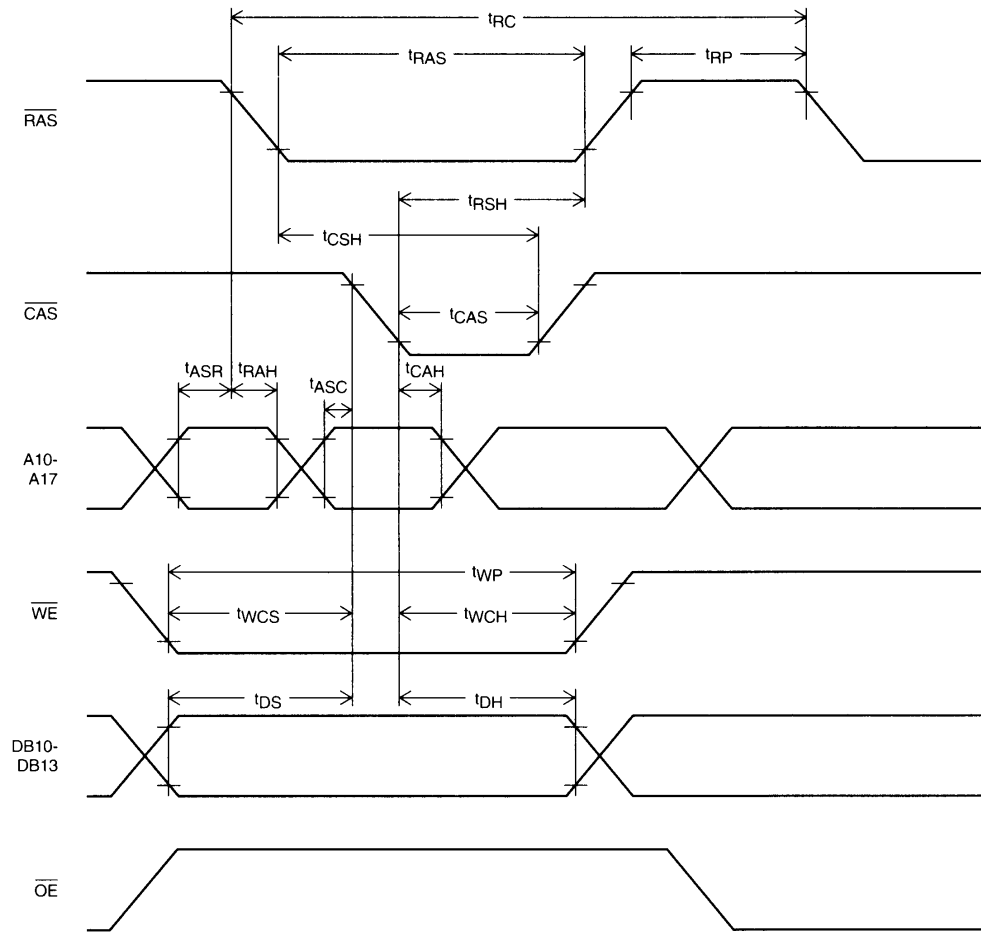
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Random read/write cycle time	t_{RC}		250			ns
Page mode cycle time	t_{PC}		130			ns
$\overline{\text{RAS}}$ precharge time	t_{RP}		100			ns
$\overline{\text{RAS}}$ pulse width	t_{RAS}		120			ns
$\overline{\text{RAS}}$ pulse width (page mode)	t_{RASP}				18000	ns
$\overline{\text{RAS}}$ hold time	t_{RSH}		60			ns
$\overline{\text{CAS}}$ hold time	t_{CSH}		120			ns
$\overline{\text{CAS}}$ pulse width	t_{CAS}		60			ns
$\overline{\text{CAS}}$ precharge time	t_{CPN}		50			ns
$\overline{\text{CAS}}$ precharge time	t_{CP}	(In page mode)	50			ns
Row address setup time	t_{ASR}		100			ns
Row address hold time	t_{RAH}		50			ns
Column address setup time	t_{ASC}		0			ns
Column address hold time	t_{CAH}		50			ns
Read command setup time	t_{RCS}		150			ns
Read command hold time	t_{RCH}	(Referenced to $\overline{\text{CAS}}$)	120			ns
Read command hold time	t_{RRH}	(Referenced to $\overline{\text{RAS}}$)	120			ns
Write command setup time	t_{WCS}		100			ns
Write command hold time	t_{WCH}		50			ns
Write command pulse width	t_{WP}		150			ns
Write data setup time	t_{DS}		100			ns
Write data hold time	t_{DH}		100			ns
$\overline{\text{CAS}}$ setup time	t_{CSR}	($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	50			ns
$\overline{\text{CAS}}$ hold time	t_{CHR}	($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	50			ns
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ active time	t_{RPC}		50			ns
Read data setup time	t_{RDS}		20			ns
Read data hold time	t_{RDH}		10			ns
Refresh time	t_{REF}				3.5	ms

DRAM Read Cycle



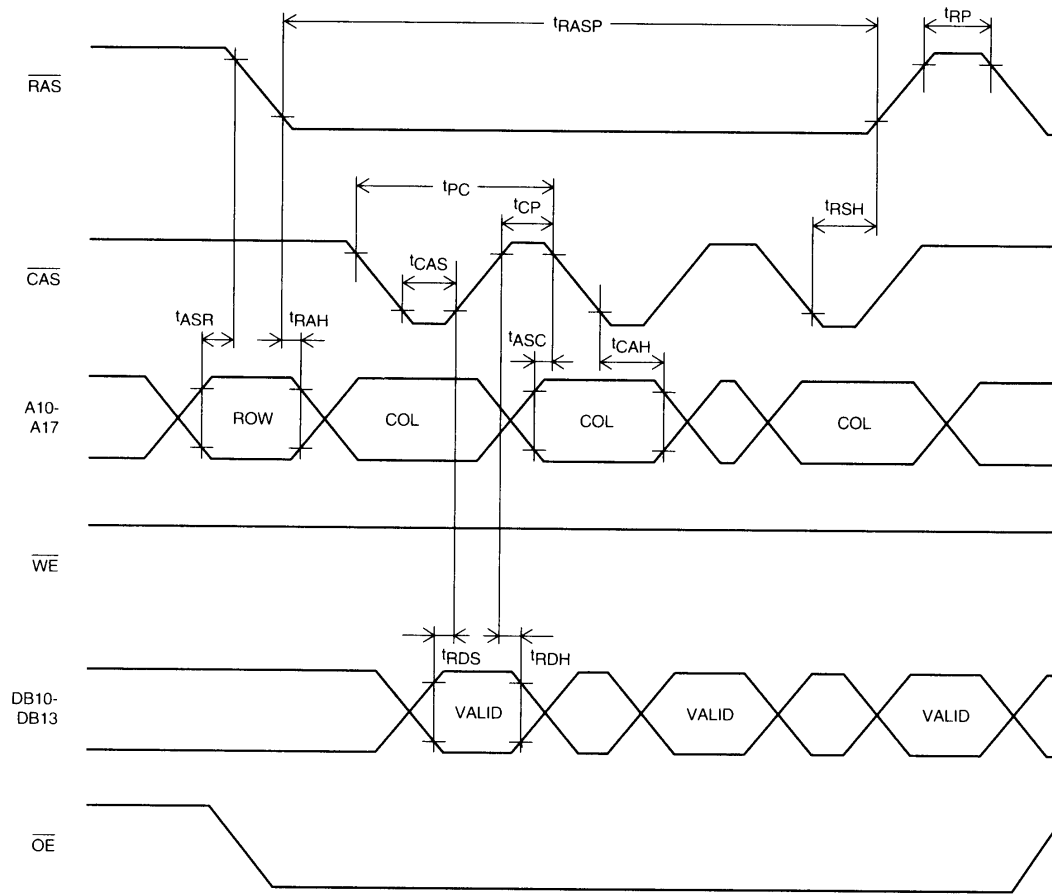
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DRAM Early Write Cycle



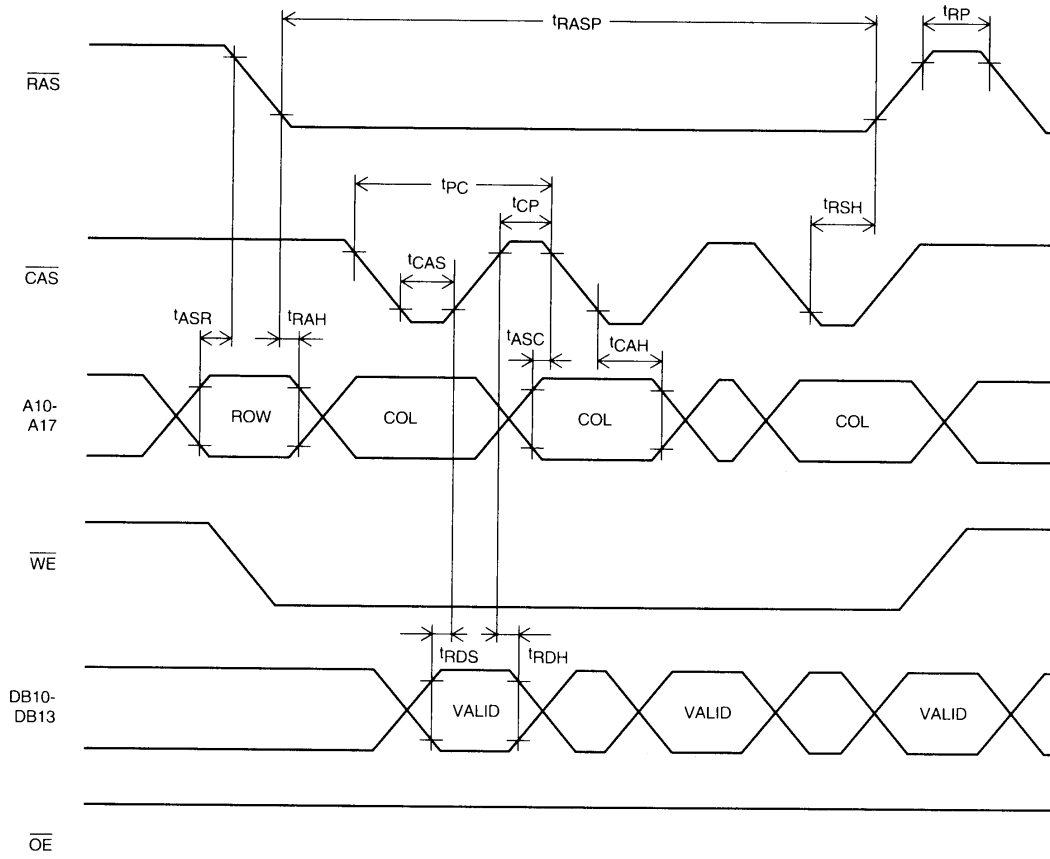
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DRAM Page Mode Read Cycle



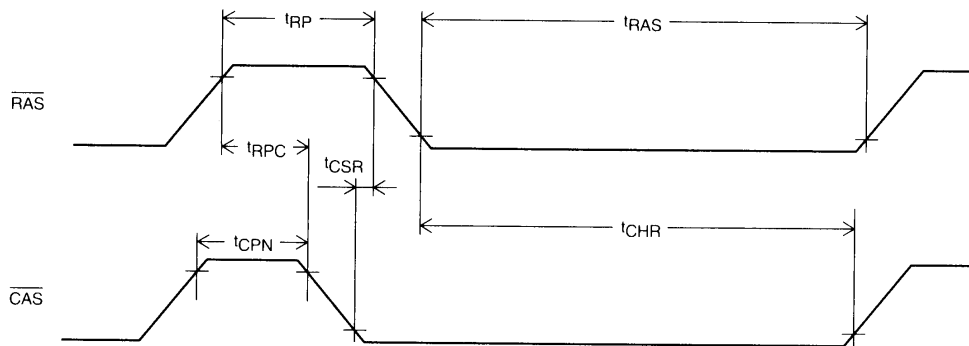
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DRAM Page Mode Write Cycle



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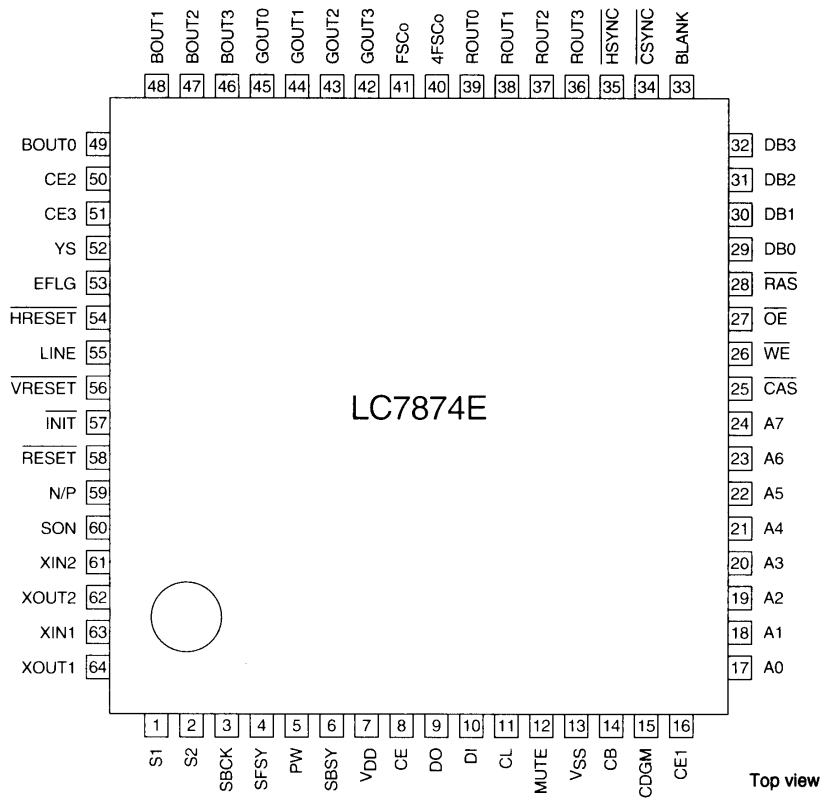
DRAM CAS-Before-RAS Refresh Cycle



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Pin Assignment



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Pin Functions

Pin	Pin Symbol	Pin Name	I/O	Polarity	Function		
					S1	S2	Selected CD DSP
1	S1	CD DSP selection pins	In	Positive	0	0	LC7861N/67
2	S2				1	0	LC7860K/63
					0	1	Setting prohibited
					1	1	LC7868/62X/63X
3	SBCK	Clock output pin	Out	—	Subcode R to W read clock output		
4	SFSY	Sync signal input pin	In	Positive	Subcode frame sync signal input (MORE+ input)		
5	PW	Data input pin	In	Positive	Subcode R to W data input (MORE+ input)		
6	SBSY	Sync signal input pin	In	Positive	Subcode block sync signal input (MORE+ input)		
7	V _{DD}	Power supply pin (+5 v)	—	—	Digital power supply		
8	CE	Enable input pin	In	Positive	Serial input/output data control input (MORE+ input)		
9	DO	Data output pin	Out	Positive	Serial data output (Nch open-drain)		
10	DI	Data input pin	In	Positive	Serial data input (MORE+ input)		
11	CL	Clock input pin	In	Positive	Serial data input/output clock input (MORE+ input)		
12	MUTE	Data input pin	In	Positive	Control signal input invalidating subcode data (MORE+ input)		
13	V _{SS}	Ground pin (GND)	—	—	GND		
14	CB	Color bar selection pin	In	Positive	L: Normal mode, H: Color bar output (built-in pull-down resistor)		
15	CDGM	Graphic data discrimination output pin	Out	Positive	Goes high when graphics data is input (can be reset low by command control).		
16	CE1	DRAM control input pin	In	Positive	Signal input setting DRAM connection pin to high impedance (MORE+ input)		
17	A0	DRAM output pin	I/O	Positive	DRAM address (A0) output		
18	A1	DRAM output pin	I/O	Positive	DRAM address (A1) output		
19	A2	DRAM output pin	I/O	Positive	DRAM address (A2) output		
20	A3	DRAM output pin	I/O	Positive	DRAM address (A3) output		
21	A4	DRAM output pin	I/O	Positive	DRAM address (A4) output		
22	A5	DRAM output pin	I/O	Positive	DRAM address (A5) output		
23	A6	DRAM output pin	I/O	Positive	DRAM address (A6) output		
24	A7	DRAM output pin	I/O	Positive	DRAM address (A7) output		
25	$\overline{\text{CAS}}$	DRAM output pin	3ST	Negative	DRAM column address strobe signal output		
26	$\overline{\text{WE}}$	DRAM output pin	3ST	Negative	DRAM data write enable signal output		
27	$\overline{\text{OE}}$	DRAM output pin	3ST	Negative	DRAM data read enable signal output		
28	$\overline{\text{RAS}}$	DRAM output pin	3ST	Negative	DRAM row address strobe signal output		
29	DB0	DRAM input/output pin	I/O	Positive	DRAM data (D0) input/output		
30	DB1	DRAM input/output pin	I/O	Positive	DRAM data (D1) input/output		
31	DB2	DRAM input/output pin	I/O	Positive	DRAM data (D2) input/output		
32	DB3	DRAM input/output pin	I/O	Positive	DRAM data (D3) input/output		
33	BLANK	Blank signal output pin	3ST	Positive	Video signal blanking period output		
34	$\overline{\text{CSYNC}}$	Composite sync output pin	3ST	Negative	Composite sync signal output		

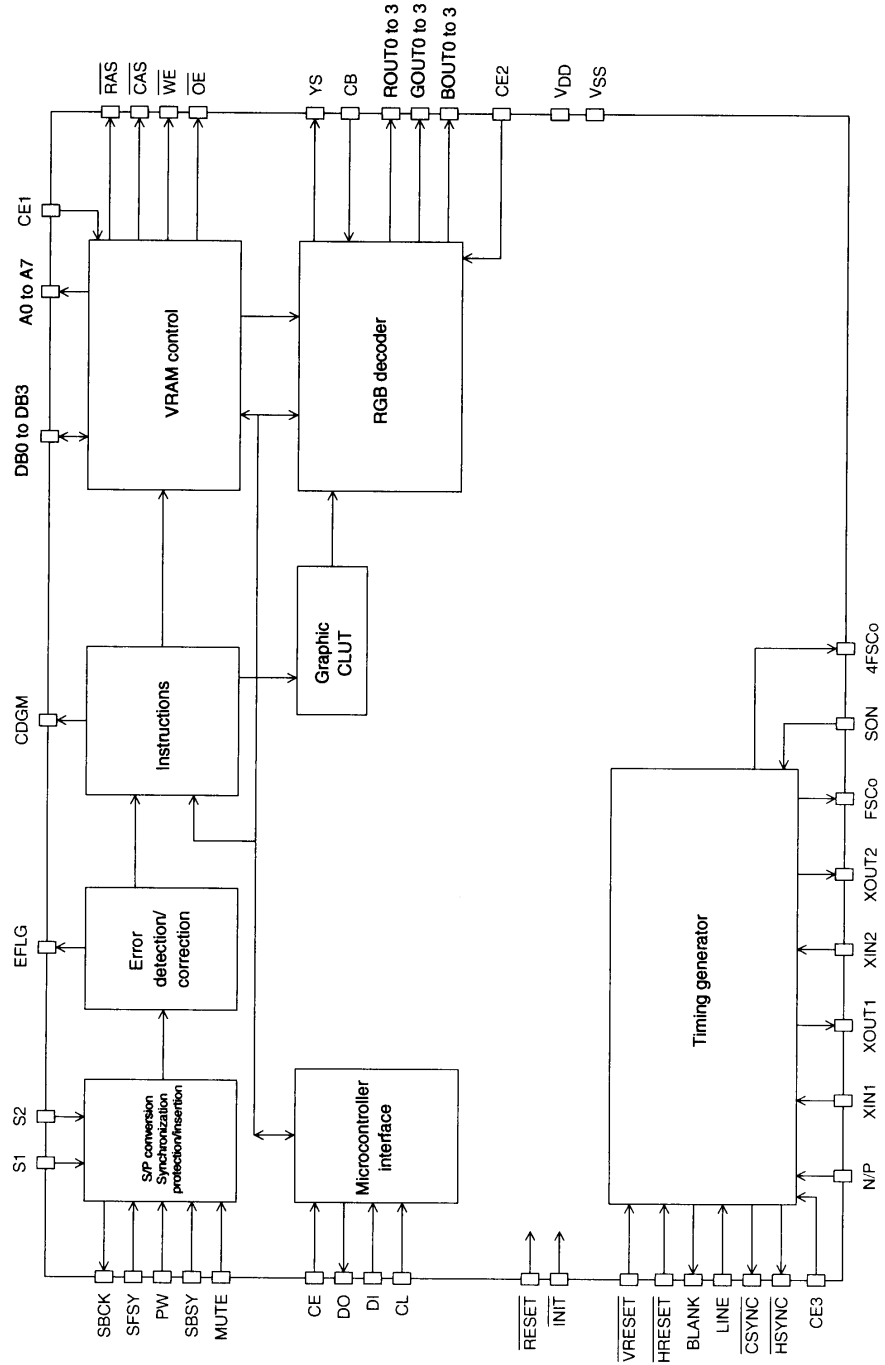
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Pin	Pin Symbol	Pin Name	I/O	Polarity	Function
35	$\overline{\text{HSYNC}}$	Horizontal synchronization output pin	3ST	Negative	Horizontal sync signal output
36	ROUT3	R data output pin	I/O	Positive	Video signal R3 data output
37	ROUT2	R data output pin	I/O	Positive	Video signal R2 data output
38	ROUT1	R data output pin	I/O	Positive	Video signal R1 data output
39	ROUT0	R data output pin	I/O	Positive	Video signal R0 data output
40	4FSC ₀	Clock output pin	3ST	Positive	4 × FSC clock output NTSC: 14.31818 MHz PAL: 17.734476 MHz
41	FSC ₀	Clock output pin	3ST	Positive	Subcarrier clock output NTSC: 3.579545 MHz PAL: 4.433619 MHz
42	GOUT3	G data output pin	I/O	Positive	Video signal G3 data output
43	GOUT2	G data output pin	I/O	Positive	Video signal G2 data output
44	GOUT1	G data output pin	I/O	Positive	Video signal G1 data output
45	GOUT0	G data output pin	I/O	Positive	Video signal G0 data output
46	BOUT3	B data output pin	I/O	Positive	Video signal B3 data output
47	BOUT2	B data output pin	I/O	Positive	Video signal B2 data output
48	BOUT1	B data output pin	I/O	Positive	Video signal B1 data output
49	BOUT0	B data output pin	I/O	Positive	Video signal B0 data output
50	CE2	Video output control input pin	In	Positive	Signal input setting video output pin to high impedance (MORE+ input)
51	CE3	Sync signal control input pin	In	Positive	Signal input setting sync signal output pin to high impedance (MORE+ input)
52	YS	Superimposition output pin	Out	Positive	Superimposition control output
53	EFLG	Error status monitor output pin	Out	Positive	Error status monitor signal output
54	$\overline{\text{HRESET}}$	External horizontal synchronization input pin	In	Negative	External horizontal synchronization timing control pin
55	LINE	Line number selection pin	In	—	Line number selection input NTSC : L = 263H, H = 262H PAL : H = 312H, L = 314H
56	$\overline{\text{VRESET}}$	External vertical synchronization input pin	In	Negative	External vertical synchronization timing control pin
57	$\overline{\text{INIT}}$	Initial input pin	In	Negative	System initial signal input
58	$\overline{\text{RESET}}$	Reset input pin	In	Negative	System reset signal input
59	N/P	NTSC/PAL selection input pin	In	Positive	NTSC/PAL selection input L: NTSC, H: PAL
60	SON	Superimposition control pin	In	Positive	Superimposition ON/OFF control input H: Superimposition ON
61	XIN2	Crystal oscillator connection pins	In	—	PAL crystal oscillator connection pin (4Fsc = 17.734476 MHz)
62	XOUT2		Out	—	
63	XIN1	Crystal oscillator connection pins	In	—	NTSC crystal oscillator connection pin (4Fsc = 14.31818 MHz)
64	XOUT1		Out	—	

Block Diagram



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CD-G Instructions

The contents of instructions in the CD Red Book which are supported by the LC7874E are as follows.

ZERO mode (MODE = 0, ITEM = 0)

LINE GRAPHICS mode (MODE = 1, ITEM = 0)

- ① INSTRUCTION (4): Write FONT
- ② INSTRUCTION (12): Write Scroll SCREEN

TV GRAPHICS mode (MODE = 1, ITEM = 1)

- ① INSTRUCTION (1): Preset MEMORY
- ② INSTRUCTION (2): Preset BORDER
- ③ INSTRUCTION (6): Write FONT FOREGROUND/BACKGROUND
- ④ INSTRUCTION (20): scroll SCREEN with preset
- ⑤ INSTRUCTION (24): scroll SCREEN with copy
- ⑥ INSTRUCTION (30): Load CLUT color-0 color-7
- ⑦ INSTRUCTION (31): Load CLUT color-8 color-15
- ⑧ INSTRUCTION (38): EXCLUSIVE-OR FONT

Outline of Functions

1. Crystal clock oscillation: XIN1, XOUT1, XIN2, XOUT2, N/P, 4FSCO, FSCO

XIN1 and XOUT1 are 14.31818 MHz (NTSC) crystal oscillator connection pins, and XIN2 and XOUT2 are 17.734476 MHz (PAL) crystal oscillator connection pins. Both modes can be supported by switching the N/P pin. The 4FSCO pin outputs the Xtal OSC clock, and the FSCO pin outputs this clock divided by 4. The pin functions in each mode are shown below.

XIN1, XOUT1	XIN2, XOUT2	N/P	TV system	4FSCO	FSCO
14.31818 MHz	*	L	NTSC/M	14.31818 MHz	3.579545 MHz
*	17.734476 MHz	H	PAL/GBIDH	17.734476 MHz	4.433619 MHz

2. Subcode interface: S1, S2, SBCK, SFSY, PW, SBSY

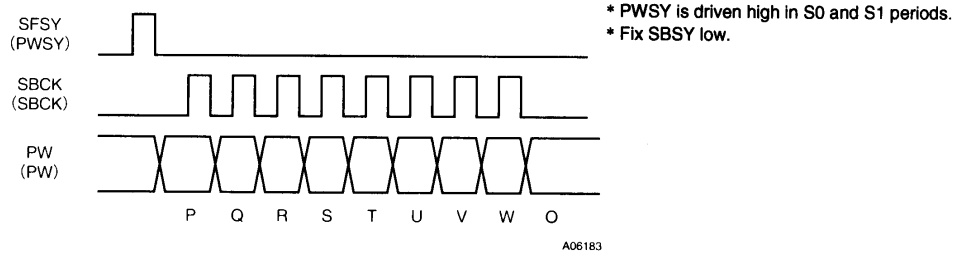
Control of the S1 and S2 pins provides interfacing with the following three modes. Driving the mute pin high disables SBSY and PW input and SBCK output.

S1	S2	Mode
L	L	LC7861N/67 interface
H	L	LC7860K/63 interface
H	H	LC78681/62X/63X interface

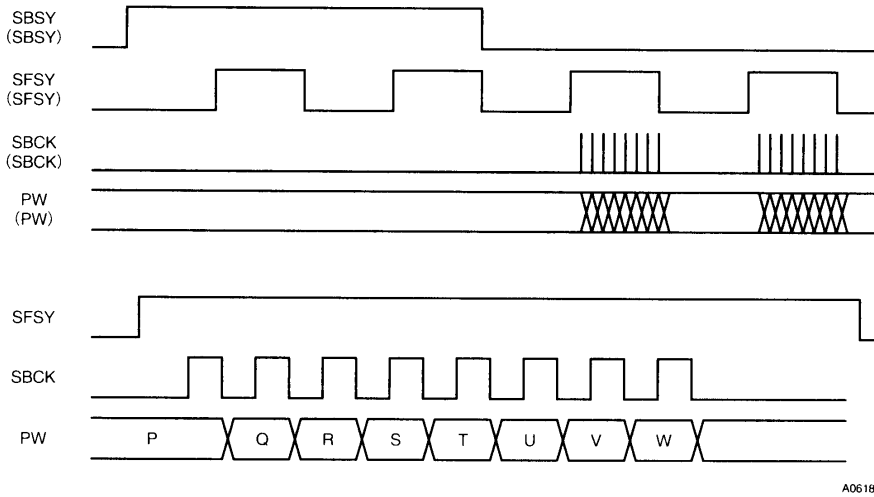
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With the LC7860K/63 interface, SBCK is transmitted when SFSY is confirmed to be low approximately 2.2 μ s after a falling edge of SFSY is detected. With other interfaces, SBCK is transmitted when SFSY is confirmed to be high and SBSY to be low approximately 2.2 μ s after a rising edge of SFSY is detected.

(1) LC7860 interface [DSP pin names shown in parentheses]



(2) LC7861N/67 interface [DSP pin names shown in parentheses]



(3) LC78681/62X/63X Series interface

Same as (2), except that the SBCK polarity is shifted inversely (shifted on rise of SBCK).

3. DRAM interface

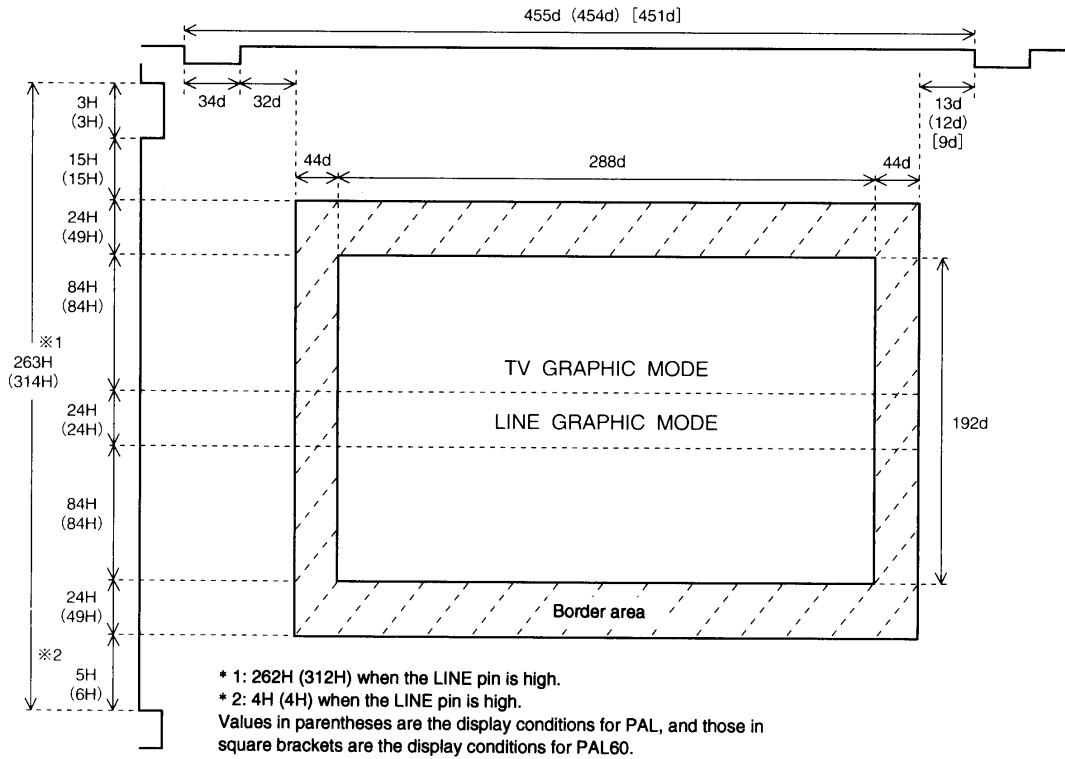
Interface pins: A0 to A7, DB0 to DB3, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$

64K \times 4-bit DRAM is connected externally. The interface pins are set to high impedance by driving the CE1 pin high. MPEG DRAM sharing is possible.

4. CD graphic monitor pin: CDGM

CDGM goes high once the LC7874E accepts any CD-G instruction. In the power-on state, once CDGM goes high it remains high. It can be driven low by driving the INIT pin low or transferring an INIT command from the microcontroller.

5. Display format

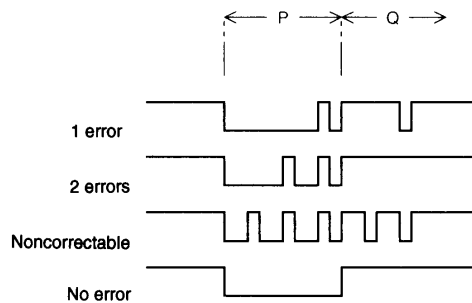


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6. Video output: ROUT0 to ROUT3, GOUT0 to GOUT3, BOUT0 to BOUT3

7. Error flag output: EFLG

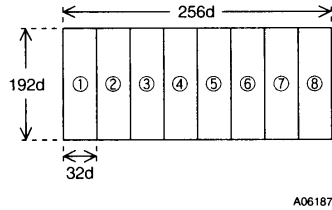
Error detection results can be monitored with the EFLG pin.



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8. Color bar output: CB

When the CB pin is driven high, color bars are output from the video output pins. Details of the color bars are shown below.



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	R	G	B
① White	F	F	F
② Gray	B	B	B
③ Yellow	F	F	O
④ Cyan	O	F	F
⑤ Green	O	F	O
⑥ Magenta	F	O	F
⑦ Red	F	O	O
⑧ Blue	O	O	F
BORDER (BLACK)	O	O	O

Drawing Functions (Graphic Functions)

1. Operating modes (scan operation, display operation)

NTSC mode

- Non-interlace 60 Hz (262 or 263 lines)
- Dot clock 2fsc: 7.15909 MHz (T = 139.67 ns)
- System clock 4fsc: 14.31818 MHz

PAL mode

- Non-interlace 50 Hz (312 or 314 lines)
- Dot clock 4fsc × 2/5: 7.09379 MHz (T = 140.97 ns)
- System clock 4fsc: 17.734476 MHz

PAL60 mode

- Non-interlace 60 Hz (262 or 263 lines)
- Dot clock 4fsc × 2/5: 7.09379 MHz (T = 140.97 ns)
- System clock 4fsc: 17.734476 MHz

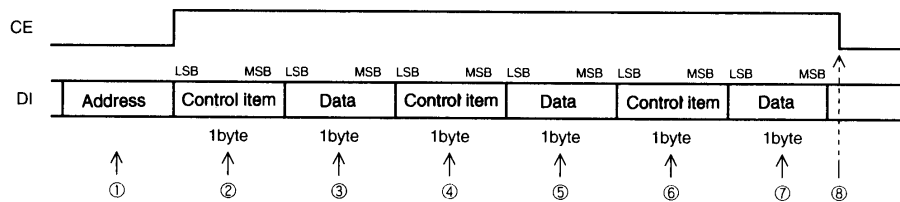
2. Display functions

- Display resolution 288 dots × 192H
- Image data area 300 dots × 216H
- 16-color display Selection of 16 colors from 4096

Microcontroller Interface (CCB)

1. Transfer format (for command transfer)

Transfer format (example)



- ① Address: F4_{HEX}
- ② ④ ⑥ Command identification code (control item)
- ③ ⑤ ⑦ Command register setting data
- ⑧ End of serial transfer

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Display Control Command Table

Command	First byte								Second byte							
	MSB Command identification code LSB								MSB							LSB
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Register 00HEX (Various mode settings)	0	0	0	0	0	0	0	0	INIT	SCP ₂	SCP ₁	SCP ₀	CB	DISK /GPH	TV/ LINE	VRAM /BG
Register 10HEX (Fine adjustment of screen position)	0	0	0	1	0	0	0	0	VP ₃	VP ₂	VP ₁	VP ₀	HP ₃	HP ₂	HP ₁	HP ₀
Register 20HEX (Channel 0 to 7 ON/OFF)	0	0	1	0	0	0	0	0	CH ₇	CH ₆	CH ₅	CH ₄	CH ₃	CH ₂	CH ₁	CH ₀
Register 30HEX (Channel 8 to 15 ON/OFF)	0	0	1	1	0	0	0	0	CH ₁₅	CH ₁₄	CH ₁₃	CH ₁₂	CH ₁₁	CH ₁₀	CH ₉	CH ₈
Register 40HEX (BGC R, G settings)	0	1	0	0	0	0	0	0	BGG ₃	BGG ₂	BGG ₁	BGG ₀	BGR ₃	BGR ₂	BGR ₁	BGR ₀
Register 50HEX (BGC B setting)	0	1	0	1	0	0	0	0	0	0	0	0	BGB ₃	BGB ₂	BGB ₁	BGB ₀
Register 60HEX (Chroma key color R, G settings)	0	1	1	0	0	0	0	0	CKG ₃	CKG ₂	CKG ₁	CKG ₀	CKR ₃	CKR ₂	CKR ₁	CKR ₀
Register 70HEX (Chroma key color B setting)	0	1	1	1	0	0	0	0	0	0	0	0	CKB ₃	CKB ₂	CKB ₁	CKB ₀
Register 80HEX (YS output phase adjustment)	1	0	0	0	0	0	0	0	CSY SEL	PAL 60	0	YT ₄	YT ₃	YT ₂	YT ₁	YT ₀
Register 90HEX (External synchronization mode, test mode)	1	0	0	1	0	0	0	0	CV SEL	MVMD	EXSN	HVMK	0	TST ₂	TST ₁	TST ₀
Register A0HEX (Subtitle scroll: vertical)	1	0	1	0	0	0	0	0	0	0	0	SCV ₄	SCV ₃	SCV ₂	SCV ₁	SCV ₀
Register B0HEX (Subtitle scroll: horizontal)	1	0	1	1	0	0	0	0	0	0	SCH ₅	SCH ₄	SCH ₃	SCH ₂	SCH ₁	SCH ₀
Register 01HEX (19-byte command input)	0	0	0	0	0	0	0	1	R	S	T	U	V	W	0	0

Description of Commands

Command transmission should be performed LSB-first.

- Control item code 00_{HEX}: Various mode settings
Default: MSB [01100000] LSB

Data 0: VRAM/BG Display screen switchover setting
0: VRAM contents displayed
1: Background color displayed

Data 1: TV/LINE Graphic display mode setting
0: TV graphic mode
1: LINE graphic mode

Data 2: DISK/GPH Disk command acceptance control
0: DISK command only accepted
1: DISK command acceptance ignored, MGC (Micro graphic command) only accepted

Data 3: CB Color bar screen output setting
0: Graphic signal output
1: Color bar signal output

Data 4: SCP0 YS output (pin 52) control

Data 5: SCP1 Superimposition compare condition (valid only when SON = 1: pin 60)

SCP1	SCP0	Compare condition
0	0	Comparison not performed
1	0	When border color is black, YS is high (display) in the parts whose color does not match the border color, and low (transparent) otherwise
1	1	High in parts whose color does not match the chroma key color; low otherwise

Data 6: SCP2 YS output (pin 52) control
0: When SCP0, SCP1 = 0, 0; 0, 1, and compare condition is not satisfied, setting is full-screen low (transparent)
1: L: When SCP0, SCP1 = 0, 0; 0, 1, and compare condition is not satisfied, setting is full-screen high (display)

Data 7: INIT Software reset setting
0: Internal reset not executed (normal)
1: Internal reset executed (display screen becomes blue background screen)

- Control item code 10_{HEX}: Fine adjustment of screen position
Default: MSB [00000000] LSB

Data 0: HP0 Horizontal fine adjustment of screen position
Data 1: HP1 Specified as two's complement with left as positive direction
Data 2: HP2 (variable by -16 to +14 dots from center in 2-dot units)
Data 3: HP3
Data 4: VP0 Vertical fine adjustment of screen position
Data 5: VP1 Specified as two's complement with up as positive direction
Data 6: VP2 (variable by -16 to +14 dots from center in 2-dot units)
Data 7: VP3

3. Control item code 20_{HEX}: Channel on/off setting
Default: MSB [0000011] LSB
Data 0: CH0 CH0 to CH7 on/off setting
Data 1: CH1
Data 2: CH2 0: Channel off
Data 3: CH3 1: Channel on
Data 4: CH4
Data 5: CH5
Data 6: CH6
Data 7: CH7

4. Control item code 30_{HEX}: Channel on/off setting
Default: MSB [0000000] LSB
Data 0: CH8 CH8 to CH15 on/off setting
Data 1: CH9
Data 2: CH10 0: Channel off
Data 3: CH11 1: Channel on
Data 4: CH12
Data 5: CH13
Data 6: CH14
Data 7: CH15

5. Control item code 40_{HEX}: BGC color (R, G) settings
Default: MSB [0000000] LSB
Data 0: BCR0 BGC color: R setting = 16 kinds
Data 1: BCR1
Data 2: BCR2
Data 3: BCR3
Data 4: BCG0 BGC color: G setting = 16 kinds
Data 5: BCG1
Data 6: BCG2
Data 7: BCG3

6. Control item code 50_{HEX}: BGC color (B) setting
Default: MSB [00001010] LSB
Data 0: BCB0 BGC color: B setting = 16 kinds
Data 1: BCB1
Data 2: BCB2
Data 3: BCB3 * R, G, B, 16 kinds each; selection of 1 color from 4096
Data 4 to data 8: Fixed at 0

7. Control item code 60_{HEX}: Chroma key color (R, G) settings
Default: MSB [0000000] LSB
Data 0: CKR0 Chroma key color: R setting = 16 kinds
Data 1: CKR1
Data 2: CKR2
Data 3: CKR3
Data 4: CKG0 Chroma key color: G setting = 16 kinds
Data 5: CKG1
Data 6: CKG2
Data 7: CKG3

8. Control item code 70_{HEX}: Chroma key color (B) setting
 Default: MSB [00000000] LSB
 Data 0: CKB0 Chroma key color: B setting = 16 kinds
 Data 1: CKB1
 Data 3: CKB3 * R, G, B, 16 kinds each; selection of 1 color from 4096
 Data 4 to data 8: Fixed at 0
9. Control item code 80_{HEX}: YS signal output/video signal output phase adjustment data setting
 Default: MSB [00000000] LSB
 Data 0: YT0 YS signal output/video signal output phase adjustment data
 Data 1: YT1
 Data 2: YT2
 Data 3: YT3
 Data 4: YT4
 Data 5: Fixed at 0
 Data 6: PAL60 PAL/PAL60 setting (valid only when N/P = 1)
 0: PAL
 1: PAL60
 Data 7: CSYSEL CSYNC output addressing (autonomous mode only)
 0: Equalization pulses used
 1: No equalization pulses
10. Control item code 90_{HEX}: External synchronization control, test mode setting
 Default: MSB [00000000] LSB
 Data 0: TST0 Test mode addressing (normally fixed low)
 Data 1: TST1
 Data 2: TST2
 Data 3: Fixed at 0
 Data 4: HVMK $\overline{\text{HRESET}}$, $\overline{\text{VRESET}}$ mask
 0: Mask used
 1: No mask
 Data 5: EXSN Sync signal rest control setting when using external clock (when SON = 1)
 0: Reset executed with $\overline{\text{HRESET}}$ (pin 54) and $\overline{\text{VRESET}}$ (pin 56) signals
 0: Reset executed with $\overline{\text{VRESET}}$ (pin 56) signal ($\overline{\text{HRESET}}$ signal unnecessary)
 Data 6: MVMD Moving display area setting
 0: Movement of display area only
 1: Border area included in movement (only horizontal movement possible)
 Data 7: CVSEL $\overline{\text{CSYNC}}$ output pin setting
 0: $\overline{\text{CSYNC}}$ output
 1: $\overline{\text{VSYNC}}$ output
11. Control item code A0_{HEX}: Superimposed text scroll amount, vertical setting
 Default: MSB [00000000] LSB
 Data 0: SCV0 Upward scroll amount (font unit) setting (scroll amount: 0 to 17 font units)
 Data 1: SCV1 Screen display position scrolled vertically by 1 font unit
 Data 2: SCV2 (1 font unit: 12 vertical dots (12H))
 Data 3: SCV3
 Data 4: SCV4
 Data 5 to data 7: Fixed at 0

12. Control item code C0_{HEX}: Superimposed text scroll amount, horizontal setting

Default: MSB [00000000] LSB

Data 0: SCH0 Left scroll amount (font unit) setting (scroll amount: 0 to 49-font units)

Data 1: SCH1 Screen display position scrolled horizontally in 1-font unit

Data 2: SCH2 (1-font unit: 6 horizontal dots)

Data 3: SCH3

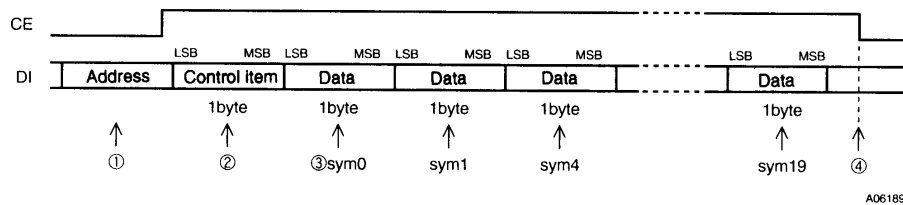
Data 4: SCH4

Data 5: SCH5

Data 6, data 7: Fixed at 0

13. Control item code 01_{HEX}: 19-byte command input (MGC write)

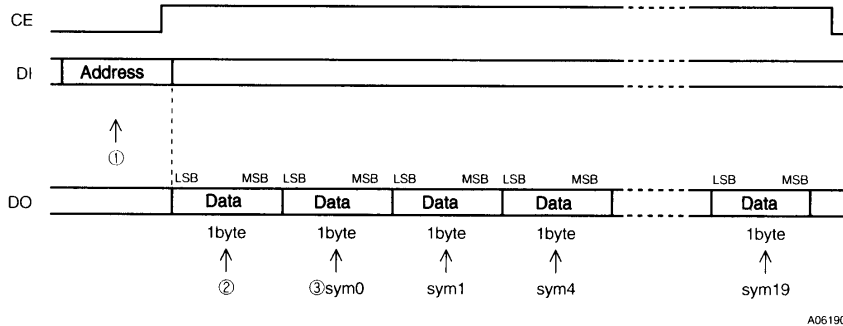
Transfer format



- ① Address: F4_{HEX}
- ② Control item: 01_{HEX}
- ③ sym0 to sym19: R to W = subcode input
- ④ Executed on fall

14. Control item code 11_{HEX}: 19-byte command input (pack data read)

Transfer format



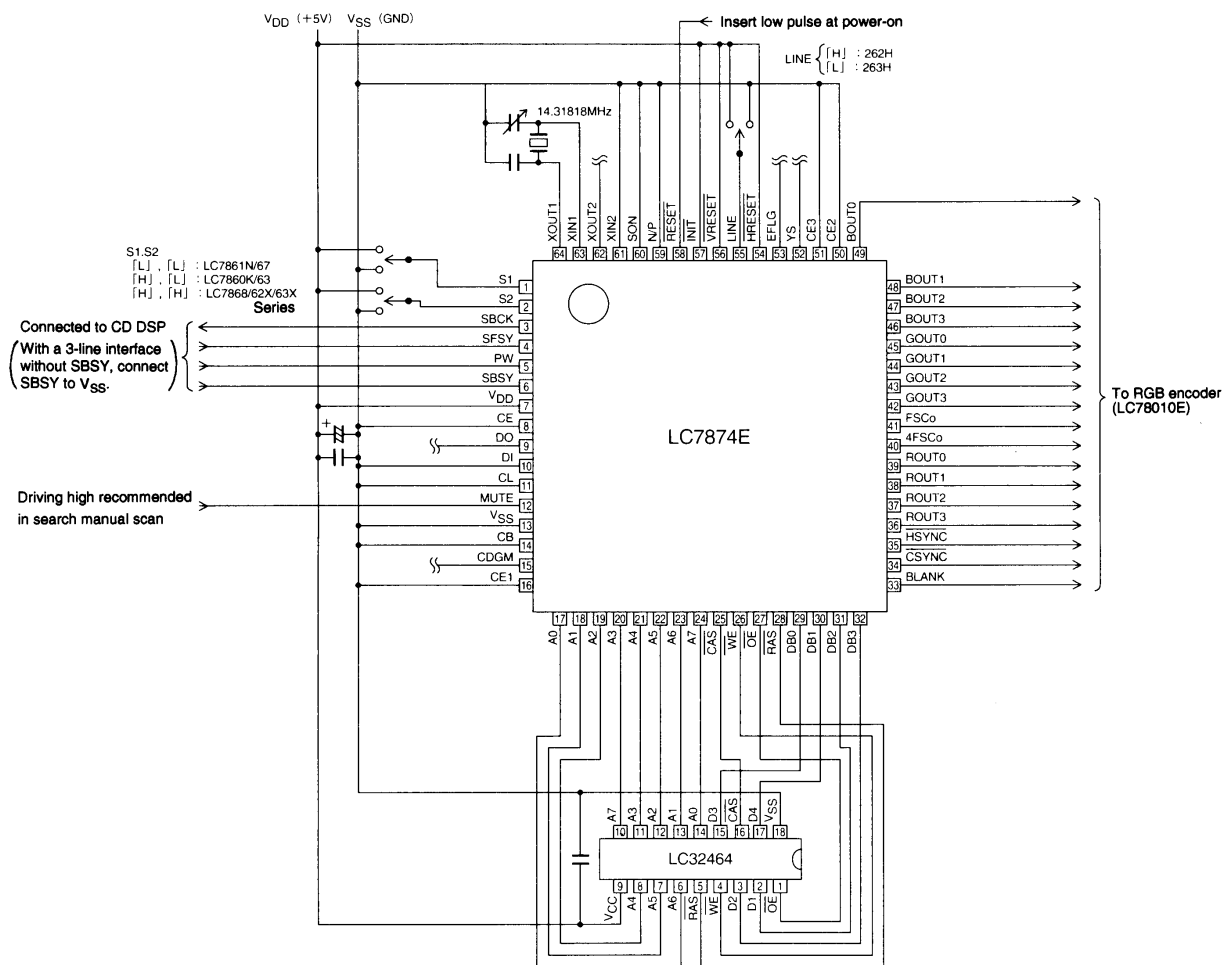
- ① Address: F5_{HEX}
 - ② Data (check flags)
- MSB [PF1, PF0, QF1, QF0, DKMD, VBLK, EXEC, OE] :LSB
- Data 0: OE 1 when the next 18 bytes are guaranteed and are the first data to be read.
 * Note: Reading must be completed within 1.1 ms after OE output setting.
- Data 1: EXEC Command status
 0: Command executing
 1: Command wait state
- Data 2: VBLK 1 output during vertical blanking (vertical retrace line) period
 Vertical retrace line period NTSC: 19H
 PAL: 25H
- Data 3: DKMD Disk identification flag
 0: CD
 1: CD-G

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Data 4: QF0 QF0 error correction Q flag data
 Data 5: QF1 QF1 error correction Q flag data
 Data 6: PF0 PF0 error correction P flag data
 Data 7: PF1 PF1 error correction Q flag data

③ sym0, 1, 4 to 19: R to W = subcode input
 MSB [R, S, T, U, V, W, 0, 0] LSB

Sample Application Circuit : NTSC



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