Ordering number: EN4001B

CMOS LSI

No.4001B

LC7867E

Digital Signal Processor for Compact Disc Players

OVERVIEW

The LC7867E is a digital signal processor (DSP) and servocontroller for compact disc players. It performs most of the signal processing and decoding for replay of audio compact discs and other compact-disc formats, including compact disc video (CD-V), compact disc interactive (CD-I) and compact disc read-only memory (CD-ROM).

The LC7867E functions include bit detection, EFM (eight-to-fourteen modulation) demodulation, signal decoding and deinterleaving, error detection and correction, and disc motor servo control. The LC7867E interfaces directly to 16-bit stereo DACs and features an EIAJ-format digital audio serial output and an output interface for non-audio applications such as CD-ROM.

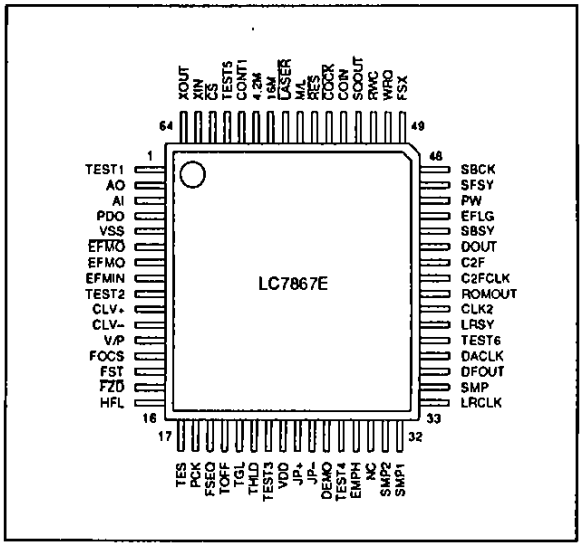
The LC7867E is controlled by an external microprocessor through a serial interface. The microprocessor controls functions such as track counting, track jumping, laser focusing, disc motor operation and audio muting. The DSP has a DEMO input which controls the automatic operation mode used during unit calibration to produce audio output without microprocessor intervention.

The LC7867E operates from a 5 V supply and is available in 64-pin QIPs.

FEATURES

- Disc motor servocontroller
- Laser focusing and tracking servocontrollers
- Track count and track jump functions
- 16-bit stereo DAC serial interface
- CD-ROM serial interface
- EIAJ-format digital audio serial interface
- Subcode bits and Q subcode outputs
- Error detection and correction
- Signal interpolation or previous-value hold if error correction fails
- ±4 frames jitter tolerance
- Single crystal for reference clock and all timing signals
- DEMO mode for automatic operation
- Supports double-speed dubbing
- 5 V supply
- 64-pin QIP

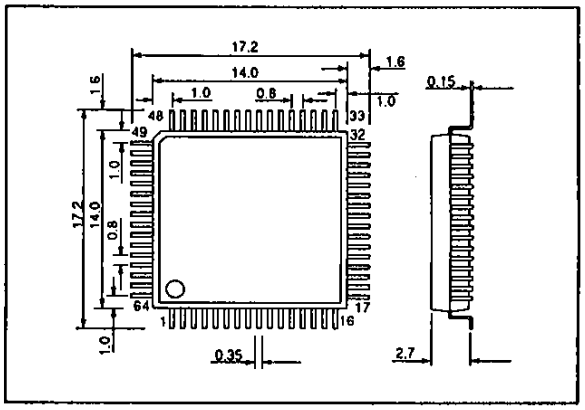
PINOUT



PACKAGE DIMENSIONS

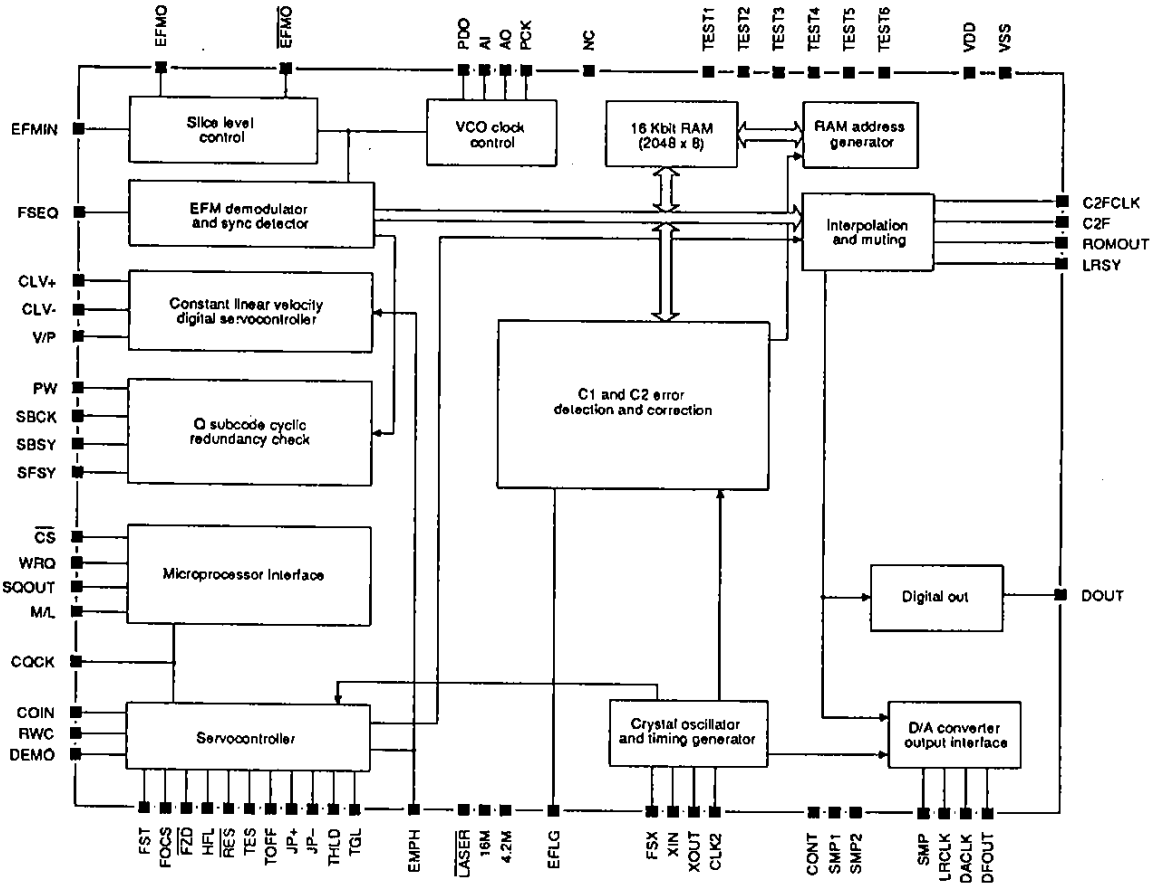
Unit: mm

3159-QIP64E



SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	TEST1	Test input 1
2	AO	8.6436 MHz PLL output
3	AI	8.6436 MHz PLL input
4	PDO	Phase detector output
5	VSS	Ground
6	$\overline{\text{EFMO}}$	EFM signal complementary outputs
7	EFMO	
8	EFMIN	HF signal input
9	TEST2	Test input 2
10	CLV+	Disc motor control outputs
11	CLV–	
12	V/P	Disc motor control mode indicator output
13	FOCS	Focus servocontroller outputs
14	FST	
15	$\overline{\text{FZD}}$	Focus servocontroller input

Number	Name	Description
16	HFL	Track count and track jump circuit inputs
17	TES	
18	PCK	4.3218 MHz PCK monitor output
19	FSEQ	Frame sync detector output
20	TOFF	Track count and track jump circuit outputs
21	TGL	
22	THLD	
23	TEST3	Test input 3
24	VDD	5 V supply
25	JP+	Track jump kick-pulse outputs
26	JP–	
27	DEMO	Automatic operation control input
28	TEST4	Test input 4
29	EMPH	Disc preemphasis indicator output
30	NC	No connection
31	SMP2	Stereo, 16-bit DAC serial interface data, clock and control outputs
32	SMP1	
33	LRCLK	
34	SMP	
35	DFOUT	
36	DACLK	
37	TEST6	Test output 6
38	LRSY	CD-ROM interface clock output
39	CLK2	CD-ROM interface clock output
40	ROMOUT	CD-ROM interface data output
41	C2FCLK	CD-ROM interface C2-flag clock output
42	C2F	CD-ROM interface C2-flag output
43	DOUT	EIAJ-format digital audio serial output
44	SBSY	Subcode block synchronization output
45	EFLG	Error detection and correction error flag output
46	PW	Subcode data output
47	SFSY	Subcode frame synchronization output
48	SBCK	Subcode data clock input
49	FSX	7.35 kHz synchronization output
50	WRQ	Q subcode status output
51	RWC	Q subcode read and command write control input
52	SQOUT	Q subcode data output
53	COIN	Command input
54	$\overline{\text{CQCK}}$	Q subcode and command clock input

Number	Name	Description
55	$\overline{RES}$	Active-LOW reset input
56	M/L	Q subcode output msb-first/lsb-first select input
57	$\overline{LASER}$	Laser control output
58	16M	16.9344 MHz clock output
59	4.2M	4.2336 MHz clock output
60	CONT	General-purpose output
61	TEST5	Test input 5
62	$\overline{CS}$	Active-LOW chip select input
63	XIN	16.9344 MHz crystal connections
64	XOUT	

SPECIFICATIONS

Absolute Maximum Ratings

T_a = 25 °C, V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	V_{SS} – 0.3 to 7	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	300	mW
Operating temperature range	Topr	–30 to 75	°C
Storage temperature range	T_{stg}	–40 to 125	°C

Recommended Operating Conditions

T_a = 25 °C, V_{SS} = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5	–	5.5	V
HIGH-level input voltage	V_{IH1}	TEST1 to 5, AI, $\overline{FZD}$, HFL, DEMO, M/L, $\overline{RES}$	0.7V_{DD}	–	V_{DD}	V
	V_{IH2}	SBCK, RWC, COIN, $\overline{COCK}$, $\overline{CS}$	2.2	–	V_{DD}	V
	V_{IH3}	EFMIN	0.6V_{DD}	–	V_{DD}	V
	V_{IH4}	TES	0.8V_{DD}	–	V_{DD}	V
LOW-level input voltage	V_{IL1}	TEST1 to 5, AI, $\overline{FZD}$, HFL, DEMO, M/L, $\overline{RES}$	V_{SS}	–	0.3V_{DD}	V
	V_{IL2}	SBCK, RWC, COIN, $\overline{COCK}$, $\overline{CS}$	V_{SS}	–	0.8	V
	V_{IL3}	EFMIN	V_{SS}	–	0.4V_{DD}	V
	V_{IL4}	TES	V_{SS}	–	0.2V_{DD}	V
Data setup time	t_{setup}	COIN, RWC, Command input timing	400	–	–	ns

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Data hold time	t_{hold}	RWC, Command input timing	400	–	–	ns
HIGH-level clock pulsewidth	$t_{W\phi H}$	SBCK, $\overline{CQCK}$, Command input timing, Subcode Q output timing, Subcode output timing	400	–	–	ns
LOW-level clock pulsewidth	$t\phi L$	SBCK, CQCK, Command input timing, Subcode Q output timing, Subcode output timing	400	–	–	ns
Data read access time	t_{RAC}	Subcode Q output timing, Subcode output timing	0	–	400	ns
Command output time	t_{RWC}	RWC, Command input timing	1000	–	–	ns
Subcode Q read output enable time	t_{SQE}	Subcode Q output timing, no RWC signal	–	11.2	–	ms
Subcode Q read output cycle	t_{sc}	Subcode output timing	–	136	–	µs
Subcode read output enable	t_{se}	Subcode ouput timing	400	–	–	ns
Crystal (X'tal) frequency	$f_{X'tal}$	XIN, XOUT	–	16.9344	–	MHz
Operating frequency range	f_{op1}	AI	2.0	–	20	MHz
	f_{op2}	EFMIN, $V_{IN} \geq 1\ V_{P-P}$	–	–	10	MHz

Electrical Characteristics

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}		–	17	30	mA
HIGH-level input current	I_{IH1}	AI, EFMIN, $\overline{FZD}$, TES, SBCK, COIN, $\overline{CQCK}$, $\overline{RES}$, RWC, M/$\overline{L}$: $V_{IN} = V_{DD}$	–	–	5	µA
	I_{IH2}	TEST1 to 5, DEMO, $\overline{CS}$: $V_{IN} = V_{DD} = 5.5$ V	25	–	75	µA
LOW-level input current	I_{IL1}	AI, EFMIN, $\overline{FZD}$, TES, SBCK, COIN, $\overline{CQCK}$, $\overline{RES}$, RWC, M/$\overline{L}$: $V_{IN} = V_{SS}$	–5	–	–	µA
HIGH-level output voltage	V_{OH1}	AO, PDO, EFMO, $\overline{EFMO}$, CLV+, CLV−, FOCS, FSEQ, PCK, TOFF, TGL, THLD, JP+, JP−, EMPH, EFLG, FSX, V/P: $I_{OH} = -1$ mA	$V_{DD} - 1$	–	–	V
	V_{OH2}	DOUT: $I_{OH} = -12$ mA	$V_{DD} - 0.5$	–	–	V
	V_{OH3}	$\overline{LASER}$, SQOUT, 16M, 4.2M, CONT, SMP, SMP1, SMP2, LRCLK, WRQ, C2F, DFOUT, DACLK, SFSY, LRSY, SBSY, CK2, PW, ROMOUT, C2FCLK: $I_{OH} = -0.5$ mA	$V_{DD} - 1$	–	–	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LOW-level output voltage	V_{OL1}	AO, PDO, EFMO, $\overline{EFMO}$, CLV+, CLV-, FOCS, FSEQ, PCK, TOFF, TGL, THLD, JP+, JP-, EMPH, EFLG, FSX, V/P: I_{OL} = 1 mA	–	–	1	V
	V_{OL2}	DOUT: I_{OL} = 12 mA	–	–	0.5	V
	V_{OL3}	$\overline{LASER}$, SQOUT, 16M, 4.2M, CONT, SMP, SMP1, SMP2, LRCLK, WRQ, C2F, DFOUT, DACLK, SFSY, LRSY, SBSY, CK2, PW, ROMOUT, C2FCLK: I_{OL} = 2 mA	–	–	0.4	V
	V_{OL4}	FST: I_{OL} = 5 mA	–	–	0.75	V
Output off leakage current	I_{OFF1}	PDO, FST: $V_{OH} = V_{DD}$	–	–	5	μA
	I_{OFF2}	PDO, FST: $V_{OL} = V_{SS}$	–5	–	–	μA

FUNCTIONAL DESCRIPTION

Threshold Level Control (EFMIN, EFMO, $\overline{EFMO}$)

The 1 to 2 V_{p-p} HF signal from the optical pickup is input on EFMIN. It is converted to an NRZ signal by a zero-crossing Schmitt-trigger. The EFMIN signal DC level is adjusted to ensure zero crossings are detected correctly using the threshold level control circuit shown in figure 1.

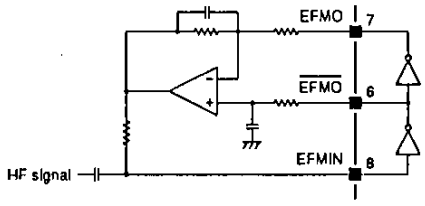


Figure 1. HF input circuit

Clock Regeneration PLL (PDO, AI, AO)

A PLL comprising a VCO can be built with an LA9210 as shown in figure 2. PDO goes positive when the VCO phase lags the NRZ EFM signal. PDO should be connected such that a positive output causes an increase in VCO frequency.

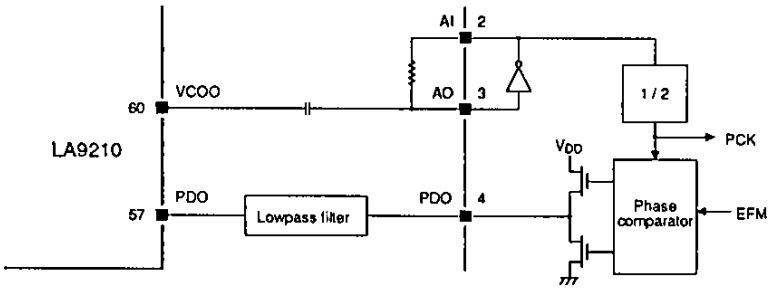


Figure 2. PLL circuit

VCO Half-frequency Clock (PCK)

The VCO output frequency is divided by two and output on PCK.

Frame Sync Detector Output (FSEQ)

FSEQ is latched HIGH for one frame when the frame sync recovered from the EFM signal matches the sync timing generated by an internal counter.

Constant Linear Velocity Servocontroller (CLV+, CLV–, V/P)

The disc motor accelerates when CLV+ is HIGH, and decelerates, when CLV– is HIGH. These outputs are set by the motor mode commands issued by the microprocessor as shown in table 1. The disc motor control circuit is shown in figure 3.

Table 1. Motor mode commands

Code								Command	CLV+	CLV–
0	0	0	0	0	1	0	0	Accelerate	HIGH	LOW
0	0	0	0	0	1	0	1	CLV	See table 2.	See table 2.
0	0	0	0	0	1	1	0	Decelerate	LOW	HIGH
0	0	0	0	0	1	1	1	Stop	LOW	LOW

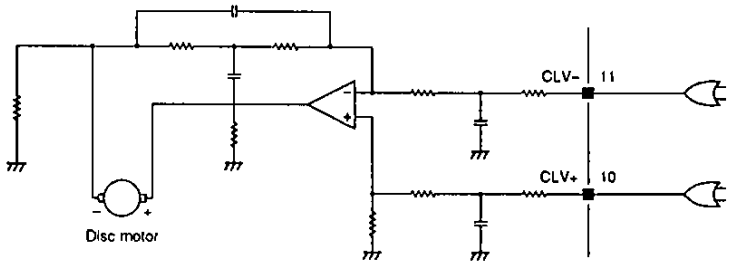


Figure 3. Disc motor control circuit

In CLV (constant linear velocity) mode, the LC7867E calculates the disc speed from the EFMIN signal and switches between the internal modes, shown in table 2, to maintain correct disc linear velocity.

Table 2. Constant linear velocity modes

Internal mode	Condition	CLV+	CLV–	V/P
Rough servo	Velocity too low	HIGH	LOW	HIGH
	Velocity too high	LOW	HIGH	HIGH
Phase control	Velocity is correct. PCK is locked to EFMIN.	PWM	PWM	LOW
Low-speed rotation	No EFMIN signal	1/64 duty cycle	LOW	HIGH

When the correct velocity is reached, phase-control mode is activated. In phase-control mode, CLV+ and CLV– are pulsewidth modulated at 7.35 kHz to constantly fine tune the disc speed.

In low-speed rotation mode, the 1/64 duty cycle period is 1.114 s.

Notes

1. TOFF is always HIGH, except when the CLV servocontrol command is in CLV mode.
2. The TOFF output command is only valid in CLV mode.

Subcode Output Circuit (PW, SBSY, SFSY, SBCK)

SBSY outputs a cycle for every subcode block as shown in figure 4. It is HIGH during the S0 and S1 synchronization cycles. Its falling edge indicates the end of synchronization and the start of EIAJ-format data within the subcode block.

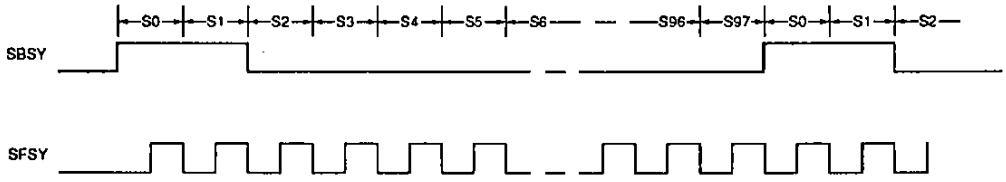


Figure 4. Subcode block synchronization

The rising edge of SFSY indicates that subcode bits P to W are ready for output. The falling edge starts the 136 µs period during which the subcode bits are output. The subcode bits from PW are clocked on the falling edge of SBCK. When SBCK is static, PW has the P bit value as shown in figure 5.

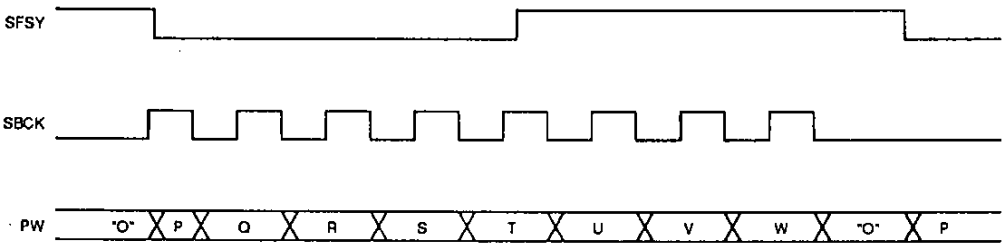


Figure 5. Subcode output

Q Subcode Channel Output (WRQ, RWC, SQOUT, $\overline{CQCK}$, M/L, $\overline{CS}$)

The LC7867E extracts a 98-bit subcode block from the Q subcode channel over 98 consecutive frames, one bit per frame. The Q subcode channel data is used for track access and display. The data format is shown in figure 6.

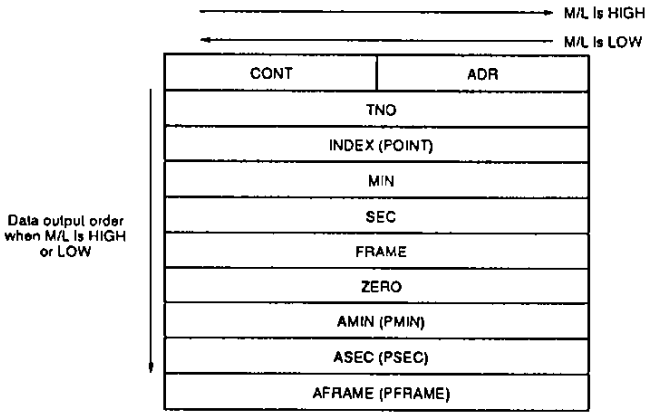


Figure 6. Q subcode channel data format

Note

Items in parentheses apply in disc lead-in area

The signal waveforms during the period when the microprocessor is reading channel data are shown in figure 7.

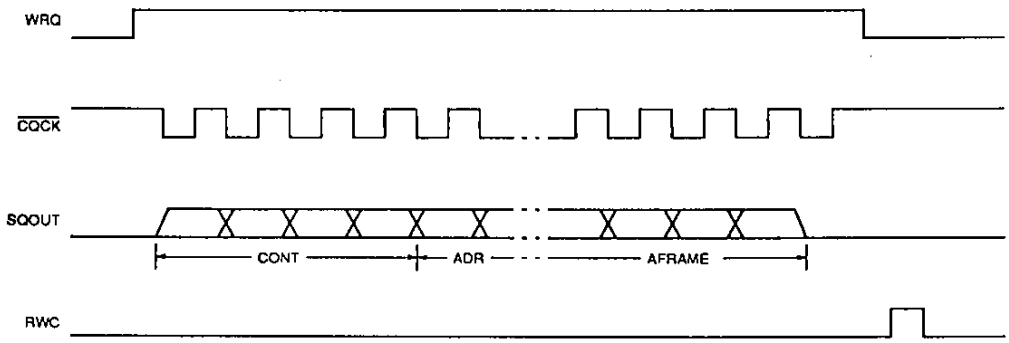


Figure 7. Q subcode output waveforms

Note

- WRQ usually indicates the state of the subcode Q. However, in track count mode its function changes. (See the Track Count Circuit section.)
- When $\overline{CS}$ is LOW, the LC7867E chip is selected and the output appears on SQOUT. When $\overline{CS}$ is HIGH, SQOUT is high impedance.

The subcode data is ready to be read when WRQ goes HIGH. WRQ goes HIGH only when the block CRC is correct and the subcode address equals 1. The subcode address is ignored if the Address Free command has previously been issued.

The Address Free command is used in CD-V applications. It is one of only two Q subcode address commands as shown in table 3.

Table 3. Q subcode address commands

Code								Command
0	0	0	0	1	0	0	1	Address Free*
1	0	0	0	1	0	0	1	Address 1*

* New command

When WRQ goes HIGH and $\overline{CQCK}$ starts to oscillate, the microprocessor reads the data from SQOUT on the falling edge of $\overline{CQCK}$. $\overline{CQCK}$ should start to oscillate in the 11.2 ms period during which WRQ is HIGH. $\overline{CS}$ should be held LOW when data is output, as SQOUT is in the high-impedance state when $\overline{CS}$ is HIGH. The data bit order is msb first when M/L is HIGH, and lsb first, when M/L is LOW.

When $\overline{CQCK}$ is activated, the DSP disables internal register updating and holds WRQ HIGH. When the microprocessor finishes reading data, it briefly sets RWC HIGH to re-enable register updating and resets WRQ LOW. (See the Track Count Circuit description for WRQ operation in track count mode.)

Servocontroller (RWC, COIN, $\overline{CQCK}$, $\overline{CS}$)

A command is issued to the DSP on COIN, on the falling edge of $\overline{CQCK}$, when RWC is HIGH and $\overline{CS}$ is LOW. The command is executed on the falling edge of RWC. Note that the LC7867E interface is active only when $\overline{CS}$ is LOW.

The LC7867E command set is compatible with those of existing LC7860N and LC7863 devices. All commands except the track count commands are 1 byte long. The 1- and 2-byte command input waveforms are shown in figures 8 and 9, respectively.

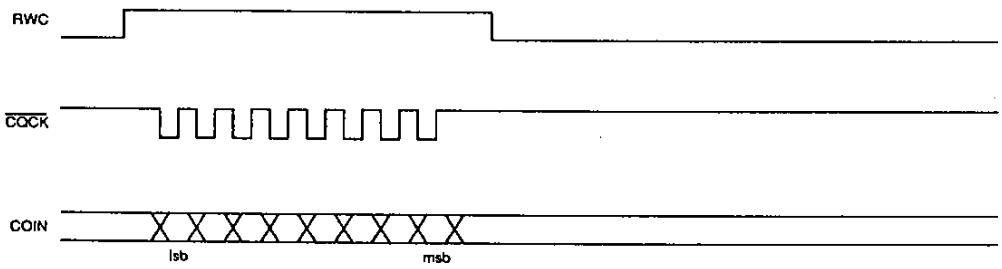


Figure 8. 1-byte command input

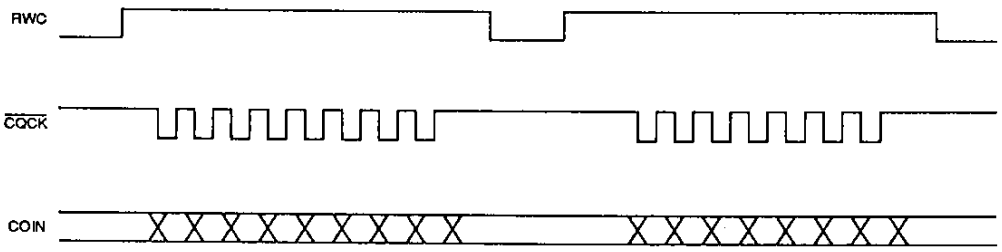


Figure 9. 2-byte command input

Focus Servocontroller (FOCS, FST, $\overline{FZD}$, $\overline{LASER}$)

The focus servo commands, focus start waveforms and focus servo circuit are shown in table 4 and figures 10 and 11, respectively.

Table 4. Focus servo commands

Code								Command
0	0	0	0	1	0	0	0	Focus Start 1
1	0	1	0	0	0	1	0	Focus Start 2*
0	0	0	0	1	0	1	0	Laser ON*
1	0	0	0	1	0	1	0	Laser OFF*

* New command

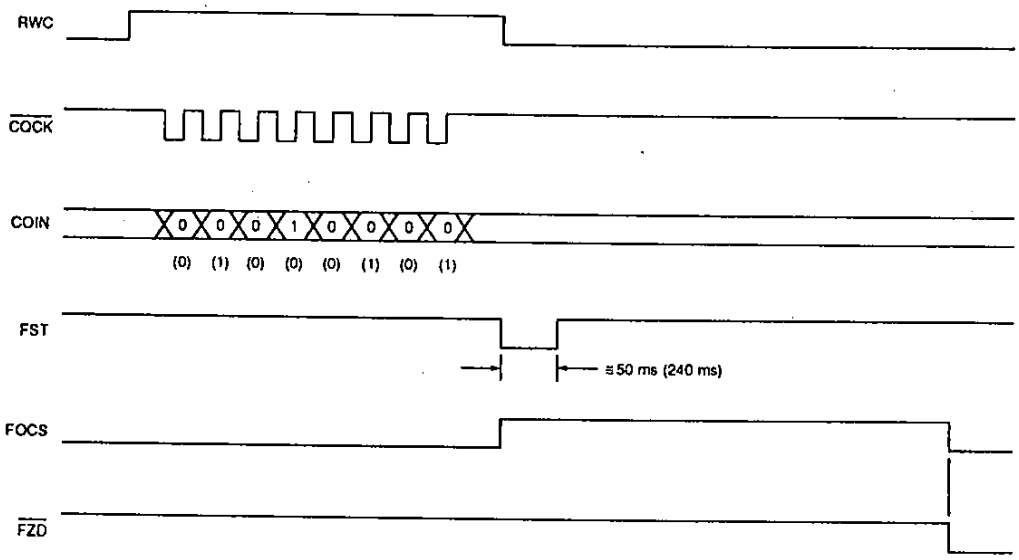


Figure 10. Focus start waveforms

Notes

1. Items in parentheses apply to the Focus Start 2 command.
2. HIGH-to-LOW transitions on $\overline{FZD}$ while FST is LOW are ignored.

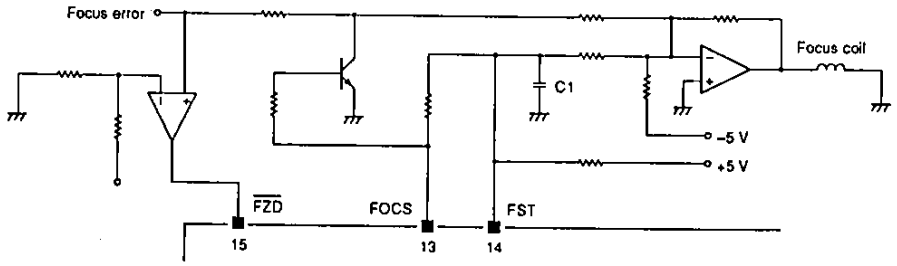


Figure 11. Focus servo circuit

When a Focus Start command is issued, the pickup lens is first lowered as C1 discharges through FST and then raised as C1 gradually recharges. $\overline{FZD}$ goes LOW when the focal point is reached, resetting FOCS and turning ON the focus servocontroller.

After the Focus Start command, the microprocessor checks the DRF signal from the LA9210M to verify that focus has been reached. If C1 fully charges before focus has been reached, the command should then be reissued to repeat the focus servo operation. If focus has not been reached after several retries, the Nothing command (00000000) should briefly be issued to reinitialize the servocontroller.

Note that a new command should not be issued until the focus operation has completed because the focus servocontroller is reinitialized when RWC goes HIGH.

The $\overline{LASER}$ output can be independently set using the Laser ON and Laser OFF commands. The laser control waveforms are shown in figure 12.

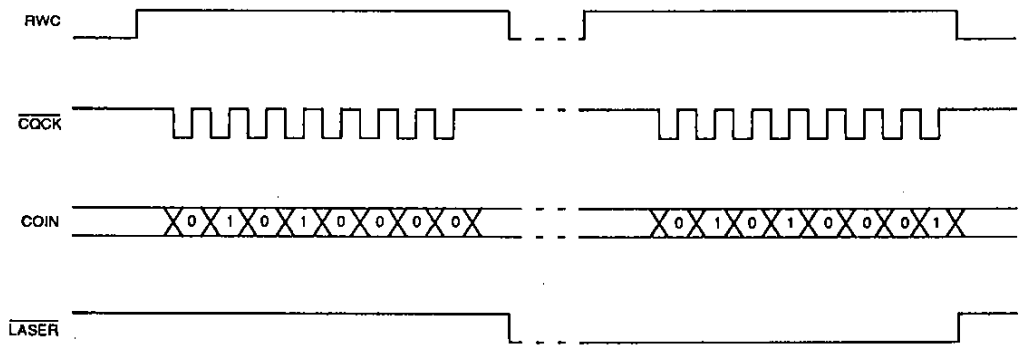


Figure 12. Laser control waveforms

Track Jump Circuit (HFL, TES, TOFF, TGL, THLD, JP+, JP–)

When one of the track jump commands, shown in table 5, is issued, the track jump servocontroller generates output pulses for *a*, *b* and *c* periods as shown in figure 13. Acceleration pulses are generated during *a* period, then deceleration pulses, during *b* period. The motor decelerates during *c* period. The *a*, *b*, and *c* periods for the commands are shown in table 6.

The specified jump finishes by the end of *c* period. During *c* period, the direction of pickup movement is detected and tracking is controlled by TES and HFL. The portion of the tracking-error signal causing internal slip is reduced. TGL is active during the jump to increase the servo gain.

Table 5. Track jump commands

Code								Command
1	0	1	0	0	0	0	0	Standard Track Jump Mode*
1	0	1	0	0	0	0	1	New Track Jump Mode*
1	0	0	0	1	1	0	0	Track Jump Brake*
0	0	0	0	1	1	1	1	TOFF*
1	0	0	0	1	1	1	1	TON*
0	0	0	1	0	0	0	1	1-track Jump In 1
0	0	0	1	0	0	1	0	1-track Jump In 2

Table 5. Track jump commands—continued

Code								Command
0	0	1	1	0	0	0	1	1-track Jump In 3*
0	0	0	1	0	0	1	1	4-track Jump In
0	0	0	1	0	1	0	0	16-track Jump In
0	0	1	1	0	0	0	0	32-track Jump In*
0	0	0	1	0	1	0	1	64-track Jump In
0	0	0	1	0	1	1	1	128-track Jump In*
0	0	0	1	1	0	0	1	1-track Jump Out 1
0	0	0	1	1	0	1	0	1-track Jump Out 2
0	0	1	1	1	0	0	1	1-track Jump Out 3*
0	0	0	1	1	0	1	1	4-track Jump Out
0	0	0	1	1	1	0	0	16-track Jump Out
0	0	1	1	1	0	0	0	32-track Jump Out*
0	0	0	1	1	1	0	1	64-track Jump Out
0	0	0	1	1	1	1	1	128-track Jump Out*
0	0	0	1	0	1	1	0	256-track Check

* New command

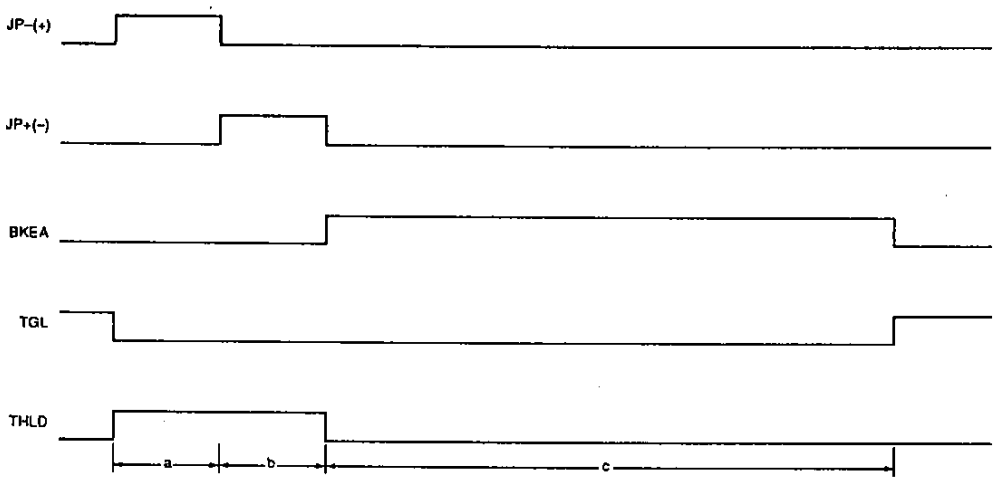


Figure 13. Track jump waveforms

Table 6. Track jump periods

Command	Standard track jump mode			New track jump mode		
	a period	*b* period	*c* period	*a* period	*b* period	*c* period
1-track Jump In (Out) 1	233 µs	233 µs	17 ms	233 µs	233 µs	17 ms
1-track Jump In (Out) 2	0.5-track jump	233 µs	17 ms	0.5-track jump	0.5-track jump	17 ms
1-track Jump In (Out) 3	0.5-track jump	233 µs	Does not occur	0.5-track jump	0.5-track jump	Does not occur
4-track Jump In (Out)	2-track jump	466 µs	17 ms	2-track jump	2-track jump	17 ms
16-track Jump In (Out)	9-track jump	7-track jump	17 ms	9-track jump	9-track jump	17 ms
32-track Jump In (Out)	18-track jump	14-track jump	17 ms	18-track jump	14-track jump	17 ms
64-track Jump In (Out)	36-track jump	28-track jump	17 ms	36-track jump	28-track jump	17 ms
128-track Jump In (Out)	72-track jump	56-track jump	17 ms	Cannot be used		
256-track Check	TOFF goes HIGH after 256 tracks are jumped. The *a* and *b* pulses are not output.		17 ms	Cannot be used		
Track-jump Brake	There are no *a* and *b* periods.		17 ms	There are no *a* and *b* periods.		17 ms

The servo command register is automatically reset after one *a*, *b*, and *c* track jump sequence. When a new track jump command is issued while a previous command is still being processed, the new command is executed immediately.

The actuator drive signals are not generated for the 256-track Check command. Instead, a pickup-motor drive signal is required because the TES signal is in track-count mode and the tracking servocontroller is turned OFF.

Of the tracking control outputs, only TOFF is LOW in CLV disc motor control mode, and HIGH in Accelerate, Decelerate and Stop modes. TOFF can also be independently set by the microprocessor. The tracking control circuit is shown in figure 14.

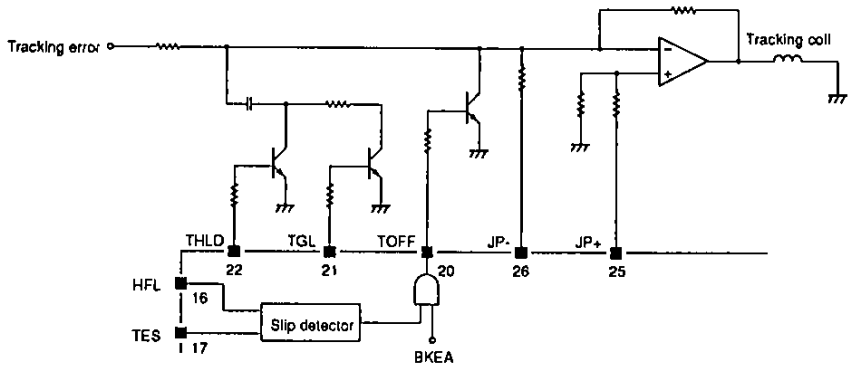


Figure 14. Track jump circuit

Track Count Circuit (HFL, TES, TOFF)

A Track Count In or Track Count Out command followed by a binary number between 16 and 254 starts track counting for that number of tracks. Counting starts on the falling edge of RWC.

The track count commands and track count waveforms are shown in table 7 and figure 15, respectively.

Table 7. Track count commands

Code								Command
1	1	1	1	0	0	0	0	Track Count In*
1	1	1	1	1	0	0	0	Track Count Out*
1	1	1	1	1	1	1	1	Two-byte Command Reset*

* New command

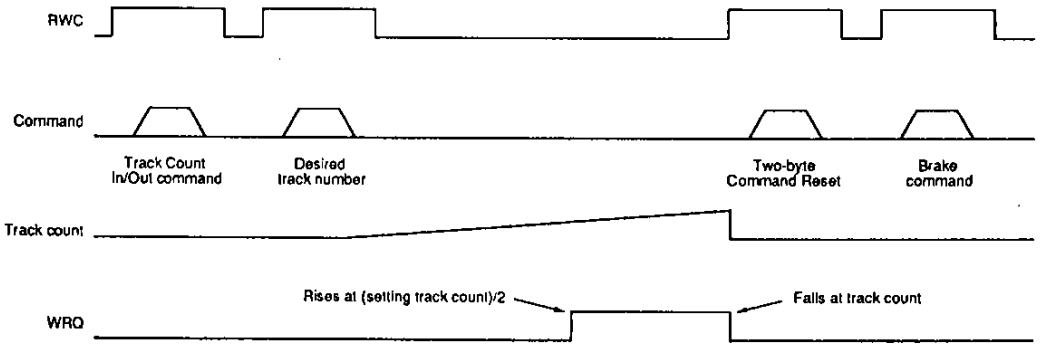


Figure 15. Track count waveforms

The track count commands also cause WRQ to change mode. WRQ goes HIGH at half the track count, and LOW again, at the end of the count. The microprocessor monitors WRQ to detect count completion.

When a 2-Byte Command Reset command is not issued, track count starts again. For example, to advance 20,000 tracks, the microprocessor can set the track count number to 200 and wait 100 WRQ pulses. The Track Jump Brake command brings the pickup to the track when counting is finished.

During track counting, TOFF is HIGH and the tracking servocontroller is turned OFF, therefore, a pickup-motor drive signal is required.

The track counting method described here and in the previous section uses the LA9210 TES signal. The LC7867E's internal track counter can be initialized using the commands shown in table 8.

Standard track counting is activated by initializing the clock with the 23H command at power-up.

Table 8. Track counter commands

Code								Command	$\overline{RES}$
0	0	1	0	0	0	1	0	New Track Count using TES and HFL*	LOW
0	0	1	0	0	0	1	1	Standard Track Count*	—

* New command

The new track counting method uses the TES signal for the internal track counter. This method, which also uses the HES signal, eliminates miscounting due to noise at the rising and falling edges of the TES signal. However care should be exercised when adopting this method since dirt or scratches on the media can cause HFL signal dropout, with subsequent loss of the track counter signal.

Audio Output For Calibration (DEMO)

When DEMO goes HIGH, the signal processor selects both 0 dB muting and CLV disc motor control mode, issues a Focus Start 1 command and turns $\overline{\text{LASER}}$ ON as shown in figure 16. The EFMIN signal and audio output are obtained without microprocessor intervention.

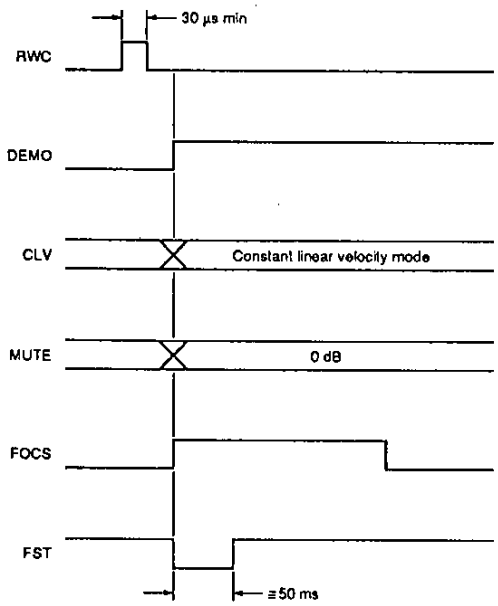


Figure 16. DEMO waveform

Reset Circuit ($\overline{\text{RESET}}$)

The operating conditions after a LOW-to-HIGH transition on $\overline{\text{RESET}}$ are shown in table 9. $\overline{\text{RESET}}$ should be momentarily held LOW after power-ON. A typical power-ON reset circuit which provides this delay is shown in figure 17.

Table 9. Reset modes

Functional block	Operating modes (Reset mode shown in reverse type)
Disc motor control	Accelerate, Decelerate, **Stop**, CLV
Muting control	0 dB, −12 dB, **∞ dB**
Q subcode address condition	**Address 1**, Address Free
Laser control	ON, **OFF**
Disc index RAM	Active, **Clear**
Track count direction	In, Out, **Reset**
Track jump mode	**Standard**, New
TOFF output	**ON**, OFF
Crystal oscillator	**ON**, OFF
Speed mode	Double-speed, **Normal**
VCO frequency	**8M**, 16M
CONT1 output	**LOW**, HIGH

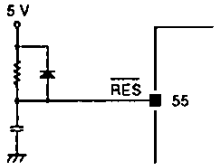


Figure 17. Power-ON reset circuit

Deemphasis Control (EMPH)

The preemphasis ON/OFF bit in the Q subcode data is output on EMPH. Deemphasis is required when EMPH is HIGH.

Error Flag Output (EFLG, FSX)

The 7.35 kHz FSX frame synchronization signal is divided down from the reference clock. The error correction status of each frame is output on EFLG, as shown in figure 18, where the number of HIGH pulses in each FSX period indicates the quality of the replay signal.

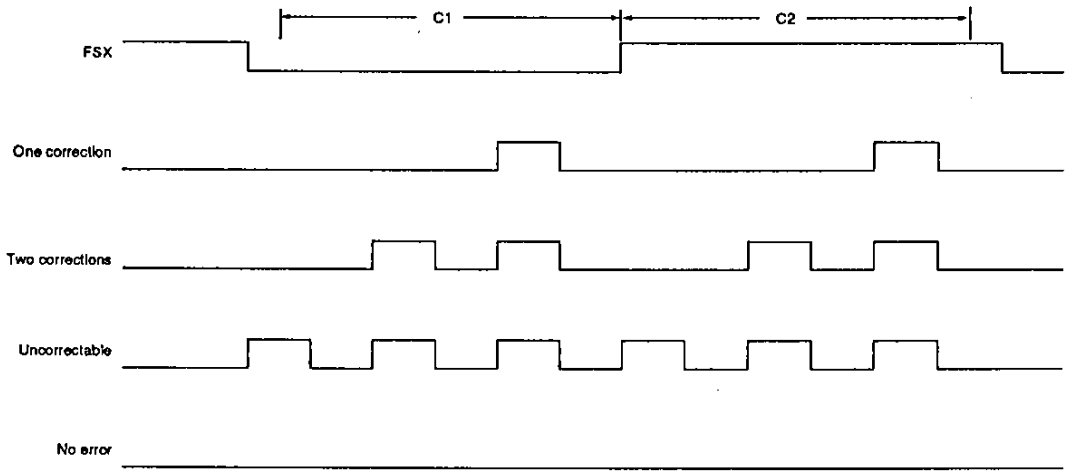


Figure 18. Error flagging waveforms

Crystal Oscillator (XIN, XOUT)

The reference clock requires a 16.9344 MHz crystal connected to XIN and XOUT as shown in figure 19. The oscillator can be enabled or disabled using oscillator commands issued by the microprocessor. The oscillator commands are shown in table 11.

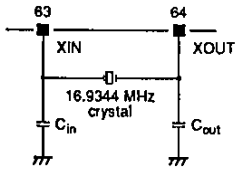


Figure 19. Crystal oscillator

Table 10. Clock crystal oscillator components

Manufacturer	Crystal	C_{in}/C_{out}
CITIZEN WATCH	CSA-309 (16.9344 MHz)	8 to 15 pF (C_{in} = C_{out})

The VCO frequency set by the VCO 8M command is 8.6436 MHz in normal-speed mode, and that by the VCO 16M command, 17.2872 MHz in both normal- and double-speed modes.

Table 11. Oscillator commands

Code								Command
1	0	0	0	1	1	1	0	Oscillator ON*
1	0	0	0	1	1	0	1	Oscillator OFF*
1	1	0	0	0	0	0	1	Double-speed Mode*
1	1	0	0	0	0	1	0	Normal Mode*
0	1	1	0	0	0	0	0	VCO 8M*
0	1	1	0	0	0	0	1	VCO 16M*

* New command

The oscillator OFF command halts oscillation of both the VCO and crystal oscillator

DAC Interface (SMP, LRCLK, DFOUT, DACLK, SMP1, SMP2)

The DAC input data is output serially, msb first, from DFOUT, and the DAC clock, from DACLK as shown in figure 20.

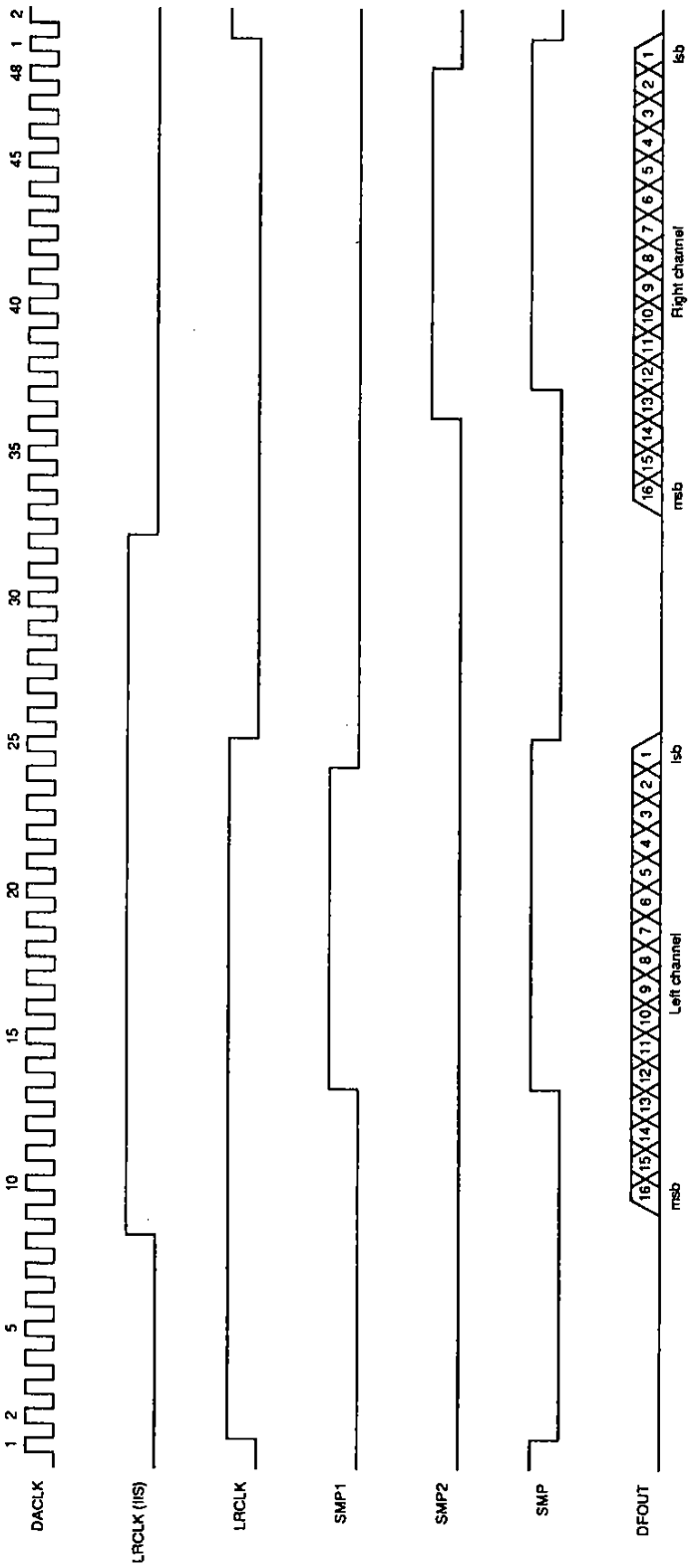


Figure 20. DAC interface waveforms

CD-ROM Interface (CLK2, LRSY, ROMOUT, C2F, C2FCLK)

Data which has not been processed by either the interpolation, previous-value hold or digital filtering circuits is clocked from ROMOUT on the falling edge of the 2.1168 MHz bit clock on CLK2. LRSY marks alternate channels. C2F flags 8-bit units of data and is synchronized to C2FCLK. The CD-ROM output waveforms are shown in figure 21.

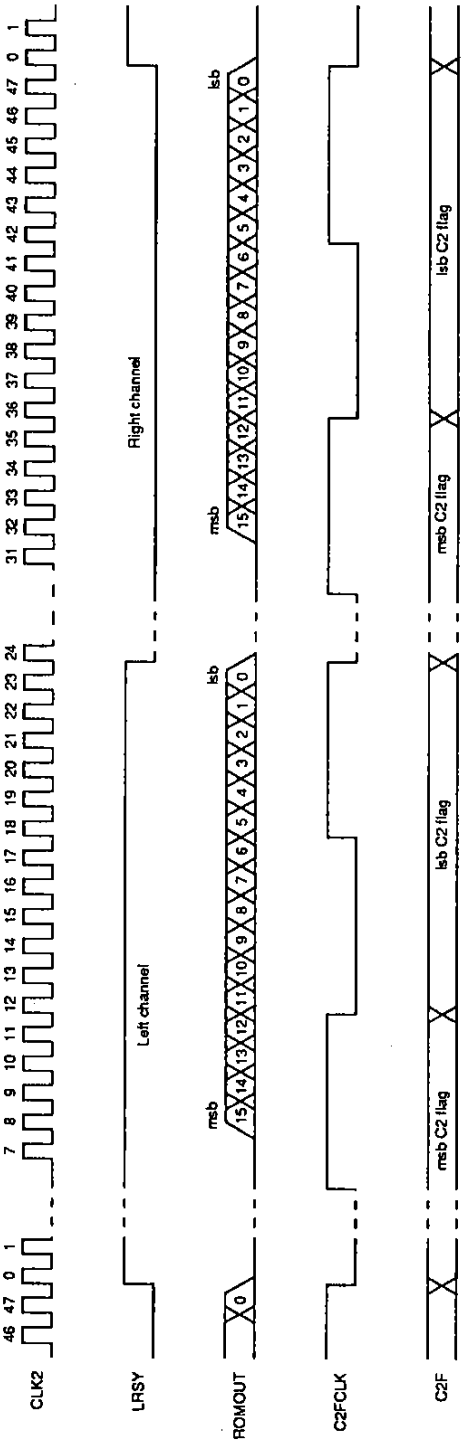


Figure 21. CD-ROM output waveforms

Mute Control Circuit

The mute commands are shown in table 12. Muting switches at zero crossings of the audio signal to prevent switching noise on the audio output. A zero crossing is judged to be any data value where the upper seven bits are all 1 or all 0.

Table 12. Mute commands

Code								Command
0	0	0	0	0	0	0	1	MUTE 0 dB
0	0	0	0	0	0	1	0	MUTE −12 dB
0	0	0	0	0	0	1	1	MUTE ∞ dB

Reference Clocks (4.2M, 16M)

The 16.9344 MHz reference clock is buffered and output on 16M. It is also divided by four to generate a 4.2336 MHz clock that is output on 4.2M. When the oscillator is disabled using the OSC OFF command, these outputs are held either HIGH or LOW. The reference clocks have the same frequency in both normal and double-speed modes.

Digital Audio Output (DOUT)

The digital audio signal after interpolation and muting is output in EIAJ format on DOUT. This signal is buffered internally and can directly drive a transistor.

CD-ROM XA

The CD-ROM XA ON command places the LC7867E in CD-ROM XA mode, and uninterpolated data is output at DFOUT. The CD-ROM XA OFF command restores normal mode, outputting interpolated data.

Note that the CD-ROM XA OFF command uses pin 60 (the same as that used for $\overline{\text{RESET}}$).

Table 13. CD-ROM XA commands

Code								Command	$\overline{\text{RES}}$
1	0	0	0	1	0	0	0	CD-ROM XA ON*	—
1	0	0	0	0	1	0	1	CD-ROM XA OFF*	LOW

* New command

TOFF Output

When the disc motor is stopped, the TOFF pin HIGH command has priority.

Table 14. TOFF output commands

Code								Command	$\overline{\text{RES}}$
0	0	0	0	1	1	1	1	TOFF pin HIGH*	LOW
1	0	0	0	1	1	1	1	TOFF pin LOW*	—

* New command

Control Output (CONT)

The Cont and Reset commands, shown in table 15, set CONT HIGH and LOW, respectively.

Table 15. Output control commands

Code								Command
0	0	0	0	1	1	1	0	Cont
1	0	0	0	1	0	1	1	CONT RESET and CDROM XA OFF

Test Inputs (TEST1 to TEST5)

TEST1 to TEST5 have internal pull-down resistors. The test inputs can be left open during normal operation.

Test Output (TEST6)

This output should be left open during normal operation.

RAM Address Control

The LC7867E incorporates a 2 Kbyte RAM buffer to remove timing variations, or jitter, from the EFM data signal caused by variations in the disc motor speed. The buffer can absorb up to ±4 frames of jitter. Data is input to the buffer at a frequency synchronized to the EFM data signal and removed at a frequency divided down from the reference clock.

The buffer controller continuously monitors buffer free space and adjusts the CLV servocontroller divider ratio to keep the data write address in the middle of the buffer, or zero, as shown in table 16. If the ±4 frames limit is exceeded, the write address is forced to the middle of the buffer. The output is muted for 128 frames because the resulting error cannot be handled by normal error processing algorithms.

Table 16. RAM address control

Write address to read address difference (frames)	CLV servo division ratio	Action on motor speed
≤ −4	Force address difference to 0	
−3	589	Increase
−2	589	Increase
−1	589	Increase
±0	588	Standard ratio
+1	587	Decrease
+2	587	Decrease
+3	587	Decrease
≥ +4	Force address difference to 0	

C1 and C2 Error Correction

After EFM demodulation and buffering, each 32-symbol frame is passed through the C1 and C2 decoding and error correction stages. The C1 stage sets the C1 flag for each symbol, as shown in table 17, and the C2 stage processes the frame and sets the C2 flags, as shown in table 18.

Table 17. C1 error processing

C1 errors detected	Error correction	C1 flag
No errors	No correction	Reset
1	Correction	Reset
2	Correction	Set
≥ 3	Not possible	Set

Table 18. C2 error processing

C2 errors detected	Error correction	C2 flag
No errors	No correction	Reset
1	Correction	Reset
2	Depends on C1 flags	
≥ 3	Depends on C1 flags	

When the C2 stage detects two errors, either the errors are corrected and the flags reset, the flags are set or the C2 flags are set to match the C1 flags.

- The errors are corrected and the flags reset if
  - C1 flags are set for both C2 error positions. Note that errors cannot be corrected if even one error position is different.
- The two C2 flags are set either if
  - five or less C1 flags are set and C1 flags match the C2 error positions, or if
  - two or less C1 flags are set and the flags do not match the C2 error positions.
- The C2 flags are set to match the C1 flags either if
  - seven or more C1 flags are set and C1 flags match the C2 error positions, or if
  - six or more C1 flags are set and the flags do not match the C2 error positions, or if
  - three or more C1 flags are set and the flags do not match one of the C2 error positions.

When the C2 stage detects three or more correctable errors, the errors are corrected. However, if two or less C1 flags are set, the three C2 flags are set because an error can still occur which passes the C1 check.

The C2 flags are used by the interpolation circuit to determine whether to interpolate or mute the signal. The interpolator uses 4-interpolation, where the immediately preceding value is held if the C2 flag is set four times in a row.