Ordering number : EN4823A

Monolithic Linear IC

LA1888NM

Car Stereo Single-Chip Tuner IC

Overview

The LA1888NM is a high-performance, multi-function single-chip tuner IC that was developed for use in car stereo systems. The LA1888NM is a second-generation single-chip tuner IC that integrates six blocks in a single package. Five of those blocks provide performance and functional improvements over the corresponding five blocks provided by the first-generation LA1886M and LA1883M, while the additional sixth block consists of an MRC circuit that reduces the noise in multipath reception.

Functions

- FM front end, FM IF, noise canceller, multiplex, MRC (multipath rejection circuit), AM, and FM/AM switching. (See the following page for details.)

Features

- A tuner's characteristics are determined by the noise suppression performance. The most significant feature of the LA1888NM is that the characteristics of the individual blocks have been redesigned to improve the noise characteristics in the cases of multipath, three signal IM, two signal suppression and AM interference.
- Excellent anti-three signal interference characteristics, equivalent to those of the LA1193M FM front end (3D AGC system).
- Improved noise canceler characteristics in the medium and weak field of antenna input signals.
- Improved stereo separation (excellent high frequency separation)
- Built-in anti-birdie filter (f = 114 kHz, 190 kHz)
- Built-in MRC circuit that detects multipath noise
- The W-AGC sensitivity, which is essentially equivalent to that of the LA1137N, was increased by 10 dB (from 95 dBμ to 85 dBμ) during seek operations to prevent stopping at spurious stations with strong interference.
- The AM detector output frequency characteristics can be set independently.
  (Low frequency and high frequency AF responses can be set independently.)
- The pin layout of the first-generation LA1883M single-chip products has been maintained, thus easing transition and supporting product miniaturization.

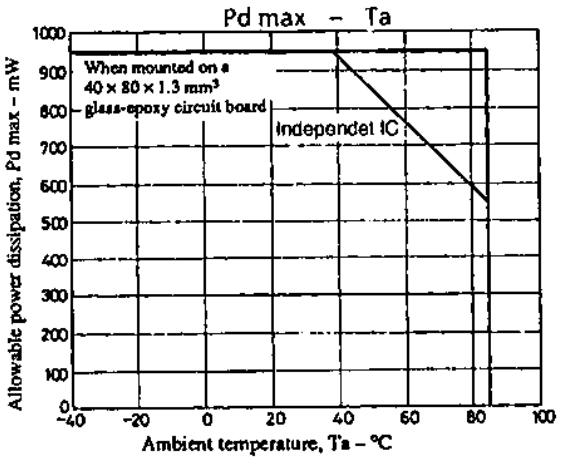
■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

O3098HA(OT)/33095TH (OT) No. 4823-1/65

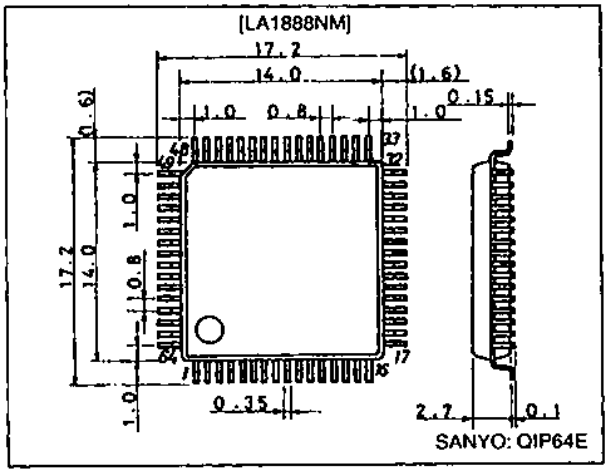
Downloaded from Elcodis.com electronic components distributor



Package Dimensions

unit: mm

3159-QFP64E



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max1	Pins 40 and 62	9.5	V
	V_{CC} max2	Pin 44, 47, 54, 60 and 61	12	V
Allowable power dissipation	Pd max	Ta ≤ 55°C	950	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}	Pins 40, 44, 47, 54, 60 and 61	8.0	V
	V_{CC} STINJ	Pin 5	5	V
Operating supply voltage range	V_{CC} op		7.5 to 9.2	V

Functions

- FM front end (equivalent to the SANYO LA1192)
  - — Double balance mixer, dual input type
  - — Pin diode drive AGC output
  - — MOSFET second gate drive AGC output
  - — Keyed AGC adjusting pin
  - — Differential IF amplifier
  - — Wide AGC sensitivity setting, narrow AGC sensitivity setting
  - — Local oscillator
- FM IF
  - — IF limiter amplifier
  - — S-meter output (also used by AM circuits) by six-stage pickup
  - — Multipath detector (dedicated FM S-meter)
  - — Quadrature detector
  - — AF preamplifier
  - — AFC output
  - — Bandwidth muting (muting for detuning)
  - — Weak input muting
  - — Soft mute adjusting pin
  - — Mute attenuation level adjusting pin
  - — IF counter buffer output (also used by AM circuits)
  - — SD (IF counter buffer activation level) adjusting pin
  - — SD output (active-high) (also used by AM circuits)

  * SD : Station Detection
- NC
  - — High-pass filter (first order)
  - — Delay circuit of low-pass filter (fourth order)
  - — Noise AGC
  - — Pilot signal compensation
  - — Noise sensitivity setting
  - — Forced noise canceller off in AM mode

Downloaded from Elcodis.com electronic components distributor

- MPX
  - — Adjustment-free VCO
  - — Level following pilot canceller
  - — HCC (high-cut control)
  - — Automatic stereo/mono switching
  - — VCO oscillator stop (AM mode)
  - — Forced monaural
  - — SNC (stereo noise control)
  - — Stereo indicator (active-low)
  - — Anti-birdie filter (f = 114 kHz, 190 kHz)
- MRC (Multipath rejection circuit)
  - — Noise amplifier
  - — Noise detection
  - — DC level shifter
  - — SNC and HCC driving
  - — Time constant control circuit
- AM
  - —Double balance mixer
  - — IF amplifier
  - — Detector (demodulator)
  - — RF AGC (narrow and wide band)
  - — PIN diode drive pin
  - — Tweet reduction circuit
  - — IF AGC
  - — S-meter output (also used by FM circuits)
  - — Local oscillator
  - — Local oscillator buffer output
  - — IF counter buffer output (also used by the FM IF circuit)
  - — SD (IF counter buffer activation level) adjustment
  - — SD output (active-high) (also used by FM circuits)
  - — Increased W-AGC sensitivity during seek operation
  - — Demodulated output frequency response setting (cutting for low frequency and de-emphasis for high frequency)
- Other functions
  - Built-in AM/FM switching circuit (linked to the front-end V_{CC})

FM General Characteristics, fr = 98.0 MHz antenna input

Parameter	Conditions	Ratings	Unit
Practical sensitivity	fm = 1 kHz, 22.5 kHz dev. demodulator output, antenna input for a 30 dB S/N (no noise meter filter)	2.5	dBμ
Demodulation output	80 dBμ input, fm = 1 kHz, 75 kHz dev. demodulator output	260	mVrms
Distortion	80 dBμ input, fm = 1 kHz, 75 kHz dev.	0.38	%
Main distortion	80 dBμ input, fm = 1 kHz, L + R 90%, pilot 10%	0.38	%
S/N ratio	Output reference, S/N for unmodulated signal	72	dB
AM rejection ratio	fm = 1 kHz 22.5 kHz dev. + fm 1 kHz 30%, AM antenna 80 dBμ output and fm 1 kHz, AM output ratio	41	dB
Limiting sensitivity	fm = 1 kHz, 22.5 kHz, antenna input when the output is down by −3 dB.	6	dB
Image rejection ratio	fr = 119.4 MHz, fm = 1 kHz, antenna input when the 22.5 kHz output is down by −3 dB.	59	dB
No input noise output	80 dBμ, fm = 1 kHz, 22.5 kHz dev. Output reference, No input noise output ratio	20	dB
Separation 1	80 dBμ, fm = 1 kHz 90%, pilot 10% 75 kHz dev., Lch 1 kHz 90% → Rch 1 kHz 90%	40	dB
Separation 2	40 dBμ, fm = 1 kHz 90%, pilot 10% 75 kHz dev., Lch 1 kHz 90% → Rch 1 kHz 90%	10.5	dB
HCC effect	80 dBμ, fm = 1 kHz, 22.5 kHz dev. reference, Antenna input when the output is down by −3 dB.	25	dBμ
Pilot cancelling	80 dBμ, Pilot 10% cancellation	30	dB
S-meter output 1	No input	0.3	V
S-meter output 2	30 dBμ	2.9	V
S-meter output 3	60 dBμ	5.1	V
Three-signal characteristics	Practical sensitivity at f_D = 98.0 MHz, $f_{UD}1$ = 98.8 MHz, 100 dBμ, non-mod, $f_{UD}2$ = 99.6 MHz, 100 dBμ, fm = 400 Hz, 22.5 kHz dev.	33	dBμ
Two-signal sensitivity suppression	−3 dB sensitivity for f_D = 98.0 MHz, $f_{UD}1$ = 98.4 MHz, with a 120 dBμ input	51	dBμ
SD sensitivity	Antenna input that turns on the SD and IF counter buffer	30	dBμ
Antenna damping activation level	Antenna input that turns on the W-AGC, with the keyed AGC on	81	dBμ

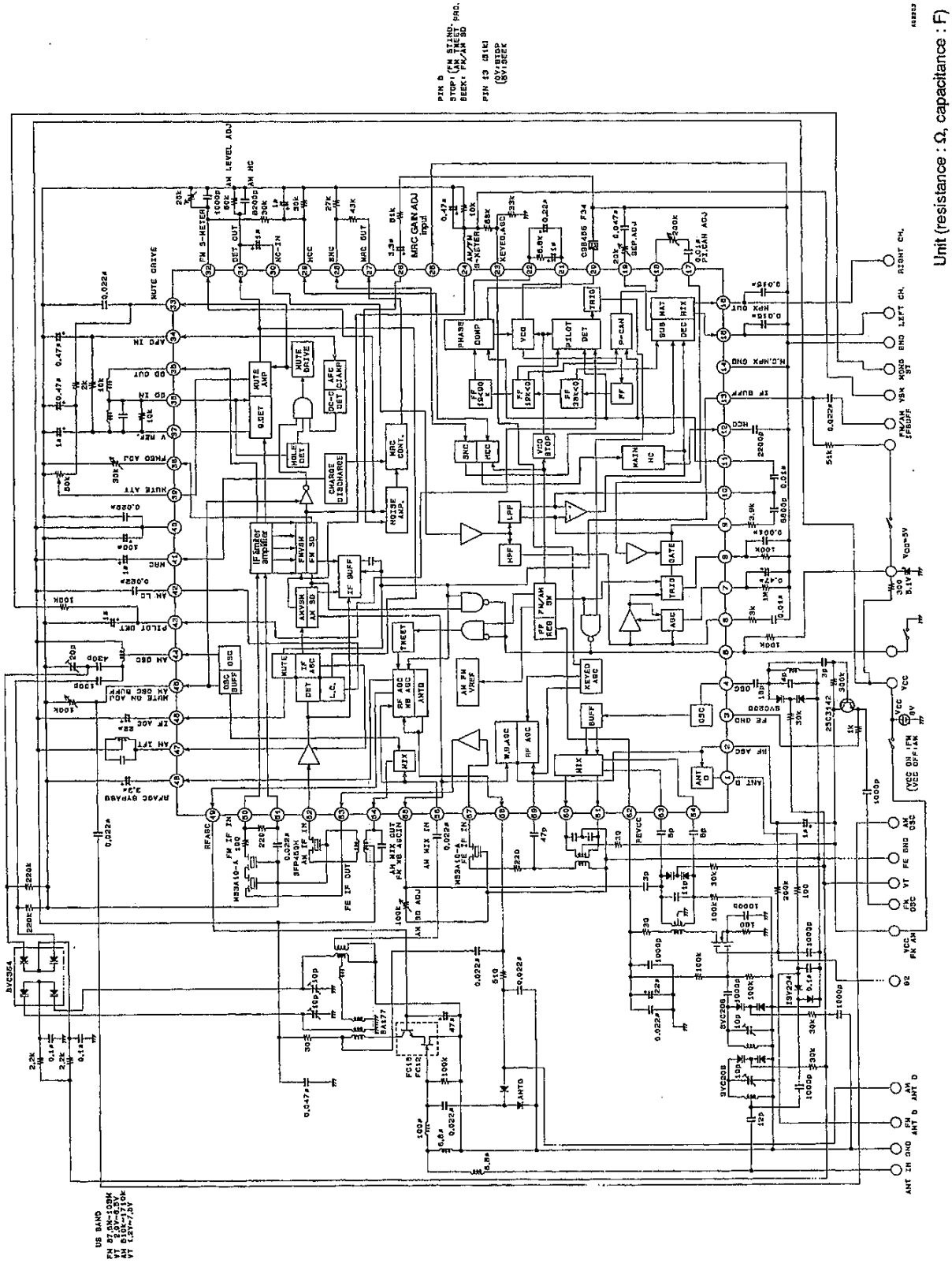
Downloaded from Elcodis.com electronic components distributor

AM General Characteristics, fr = 1 MHz, JIS standard dummy antenna

Parameter	Conditions	Ratings	Unit
Practical sensitivity	fm = 1 kHz 30%, antenna input for a 20 dB S/N	24	dBμ
Detector output	74 dBμ, fm = 1 kHz 30%, detector output	120	mVrms
AGC FOM	Detector output reference, antenna input ratio such that the output is down by −10 dB	55	dB
S/N ratio	Detector output reference, S/N ratio for unmodulated signal	52	dB
Distortion	74 dBμ, fm = 1 kHz 80% mod, THD	0.22	%
SD sensitivity	The antenna input that turns on the SD and IF counter buffer	30	dBμ
S-meter output 1	No input	0.1	V
S-meter output 2	74 dBμ	3.2	V
S-meter output 3	120 dBμ	4.4	V
Image rejection ratio	fr = 1900 kHz, fm = 1 kHz 30% mod, antenna input ratio such that it becomes the same as the AGC FOM −10 dB detector output.	115	dB
Antenna damping activation level	Antenna input such that the antenna damping is 0.7 V or greater	66	dBμ
Tweet reduction on antenna damping activation level	Antenna input such that the antenna damping is 0.7 V or greater, pin 5 low	60	dBμ
W-AGC activation level	fr = 1.4 MHz, antenna input such that the antenna damping is 0.7 V or greater	94	dBμ
W-AGC activation level (during seek)	Antenna input such that the antenna damping is 0.7 V or greater during a seek operation	85	dBμ

Downloaded from Elcodis.com electronic components distributor

Sample Application Circuit



Downloaded from Elcodis.com electronic components distributor

Operating Specifications

Ta = 25°C, V_{CC} = 8.0 V, specified FM IF test circuit, AC3, with an fr input of 10.7 MHz
Note that these measurements were made using IC sockets manufactured by Yamaichi Electric (IC-51-0644-824, KS8277).

Parameter	Symbol	Conditions	Test point	Filter	SW No. (on = 1, off = 0)									min	typ	max	Unit
					1	2	3	4	5	6	7	8	9				
Quiescent current	I_{CCO}-FM	No input, I40 + I54 + I47 + I60 + I61 + I44 + I62			1	I	0	0	0	0	0	1	1	52	75	93	mA
Demodulator output	V_O-FM	10.7 MHz, 100 dBμ, 1 kHz, 100% mod, pin 15 output	VA4	IHF T200	1	I	0	0	0	0	0	1	1	240	360	480	mVrms
Channel balance	CB	100 dBμ, 1 kHz, ratio between pins 15 and 16	VA4 VA5	IHF T200	1	I	0	0	0	0	0	1	1	−1.0	0	+1.0	dB
Total harmonic distortion L	THD-FM L	100 dBμ, 1 kHz, 100% mod, pin 15	VA4		1	I	0	0	0	0	0	1	1		0.5	1.2	%
S/N ratio	S/N FM	100 dBμ, 1 kHz, 100% mod, pin 15, output reference, ratio with the un-modulated output	VA4	IHF T200	1	I	0	0	0	0	0	1	1	75	82		dB
AM rejection ratio	AMR	100 dBμ, 1 kHz, 100% mod, output reference 1 kHz, fm = 1 kHz, 30%, the ratio with pin 15 output in AM mode	VA4	IHF T200	1	I	0	0	0	0	0	1	1	62	75		dB
Muting attenuation	ATT1	100 dBμ, 1 kHz, V_{CC}2, pin 16 attenuation when V33 goes from 0 to 1 V	VA4	IHF T200	1	I	0	0	0	0	0	1	1	20	25	30	dB
	ATT2	100 dBμ, 1 kHz, V_{CC}2, pin 16 attenuation when V33 goes from 0 to 2 V.	VA4	IHF T200	1	I	0	0	0	0	0	1	1	28	33	38	
Separation L	Sep L	100 dBμ, 1 kHz, L90% → R90%, pilot = 10%, pin 15 output ratio	VA4	IHF T200	1	I	0	0	0	0	0	1	1	30	40		dB
Stereo detection level	ST-ON	Pilot modulation such that V5 < 1.5 V	VD2		1	I	0	0	0	0	0	1	1	1.4	2.6	4.5	%
	ST-Hy	Pilot modulation such that V5 > 3.5 V	VD2		1	I	0	0	0	0	0	1	1	0.6	1.7		
Main THD L	THD-main L	100 dBμ, L + R = 90%, pilot = 10%, pin 15	VA4	BL-43	1	I	0	0	0	0	0	1	1		0.4	1.5	%
Pilot cancellation	PCAN	100 dBμ, Pilot = 10%, pin 15 signal, 19 kHz cancellation with SW10 on or off.	VA4	DIN AUDIO	1	I	0	0	0	0	0	1	1/0	20	30		dB
SNC output voltage	V_O SUB	100 dBμ, L − R = 90%, pilot = 10%, V_{EE}3 V28 = 0.1 V, pin 16	VA4	IHF T200	1	I	0	0	0	0	0	1	1		3.0	10.0	mVrms
SNC output attenuation	ATT SNC	100 dBμ, L − R = 90%, pilot = 10%, V_{EE}3 V28 = 0.6 V, pin 16	VA4	IHF T200	1	I	0	0	0	0	0	1	1	2.0	6.0	10.0	dB
HCC output attenuation	ATT HCC1	100 dBμ, L + R = 90%, pilot = 10%, fm = 10 kHz, V_{EE}3 V29 = 0.6 V, pin 16	VA4	IHF T200	1	I	0	0	0	0	0	1	1	0	4.0	8.0	dB
	ATT HCC2	100 dBμ, L + R = 90%, pilot = 10%, fm = 10 kHz, V_{EE}3 V29 = 0.1 V, pin 16	VA4	IHF T200	1	I	0	0	0	0	0	1	1	6.0	10.0	14.0	
Input limiting voltage	Vi-lim	100 dBμ, fm = 1 kHz, 30% mod, input reference output, IF input for −3 dB down when muting is off.	VA4	IHF T200	1	I	0	0	0	0	1	0	1	27	34	41	dBμ
Muting sensitivity	Vi-mute	Unmodulated input level such that VD5 becomes 2 V.	VD5		1	I	0	0	0	0	0	0	1	26	34	42	dBμ
SD sensitivity	SD-sen	Input level such that VD2 becomes 3.5 V and VA3 becomes 100 mV rms or over.	VD2 VA3		1	I	0	0	0	1	0	0	1	63	75	87	dBμ
IF counter buffer output	VIFBUFF-FM	100 dBμ, non-mod	VA3		1	I	0	0	0	1	0	0	1	220	310	440	mVrms
S-meter output	V_{SM} FM-1	No input, pin 24 DC output	VD3		1	I	0	0	0	0	0	0	1	0	0.1	0.3	V
	V_{SM} FM-2	50 dBμ, pin 24 DC output	VD3		1	I	0	0	0	0	0	0	1	0.4	1.2	2.3	
	V_{SM} FM-3	70 dBμ, pin 24 DC output	VD3		1	I	0	0	0	0	0	0	1	1.6	2.8	4.7	
	V_{SM} FM-4	100 dBμ, pin 24 DC output	VD3		1	I	0	0	0	0	0	0	1	4.3	5.3	6.7	
Muting bandwidth	BW-mute	100 dBμ, bandwidth such that pin 33 VD5 becomes 2 V.	VD5		1	I	0	0	0	0	0	0	1	80	150	240	kHz
Muting drive output	Vmute	100 dBμ, unmodulated, pin 33 VD5 (the mute drive output) voltage	VD5		1	I	0	0	0	0	0	0	1	0	0.03	0.2	V

Downloaded from Elcodis.com electronic components distributor

1 MHz AM ANT input, with SW1 set to the AM MOD position. See specified Test Circuit.

Parameter	Symbol	Conditions	Test point	Filter	SW No. (on = 1, off = 0)									min	typ	max	Unit
					1	2	3	4	5	6	7	8	9				
Practical sensitivity	S/N-27	Input: 27 dBμ, fm = 1 kHz, 30% mod	VA4	IHF	0	0	0	0	0	0	0	1	1	20	25		dB
Detector output	V_O-AM	74 dBμ, fm = 1 kHz, 30% mod, pin 16	VA4	IHF T200	0	0	0	0	0	0	0	1	1	85	120	170	mVrms
AGC FOM		74 dBμ output reference, input width such that the output is reduced 10 dB	VA4	IHF T200	0	0	0	0	0	0	0	1	1	52	57	62	dB
S/N ratio	S/N-AM	ANT IN = 74 dBμ, fm = 1 kHz and an unmodulated signal	VA4	IHF T200	0	0	0	0	0	0	0	1	1	47	52		dB
Total harmonic distortion	THD-AM	74 dBμ, fm = 1 kHz, 80% mod	VA4		0	0	0	0	0	0	0	1	1		0.3	1.0	%
S-meter output	V_{SM} AM-1	No input	VD3		0	0	0	0	0	0	0	1	1	0	0.1	0.4	V
	V_{SM} AM-2	130 dBμ, unmodulated	VD3		0	0	0	0	0	0	0	1	1	3.3	5.0	7.0	
OSC buffer output	$V_{OSCBUFF}$-AM	No input	VA9		0	0	0	0	0	0	0	1	1	220	270		mVrms
Bandwidth AGC sensitivity	W-AGCsen-1	Input frequency = 1.4 MHz and VD6 = 0.7 V	VD6		0	0	0	0	0	0	0	1	1	85	91	97	dBμ
	W-AGCsen-2	Input frequency = 1.4 MHz and VD6 = 0.7 V (during a seek operation)	VD6		0	0	0	0	0	1	0	1	1	76	82	88	
SD sensitivity	SD-senAM	IF counter output: 100 mV rms or higher, an input such that VD2 becomes 3.5 V or higher	VD2		0	0	0	0	0	1	0	1	1	20	27	34	dBμ
Tweet reduction circuit sensitivity	Tweet-sen	AC3 fr = 1 MHz, unmodulated, antenna input such that VD6 becomes 0.7 V or lower.	VD6		0	0	0	0	1	0	0	1	1	46	52	58	dBμ
IF buffer output	V_{IFBUFF}-AM	74 dBμ, unmodulated, VA3 output	VA3		0	0	0	0	0	1	0	1	1	270	350		mVrms

FM front end mixer input, AC2 fr = 83 MHz, SW2 set to the MIX position. See specified Test Circuit.

Parameter	Symbol	Conditions	Test point	Filter	SW No. (on = 1, off = 0)									min	typ	max	Unit
					1	2	3	4	5	6	7	8	9				
RF AGC on input	V_N AGC	MIX input such that pin 2 becomes 2 V or lower	VD1		1	M	1	0	0	0	0	1	1	82	89	96	dBμ
W-AGC on input	V_W AGC	MIX input such that pin 2 becomes 2 V or lower, set the keyed AGC ($V_{CC}2$) to 0.1 V.	VD1		1	M	1	0	0	0	0	1	1	96	103	110	dBμ
Conversion gain	AV	Mix input 83 MHz, 70 dBμ, non-mod, FE CF output	VA2		1	M	1	0	0	0	0	1	1	16.0	25.0	40.0	mVrms
OSC buffer output	V_{OSC}	No input	VA1		1	M	1	0	0	0	0	1	1	190	270	350	mVrms

Noise canceller input (pin 30), SW4 set to the NC input position. See specified Test Circuit.

Parameter	Symbol	Conditions	Test point	Filter	SW No. (on = 1, off = 0)									min	typ	max	Unit
					1	2	3	4	5	6	7	8	9				
Gate time	$T_{GATE}1$	The time required for VD7 to exceed 1 V, PG1 = 1 kHz, 1 μs, 100 mVp-p pulse input	VD7		1	0	0	N	0	0	0	1	1	35	55	75	μs
	$T_{GATE}2$	The time required for VD7 to exceed 1 V, PG1 = 1 kHz, 1 μs, 100 mVp-p pulse input, AC5 f = 1 kHz,30 mV rms input	VD7		1	0	0	N	0	0	0	1	1	10	25	40	
Noise sensitivity	SN	1 kHz 1 μs pulse input level such that the noise canceller operates.	VD7		1	0	0	N	0	0	0	1	1		40	60	mVp-p

Downloaded from Elcodis.com electronic components distributor

MRC input (pin 26). See specified Test Circuit.

Parameter	Symbol	Conditions	Test point	Filter	SW No. (on = 1, off = 0)									min	typ	max	Unit
					1	2	3	4	5	6	7	8	9				
MRC output	VSASC	Pin 27 VD4 voltage when V32 = 2 V, for pin 26 input of 1 kHz, 5 mVrms	VD4		1	0	0	0	0	0	0	0	1	1.8	1.9	2.0	V
MRC operation level	SASC-ON	Pin 26 input such that pin 27 VD4 voltage becomes 1.9 V. Pin 32 level = 2 V	VD4		1	0	0	0	0	0	0	0	1		10	25	mVrms

Operating Characteristics and Test Circuit Signals

1. Switches

   An on switch has the value 1, and an off switch the value 0.

   There are two switches used for transfers.

   - SW2 switches between the MIX input and the IF input.
   - SW4 switches between the IF OUT + NC input.

2. SG Types

PG1 (AC1)	For NC measurement. Requires a pulse generator and an AF oscillator.
AC2	For FM front end measurement. 83 MHz output
AC3	For FM IF, NC, and MPX measurement. Must provide a 10.7 MHz output and support stereo modulation.
AC4	For AM measurement. 1 and 1.4 MHz outputs.
AC5	For MRC. Variable AF oscillator.

3. Power Supply

V_{CC}	8 V		
$V_{CC}1$	5 V		SD, stereo, seek/stop
$V_{CC}2$	0.1 V/0.7 V/2 V/4 V	These must be variable voltage.	Keyed AGC, mute ATT
$V_{CC}3$	0.1 V/0.6 V/2 V		HCC, SNC, SASC (MRC)

4. (a) Switches

SW	Function	On	Off	(O/T)
SW1	Switches between AM and FM, front end V_{CC} supply, pin 62	FM	AM	O
SW2	FM IF input switch, pin 50/front-end output	Connects the front-end IF output to pin 50.	Connects AC3 to pin 50	T
SW3	For conversion gain measurement	Conversion gain measurement	Other use	O
SW4	Switches between NC input and IF OUT + NC.	Connects PG1 (AC1) during NC measurement.	Other use	T
SW5	Tweet reduction circuit (pin 5)	When tweet reduction is on	Other use	O
SW6	Seek/stop (IF BUFF on/off), pin 13	Seek (IF buffer output)	Stop	O
SW7	Mute off (pin 39)	Mute off	Mute on	O
SW9	For pilot canceller measurement	When Pi-Can in on	When Pi-Can in off	O

(b) Trimmers

VR1	For separation adjustment
VR2	For pilot canceller adjustment

Downloaded from Elcodis.com electronic components distributor

5. Measurement Points

(a) DC voltages

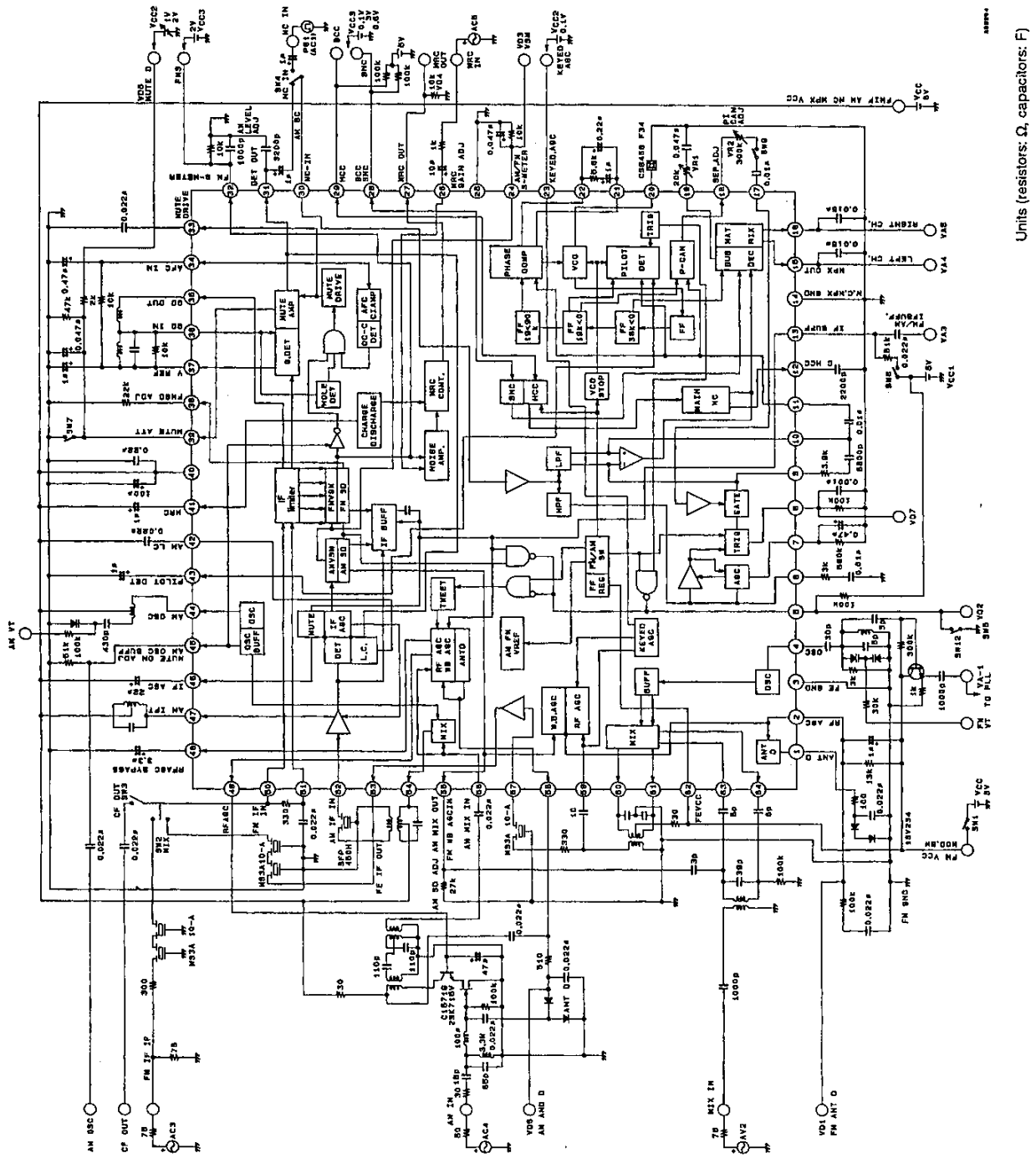
VD1	FM RF AGC voltage	Pin 2
VD2	AM/FM SD, AM tweet reduction, FM stereo indicator	Pin 5
VD3	AM/FM S-meter	Pin 24
VD4	MRC output	Pin 27
VD5	Mute drive output	Pin 33
VD6	AM antenna damping voltage	Pin 58
VD7	NC gate time	Pin 8

(b) AC voltages

VA1	FM OSC buffer	Pin 4 transistor buffer (72.3 MHz)
VA2	First IF output	Pin 53 to CF to pin 50 load level (10.7 MHz)
VA3	IF counter buffer	Pin 13 (10.7 MHz/450 kHz)
VA4	MPX out left ch	Pin 15 (AF)
VA5	MPX out right ch	Pin 16 (AF)
VA9	AM OSC buffer	Pin 45 output (1450 kHz)

Downloaded from Elcodis.com electronic components distributor

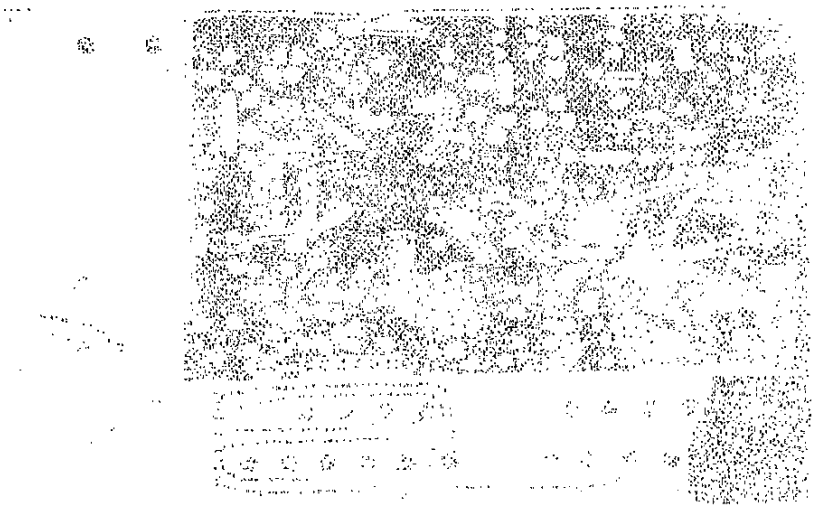
AC Test Circuit



Downloaded from Elcodis.com electronic components distributor

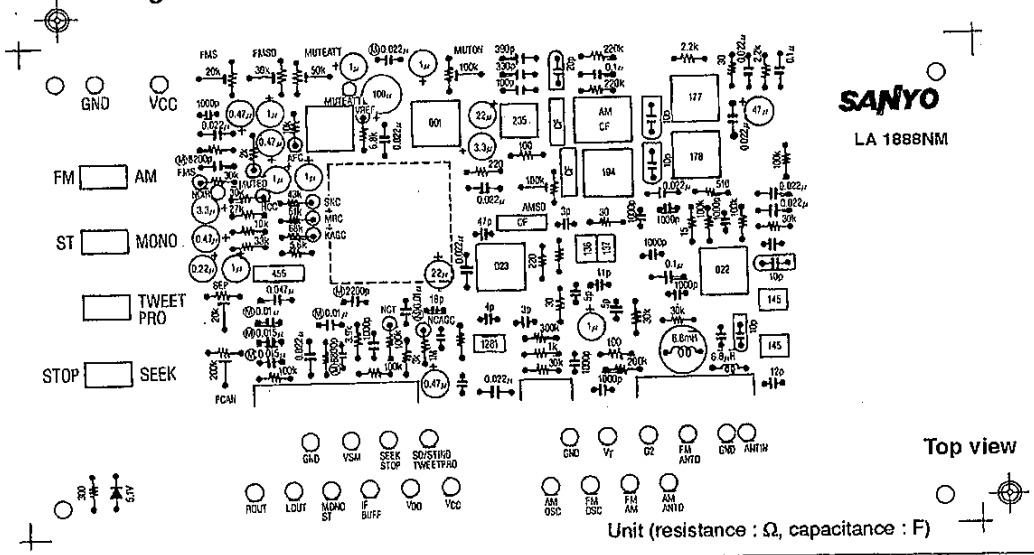
Printed Circuit Board Pattern

Solder Surface (bottom view)



Component Surface (top view)

Component Mounting



Unit (resistance : Ω, capacitance : F)

Downloaded from Elcodis.com electronic components distributor

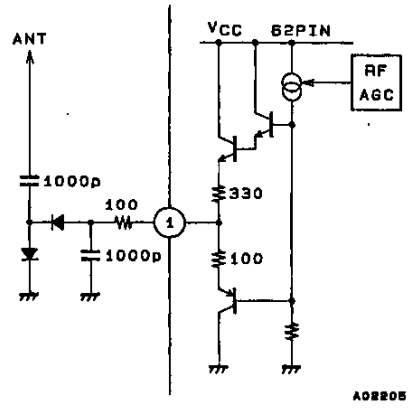
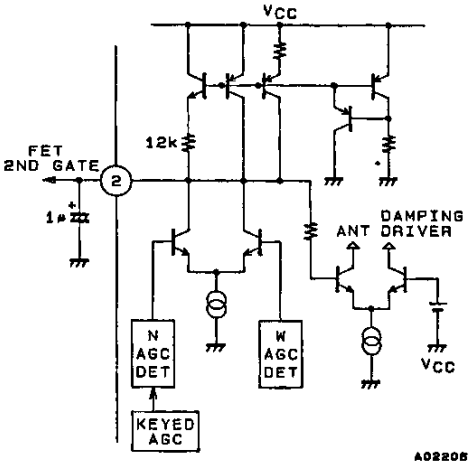
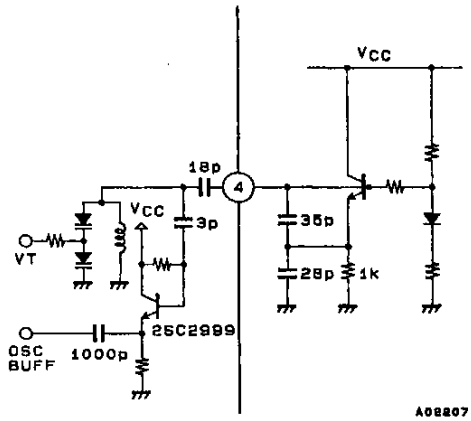
Pin Function Blocks

Pin No.	Block	Pin No.	Block	Pin No.	Block
1	FE	23	FM FE	45	AM/IF
2	FE	24	AM/FM	46	AM
3	FE GND	25	IF.AM.GND	47	AM
4	FE	26	MRC	48	AM
5	AM/FM	27	MRC	49	AM
6	NC	28	MPX	50	FM IF
7	NC	29	MPX	51	FM IF
8	NC	30	NC	52	AM
9	NC	31	AM/FM	53	FM FE
10	NC	32	FM/MRC	54	AM
11	MPX	33	FM IF	55	FM FE/AM
12	MPX	34	FM IF	56	AM
13	AM/FM	35	FM IF	57	FM FE
14	MPX.NCMRC.GND	36	FM IF	58	AM
15	MPX	37	FM IF	59	FM FE
16	MPX	38	FM IF	60	FM FE
17	NC	39	FM IF	61	FM FE
18	MPX	40	V_{CC}	62	FM FE V_{CC}
19	MPX	41	MRC	63	FM FE
20	MPX	42	AM	64	FM FE
21	MPX	43	MPX		
22	MPX	44	AM		

Downloaded from Elcodis.com electronic components distributor

Pin Functions

Unit (resistance: Ω, capacitance: F)

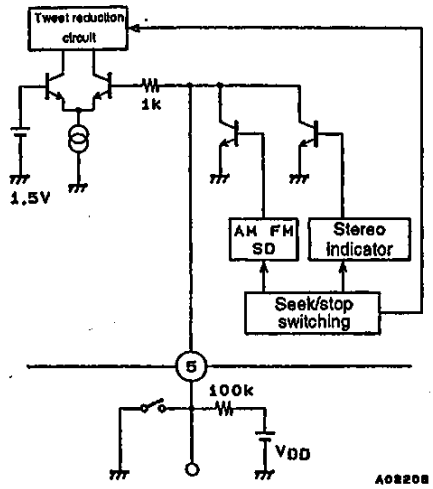
Pin No.	Function	Equivalent circuit	Notes
1	Antenna damping drive		Antenna damping current flows when the pin 2 RF AGC voltage reaches V_{CC}-V_{BE}.
2	RF AGC		Second FET gate voltage control pin
3	FE.GND		
4	OSC		Oscillator pin The transistor and capacitors required for an oscillator circuit are built in. However, the oscillator buffer must be supplied externally. V_4 = 2.08 V

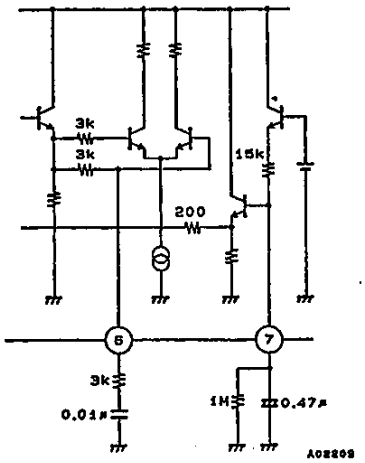
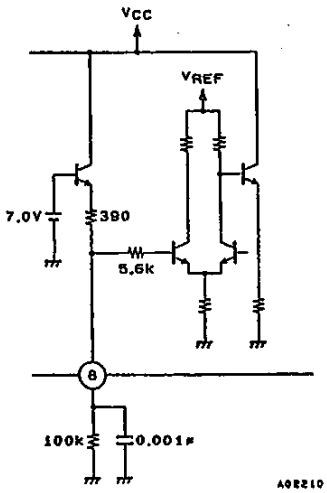
Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

<table>
<tr><th>Pin No.</th><th>Function</th><th>Equivalent circuit</th><th>Notes</th></tr>
<tr><td>5</td><td>SD
Stereo indicator
AM tweet reduction circuit</td><td> 

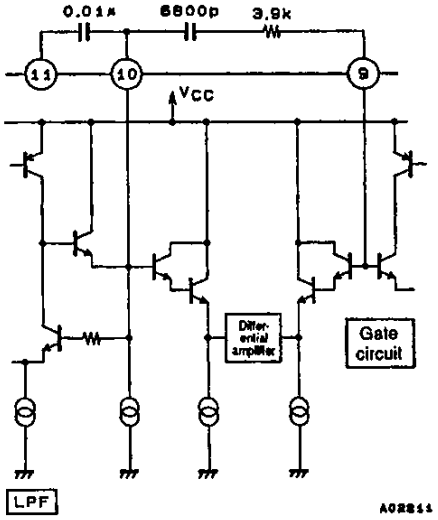
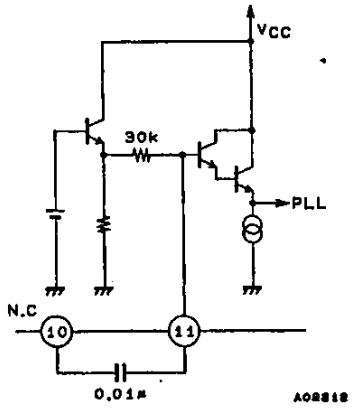
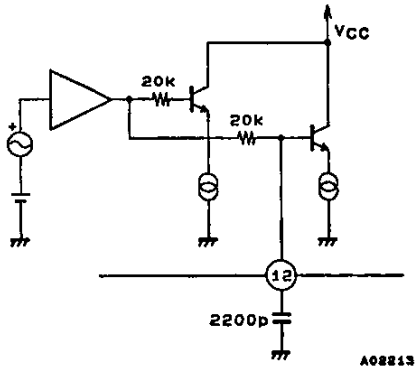
Turning this switch on in AM mode activates the tweet reduction circuit.</td><td>
<table>
<tr><th>AM</th><th>Function</th></tr>
<tr><td>Seek</td><td>SD output</td></tr>
<tr><td>Stop</td><td>Tweet reduction circuit</td></tr>
</table>
<table>
<tr><th>FM</th><th>Function</th></tr>
<tr><td>Seek</td><td>SD output</td></tr>
<tr><td>Stop</td><td>Stereo indicator</td></tr>
</table>
This pin is used for the four functions listed above.
Note: The stereo indicator is an active low signal, i.e., it goes low in stereo mode. It cannot drive an LED.</td></tr>
<tr><td>6
7</td><td>Noise AGC sensitivity
Noise AGC setting</td><td> 
</td><td>First set the pin 6 noise sensitivity field setting for medium field reception (about 50 dBμ). Then set up pin 7 for weak field reception (20 to 30 dBμ) for noise AGC sensitivity.</td></tr>
<tr><td>8</td><td>Monostable multivibrator time constant</td><td> 
</td><td>The noise exclusion is improved by setting the time constant of the circuit connected to this pin so that the gate time is increased by 40 μs. However, care is required in setting this value, since distortion due to multipath or overmodulation can become more noticeable.</td></tr>
</table>

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

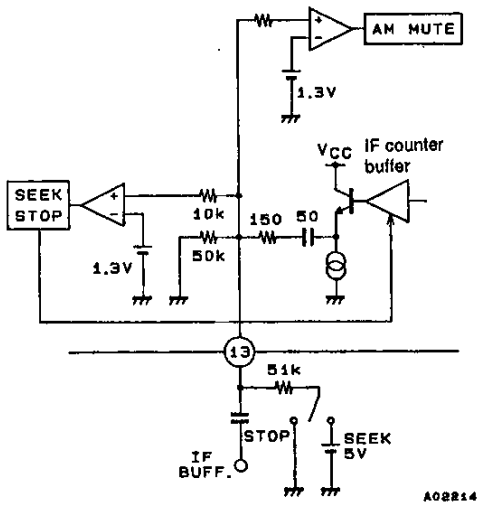
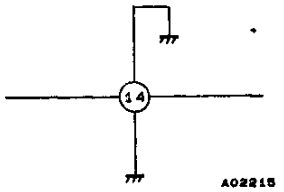
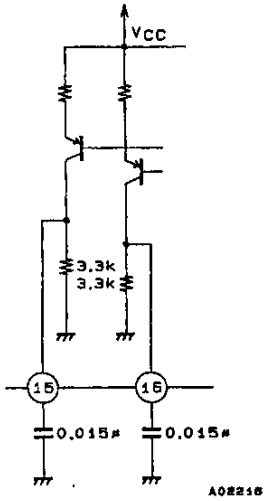
Pin No.	Function	Equivalent circuit	Notes
9 10	Voltage memory circuit		The memory circuit used during noise canceler operation
11	Pilot input		Pin 11 is the signal input pin of the PLL circuit.
12	HCC capacitor		The HCC frequency characteristics are determined by the capacitor connected to this pin.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

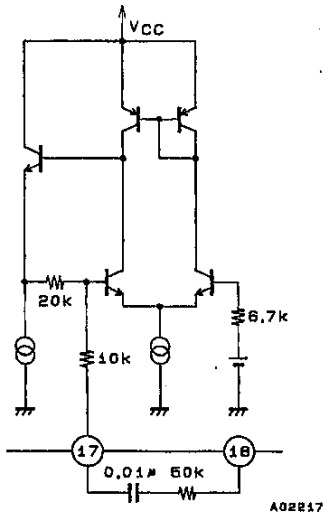
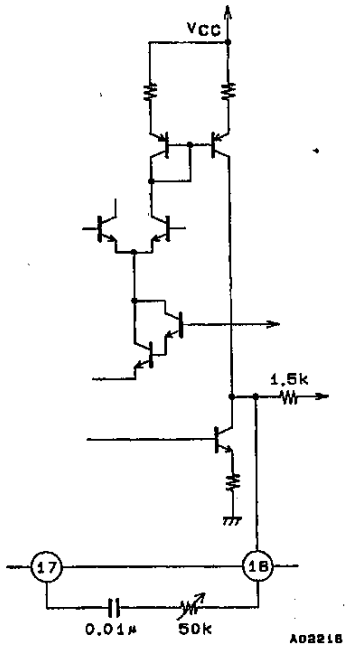
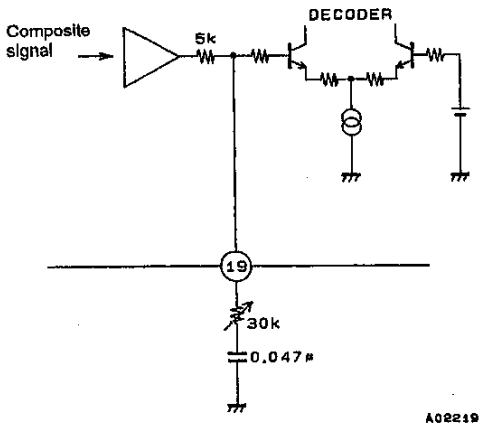
Pin No.	Function	Equivalent circuit	Notes
13	IF counter buffer Seek/stop switching		This pin is used for both the IF counter buffer (AC output) and switching for seek/stop.
14	NC MPX MRC GND		The ground for NC, MPX and MRC circuit
15 16	MPX output (left) MPX output (right)		0.015 μF is used for 50 μs de-emphasis (Japan). For 75 μs de-emphasis (USA) 0.022 μF is used instead of 0.015 μF.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

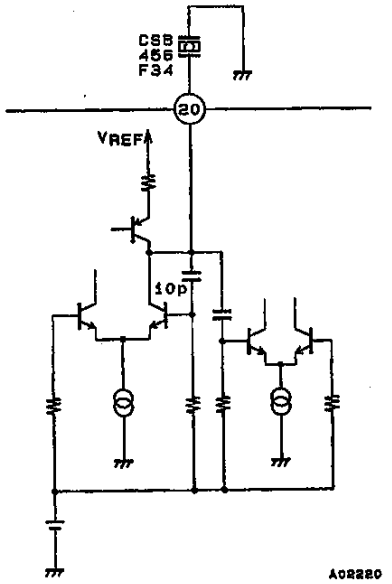
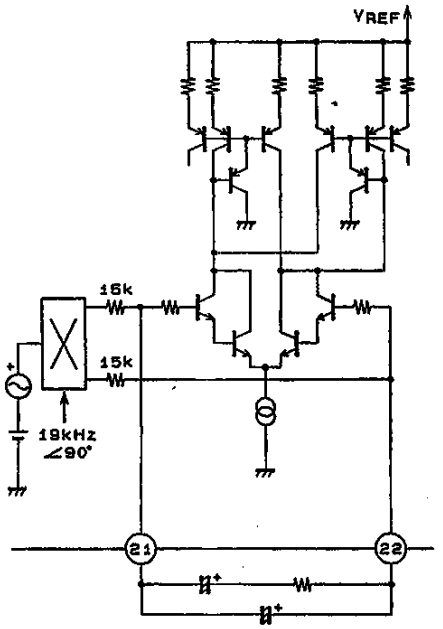
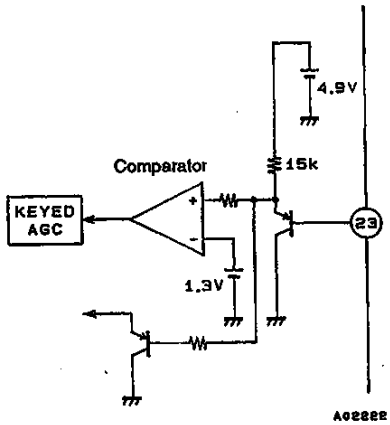
Pin No.	Function	Equivalent circuit	Notes
17	Pilot canceller signal input		The pilot signal level adjustment
18	Pilot canceller signal output		Pin 18 is the pilot canceller signal output.
19	Separation adjustment		The sub-decoder input level is changed using a trimmer connected to this pin. (The output levels in mono and main modes are not changed.)

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

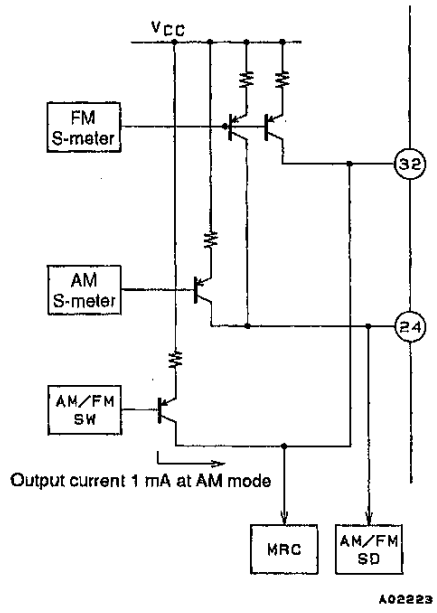
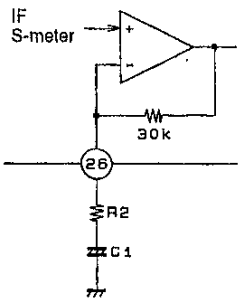
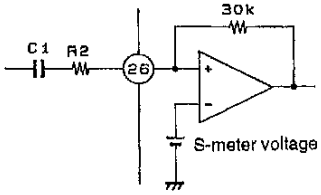
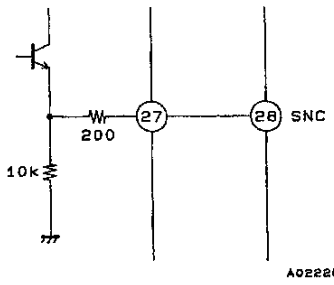
Pin No.	Function	Equivalent circuit	Notes
20	VCO		The oscillator frequency is 456 kHz.
21 22	Phase comparator		
23	Keyed AGC		The keyed AGC circuit starts operation when V23 becomes less than or equal to 0.5 V.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

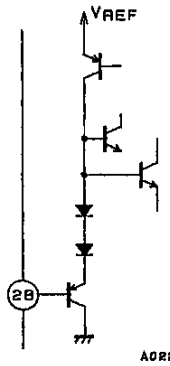
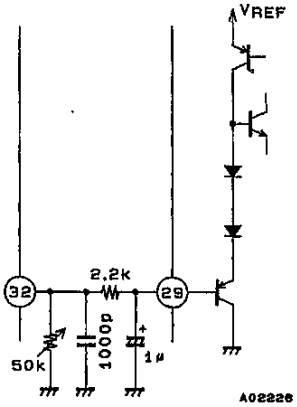
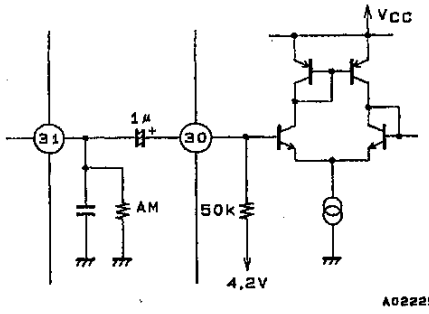
Pin No.	Function	Equivalent circuit	Notes
24 32	AM/FM S-meter Dedicated FM S-meter and MRC DC input		Fixed current drive type circuit The slope can be changed by changing the value of the S-meter output resistor. Since pin 32 outputs a 1 mA current in AM mode, HCC is turned off.
26	MRC AC input	 Figure 1 A02224  Figure 2 A02225	In techniques which directly detect the S-meter AC component, the noise amplifier gain is determined by the resistor R_2 (30 kΩ) in Figure 1. The frequency characteristics can be adjusted somewhat with the capacitor C_1. In techniques which detect the IF and S-meter high frequency components and in techniques which detect the NC HPF noise output, the noise amplifier gain is determined by the resistor R_2 (30 kΩ) in Figure 2. The frequency characteristics are determined by the capacitor C_1.
27	MRC output		

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

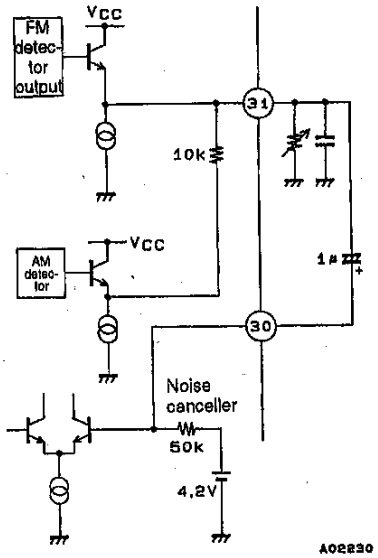
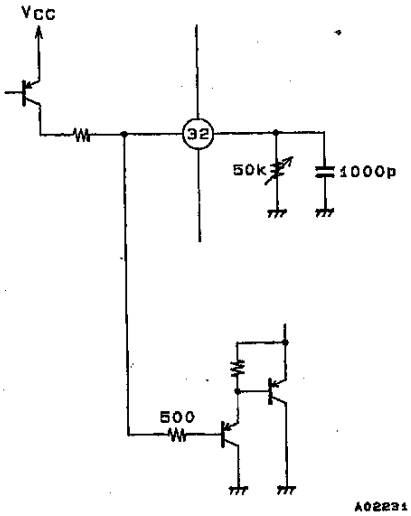
Pin No.	Function	Equivalent circuit	Notes
28	SNC control input		The sub-output level is controlled by the input DC voltage in the range 0 to 1 V.
29	HCC control input		
30	Noise canceller input		The input impedance is about 50 kΩ.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

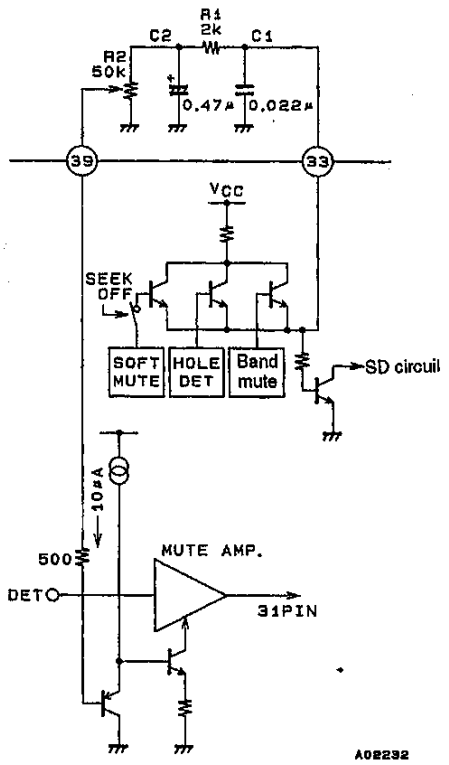
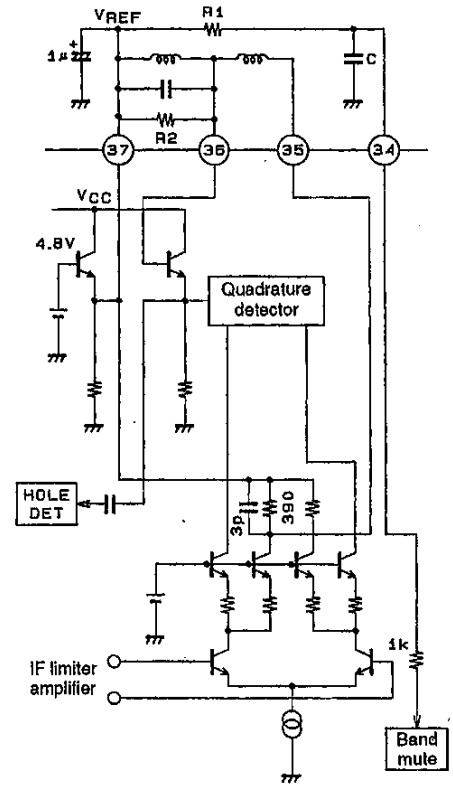
Pin No.	Function	Equivalent circuit	Notes
30 31	Noise canceler input AM/FM detector output		Pin 30: NC input Input impedance: about 50 kΩ Pin 31: AM and FM detector output FM mode: low impedance AM mode: output impedance is 10 kΩ
32	Dedicated FM S-meter output and MRC DC input		FM S-meter output block MRC DC input block

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

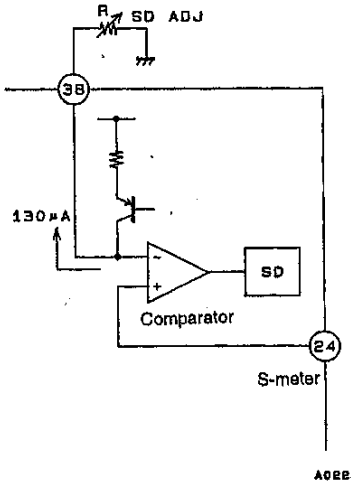
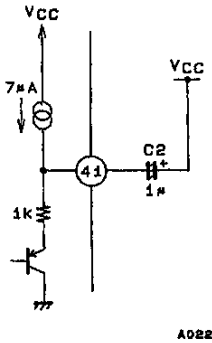
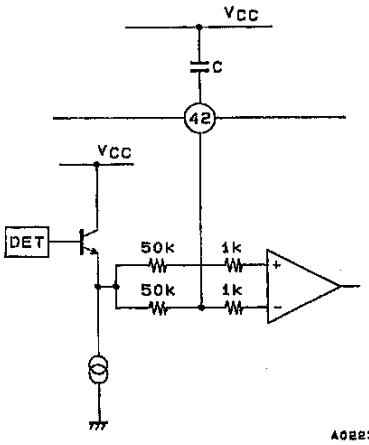
Pin No.	Function	Equivalent circuit	Notes
33 39	Mute drive output Mute input		• The muting time constants are determined by the external RC circuit as follows: Attack time: $T_A = R_1 \times C_2$ Release time: $T_R = R_2 \times C_2$ • Noise convergence adjustment When there is no input to the ANT input, V_{33} is divided by R_2 and input to pin 39. The noise convergence is maximum when V39 is 2 V. (The reference can be varied between 5 and 35 dB when the output is 1 kHz, 22 kHz dev.) • Muting off function The muting function is turned off when pin 39 is shorted to ground.
34 35 36 37	AGC QD output QD input Vref		• R_1 determines the muting bandwidth as follows: Increasing R_1 decreases the bandwidth. Decreasing R_1 increases the bandwidth. • Null voltage The voltage between pins 34 and 37 ($V_{34\text{-}37}$) is 0 V when locked (synchronized). The band muting is turned on when $\lvert V_{34\text{-}37} \rvert \geq 0.7$ V.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

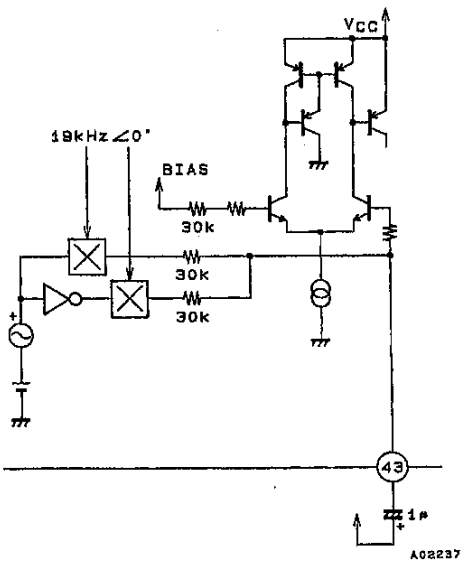
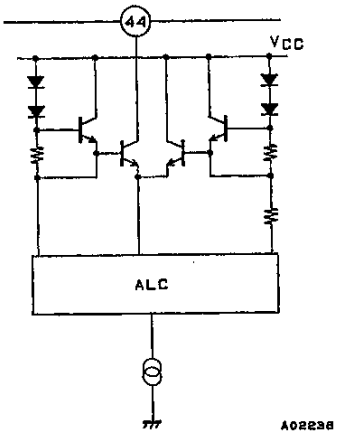
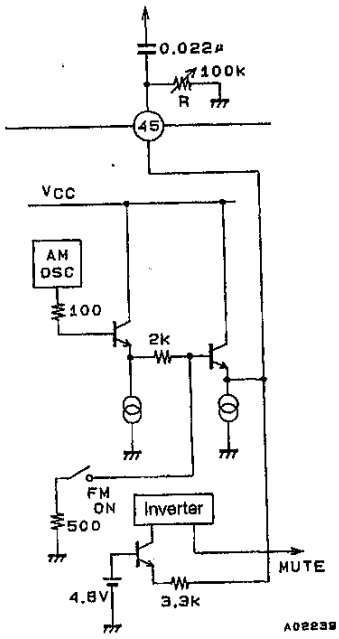
Pin No.	Function	Equivalent circuit	Notes
38	FM SD adjustment		A current of 130 μA flows from pin 38. The comparison voltage is determined by the external resistor R.
41	MRC Control voltage time constant		The MRC detection time constants are determined as follows: The discharge time is determined by a 1 kΩ resistance and C_2. The charge time is determined by a fixed 7 μA current and C_2.
42	AM LC		This pin is used to change the frequency characteristics for the unnecessary section of the audio band below 100 Hz, and to thus acquire clear audio. Note: The low-cut capacitor must be connected to V_{CC} (pin 40). This is because the detector circuit operates referenced to V_{CC}. The formula shown below determines the cutoff frequency f_C. $f_C = 1/2\,\pi \times 50\,k \times C$

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

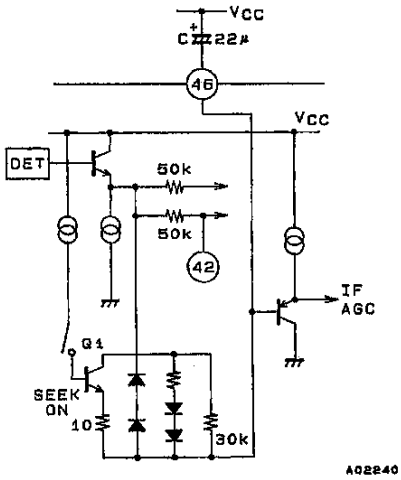
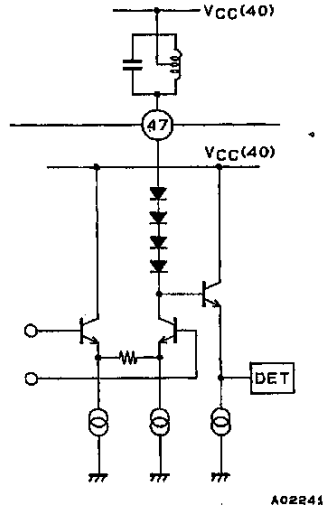
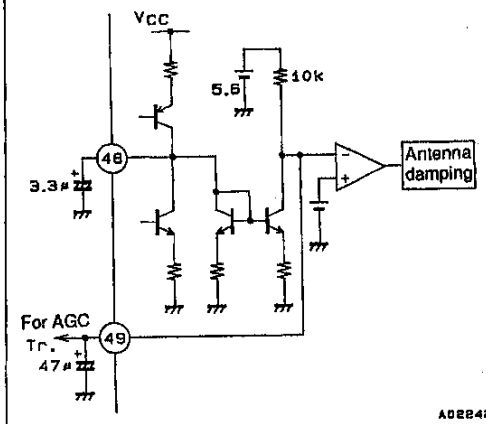
Pin No.	Function	Equivalent circuit	Notes
43	Pilot detector		The system can be forced to mono by adding a 1 MΩ resistor in paralle with the 1 µF capacitor.
44	AM OSC		AM oscillator This circuit can operate through the SW band. It includes an ALC circuit.
45	AM oscillator buffer FM mute on adjustment		Since this pin is used by both the AM and FM bands, oscillator buffer output is available up to the MW band. Note: An external transistor oscillator buffer is required for the SW band. The muting activation level is adjusted by varying the external resistor.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

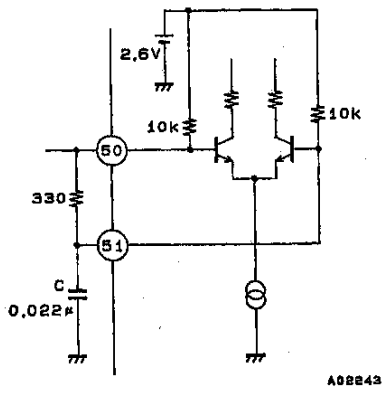
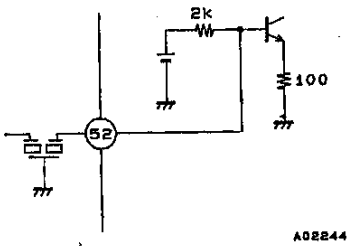
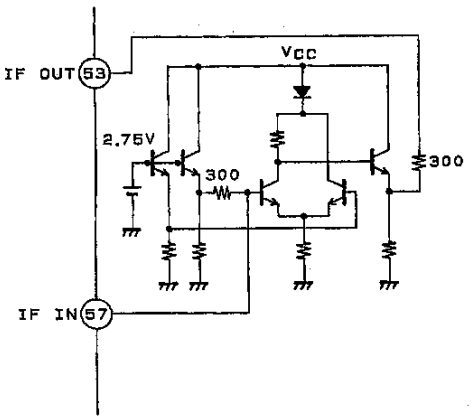
Pin No.	Function	Equivalent circuit	Notes
46	IF AGC		Q_1 is a switch for changing the seek time function time constant. Diodes; 22 µF The diodes are used for discharge. • Reception $\tau = 22\ \mu \times 30$ k • Seek $\tau = 22\ \mu \times 10$ The external capacitor is connected to V_{CC}. This is because the IF amplifier uses V_{CC} as a reference.
47	IF output		IF amplifier load
48 49	RF AGC bypass RF AGC		RF AGC rectification capacitor This capacitor determines the distortion for low frequency modulation. Increasing C48 and C49 improves distortion but slows the response time.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

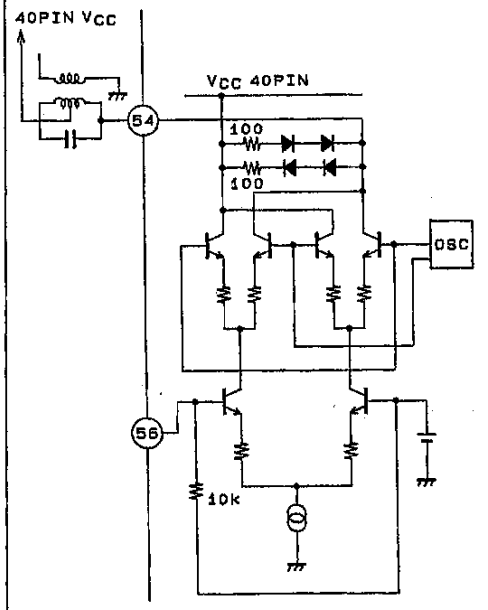
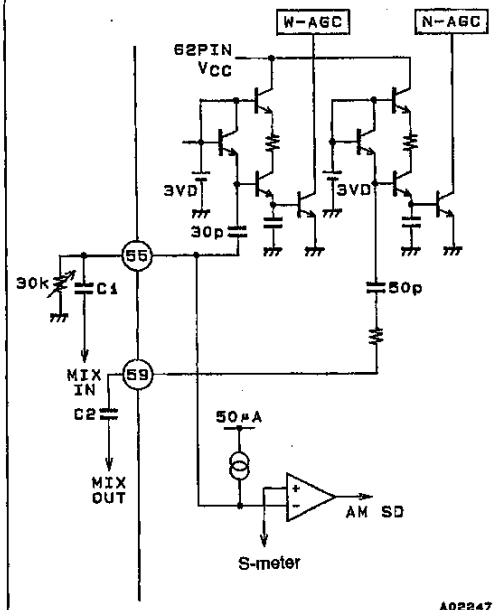
Pin No.	Function	Equivalent circuit	Notes
50 51	FM IF input IF bypass		Because the limiter amplifier has high gain, use care when choosing the grounding point for the limiter amplifier input capacitor to prevent oscillation.
52	IF input		The input impedance is 2 kΩ.
53 57	IF amplifier output IF amplifier input		• First IF amplifier input pin • Inverting amplifier V_{57} = 2 V The input impedance R_{IN} is 330 Ω. V_{53} = 5.3 V The output impedance R_{OUT} is 330 Ω.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

Unit (resistance: Ω, capacitance: F)

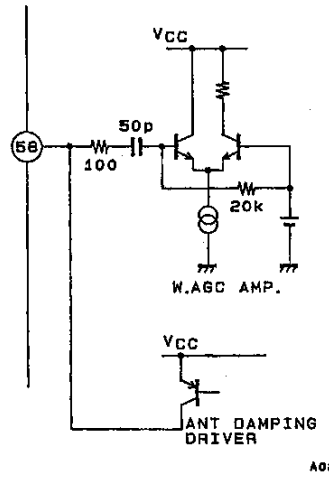
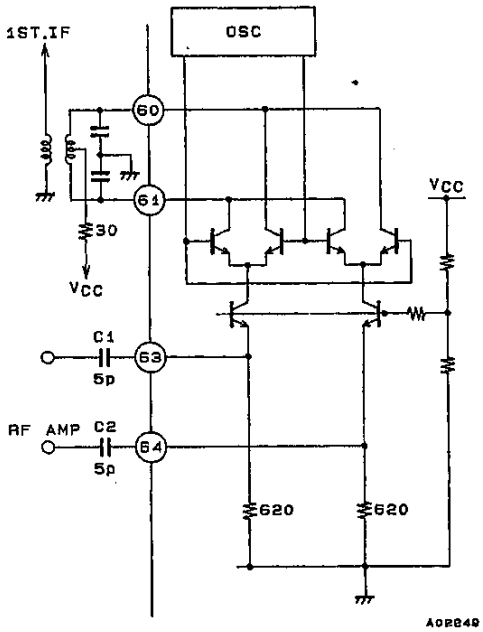
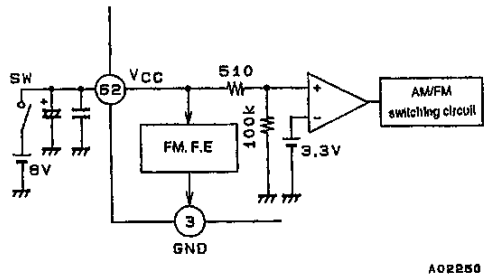
Pin No.	Function	Equivalent circuit	Notes
54 56	Mixer output Mixer input		The mixer coil connected to pin 54 mixer output must also be connected to pin 40 (V_{CC}). Pin 56 is the mixer input. The input impedance is 10 kΩ.
55 59	W-AGC input AM SD adjustment N-AGC input		The pin 56 and pin 59 circuits include built-in DC cut capacitors. The values of capacitors C_1 and C_2 determine the AGC activation level. Pin 55 is used for AM mode SD sensitivity adjustment. The current (I55) output from pin 55 is a fixed 50 μA. V55 is therefore determined by the value of pin 55's external resistor. This circuit compares V55 to the S-meter voltage to operate the SD function.

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

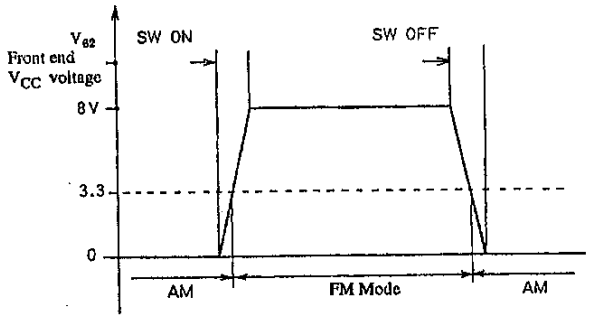
Unit (resistance: Ω, capacitance: F)

Pin No.	Function	Equivalent circuit	Notes
58	AM Antenna damping drive output Wide band AGC Input		I58 = 6 mA Antenna damping current
60 61 63 64	Mixer output Mixer input		Double balance mixer Pins 60 and 61 are the mixer output and provide a 10.7 MHz output frequency. Pins 63 and 64 are the mixer input. This circuit is an emitter insertion type circuit, and the insertion level is determined by capacitors C_1 and C_2. Note: Lines from pins 63 and 64 must not be located in the vicinity of lines from pins 60 and 61.
62	Front-end V_{CC} AM/FM switching		Pin 62 is used both as the FM front-end V_{CC} and as the AM/FM switch. V_{62} voltage → Mode 8 V → FM Open → AM

Downloaded from Elcodis.com electronic components distributor

Application Notes

1. Pin 62: AM/FM switch (front-end V_{CC}) block
   Pin 62 is also used as the front-end V_{CC}. When the FM front-end is operated, the IC automatically switches to FM mode. The switching reference voltage is 3.3 V.



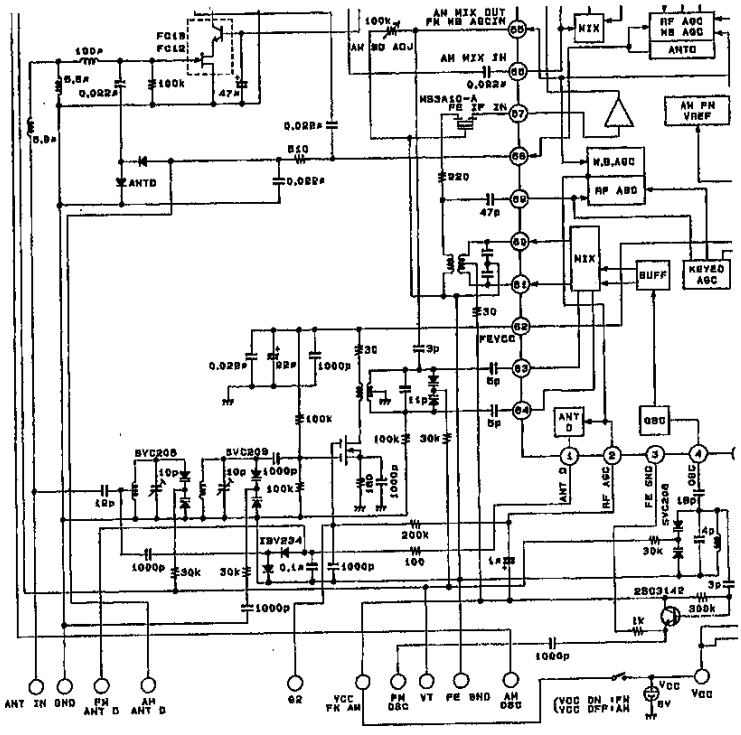
Pin 62	Mode
8 V	FM
Open	AM

Figure 1

2. Pin 5: AM/FM SD, stereo indicator and AM tweet reduction circuit
   Pin 5 is used for four functions: AM/FM SD, stereo indicator and AM tweet reduction. During a seek operation (when pin 13 is high), it functions as the AM/FM SD. In FM reception mode, it functions as the stereo indicator (active-low). In AM reception mode, setting pin 5 low increases the RF AGC activation level by 10 dB and thus functions as a tweet reduction measure.

3. FM front-end block
   Interference characteristics
   The LA1888NM incorporates a newly developed 3D-AGC (triple dimension AGC) circuit. This circuit achieves improvements in both the three signal interference characteristics (intermodulation characteristics) and the two signal sensitivity suppression characteristics. Improving both of these characteristics at the same time had previously been considered difficult.

   3-1. Intermodulation characteristics
   The LA1888NM prevents IM (intermodulation) by applying wide-band AGC in duplicate.



Unit (resistance: Ω, capacitance: F)

Figure 2

Downloaded from Elcodis.com electronic components distributor

As shown in Figure 2, the LA1888NM includes a double AGC system; a narrow AGC (pin 59 mixer input detection type) and a wide AGC (pin 55 input). Figure 3 shows the antenna input frequency characteristics.

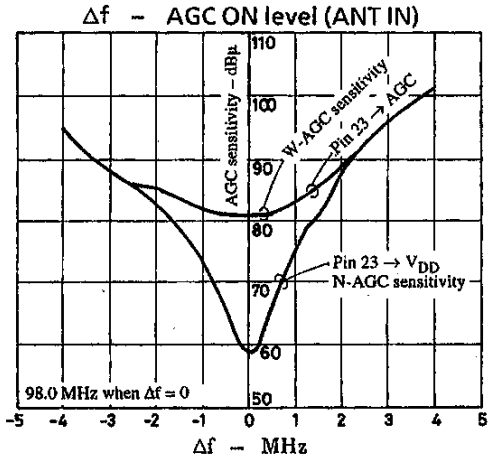


Figure 3

Double Wide AGC System Features

— Since the wide AGC is a mixer input detection type circuit, it prevents the occurrence of intermodulation due to interference sources with a Δf of over 1 MHz. (TV band interference prevention)

— For the adjacent channel interferences, the narrow-band AGC is activated, therefore the sensitivity of the wide-band AGC can be set low so as not to respond to the local oscillator output leakage.

— Since the sensitivities of both the wide and narrow AGC circuits can be adjusted with external components, optimum sensitivities for the field conditions can be set up.

— Since the input level of the desired station can be limited by the narrow AGC, excessive levels will not be input to the MIX and beating at multiples of 10.7 MHz is reduced.

3-2. Two signal sensitivity suppression characteristics

Until now, keyed AGC systems have been used to achieve good intermodulation characteristics and good two signal sensitivity suppression characteristics at the same time. However, in keyed AGC systems, the wide band AGC would become essentially inactivated for weak signals. As a result, the automatic station selection function would operate incorrectly and blocking oscillation would occur in the presence of strong interfering stations. Thus these systems were difficult to apply in actual use. To resolve these problems, we developed a new AGC system (3D-AGC) whose application circuits are extremely simple, and incorporated this system in the LA1888NM.

What is 3D-AGC?

3D-AGC is Sanyo's unique system that determines the wide-band AGC level using information that has three frequency characteristics, as shown below.

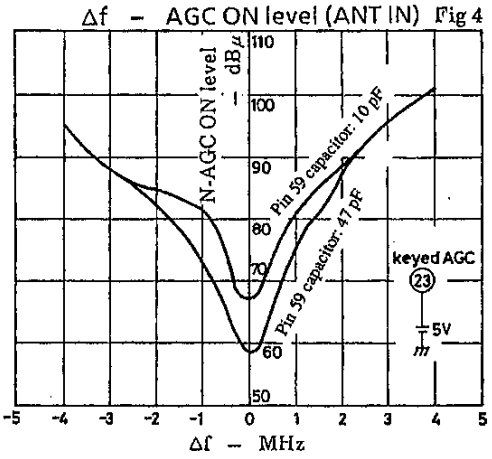
Information from RF and antenna circuit	Mixer input AGC	Three dimensions
Information from MIX circuit	Mixer output AGC	
Information from IF circuit with ceramic filter selectivity	S-meter output	

Downloaded from Elcodis.com electronic components distributor

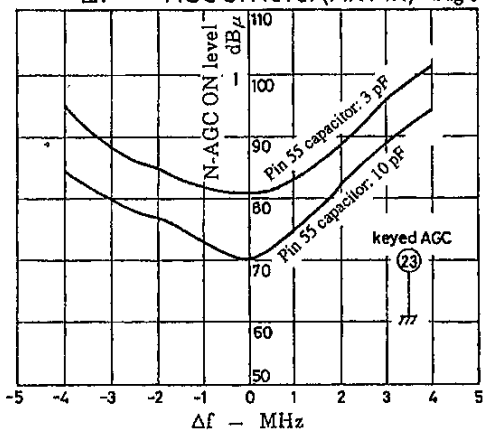
3-3. 3D-AGC Features

Feature	Merit
The 3D-AGC system controls the narrow AGC sensitivity (operation at $\Delta f < 1.5$ MHz) only according to field strength of the desired station.	• Effective as a measure for two signal sensitivity suppression.
It controls the narrow AGC sensitivity at $V_{23} < 0.5$ V.	• Allows the circuit to function as a measure for two-signal sensitivity suppression without degrading the three signal characteristics.
The wide AGC operates even at $V_{23} = 0$, i.e., even when there is no desired station.	• It is possible to prevent incorrect stopping during seek due to intermodulation occurrence. • Allows the prevention of the occurrence of intermodulation in the presence of a strong field interfering station. Blocking oscillation due to AGC operation can be prevented.
The sensitivities of the narrow and wide AGC circuits can be set independently. See Figures 4 and 5.	• Optimal settings for given field conditions are possible.
It includes double AGC systems, a narrow AGC and a wide AGC. See Figure 6.	• Since the narrow AGC operates at the desired station and at adjacent stations, the wide AGC sensitivity can be suppressed and incorrect AGC operation due to local oscillator jump-in prevented.

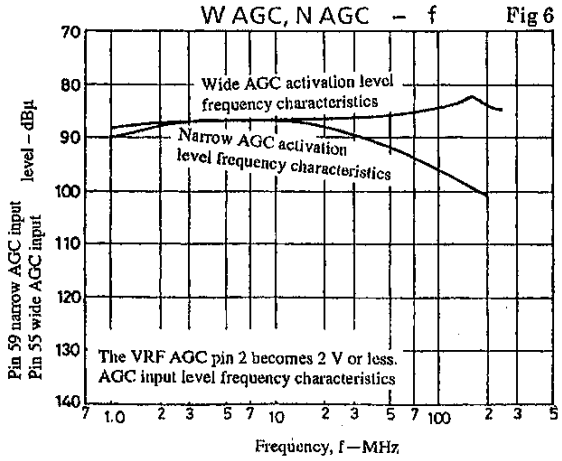
Δf – AGC ON level (ANT IN) Fig 4



Δf – AGC ON level (ANT IN) Fig 5



W AGC, N AGC – f Fig 6



Downloaded from Elcodis.com electronic components distributor

3D-AGC Sensitivity Characteristics

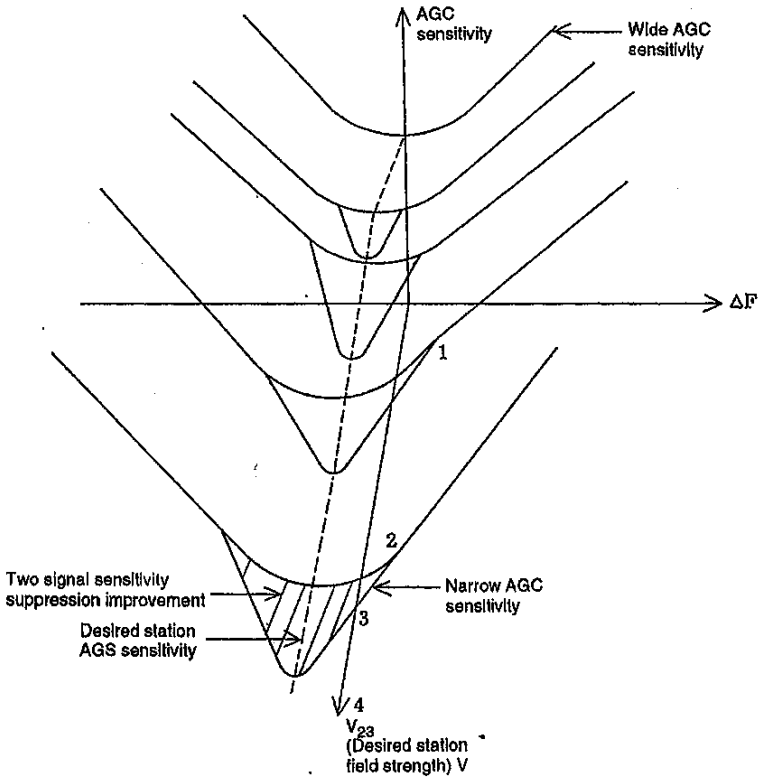


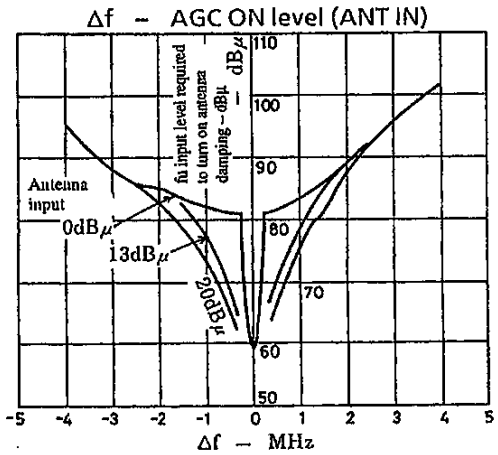
Figure 7

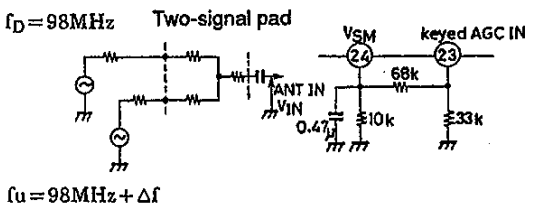
Figure 7: 3D-AGC sensitivity, Δf, and V_{23} characteristics

— The wide AGC sensitivity characteristics determined by the antenna RF circuit selectivity regardless of the value of V_{23}.

— The narrow AGC sensitivity characteristics is determined by the total selectivity of the antenna, RF and MIX circuits when V_{23} is 0.5 V or higher.
When V_{23} is less than 0.5 V, the narrow AGC is not activated.

— The improvement in two signal sensitivity suppression is indicated by slanted line shading in the figure and corresponds to the portion of the total AGC sensitivity due to the narrow AGC.
Figure 8 shows the actual operation of this function.





Unit (resistance: Ω, capacitance: F)

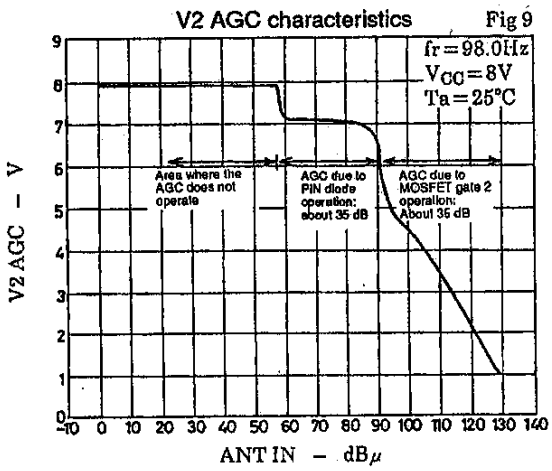
Figure 8

Downloaded from Elcodis.com electronic components distributor

3-4. There are two AGC circuits in the LA1888NM front-end block.
— Pin diode antenna input limiter
— FET second gate control

Pin 59 is the AGC input, and the AGC circuit is activated by inputs of about 30 mVrms or greater.

AGC Operation
The PIN diode drive circuit activates when $V_{CC} - V_2$ is over 1 V (approx.) and it applies input limitation at the antenna circuit. In application circuits the attenuation will be on the order of 30 to 40 dB. Following drive circuit activation, a current adequate for operation flows in the antenna attenuator PIN diode. When the impedance falls, the FET second gate voltage falls and the FET gm falls and then the AGC operates. We recommend using the Sanyo 3SK263 as the FET. Since this device is an enhancement type MOSFET, full AGC is applied when the voltage VG2-S (the voltage between the second gate and the source) is zero. Note that AGC will not be applied until $V_{G2\text{-}S}$ is less than zero if a depletion type MOSFET is used.



3-5. Mixer
The LA1888NM mixer is a balanced input, balanced output, double balance type mixer circuit.

Input circuit type: Emitter input
Input impedance: 25 Ω

The following characteristics were achieved by optimizing the element morphologies and the emitter current.

MIXer input practical sensitivity: 15 dBμ
MIXer input IMQS: 90.5 dBμ
(The oscillator level will be 200 mVrms at this time.)

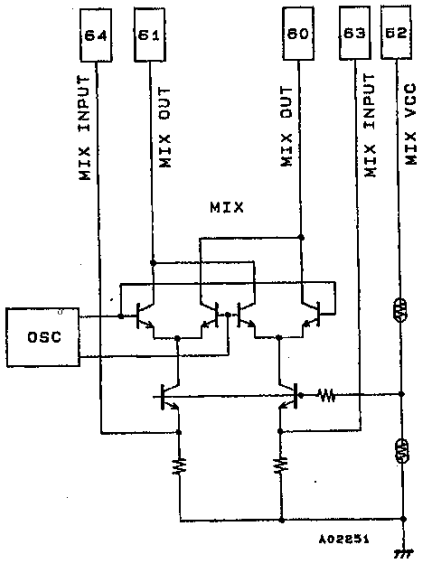


Figure 10 Mixer Circuit
(Improved by 6.5 dBμ over previous products.)

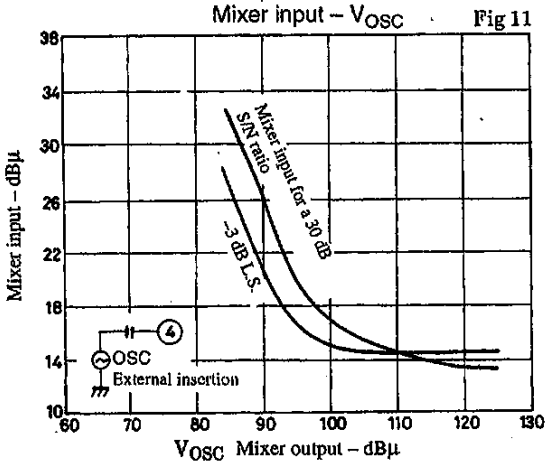
MIXer input IMQS is as follows:

f_r = 98.8 MHz, no input
f_{u1} = 98.8 MHz, 1 kHz, 30% modulation
f_{u2} = 99.6 MHz, no modulation

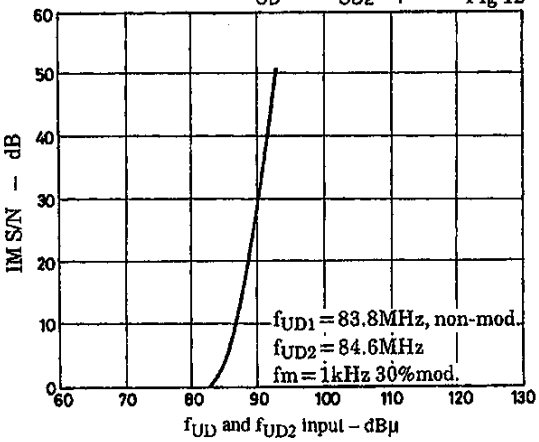
IMQS is the interference 1 and 2 input levels such that when an interference signal with the same level is input to the mixer and distortion occurs at the mixer, the generated IM output has a S/N ratio of 30 dB.

Downloaded from Elcodis.com electronic components distributor

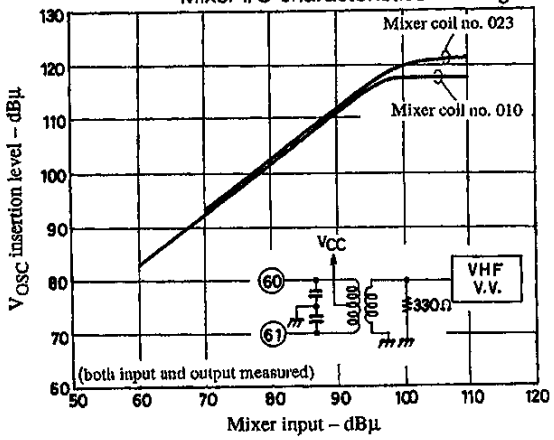
Mixer input – V_{OSC} Fig 11

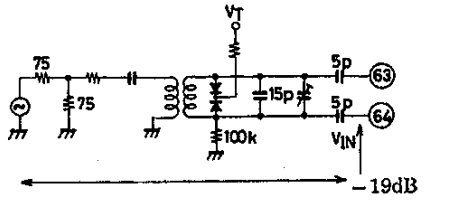


IM S/N – f_{UD} and f_{UD2} Input Fig 12



Mixer I/O characteristics Fig 13

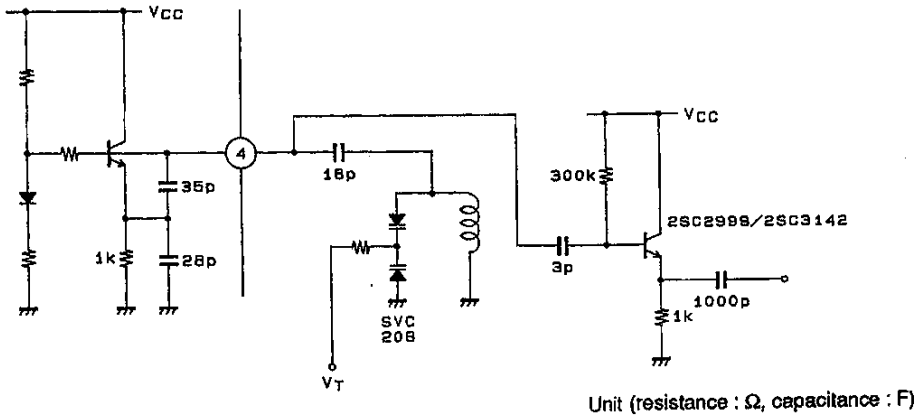




Unit (resistance : Ω, capacitance : F)

3-6. Oscillator

The oscillator circuit in this IC is the clamp oscillator shown in Figure 14. An external oscillator buffer (one transistor) is required. The pin 4 oscillator level must be 200 mVrms to achieve optimum practical sensitivity and limiting sensitivity at the mixer input . It is best to pick up the signal from pin 4 (the IC side of the 18 pF capacitor) to assure that the oscillator buffer circuit capacitance component does not influence the synchronization circuits. Also, note that the signal can be picked up from the coil side of the 18 pF capacitor to increase the oscillator buffer level. Currents of 2 mA or over are required in the 2SC2999 and the 2SC3142 to obtain good buffering from the oscillator buffer circuit.



Unit (resistance : Ω, capacitance : F)

Figure 14

A02252

Downloaded from Elcodis.com electronic components distributor

3-7. Since the FM first IF amplifier is an inverting amplifier (as shown in Figure 15), negative feedback can be provided by the resistor R_{NF}. (Note that R_{NF} must be over 2 kΩ.)

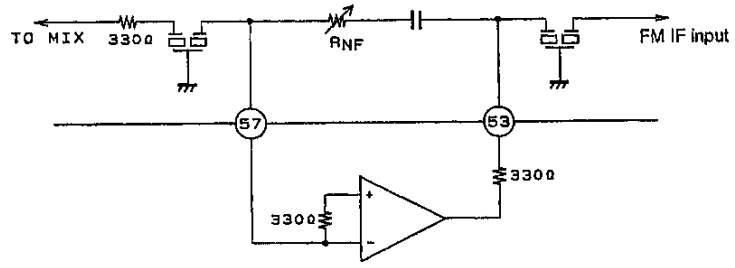
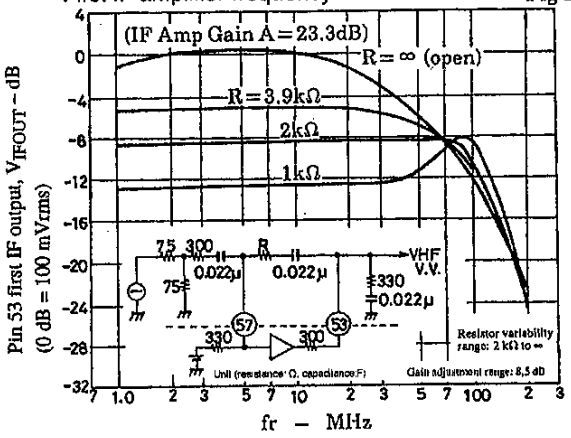
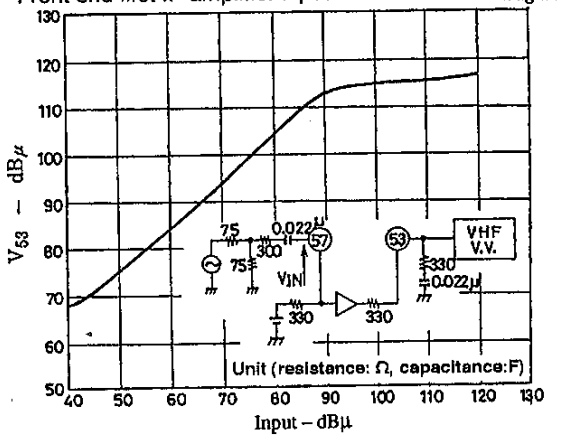


Figure 15

First IF amplifier frequency characteristics Fig 16



Front end first IF amplifier input characteristics Fig 17



4. FM IF block

4-1 FM SD and SD Adjustment

The FM SD and IF counter buffer circuits operate using the elements shown in the figure below.

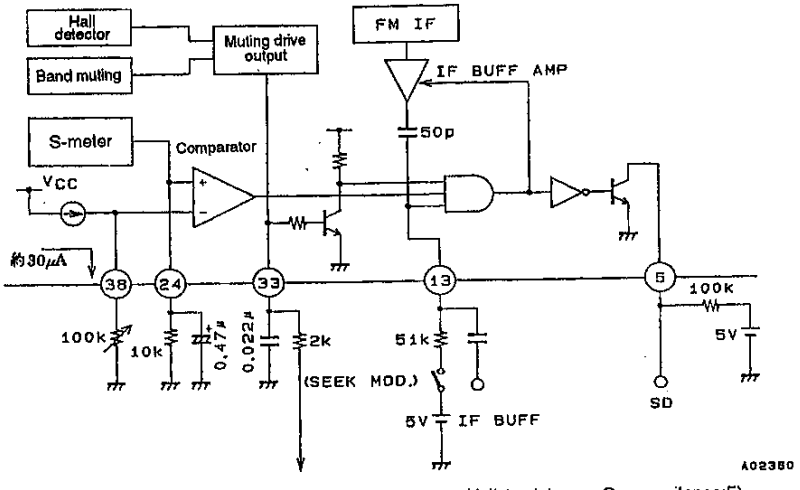


Figure 18 Unit (resistance: Ω, capacitance:F)

The following conditions must be met for the SD and IF counter buffer to operate.

— V24 > V38	The S-meter voltage must be higher than the pin 38 voltage.
— V33 < 0.7 V (V_{BE})	The hall detector and the band width muting functions must not be operating.
— V13 = High	A high level must be applied from the pin 13 through 51 kΩ resistor.

Downloaded from Elcodis.com electronic components distributor

Figure 19 shows the relationships between the FM SD, the IF buffer output, the S-meter and the muting drive output. (V62 = 8 V and V13 = high.)

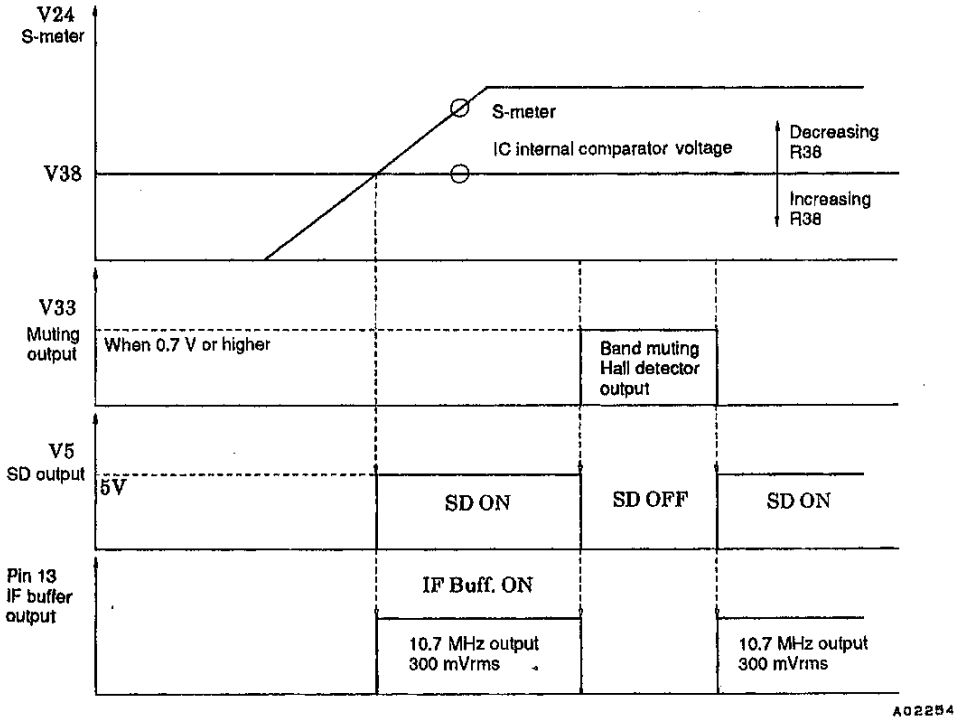
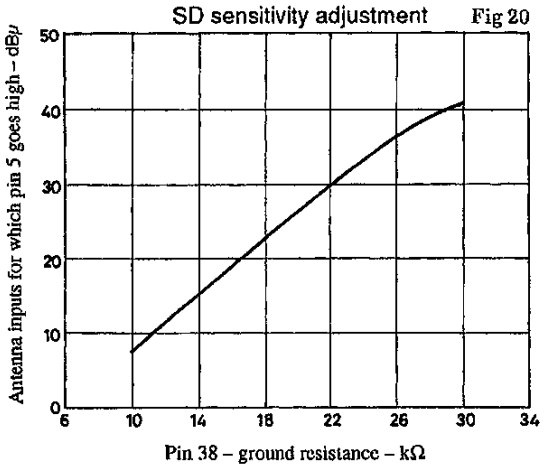


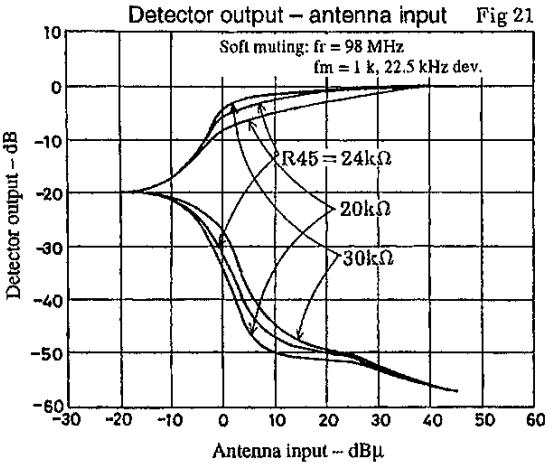
Figure 19 Relationships between FM S-meter, Muting Output, FM-SD and IF Buffer Output

As shown in Figure 19, even if the S-meter voltage is larger than V38, if the V33 muting drive output is over 0.7 V, the FM SD and IF buffer are turned off to prevent any erroneous stoppage of operation.



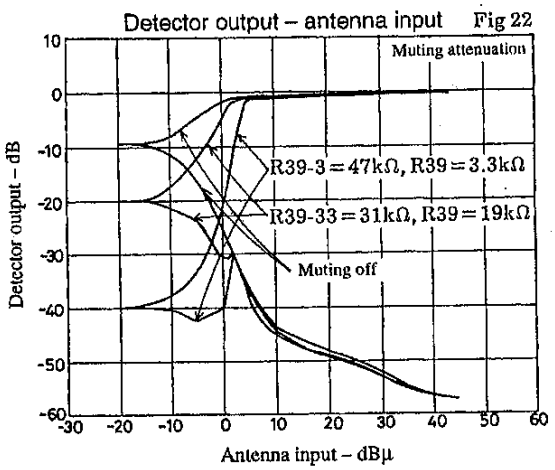
Downloaded from Elcodis.com electronic components distributor

4-2. FM Muting On, Pin 45 (R45 is a 100 kΩ variable resistor.)
By adjusting the value of R45, a –3 dB limiting sensitivity can be achieved.



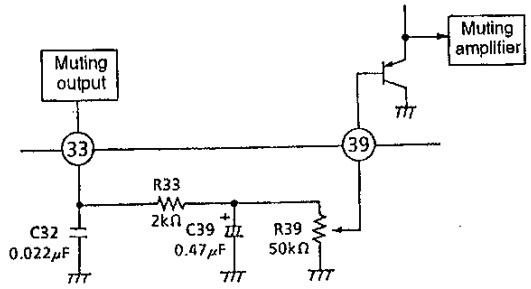
(Approximately, a 25 kΩ resistance is used for R45 to achieve a –3 dB limiting sensitivity.)

4-3. FM Muting Attenuation Adjustment, Pin 39 (R39 is a 50 kΩ or 30 kΩ variable resistor.)
Pin 33's voltage is divided by the variable resistor R39 and the input to pin 39. The noise convergence is determined by the voltage at pin 39 when there is no input signal.



(The LA1888NM is designed for a noise convergence of between 10 and 40 dB.)

4-4. Muting Time Constant
The DET output level changes associated with field variations during weak field reception can be made smoother by setting the soft muting operation attack and release times in this IC.



Attack time setting
$\tau a = R33 \times C39 = 940\ \mu s$
Release time setting
$\tau r = C39 \times R39 = 23500\ \mu s$

Figure 23

Downloaded from Elcodis.com electronic components distributor

4-5. FM Muting Off Function

Muting is turned off when pin 39 is forced to ground.

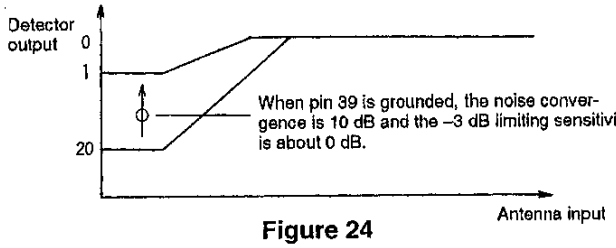
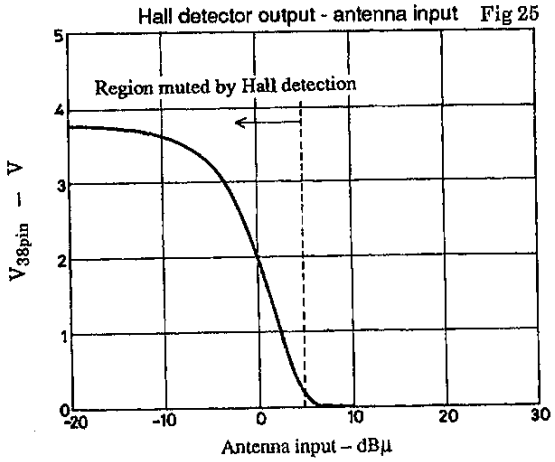


Figure 24

4-6. Hall Detector

The hall detector detects the level of the quadrature input signal at pin 36 performs peak detection, and finally outputs the result from pin 33. There are three cases where this is useful.

— Weak input muting operates reliably for antenna inputs of 5 dBμ or under. The attenuation is variable over the range 10 to 40 dB when there is no input referenced to an antenna input of 60 dBμ, fm = 1 kHz, 22.5 kHz dev. Thus one feature is that the weak input noise attenuation and the –3 dB limiting sensitivity for 5 dBμ or greater signals can be set independently.



— When the quadrature input at pin 36 is saturated and the antenna input has a field strength of 5 dBμ or greater. In locations where abrupt field fluctuations occur or where multipath is severe, pin 36 noise level detection is performed (Va) and a peak hold function is applied to pin 33 (Vb). Muting is operated by the voltage Vc, which is created by integrating and rectifying that signal. This reduces the noise generated by the detector.

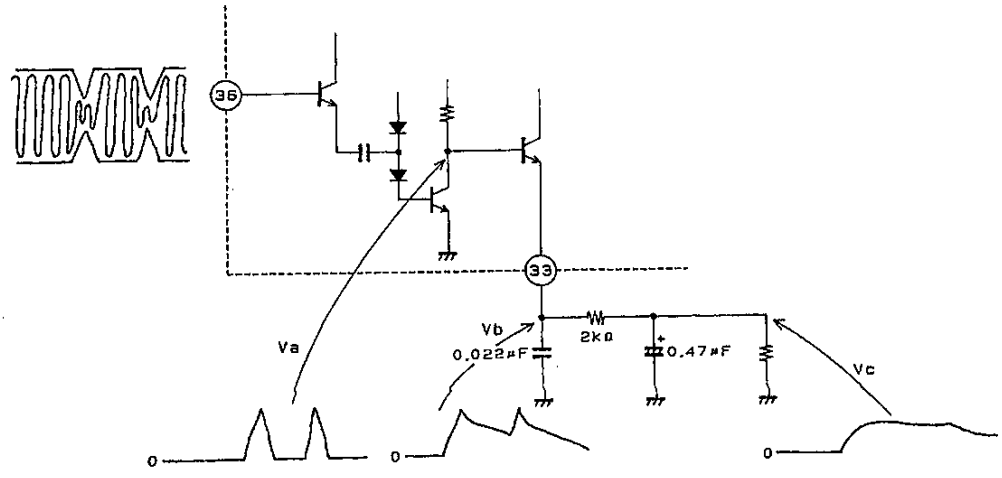


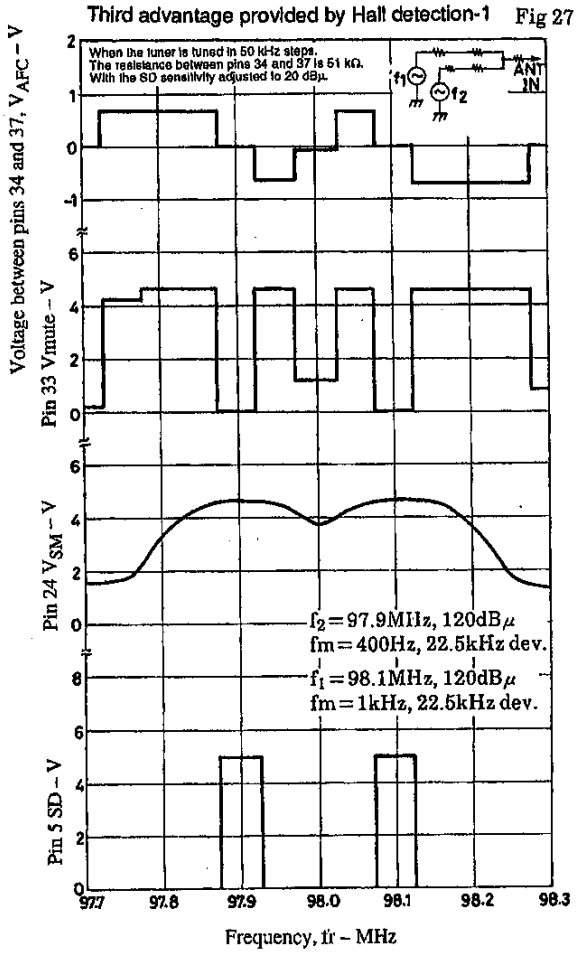
Figure 26 Hall Detector Weak Input Muting

A02255

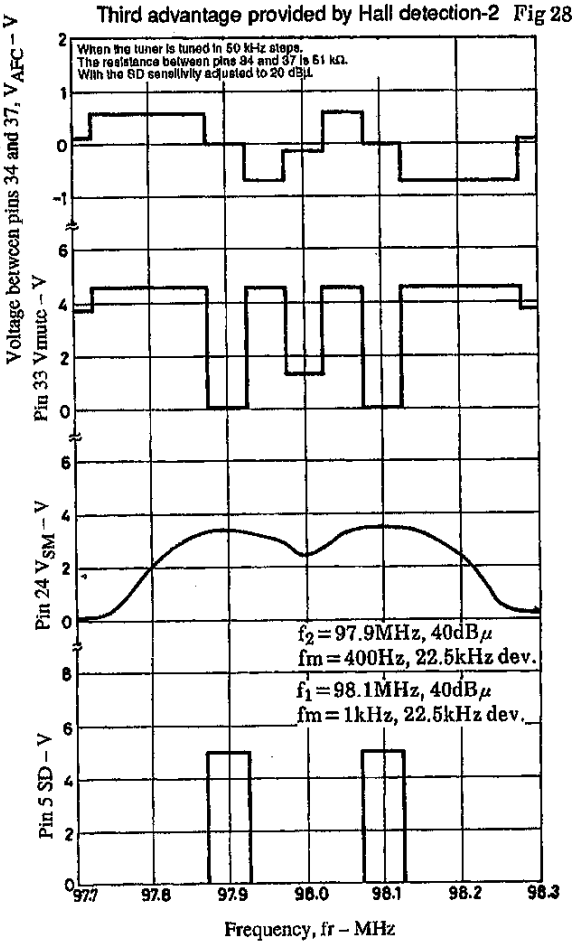
Downloaded from Elcodis.com electronic components distributor

— For the third advantage of this circuit, consider the case where there are two adjacent broadcast stations at f_1 = 98.1 MHz and F_2 = 97.9 MHz. This circuit has the feature that during a seek operation it will not incorrectly stop at 98.0 MHz. As shown in Figures 27 and 28, since V_{AFC} = 0 V and V_{SM} = 3.6 V at 98.0 MHz, the SD signal will be high. However, in the LA1888M, since the hall detector operates, V_{Mute} becomes 1.2 V (which is over 0.7 V), and SD goes low, this incorrect stop is prevented.

Third advantage provided by Hall detection-1 Fig 27



Third advantage provided by Hall detection-2 Fig 28



4-7. Quadrature Input Level

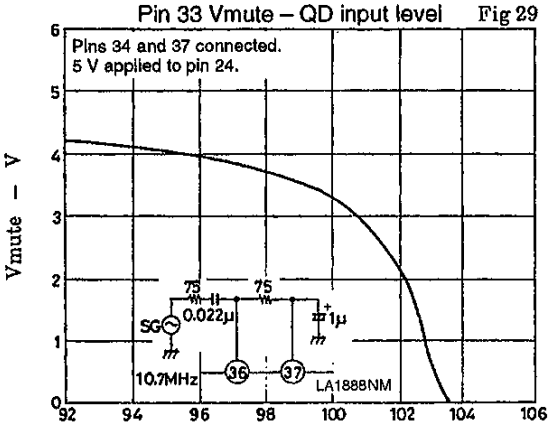
The quadrature input signal at pin 36 must be at least 200 mVrms in strong field reception. The design of the detector transformer and the damping resistor connected between pins 36 and 37 are critical.

(We recommend using the SA-208 (manufactured by Sumida Electric) for this transformer and a resister of 10 kΩ between pins 37 and 36.)

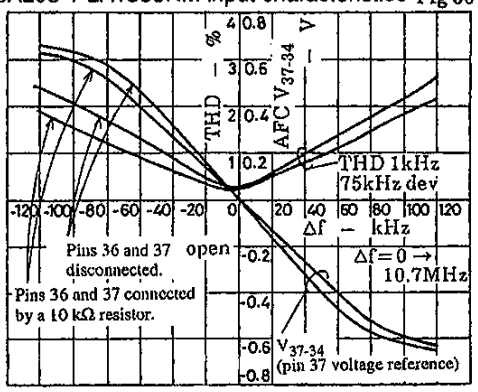
The hall detector operates when pin 36's input level falls below 160 mVrms and pin 33's muting drive output voltage increases. Therefore, if pin 36's input is between 160 and 200 mVrms in strong field reception, IC manufacturing variations can cause the muting circuit to operate and SD to not operate. This can reduce the audio output level. Thus, incorrect operation due to manufacturing variations and temperature characteristics can be avoided by assuring that pin 36's voltage is at least 200 mVrms in these conditions.

Downloaded from Elcodis.com electronic components distributor

Pin 33 Vmute – QD input level Fig 29



SA208 + LA1888NM input characteristics Fig 30



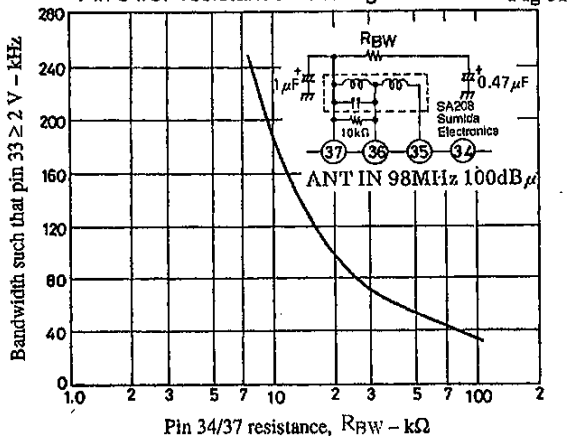
R_{36-37}	Detector output MPX out V_O	Pin 36 AC level QDIN
Open	330 mVrms	235 mVrms
10 kΩ	280 mVrms	200 mVrms

Unit (resistance : Ω, capacitance : F)

4-8. Bandwidth Muting Setting

The muting bandwidth can be changed with the resistor R_{BW} connected between pins 34 and 37 as shown in the figure below.

Pin 34/37 resistance – muting bandwidth Fig 31



4-9. Transient Response Characteristics for Automatic Station Selection

The transient characteristics for which the SD and IF counter buffer are turned on and off are determined by the time constants of the circuits attached to the pins listed below.

— Muting time constant: pin 33
— S-meter time constant: pin 24
— AFC time constant: pin 34

There are two points that must be investigated for high-speed station detection.

Downloaded from Elcodis.com electronic components distributor

— SD Time Constant Dependence on the S-Meter Time Constant

Since the current at pin 24 (I_{24}) varies with the field strength, the time constant changes. Since there is no hysteresis in the SD comparator. If C_{24} is reduced and pin 24's voltage is used by the keyed AGC (pin 23), then C_{23} must be chosen so that the AGC does not become unstable when the keyed AGC operates.

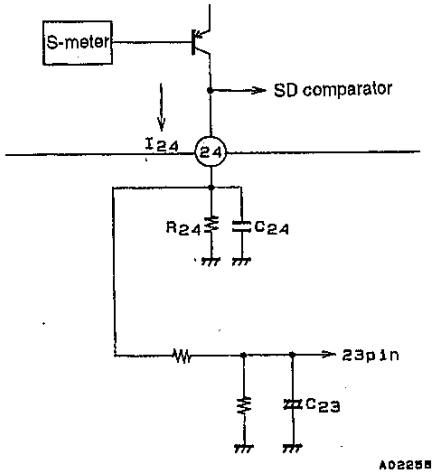
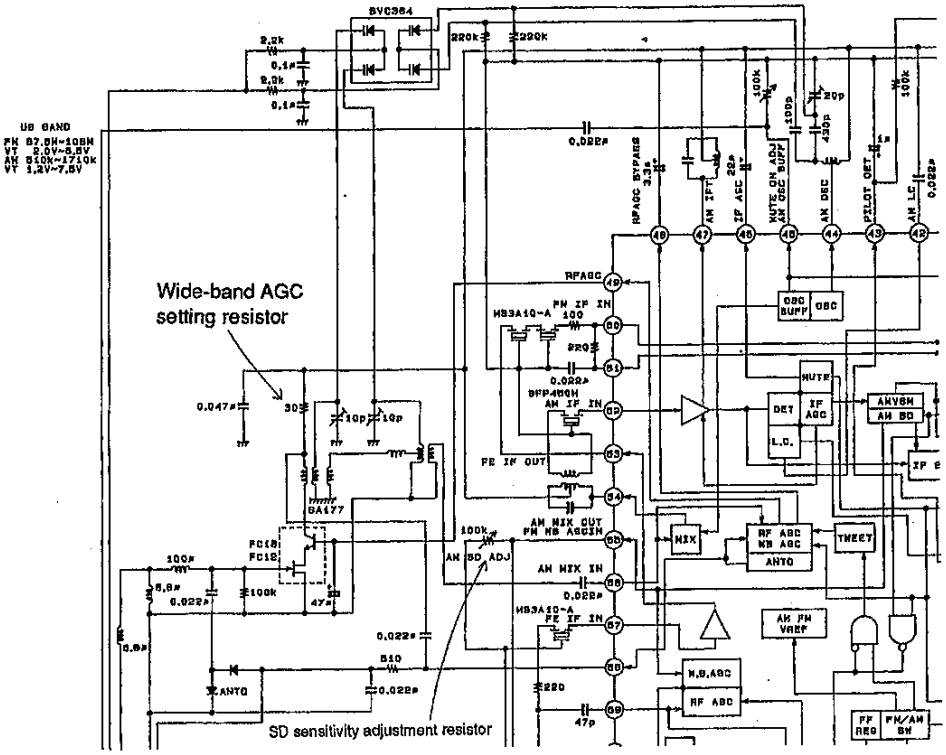


Figure 32

5. AM Tuner Block



Unit (resistance : Ω, capacitance : F)

Figure 33

Downloaded from Elcodis.com electronic components distributor

5-1. RF AGC

The LA1888NM incorporates double RF AGC systems.

— Mixer input level detector (pin 56)

— FET input level detector (pin 58)

These two systems operate as shown in the figure below.

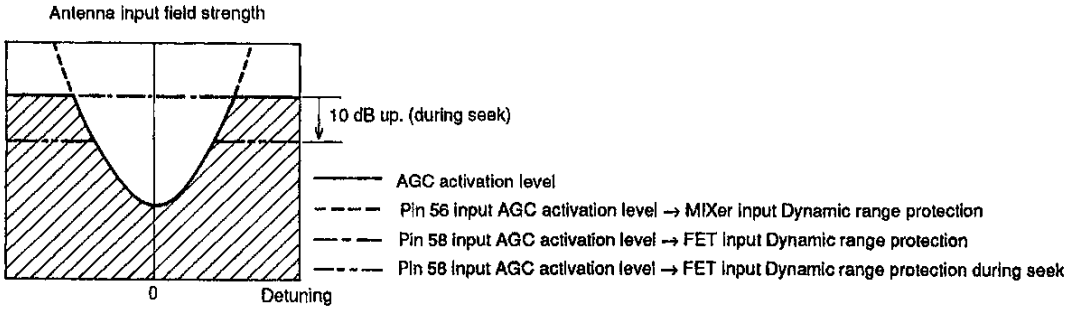


Figure 34 Detuning Characteristics in Wide Band AGC Operation

The procedure described below is used to change the AGC activation level for these two AGC systems.

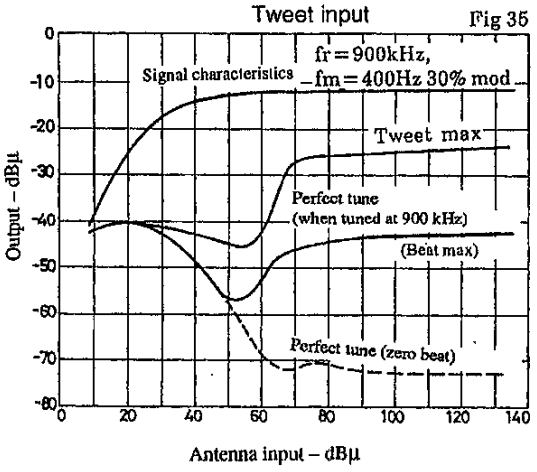
— AGC of mixer input level detector (RF AGC) (pin 56)

Since this AGC circuit is provided to protect the mixer input dynamic range, its activation level is determined internally. This AGC operates for both a desired station and adjacent stations. (i.e., adjacent stations within the ±40 kHz RF amplifier bandwidth) Stations within the RF bandwidth are controlled to lie within the shaded section in Figure 34 by this AGC. The LA1888NM also provides a function for varying the mixer input AGC activation level (the broken line with the single dot) in the figure. This function increases the AGC sensitivity by about 10 dB.

→ Figure 33 Tweet Improve BLOCK

Tweet reduction circuit

Figure 35 shows the detuning beat characteristics when fr is 900 kHz. With a standard input the minimum S/N ratio is about 30 dB.



Downloaded from Elcodis.com electronic components distributor

Tweet happened mechanism

The 900 kHz signal (fr) input to the antenna is amplified by an FET (RF amplifier) and input to the mixer after passing through the double tuned coils. However, the RF amplifier's varactor diode distorts on large input signals, generating a second harmonic (1800 kHz). These two signals are input to the mixer simultaneously. Furthermore, due to the dispersion in these signals, the following two IF frequencies are created.

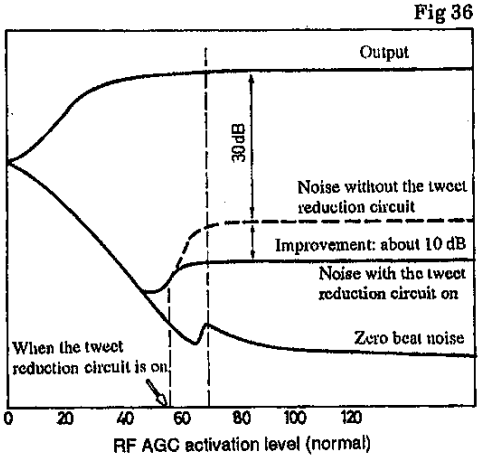
900 kHz → 450 + α kHz

1800 kHz → 450 + α kHz

These two signals generate a beat frequency of two times α kHz.

Improvement in the LA1888NM

Fig 36

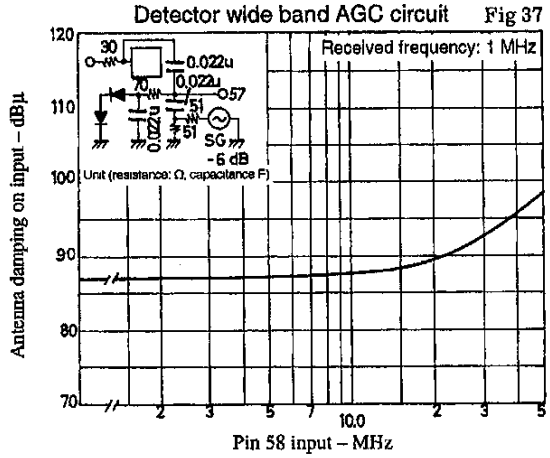


This circuit increases up the RF AGC activation level by about 10 dB only when fr is 900 kHz, and reduces the AC signal voltage applied to the varactor diode. The control microprocessor must determine when a signal with an fr of 900 kHz is being received and set the pin 5 potential to low. (It will be at the high level (V_{DD}) when the seek function is stopped.) This will increases the RF AGC activation level by about 10 dB resulting in S/N characteristics essentially equivalent to those shown in Figure 36.

The mixer input detector AGC circuit turns on when a signal of about 80 dBμ (10 mVrms) is input to pin 56. The AGC operation is controlled in two ways: by the antenna circuit output level and by the FET V_{DS}. When a 10 mVrms signal is input to pin 56, the DC voltage will fall, and when V49 falls under 2.5 V the pin diode drive circuit will operate. This holds the antenna circuit at a fixed level of about 60 to 70 dBμ. The antenna circuit level attenuation due to the pin diode is about 30 to 40 dB. When the PIN diode impedance falls completely, pin 49's DC voltage will begin to fall and the FET's V_{DS} will fall. This lowers the RF amplifier gain and holds the mixer input level fixed.

— AGC of FET input level detector (pin 58) (wide band AGC)

Detector wide band AGC circuit Fig 37



Downloaded from Elcodis.com electronic components distributor

The wide-band AGC circuit used in the LA1888M has the frequency response shown in Figure 37. The frequency characteristics for input to pin 58 are the same as the frequency characteristics for the RF amplifier. This AGC circuit is provided to prevent the FET from distorting when a strong station signal is input to the antenna circuit. The AGC activation level for this circuit can be set to an arbitrary level by varying the wide-band AGC adjustment resistor shown in Figure 33. Although the AGC activation level can be set by decreasing the resistance of this resistor, the higher AGC level may, depending on the type of FET used, require the use of the application circuit shown in Figure 38.

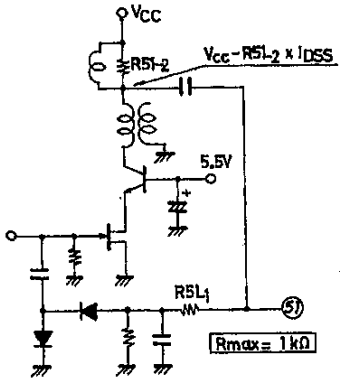


Figure 38

This circuit is designed so that it does not limit the dynamic range.
If there are problems with the dynamic range, a choke coil for DC bias may be required.

Since the load is parallel $R_{51\text{-}1}$ and $R_{51\text{-}2}$, if $R_{51\text{-}2}$ is over 100 Ω, $R_{51\text{-}1}$ must also be increased.

— Type of cascade transistor used for FET V_{DS} control

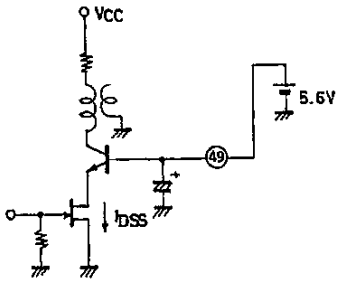


Figure 39

No input: $V49 \approx 5.6\ V - 10\ k \times \frac{I_{DSS}}{h_{FE}}$
h_{FE}: Cascade transistor
This means that it is desirable to use a low-noise and high-h_{FE} transistor as the cascade transistor to assure stability.

— Notes on double-tuned coil design

Double-tuned coils have the features that they provide a flat frequency response and only small changes in RF amplifier gain for small frequency mistuning. Thus sensitivity differences within the received band are minimal. However, in a double tuning circuit, three types of coupling can occur: loose coupling, critical coupling, and tight coupling. In particular, for tight coupling at an fr of 1400 kHz, it is possible for the two signal characteristics (when there is an interfering station at ±40 kHz) to be degraded as shown on next page.

Downloaded from Elcodis.com electronic components distributor

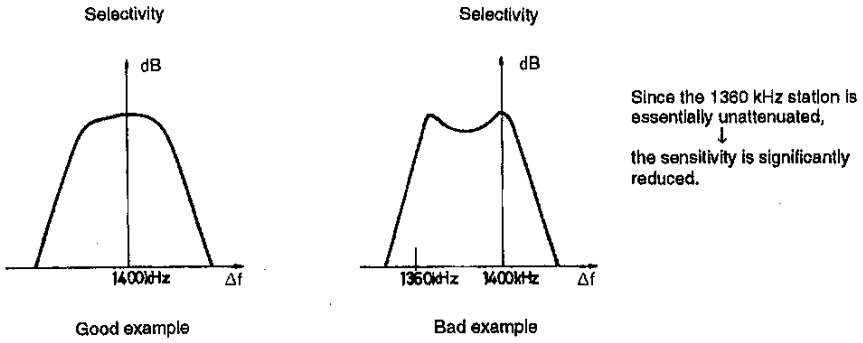


Figure 40

When evaluating the two signal characteristics for an f_D of 1400 kHz, if the characteristics for the upper and lower interfering characteristics at fu = 1400 ± 40 kHz are different, then the circuit corresponds to the bad example in Figure 40. Thus extra care must be taken when designing the coil.

The RF amplifier's gain increases if the number of windings in the primary side is increased in the coil shown in Figure 33, and the gain decreases if the number of windings is decreased. This can be used as an adjustment with almost no adverse consequences.

5-2. Oscillator Circuit

This oscillator circuit is capable of oscillating through the short wave band. However, the oscillator buffer (pin 45) is also used by the FM block and this oscillator buffer has frequency characteristics of its own. As a result the oscillator only functions through the medium wave band. An external oscillator buffer is required to use the LA1888NM for short wave reception. However, the LA1888NM corrects the problems in automatic station detection that occurred due to 50 to 100 MHz parasitic oscillation (that occurred in previous IC's).

5-3. AM SD (pin 5) and SD Adjustment

The SD and the IF buffer operate by comparing the V24 S-meter voltage and the V55 reference voltage, as shown in Figure 41.

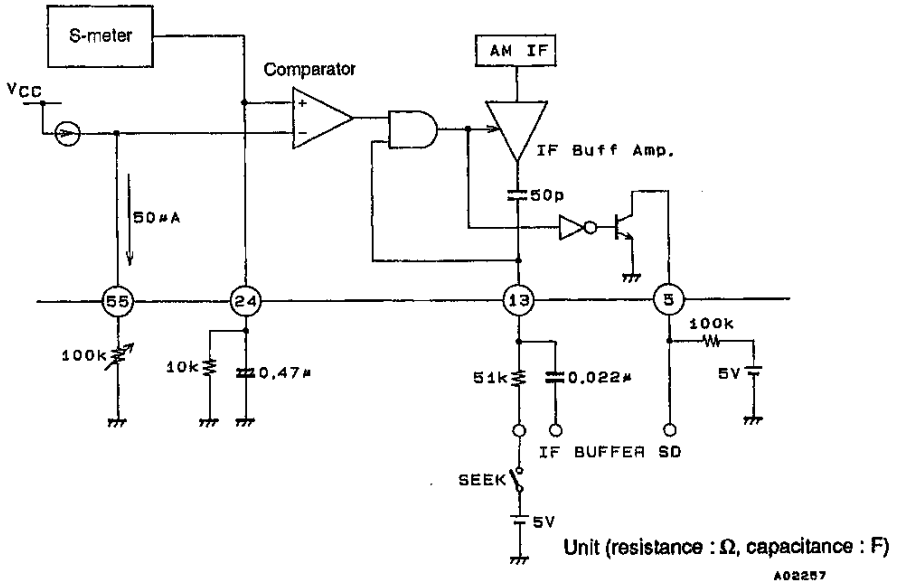


Figure 41

Downloaded from Elcodis.com electronic components distributor

Figure 42 shows the relationship between the AM SD signal (pin 5), the IF counter buffer (pin 13), and the S-meter (pin 24). However, note that this is for the case where V62 is 0 V and V13 is high.

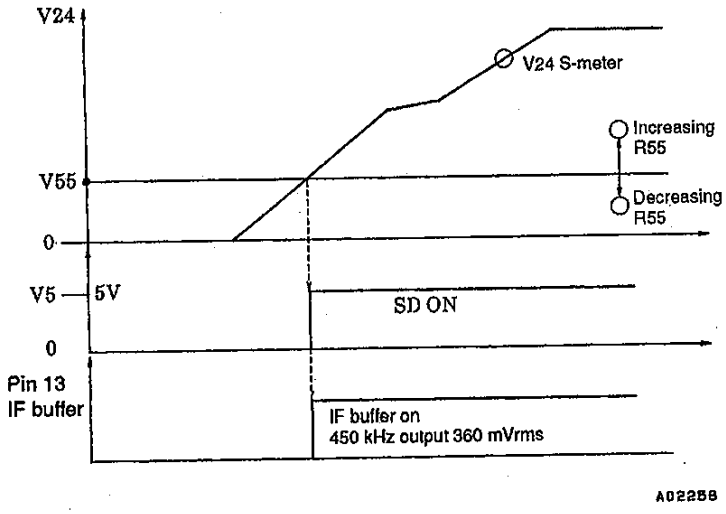
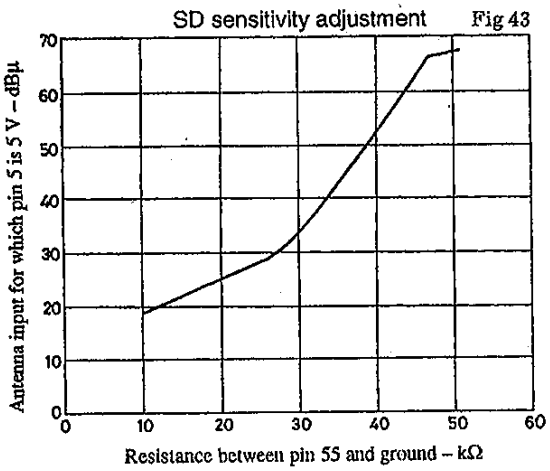


Figure 42 AM SD, IF Buffer, and S-Meter Relationship



5-4. The AM wide AGC sensitivity is about 95 dB at the antenna input. However, this is increased by about 10 dB (to 85 dB) in seek mode, when pin 13 is high.

Downloaded from Elcodis.com electronic components distributor

5-5. AM high-frequency cut and detector output level setting

The AM/FM detector output (pin 31) has an impedance of 10 kΩ in AM mode, and an impedance of a few tens of Ohms in FM mode. Therefore, R31 is used to set the AM detector output level and C31 to set the AM high frequency characteristics.

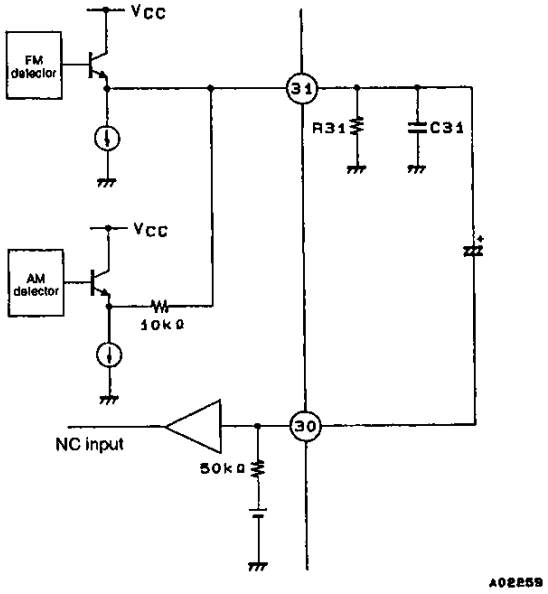


Figure 44

5-6. AM low-frequency cut setting

The AM low-frequency characteristics can be set with the external capacitor C42 connected between pin 42 and V_{CC}. C42 must be connected to V_{CC}, since the AM detector is designed with V_{CC} as the reference voltage.

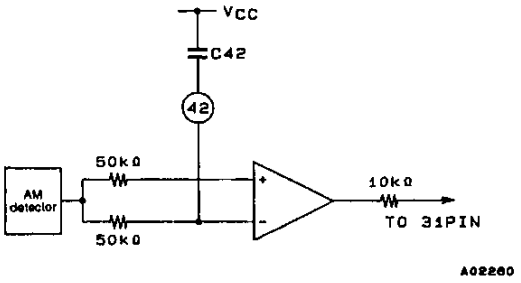
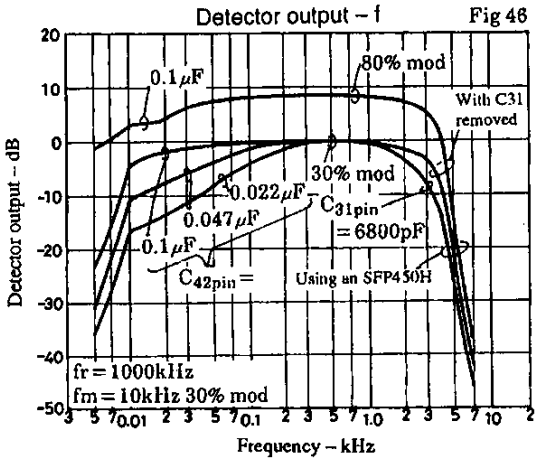


Figure 45



6. NC Block

6-1. The noise canceler input (pin 29) has an input impedance of about 50 kΩ. Keep the low-frequency characteristics in mind when determining the value of the coupling capacitor. Note that f_C will be 3 Hz if the application uses a 1 μF capacitor.

6-2. Pin 6 and pin 7 are used to set the noise detector and the noise AGC sensitivities. To achieve good settings, first set the noise sensitivity (pin 6) for medium field (an antenna input of about 50 dBμ) reception, and then set the AGC sensitivity (pin 7) for weak field (20 to 30 dBμ) reception. Note that although increasing the noise detector's sensitivity will cause an increase in the AGC sensitivity , it will reduce the noise detector sensitivity for weak field reception.

Downloaded from Elcodis.com electronic components distributor

6-3. The time constant of the monostable multivibrator (determined by pin 8) will be about 40 μs for a C of 1000 pF and an R of 100 kΩ. Increasing the gate time will increase the noise rejection. However, note that the distortion due to multipath or overmodulation will increase.

6-4. The noise canceler may function incorrectly if a 10 kHz overmodulated signal is input. The reason for this is that the IF detector output takes on the waveform shown in Figure 47 due to the IF ceramic filter band. (This figure is for an antenna input of 60 dBμ; bandwidth of ceramic filters are one 150 kHz and two 180 kHz performance; and 10 kHz modulation frequency, 180 kHz dev.) The noise canceler responds to the whisker components created by this overmodulation, and, as a result, distorts the audio output. (The whisker components due to the overmodulation are created by the ceramic filters.) The following circuit can be used to prevent this malfunction. The whisker components due to the overmodulation can be removed with a low-pass filter formed by a 1 kΩ resistor and a 2200 pF capacitor; however, it may change the FM separation characteristics (especially high frequency) and the AM frequency response.

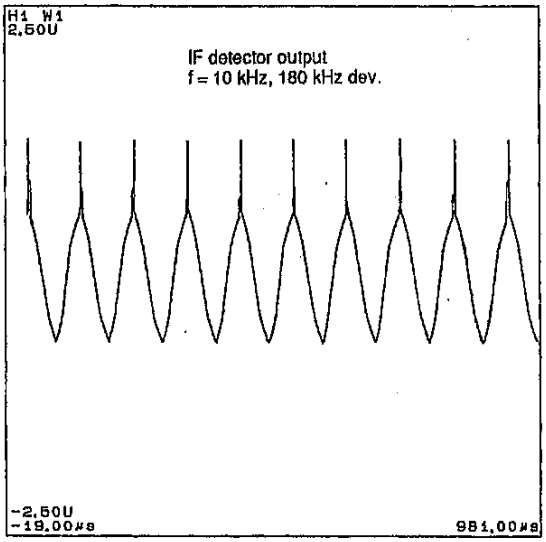


Figure 47

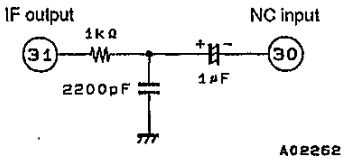


Figure 48

7. MPX Block

7-1. HCC (high-cut control) frequency characteristics (pin 12)
The capacitance of the external capacitor connected to pin 12 determines the audio output signal frequency characteristics during HCC control.

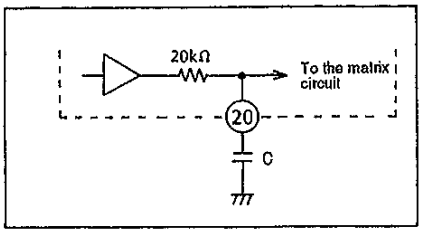


Figure 49

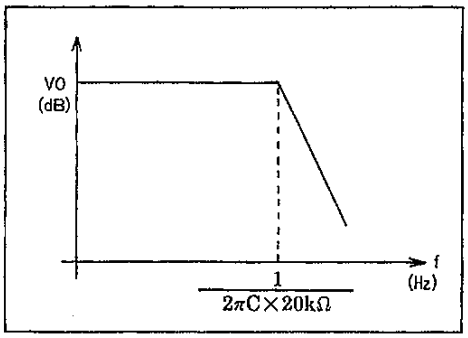
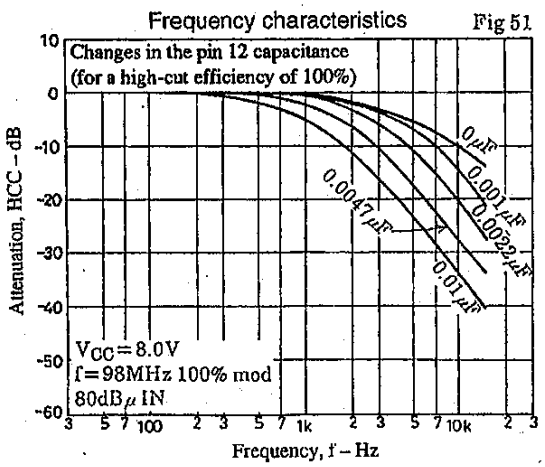


Figure 50

$$f_C = \frac{1}{2\pi \times C \times 20\ k\Omega}\ [Hz]$$

Downloaded from Elcodis.com electronic components distributor



7-2. Pilot canceller adjustment (pins 17 and 18)

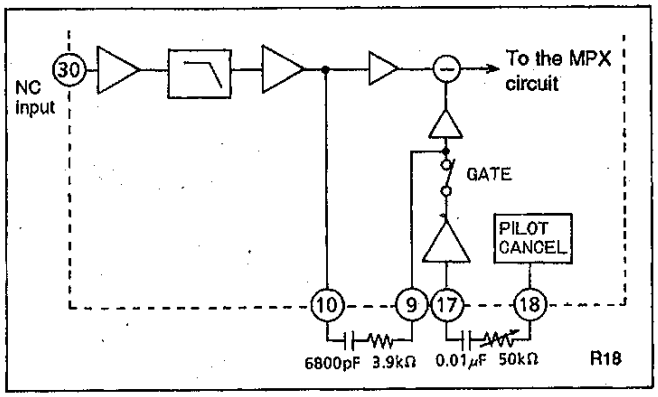


Figure 52

The pin 18 pilot canceler signal waveform is a 19 kHz signal that does not include a third and fifth harmonic component, as shown in Figure 54. Since this signal is in phase with the pilot signal, no capacitor is required between pin 18 and ground. Since it does not include a third and fifth harmonic component, good pilot cancelation in both the left and right channels can be achieved by adjusting the circuit with the trimmer R18.

7-3. Separation adjustment (pin 19)

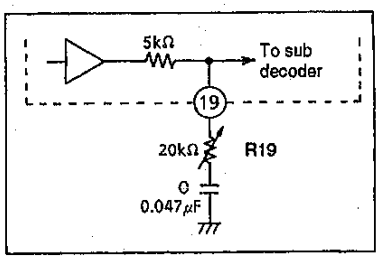


Figure 53

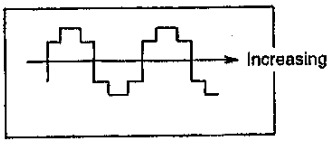


Figure 54

The separation is adjusted by varying the sub-decoder input level with the trimmer on pin 19. When the trimmer is changed, only the subcarrier level (L-R) changes; the mono (main) output level does not change. High frequency separation degradation in the decoder can be avoided in the subcarrier (L-R) frequency (23 to 53 kHz) by making the capacitance of the external capacitor C small compared to the resistance of trimmer R19.

Downloaded from Elcodis.com electronic components distributor

8. MRC Block

8-1. Figures 55 and 56 show two techniques for using the MRC (multipath rejection circuit). In Figure 55, multipath noise is directly detected by detecting the AC component of the S-meter signal and in Figure 56 the NC high pass filter noise is detected.

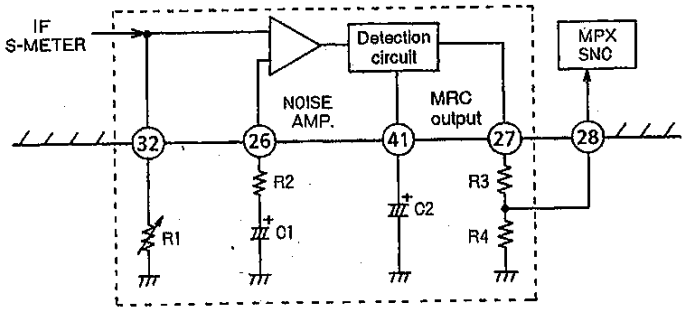


Figure 55 Application Circuit Using the AC Component of the S-meter

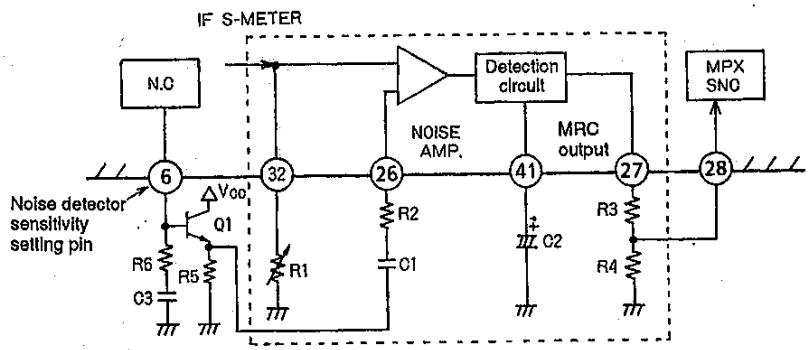


Figure 56 Application Circuit Using Noise Canceller High Pass Filter

8-2. In Figure 55, the noise amplifier gain is determined by R2 and an internal 30 kΩ resistance as shown in Figure 57. The capacitor C1 can be used to provide some degree of filtering characteristics.

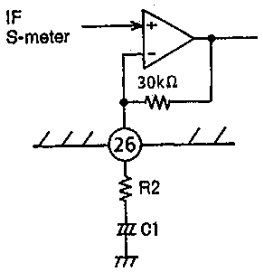


Figure 57

8-3. In Figure 56, the noise amplifier gain is determined by R2 and an internal 30 kΩ resistance as shown in Figure 58. The frequency characteristics are determined by C1.

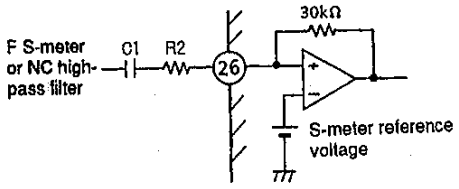


Figure 58

Downloaded from Elcodis.com electronic components distributor

8-4 The S-meter DC voltage input is set by the variable resistor connected at pin 32. Generally speaking, the curves shown in Figure 59 are ideal for separation control when multipath occurs, if the pin 32 voltage is too high, the separation control becomes difficult, as shown in Figure 60. Therefore it is desirable to adjust the pin 32 voltage so that it is 2 V or lower at saturation.

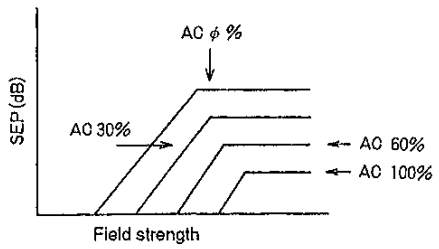


Figure 59

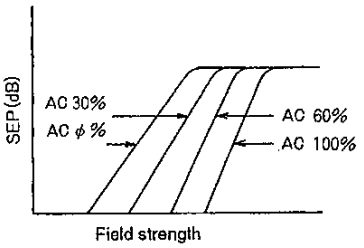


Figure 60

8-5. The MRC separation control time constants are determined by an internal 1 kΩ resistance and C2 on discharge, and by a fixed 7 μA current and C2 on charge.

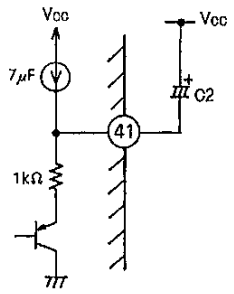
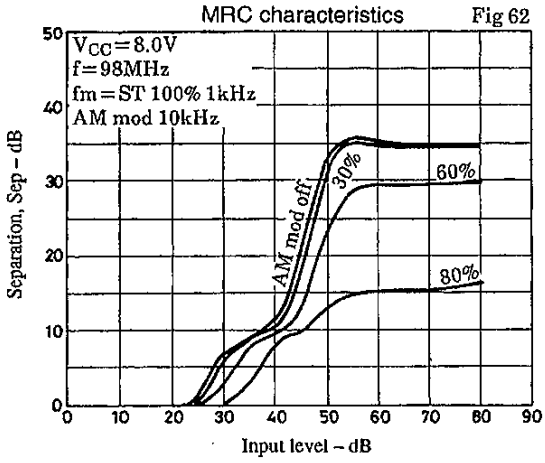


Figure 61



Downloaded from Elcodis.com electronic components distributor

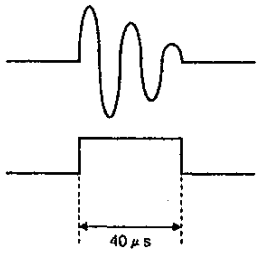
Noise Canceler

The following aspects have changed in the LA1888NM:

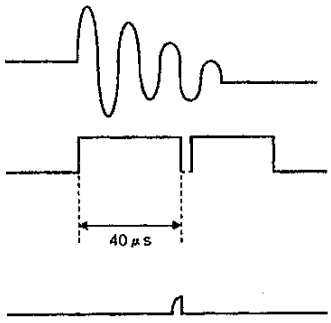
1. A circuit that resets the gate time has been added.
2. The noise canceler low-pass filter fc frequency has been lowered.

• Added gate time reset circuit

The gate width in the LA1888M is fixed at 40 µs. Since most automotive ignition noise is under 40 µs, as shown in figure 1, this circuit removes this noise without problem. However, since noise cancelers are tested under conditions that are more severe than those during normal operation, pulses are larger. As a result, with a 40-µs gate width noise can occur in the period prior to the rise of the next gate (as shown in figure 2). Also note that motor noise has wider pulse widths and thus is subject to the same phenomenon.

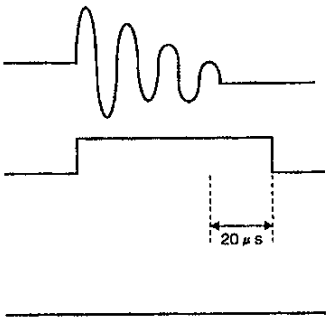


A06154



A06155

In the LA1888NM, the gate time is set at 20 µs. If the next noise pulse enters the circuit before that 20 µs has elapsed, the monostable circuit time constant is reset and the noise is gated until 20 µs has elapsed after the last noise input. This function also applies to motor noise.



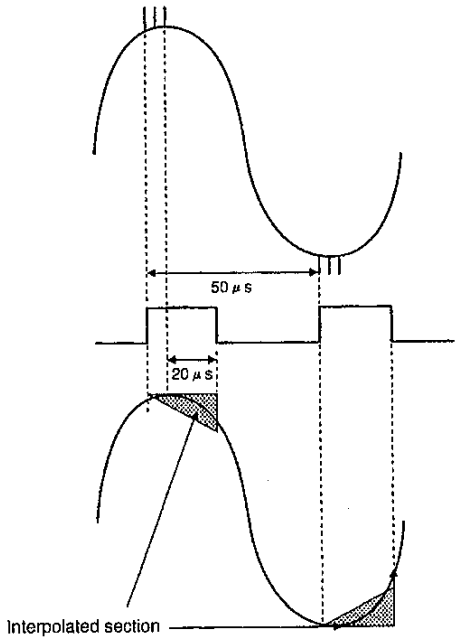
A06156

Another point is that during overmodulation of a 10-kHz signal, a whisker appears at the point of maximum amplitude in the signal due to the bandwidth of the ceramic filter. This noise canceler functions for this noise as well.

Since the LA1888NM gate period ends 20 µs after the end of the noise pulse, the muted section of the signal is held to a minimum and there is no influence on the waveform. (Since the half-period of a 10-kHz waveform is 50 µs, the waveform is not deformed.)

• Reduction in the low-pass filter fc frequency

An adequate delay time cannot be provided if the fc frequency is too high, and switching delay may occur, thus reducing the effect of the noise canceler. In the LA1888NM, the low-pass filter fc frequency has been reduced allowing an adequate amount of delay to be provided. This increases the rejection of monaural pulse noise.

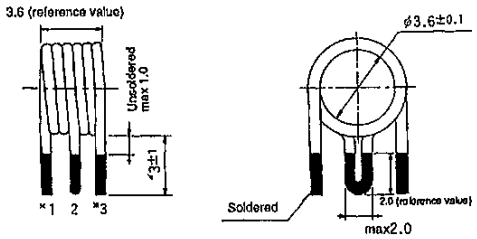


A06157

Downloaded from Elcodis.com electronic components distributor

9. Coil Specifications

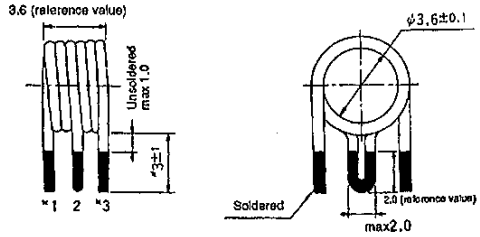
• FM ANT1



	SA-145 (SUMIDA)
1-2	2 3/4 T
2-3	2 3/4 T

0.55 UEW

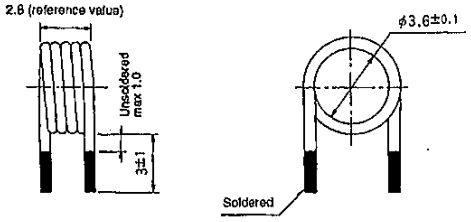
• FM ANT2



	SA-145 (SUMIDA)
1-2	2 3/4 T
2-3	2 3/4 T

0.55 UEW

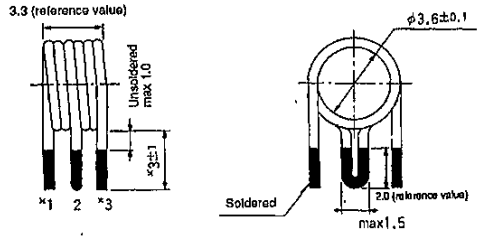
• FM RF1



	SA-137 (SUMIDA)
	4 1/2 T

0.50 UEW

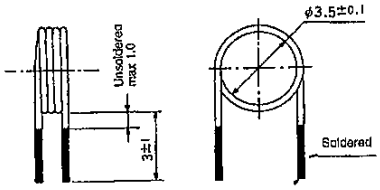
• FM RF2



	SA-136 (SUMIDA)
1-2	2 3/4 T
2-3	2 3/4 T

0.50 UEW

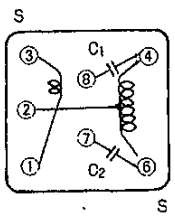
• FM OSC



	0708-1281 (SUMIDA)
	4 1/2 T

0.60 UEW

• FM MIX



	2136-023 (SUMIDA)
3-1	2 T
6-2	6 1/2 T
2-4	6 1/2 T

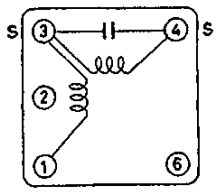
Q_O = 45
Cin = 100 p: pins 4-8, pins 6-7

Continued on next page.

Downloaded from Elcodis.com electronic components distributor

Continued from preceding page.

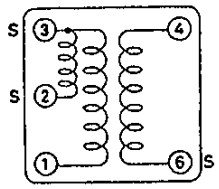
• FM QOD DET



	SA-208 (SUMIDA)
4-3	18 1/2 T 0.08 MUEW
3-1	70 1/2 T 0.06 UEW

Q_O = 45

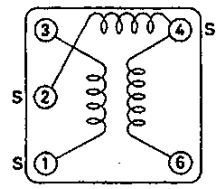
• AM RF1



	SA-177 (SUMIDA)
2-3	8 T
6-4	6 T
3-1	69 T

0.045 UEW
Q_O = 45

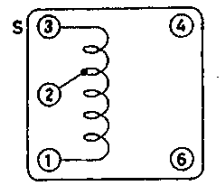
• AM RF2



	SA-178 (SUMIDA)
2-4	41 1/2 T
1-3	31 T
4-6	77 T

0.045 UEW
Q_O = 50

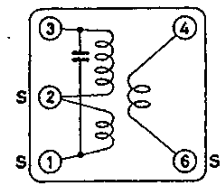
• AM OSC



	2135-JPS-001 (SUMIDA)
3-2	17 T
2-1	33 T

0.07 UEW
Q_O = 40

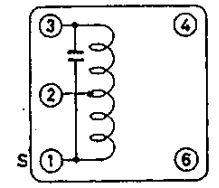
• AM IF1 (MIX)



	SA-194 (SUMIDA)
1-2	28 T
6-4	18 T
2-3	143 T

0.05 UEW
Q_O = 50

• AM IF2

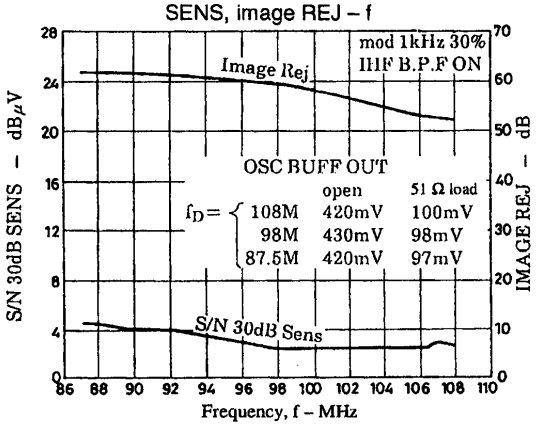


	4161-235 (SUMIDA)
1-2	92 T
2-3	92 T

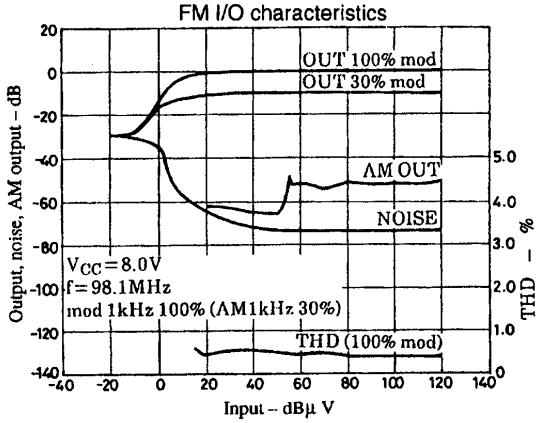
0.05 UEW
Q_O = 35

Downloaded from Elcodis.com electronic components distributor

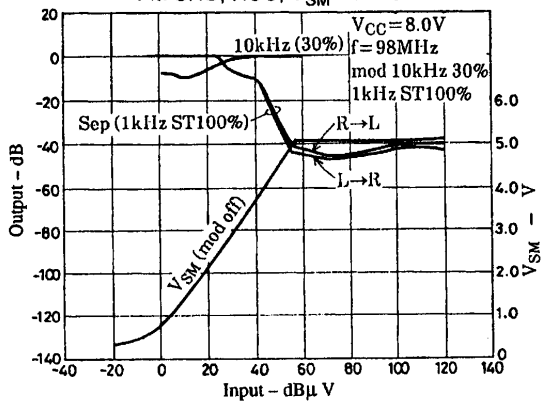
SENS, image REJ – f



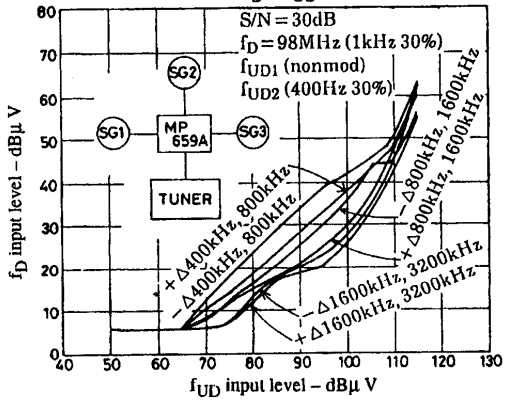
FM I/O characteristics



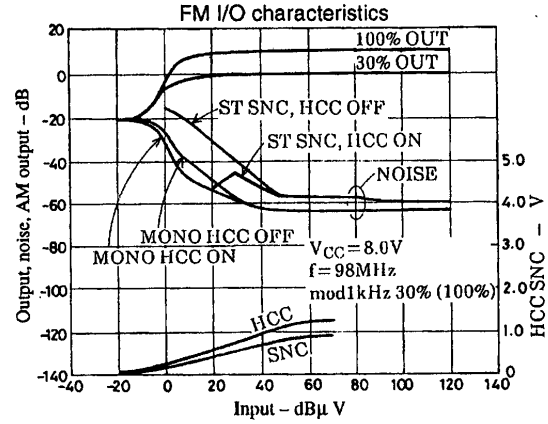
FM SNC, HCC, V_{SM} – INPUT



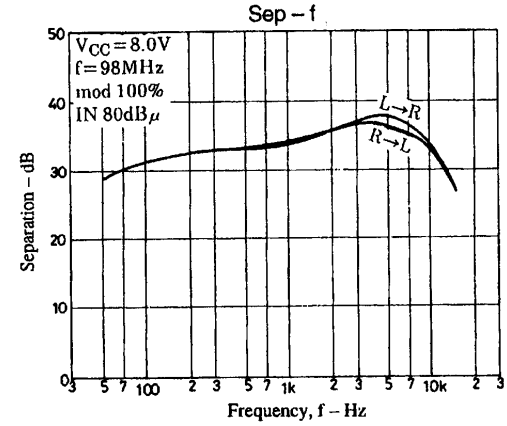
$f_D - f_{UD}$



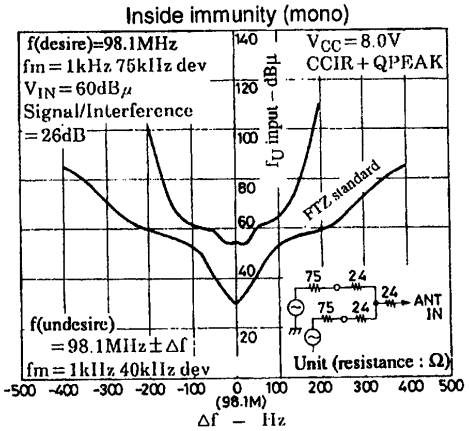
FM I/O characteristics



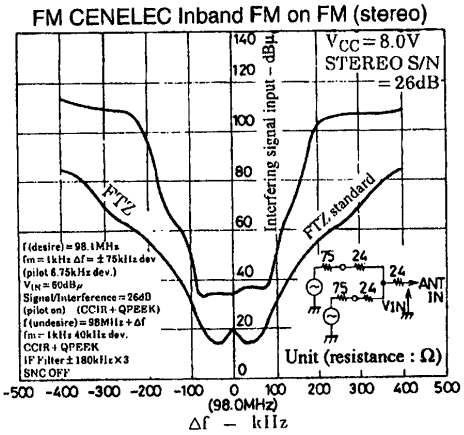
Sep – f



Inside immunity (mono)

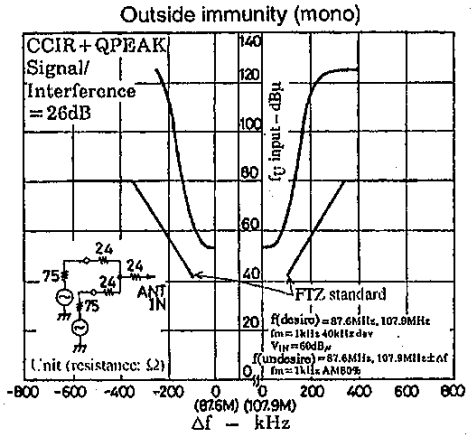


FM CENELEC Inband FM on FM (stereo)

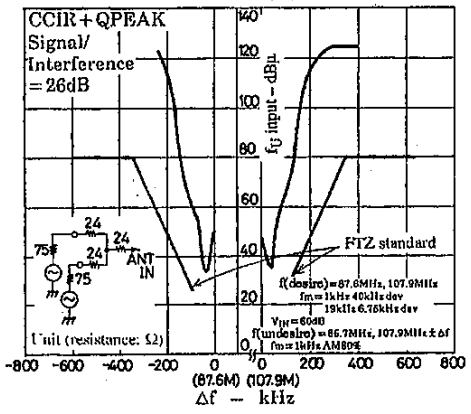


Downloaded from Elcodis.com electronic components distributor

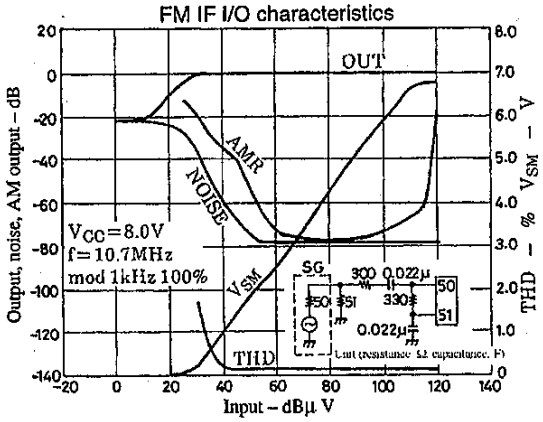
Outside immunity (mono)



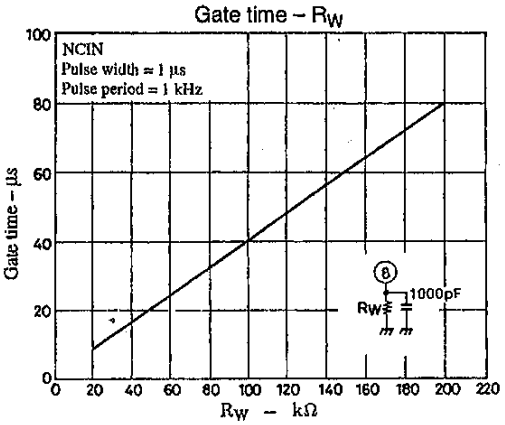
Outside immunity (stereo)



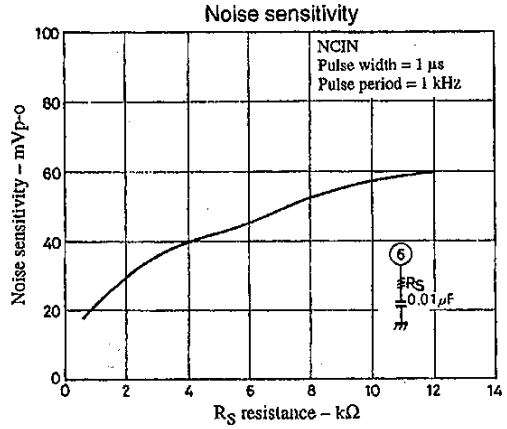
FM IF I/O characteristics



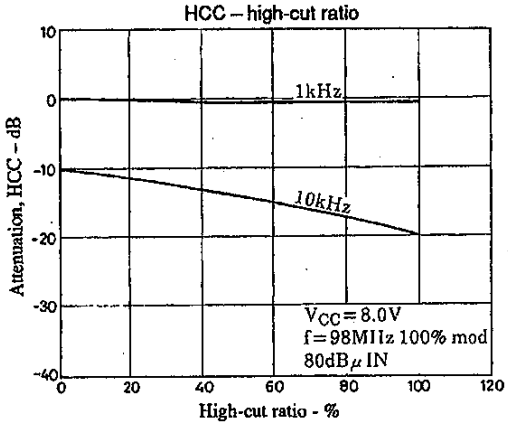
Gate time – R_W



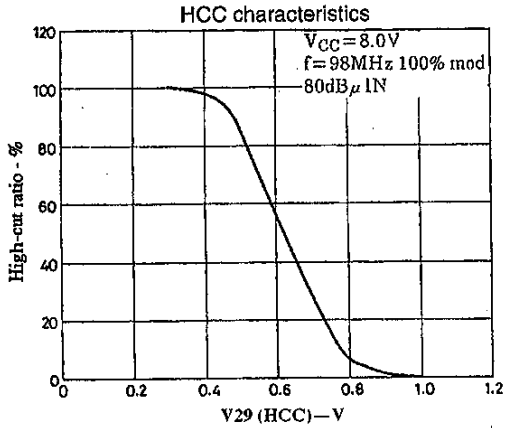
Noise sensitivity



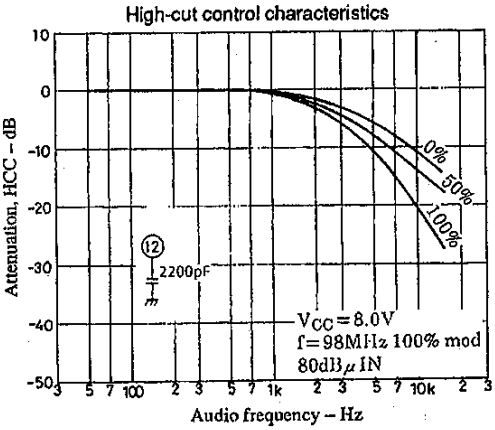
HCC – high-cut ratio



HCC characteristics

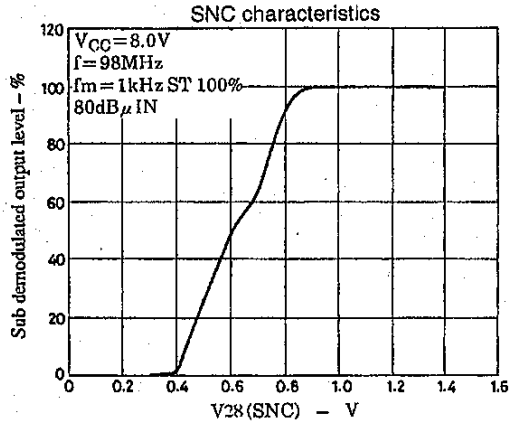


High-cut control characteristics

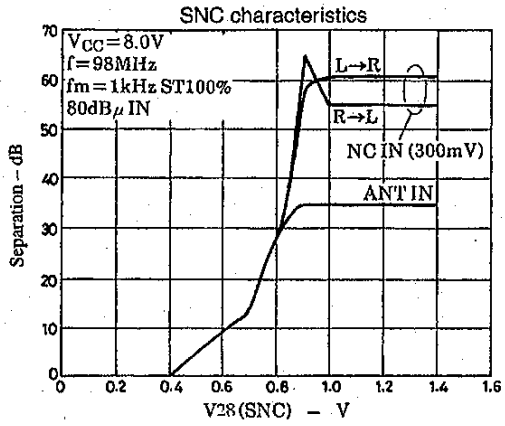


Downloaded from Elcodis.com electronic components distributor

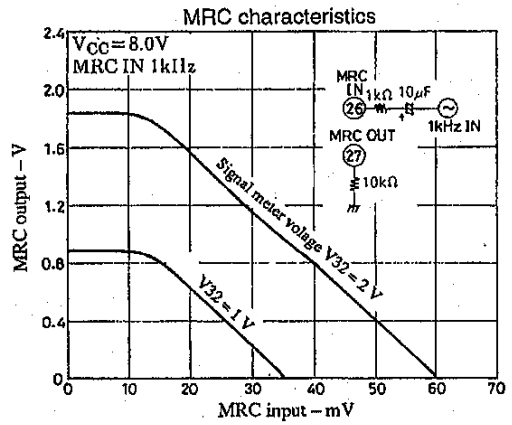
SNC characteristics



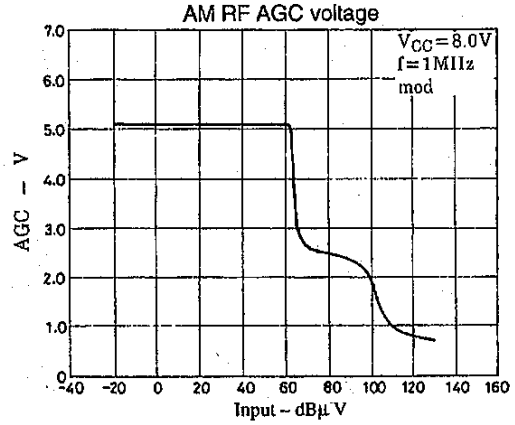
SNC characteristics



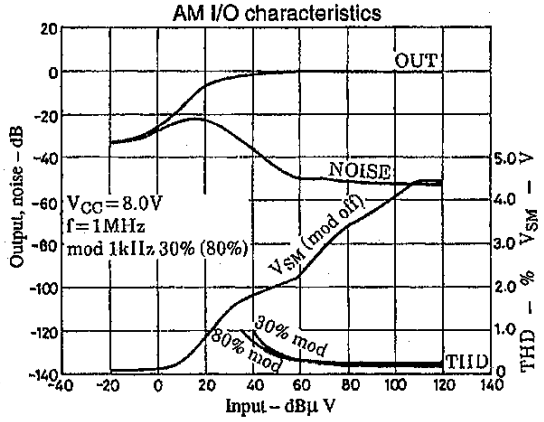
MRC characteristics



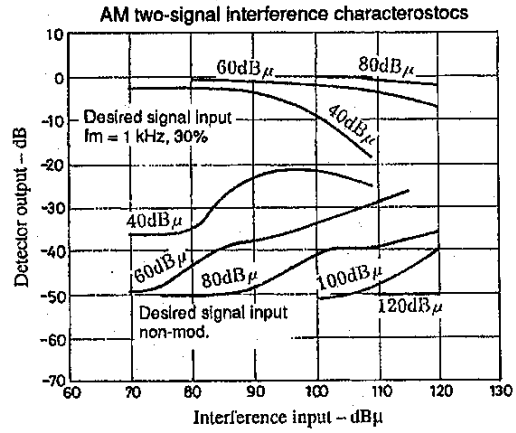
AM RF AGC voltage

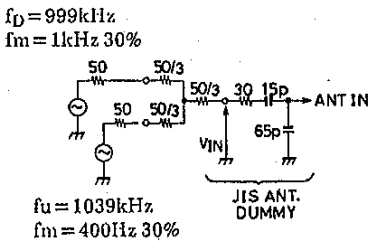


AM I/O characteristics



AM two-signal interference characterostocs

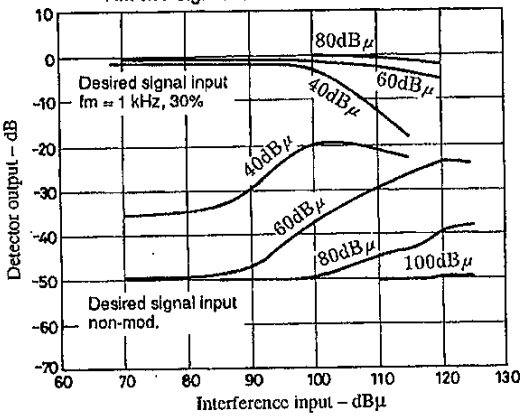


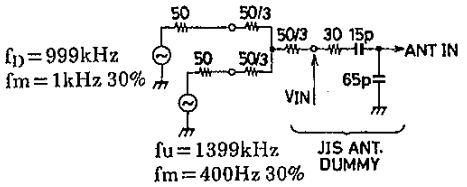


Unit (resistance : Ω, capacitance : F)

Downloaded from Elcodis.com electronic components distributor

AM two-signal interference characterostocs

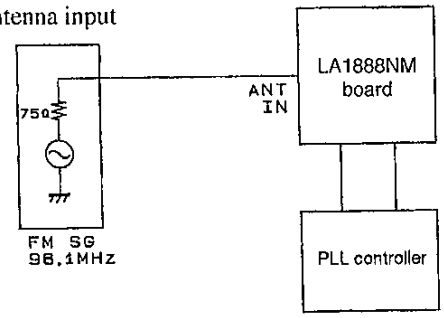




Unit (resistance : Ω, capacitance : F)

Temperature Characteristics

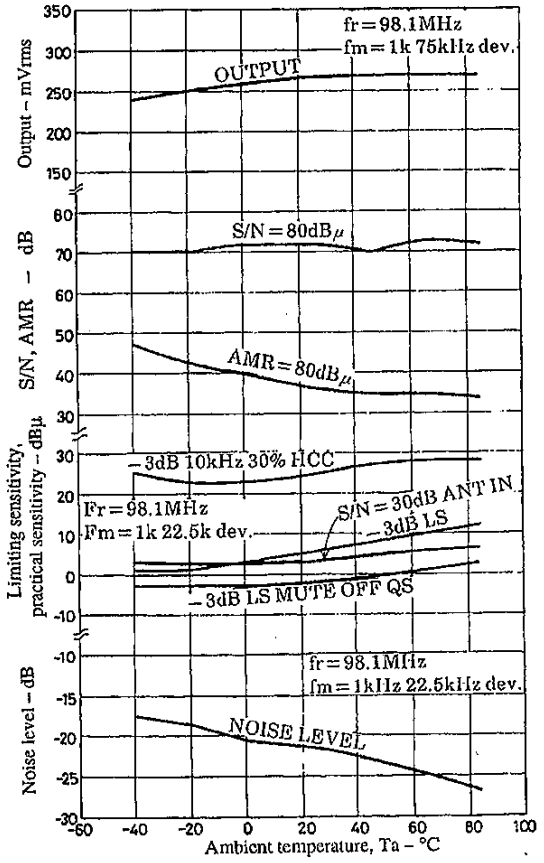
1. FM Antenna Input
   - FM antenna input



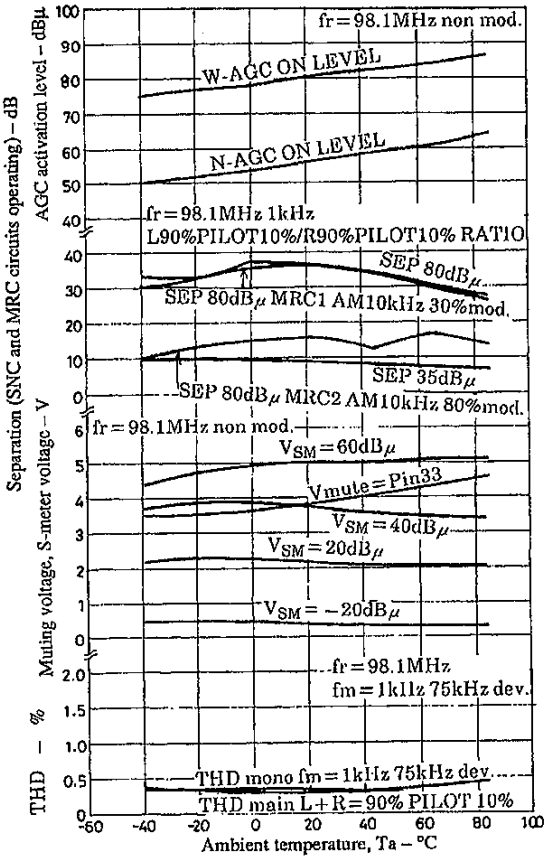
V_{CC} = 8.0V
98.1MHz 80dBμV
fm = 1kHz 75kHz dev
22.5kHz dev

A02369

FM antenna input temperature characteristics (1)

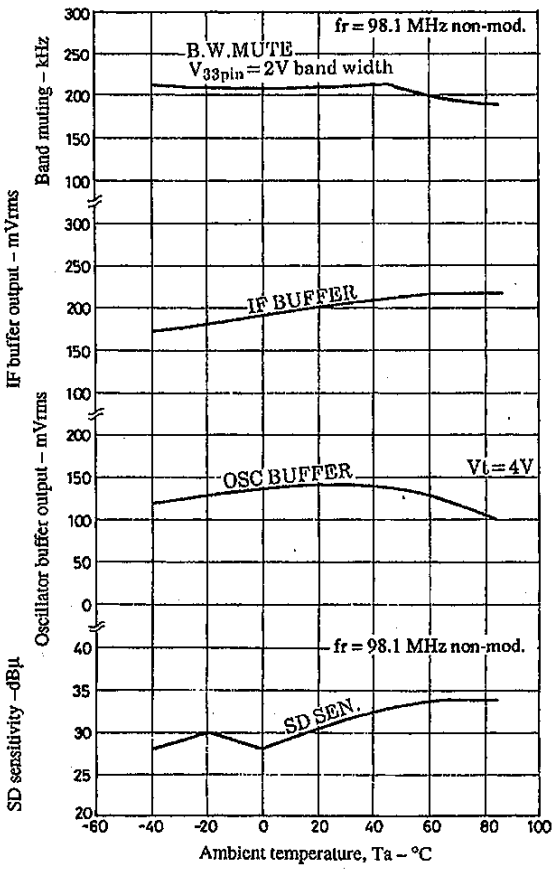


FM antenna input temperature characteristics (2)



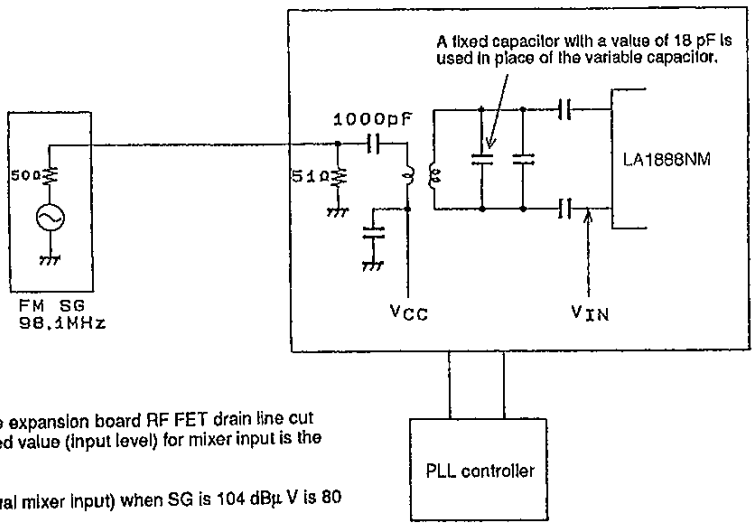
Downloaded from Elcodis.com electronic components distributor

FM antenna input temperature characteristics (3)



Downloaded from Elcodis.com electronic components distributor

• FM mixer input



- Input with the expansion board RF FET drain line cut
- The measured value (input level) for mixer input is the direct SG reading.
- V_{IN} (the actual mixer input) when SG is 104 dBμ V is 80 dBμ V (direct reading). (Actual measurement using an RF balance volt meter.)

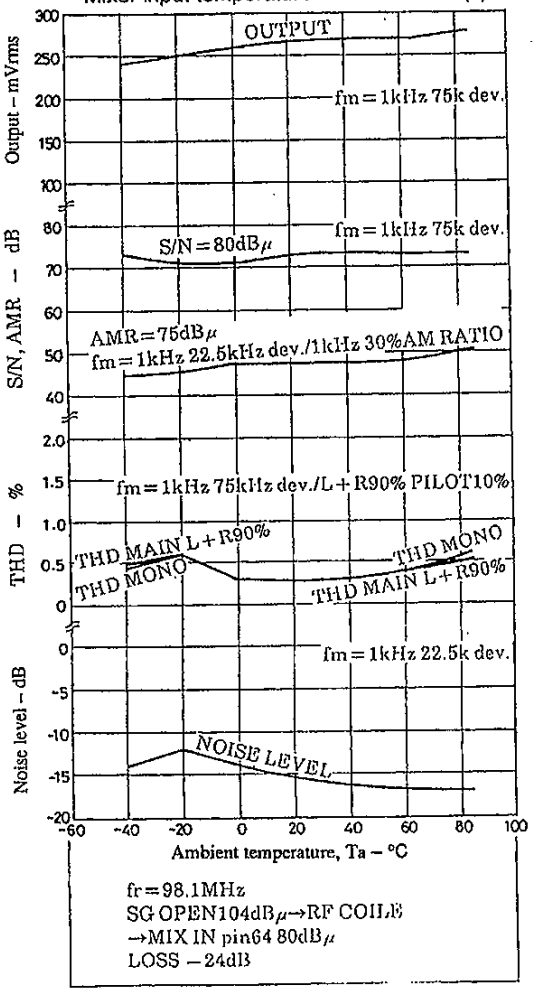
V_{CC} = 8.0 V A02370

98.1 MHz 80 dBμV (SG104dBμV)

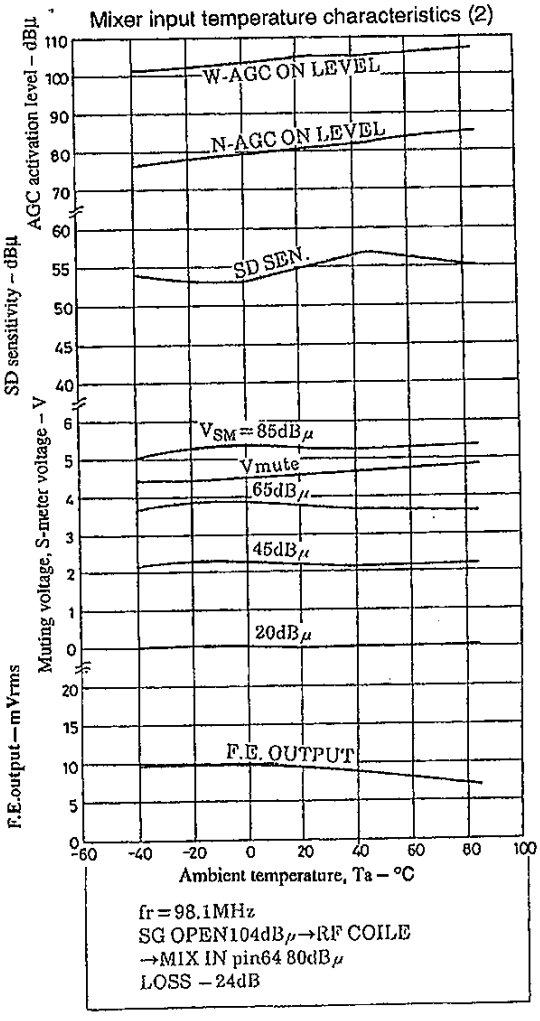
fm = 1 kHz 75 kHz dev

22.5 kHz dev

Mixer input temperature characteristics (1)

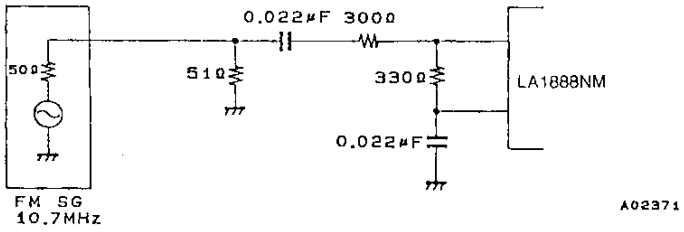


Mixer input temperature characteristics (2)



Downloaded from Elcodis.com electronic components distributor

• FM IF input

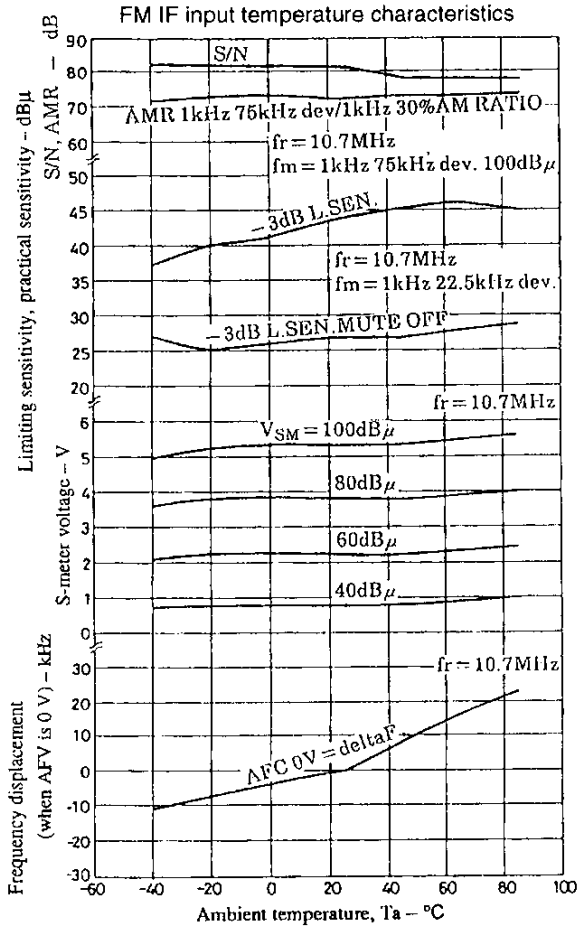


V_{CC}=8.0V

10.7MHz 100dBμV (SG112dBμV)

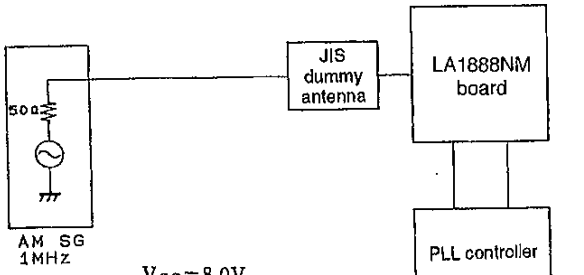
fm=1kHz 75kHz

22.5kHz

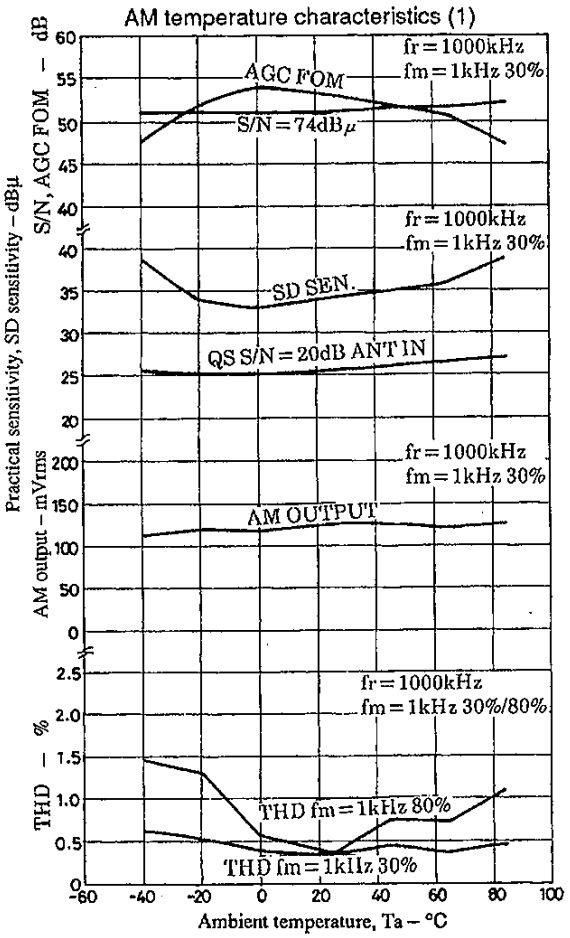


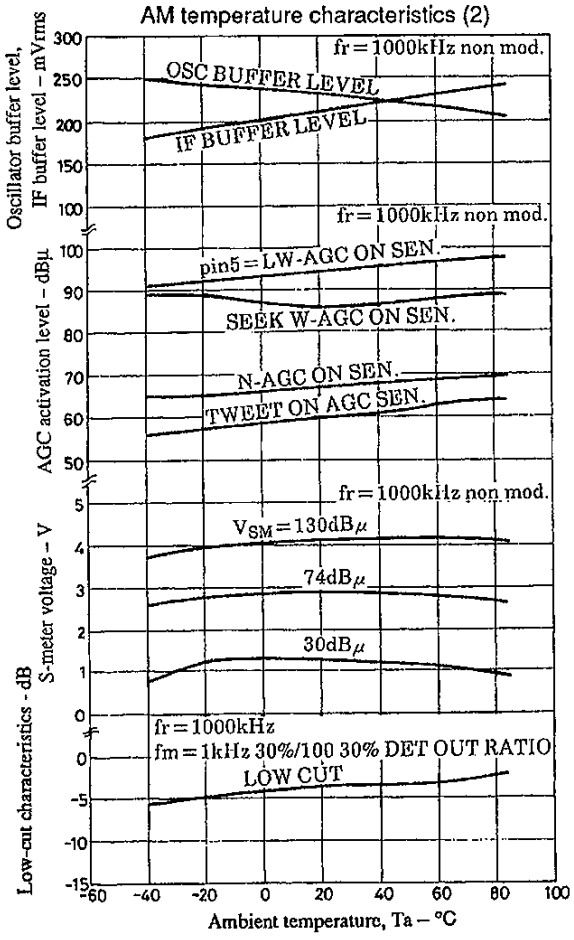
Downloaded from Elcodis.com electronic components distributor

2. AM Antenna Input



V_{CC}=8.0V
1MHz 74dBμV
fm=1kHz 30%
80%



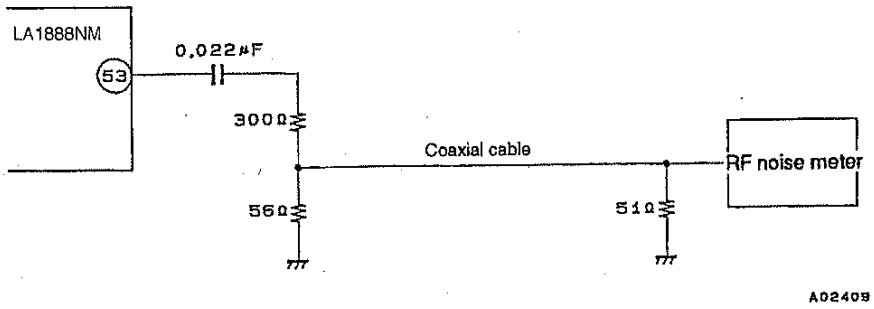


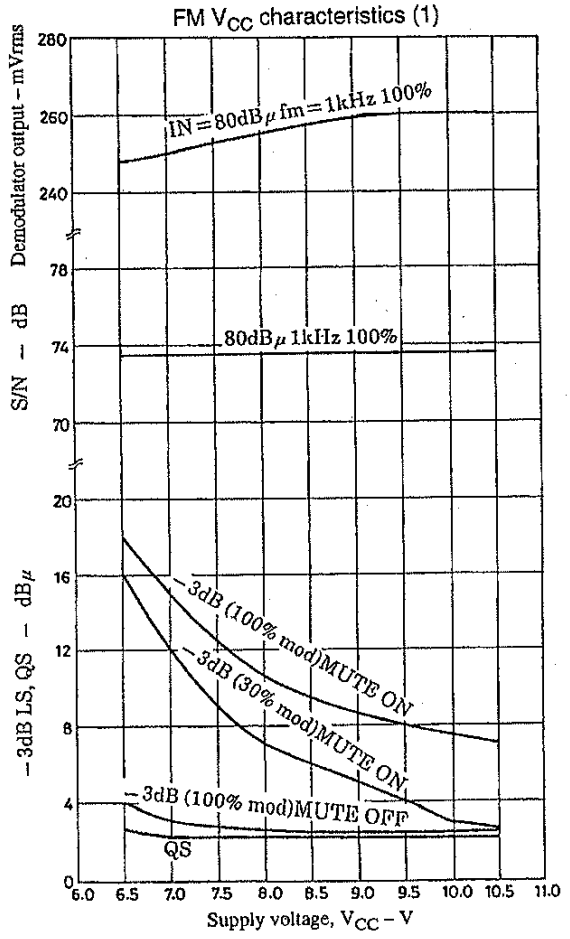
Downloaded from Elcodis.com electronic components distributor

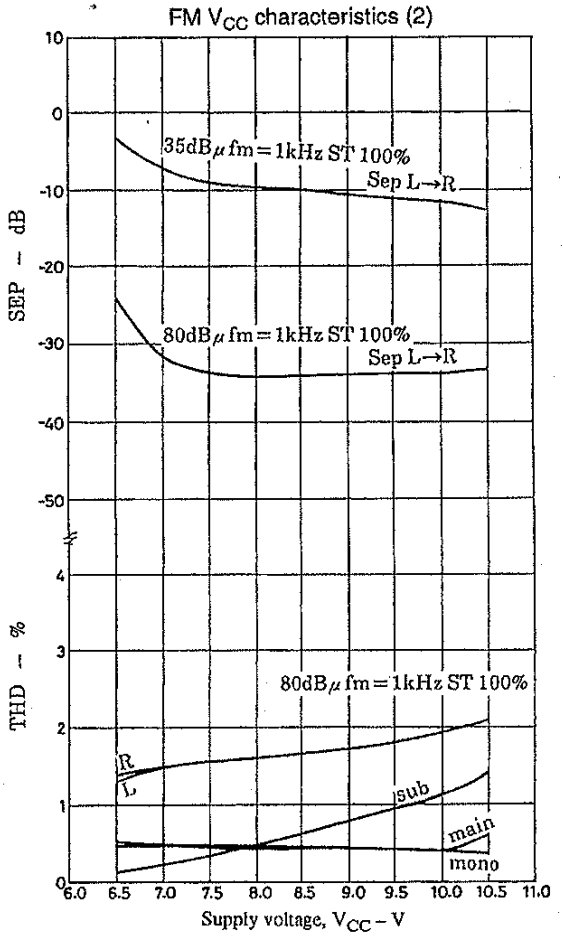
3. Levels are reduced somewhat in items measured with an RF vacuum tube voltage meter since there is cable loss in the coaxial cable between the test board and the RF vacuum tube voltage meter.

	No coaxial cable	
FM IF buffer	370 mV	→ 200 mV
AM IF buffer	395 mV	→ 212 mV
FM oscillator buffer	430 mV	→ 143 mV
AM oscillator buffer	270 mV	→ 230 mV

4. The figure below shows the test conditions for mixer input and FE output level measurements.

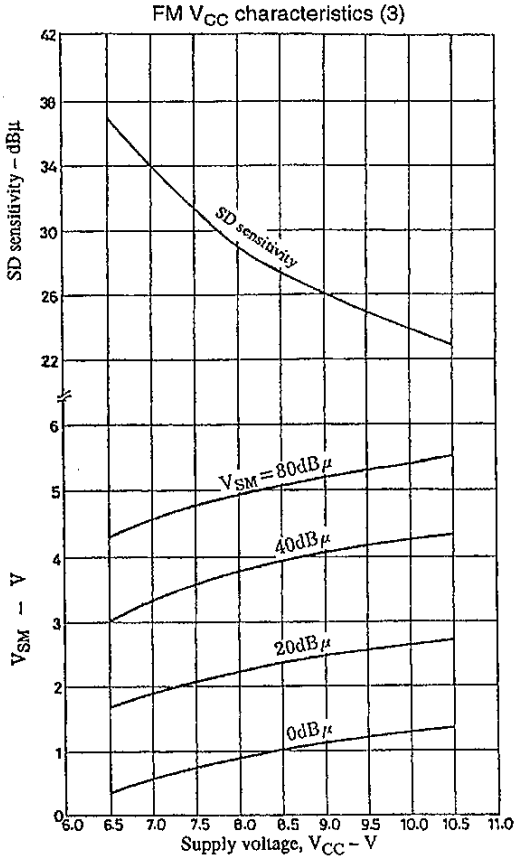




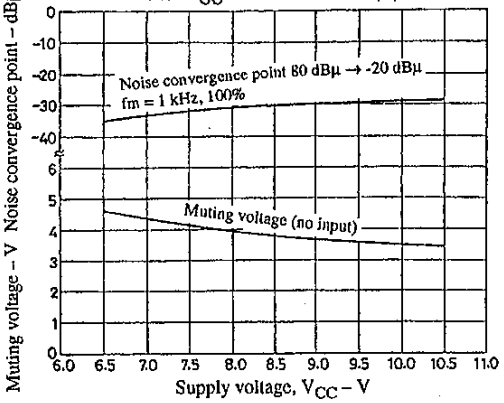


Downloaded from Elcodis.com electronic components distributor

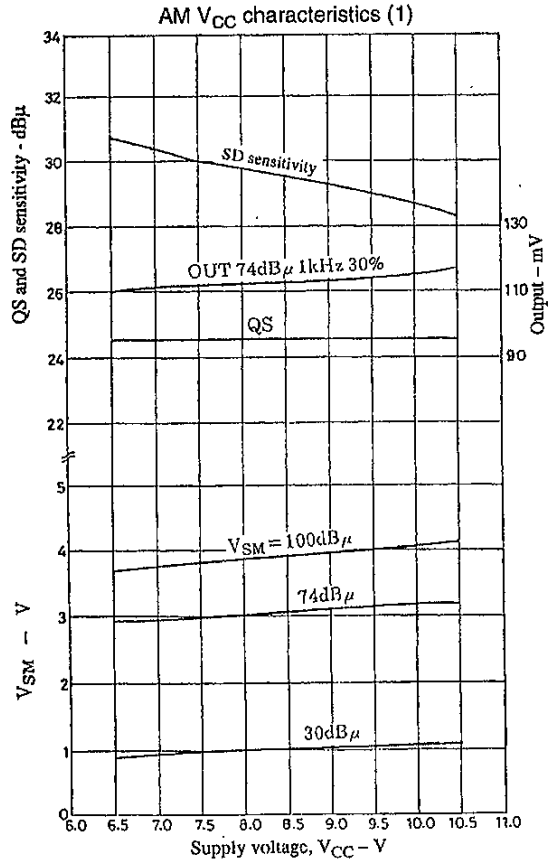
FM V_{CC} characteristics (3)



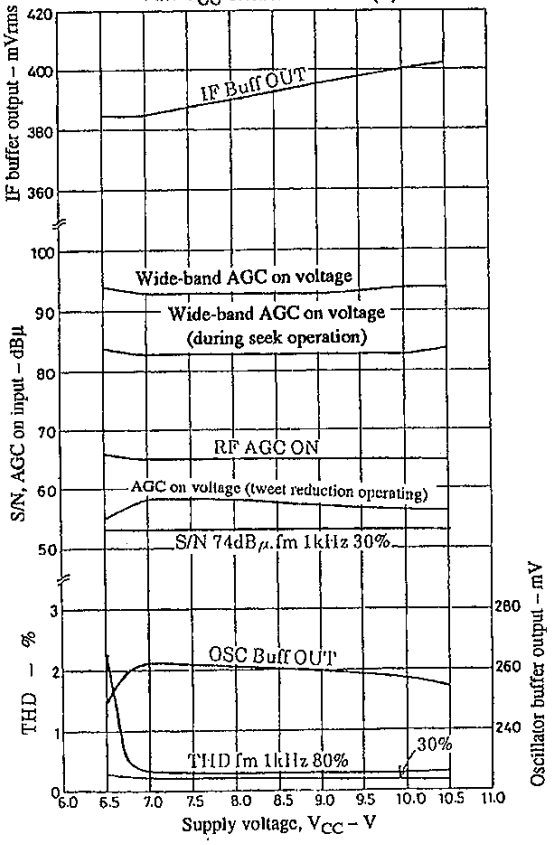
FM V_{CC} characteristics (4)



AM V_{CC} characteristics (1)



AM V_{CC} characteristics (2)



Downloaded from Elcodis.com electronic components distributor

■ Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

■ SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

■ In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of October, 1998. Specifications and information herein are subject to change without notice.

Downloaded from Elcodis.com electronic components distributor