Ordering number: EN 4092B

Monolithic Linear IC

LA1862M

Single-chip Tuner System for Car Stereo

Overview

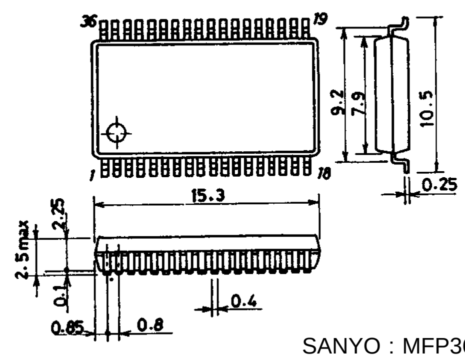
The LA1862M is a single-chip car stereo FM IF/NC/MPX tuner IC which offers improved IF stability and S-meter characteristics, compared with the LA1861M.
The LA1862M makes the design of high-performance FM tuners at low cost easy.

Package Dimensions

unit : mm

3129-MFP36S

[LA1862M]



SANYO : MFP36S

Functions

- IF amplifier
- Peak detector
- AF preamplifier
- AFC output
- S-meter driver
- Soft mute circuit
- IF buffer output
- Noise canceller
- Adjustment-free VCO
- Pilot signal canceller
- SNC High-cut control (HCC)

Features

- Pin compatible with the LA1861M
- Improved I/O S-meter characteristics
- Excellent sound quality at low input levels
- Easy adjustment of muting characteristics
- Because this device has a 36-pin flat package, it requires few external components and offers excellent cost performance.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	Pin 8	10	V
Allowable power dissipation	Pd max	Ta = 25°C	720	mW
Input voltage	V_{IN} IF	Pin 36-35 (IF input)	±0.7	Vp-p
	V_{IN} MPX	Pin 26 (NC-MPX input)	1.0	Vrms
Input current	I_L max	Pin 25 (stereo lamp drive current)	20	mA
Output current	I_{SD} max	Pin 5 (SD output)	1.0	mA
Operating temperature	Topr		–30 to +80	°C
Storage temperature	Tstg		–40 to +150	°C

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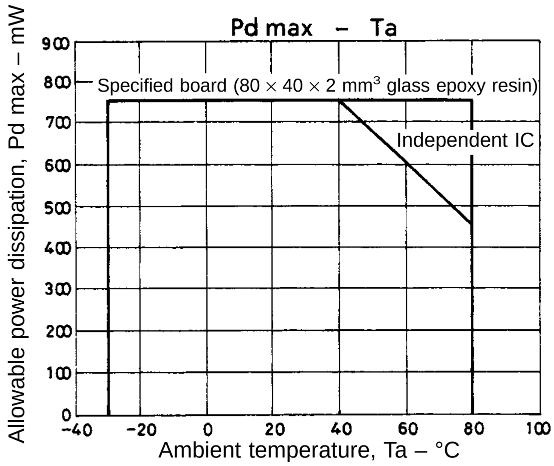
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		8.5	V
Operating supply voltage range	V_{CC} op		7.5 to 10	V

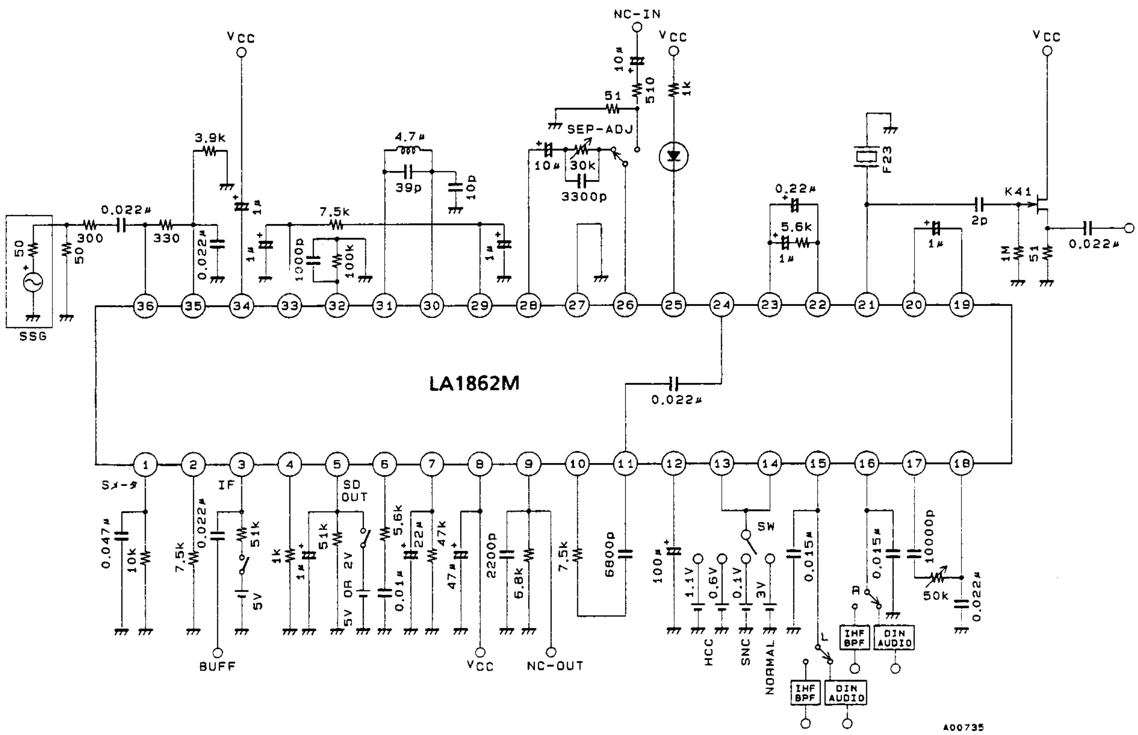
Operating Characteristics at Ta = 25°C, V_{CC} = 8.5 V, f = 10.7 MHz, unless otherwise noted SW-1 is off.

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	I_{CCO}	No input signal		45	70	mA
Current drain	I_{CC-100}	V_{IN} = 100 dBµ		47	72	mA
Demodulator output voltage	V_O	V_{IN} = 100 dBµ, f = 1 kHz, 100% modulation, pin 15 output	225	350	495	mVrms
Total harmonic distortion	THD 1	Mono, V_{IN} = 100 dBµ, f = 1 kHz, 100% modulation, pin 15 output		0.3	1.2	%
	THD 2	Stereo (L + R), V_{IN} = 100 dBµ, f = 1 kHz, 100% modulation, pin 15 output		0.3	1.2	%
Signal-to-noise ratio	S/N	V_{IN} = 100 dBµ, f = 1 kHz, 100% modulation	64	71		dB
Input limiting voltage	$V_{IN\ lim}$	V_{IN} = 100 dBµ reference, 3 dB audio output attenuation, IF input level, soft muting ON	32	41	50	dBµ
Muting attenuation (1)	Mute $_{Att}$	V5 = 5 V, V_{IN} = 100 dBµ, f = 1 kHz, 100% modulation	21	25	29	dB
Muting attenuation (2)	Mute $_{Att}$	V5 = 2 V, V_{IN} = 100 dBµ, f = 1 kHz, 100% modulation	5	10	15	dB
Muting bandwidth	BW $_{Mute}$	V_{IN} = 100 dBµ, V5 = 2 V	135	200	305	kHz
AM rejection ratio	AMR	V_{IN} = 100 dBµ, 400 Hz, 100% modulated FM carrier. 1 kHz, 30% modulated AM interference signal	47	60		dB
Muting drive output voltage	V_{5-0}	No input signal	3.5	4.7		V
	V_{5-100}	V_{IN} = 100 dBµ		0	0.3	
S-meter output voltage	V_{1-0}	No input signal		0.1	0.5	V
	V_{1-50}	V_{IN} = 50 dBµ	1.1	1.9	2.7	V
	V_{1-100}	V_{IN} = 100 dBµ	5.4	6.4	7.4	
IF COUNT output sensitivity		IF input level at IF COUNT ON. SW-1 is ON.	44	53	62	dBµ
IF buffer output voltage	V_{IF-ON}	V_{IN} = 100 dBµ. SW-1 is ON.	200	300	480	mVrms
Input impedance	Z_{in}	f = 1 kHz		20		kΩ
Output noise voltage	V_{NO}	Pin 26 connected to ground		27		µV
Gate time	tgate	V_{IN} = 100 mVp-p, 1 µs pulsewidth, f = 1 kHz	13	23	35	µs
Noise sensitivity	SN	V_{IN} = 1 µs pulsewidth, f = 1 kHz			35	mVp-o
Channel separation	Sep	f = 1 kHz, 90% L+R signal modulation. 10% pilot signal modulation, IHF bandpass filter.	36	50		dB
Stereo indicator threshold level		Pilot signal level when the LED turns ON.	1.0	2.5	5.0	%
Stereo indicator hysteresis	hy	LED ON level - LED OFF level		3.2	6.5	dB
Capture range	C.R	CR = | (f – 456)/456 x 100 |		±1.2		%
SCA rejection ratio	SCA rej	90% L + R signal modulation. 10% pilot signal modulation. 67 kHz, 10% modulated SCA signal		75		dB
SNC output attenuation	Att_{SNC}	V14 = 0.6 V, 90% L – R signal modulation. 10% pilot signal modulation	–12.0	–7.5	–3.0	dB
SNC output voltage	V_{Osub}	V14 = 0.1 V, 90% L – R signal modulation. 10% pilot signal modulation			5	mV
High-out control attenuation	$Att_{HCC}1$	V13 = 0.6 V, 90% L + R signal modulation. 10% pilot signal modulation	–15	–5	0	dB
	$Att_{HCC}2$	V = 1.1 V, 90% L + R signal modulation. 10% pilot signal modulation	–2.0		0	dB
Ripple rejection	R_r	f = 50 Hz, V = 100 mVrms		27		dB
Channel balance	CB	| Pin 15 output – pin 16 output |		0	1.5	dB
Pilot signal attenuation		Left channel adjusted and measured DIN audio filter. See Note.	15	22		dB
Stereo indicator LED current		Minimum stereo drive current	1.0			mA
Pin 25 saturation voltage		I_L = 10 mA		1.0		V

Note: When a filter is not specified, connect an IHF bandpass filter to the MPX outputs.



Test Circuit

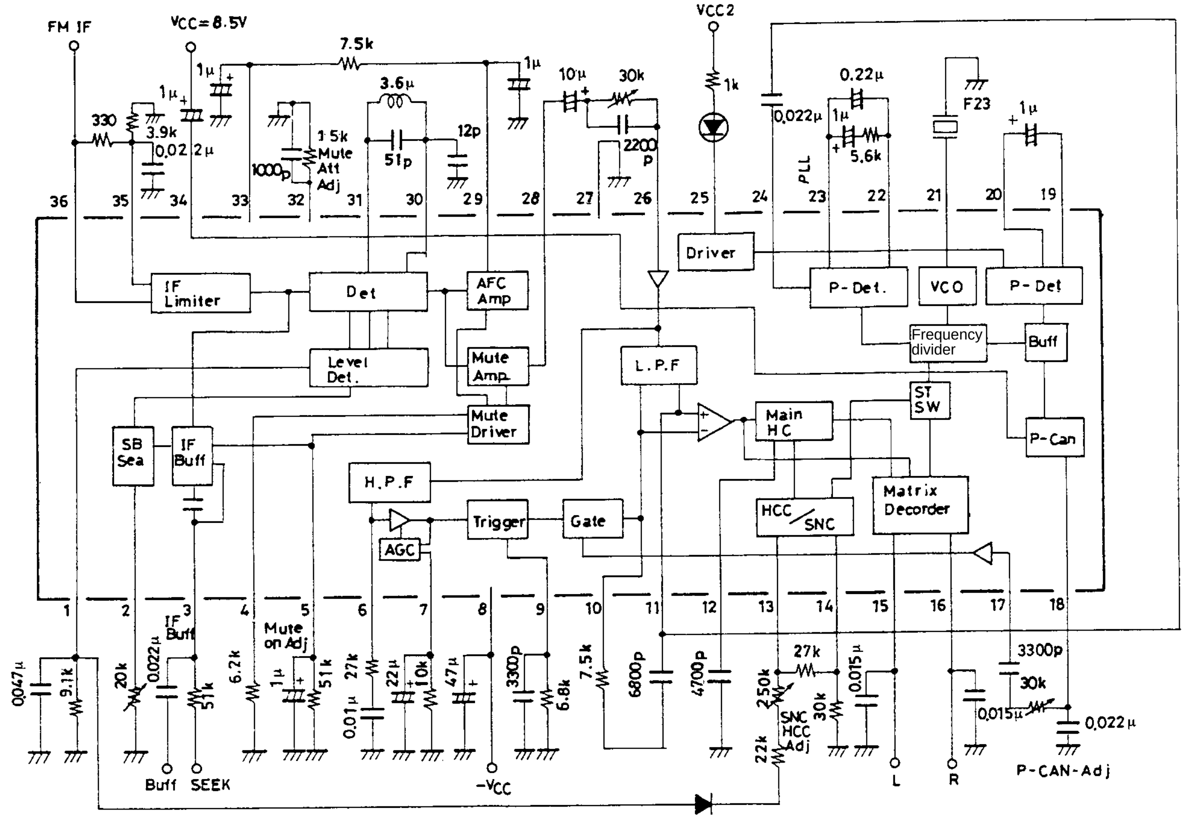


Unit (resistance: Ω, capacitance: F)

Pin Description

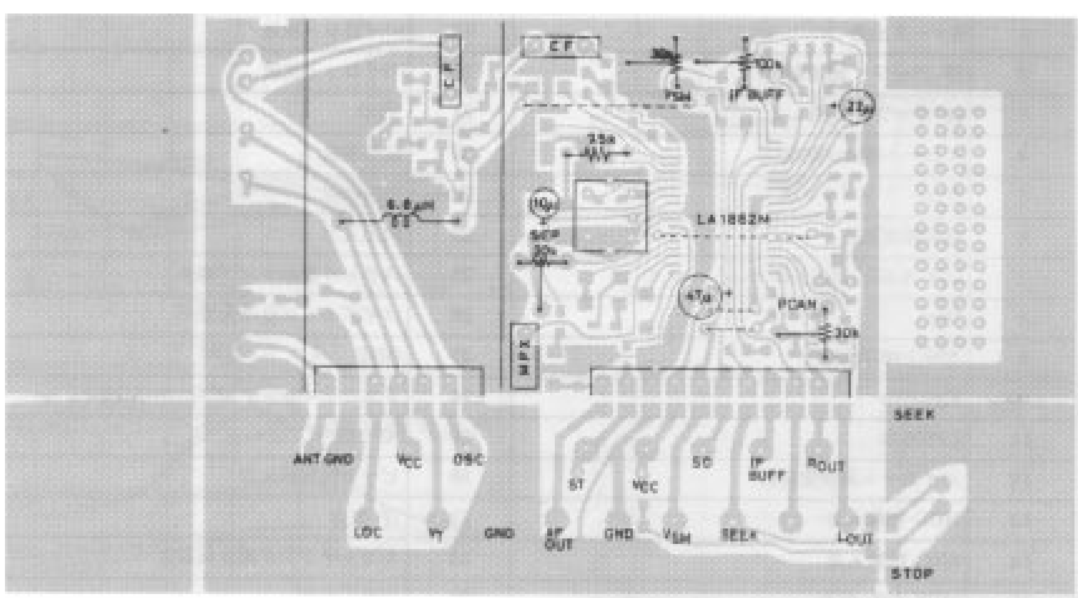
Pin No.	Description
1	S-meter output
2	IF buffer sensitivity control
3	IF buffer output
4	Muting threshold control
5	Muting drive control output
6	Noise sensitivity control
7	Noise AGC sensitivity control
8	Supply voltage (V_{CC})
9	Gate time control output
10	Peak hold network connection
11	Lowpass filter output
12	High-cut attenuation control
13	High-cut control input
14	SNC control input
15	MPX left-channel audio output
16	MPX right-channel audio output
17	Pilot cancel signal input
18	Pilot cancel signal output
19	Pilot detector capacitor connection 1
20	Pilot detector capacitor connection 2
21	External VCO (F23) connection
22	Phase detector network connection 1
23	Phase detector network connection 2
24	PLL input
25	Stereo indicator LED driver output
26	Noise canceller input
27	Ground
28	Audio muting amplifier output (AF output)
29	AFC output
30	Peak detector input
31	IF signal output
32	Muting attenuation control
33	Voltage reference output
34	Pilot signal canceller detector
35	IF input
36	IF bypass input

Sample Application Circuit



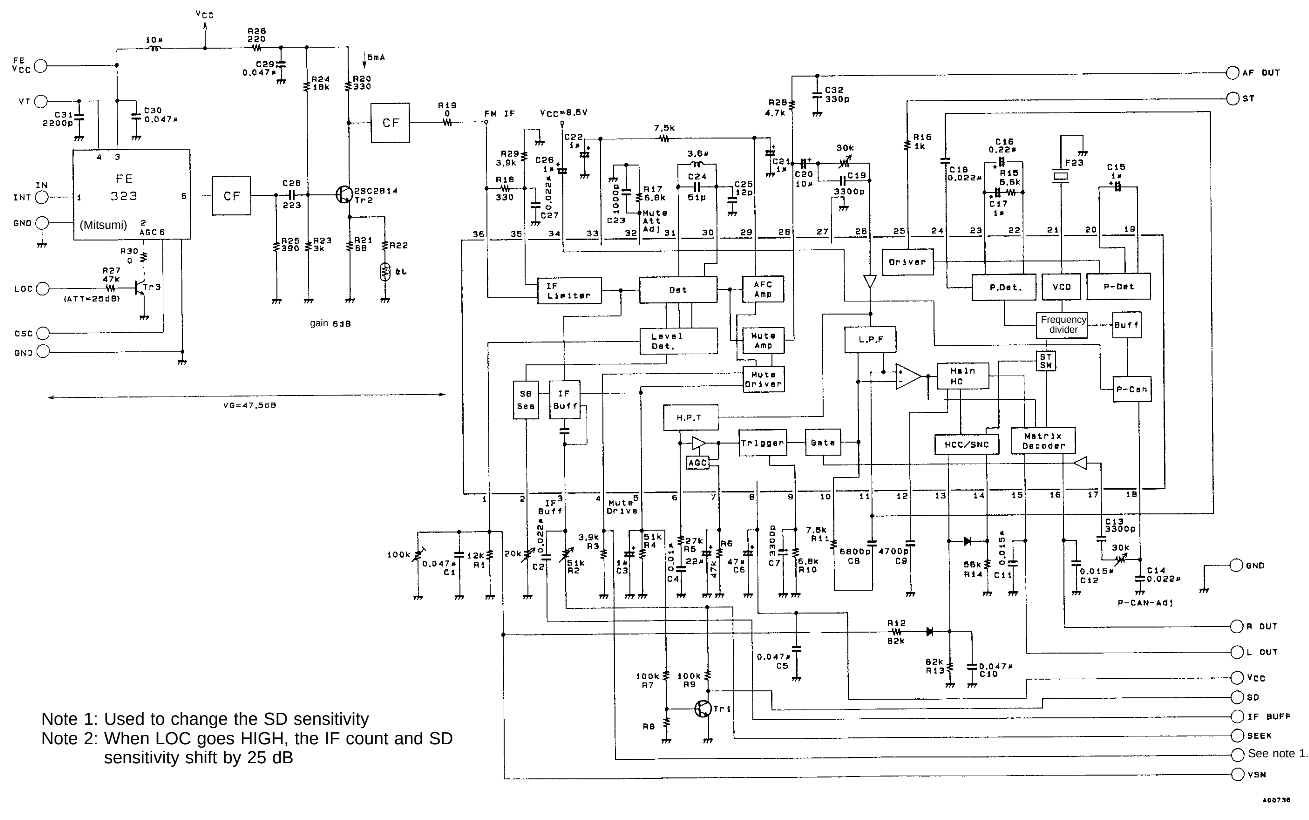
Unit (resistance: Ω, capacitance: F)

PCB Pattern



Unit (resistance: Ω, capacitance: F)

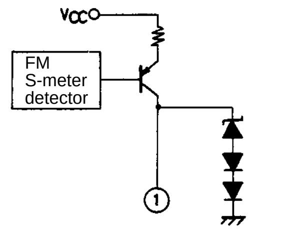
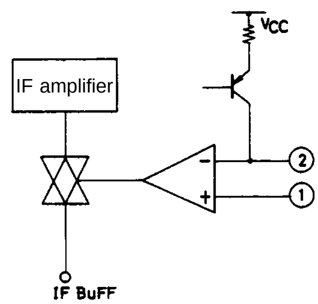
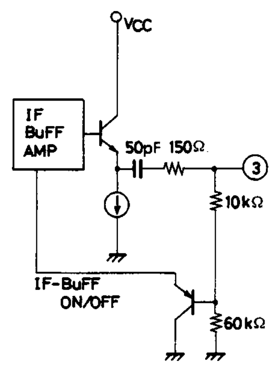
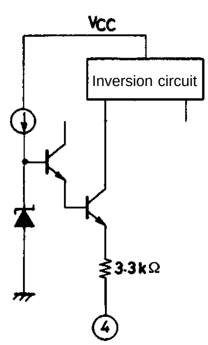
Sample Application Circuit (USA)



Note 1: Used to change the SD sensitivity
Note 2: When LOC goes HIGH, the IF count and SD sensitivity shift by 25 dB

Unit (resistance: Ω, capacitance: F)

Pin Functions

Pin No.	Function	Equivalent circuit	Remarks
1	S-meter output		Current-drive waveform S-meter circuit
2	IF buffer ON adjust		
3	IF buffer output		Control signal: SEEK when HIGH (V_{DD}) STOP when LOW (GND) Pin 3 should be left open if not using the IF count
4	Mute adjust		

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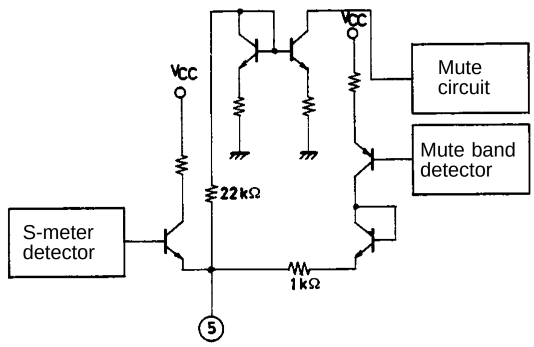
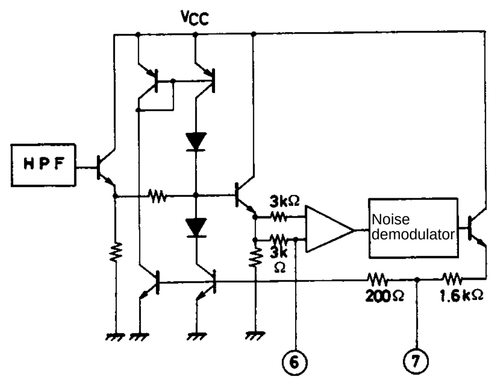
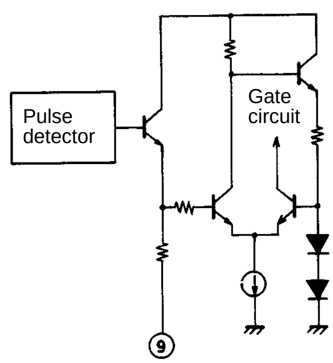
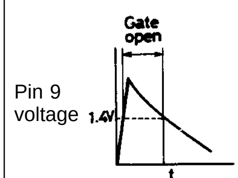
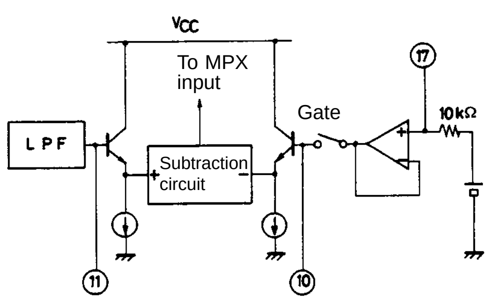
Pin No.	Function	Equivalent circuit	Remarks
5	Mute drive		
6	Noise sensitivity adjust		
7	Noise AGC		
9	Gate time adjust		 The gate is open when the voltage on pin 9 is 1.4 V ($2V_D$) or higher.
10	Memory circuit		
11	LPF output		
17	Pilot cancel signal input		

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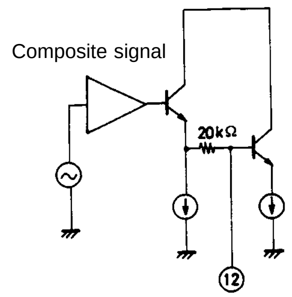
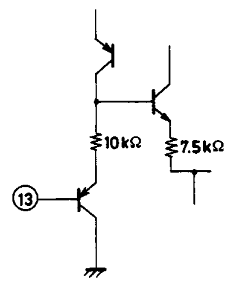
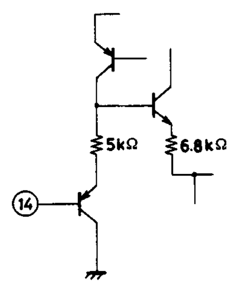
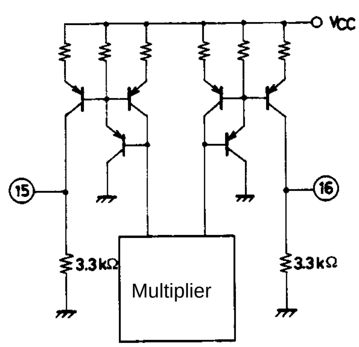
<table>
<tr><th>Pin No.</th><th>Function</th><th>Equivalent circuit</th><th>Remarks</th></tr>
<tr><td>12</td><td>High-cut capacitive coupling</td><td>
</td><td>High-cut frequency set pin</td></tr>
<tr><td>13</td><td>HCC control input</td><td>
</td><td></td></tr>
<tr><td>14</td><td>SNC control input</td><td>
</td><td></td></tr>
<tr><td>15</td><td rowspan="2">MPX outputs</td><td rowspan="2">
</td><td rowspan="2">Output R = 3.3 kΩ
Load R built-in</td></tr>
<tr><td>16</td></tr>
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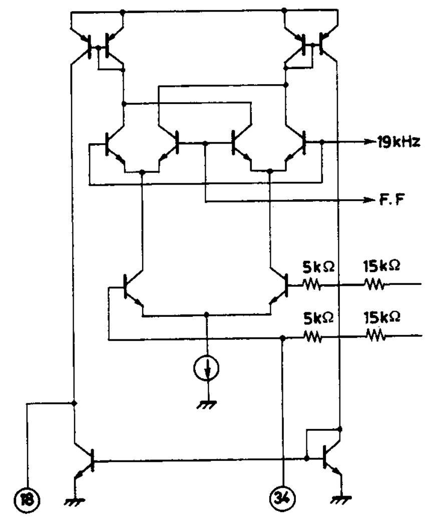
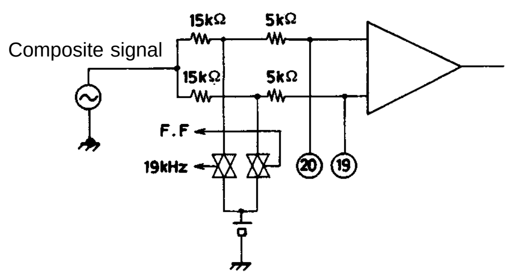
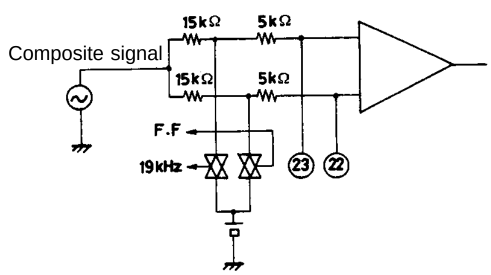
Pin No.	Function	Equivalent circuit	Remarks
18	Pilot cancel signal output		
34	Pilot cancel signal detector		
19	Pilot detectors		
20			
21	VCO		
22	Phase detectors		
23			

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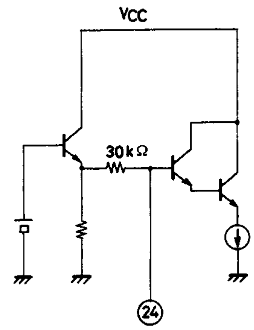
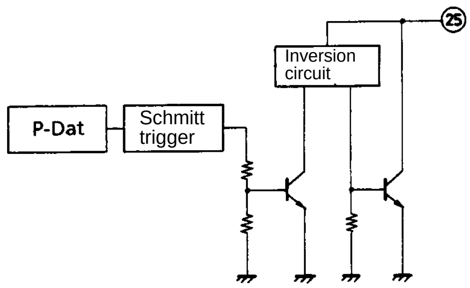
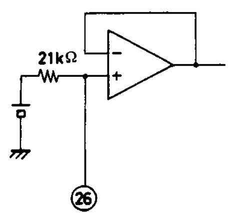
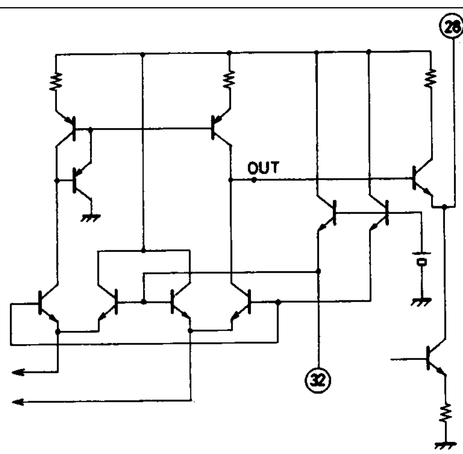
Pin No.	Function	Equivalent circuit	Remarks
24	PLL input		
25	ST indicator		ST indicator Mono when HIGH and stereo when LOW
26	Noise canceller input		
28	Muting circuit output		pin 28: Output impedance 50 Ω
32	Muting attenuation adjust		

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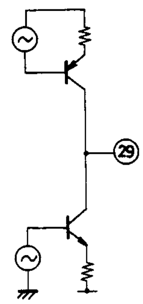
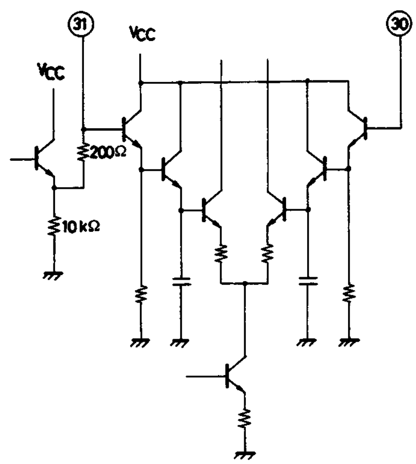
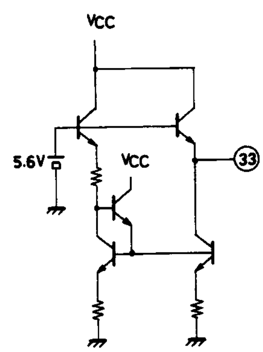
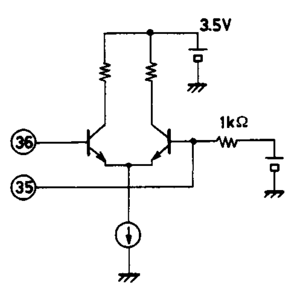
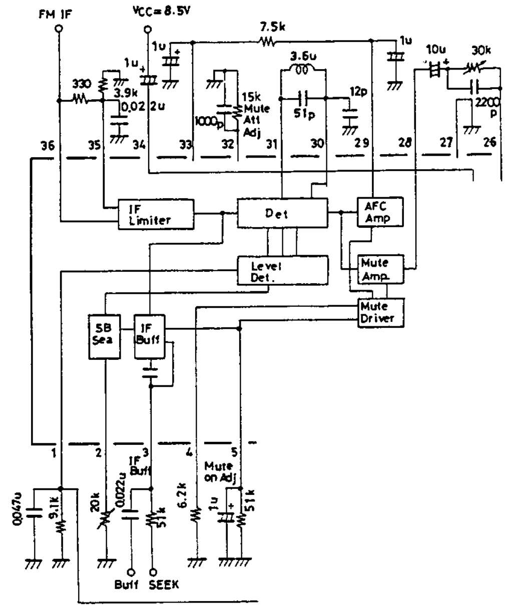
Pin No.	Function	Equivalent circuit	Remarks
29	AFC output		
30	Peak detector input		
31	Constant voltage output		
33	Constant voltage circuit		
35	IF input		
36	IF bypass		

IF Block

Obtaining Stable Characteristics

1. Pin 36 is the IF input; pin 35, the IF bypass. Connect a 330 Ω resistor between them for ceramic filter matching.
2. Position the capacitor between thr IF bypass (pin 35) and the ground pattern so as to maximize AM rejection.
3. Provide separate ground pattern islands for the IF input and detection circuits, as sharing the same island reduces stability.
4. Position the IF input and detector coil as far apart as possible, as proximity reduces stability and introduces beat noise in the output.



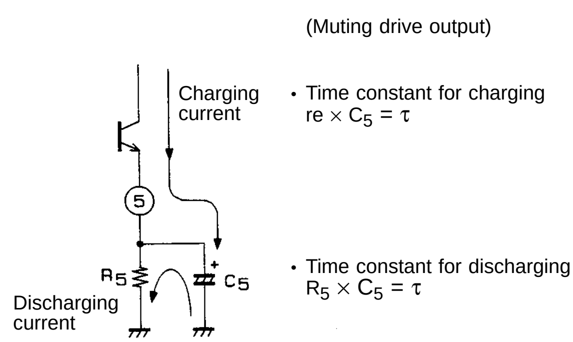
Unit (resistance: Ω, capacitance: F)

S-meter Output V_{SM}

1. Pin 1 is the field strength indicator (or ‘‘S-meter’’) output. Its current-driven circuit uses an external resistance to adjust the slopes of the I/O characteristics curves.
2. The S-meter output is internally connected to the soft muting and IF buffer blocks for use as a control signal for the soft muting drive and IF count buffer.
3. The point at which the input produces an S-meter output depends on the front end (FE) and interstage amplifier gains.
4. Too large a front end gain produces floating S-meter output even when there is no input. Either use a smaller load resistance on pin 1 or reduce the front end gain so that the output with no load does not exceed 0.5 V.
5. The S-meter output circuit has a dynamic range of approximately 80 dB, but this is limited by the front end noise component and broadband AGC circuit.

Soft Muting

1. The soft muting circuit operates in response to the S-meter output voltage. The amount of muting is related to the pin 5 output voltage.
2. There are two mechanisms for adjusting the soft muting I/O characteristic curve:
   a. Start point for muting: Resistance attached to pin 4
   b. Attenuation for muting: Resistance attached to pin 32
   *Note that the resistance attached to pin 1 also affects the curve.
3. The soft muting circuit automatically varies the amount of muting in response to the IF input. In the absence of front end broadband AGC effects, the time constant of the RC circuit between pins 1 and 5 determines the response.



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Band Muting

1. Band muting uses the detector’s S-curve. The band-width depends on the resistance between pins 29 and 33. Select this value to match the needs of the destination market.
2. Keep in mind that changing the detector coil or tuning capacity Q changes the slope of the S-curve and hence the bandwidth.
3. The attenuation muting depends on the resistance connected to pin 32.
4. The muting transient response depends on the resistance between pins 29 and 33, the capacitance at pin 29, and the time constant for the RC circuit at pin 5.

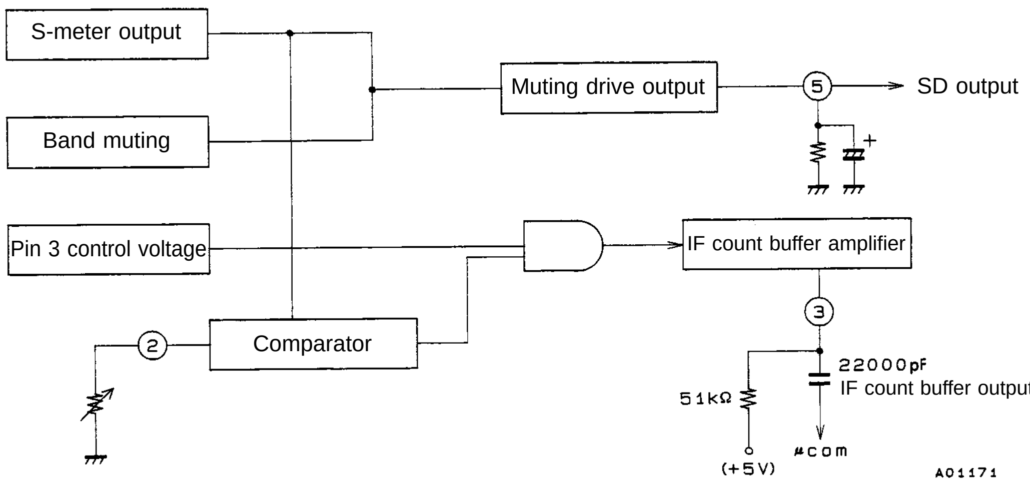
Detector

1. This IC uses a peak differential detector.
2. To adjust the detector coil, use the built-in automatic frequency circuit (AFC) and rotate the coil core until the voltage drop between pins 29 and 33 is 0 V.
3. Zeroing the AFC and minimizing the total harmonic distortion requires adjusting the capacitance between pin 30 and ground. Note that stray circuit board capacitance can affect this capacitance value.
4. The level of demodulation that is output depends on the inductance of the coil between pins 30 and 31, tuning capacity Q and the capacitor size. Note that although raising Q increases the slope of the S-curve and thus the demodulation output, it does so at the risk of increasing distortion.
5. If the destination market is Europe, increasing the slope of the S-curve helps reduce interference from neighboring channels.

IF Count Buffer

1. Pin 3 is the IF count buffer output. To activate the IF count circuit, apply a 5 V input to pin 3 through a 51 kΩ resistor.
2. The resistor connected to pin 2 determines the IF count buffer output sensitivity (seek stop sensitivity).
3. Leave pins 2 and 3 open if the IF count buffer is not used.
4. The largest time constant among those for the following pins determines the transient response characteristic of the IF count buffer.
   Pin 1: the S-meter output, pin 4: the start of muting, pin 5: the muting drive output and pin 29: the AFC output.

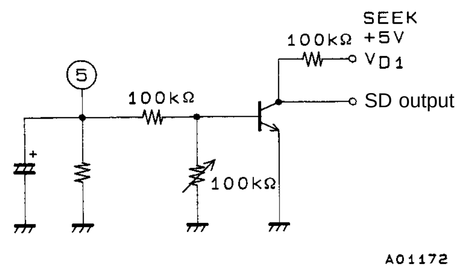
IF count system block diagram



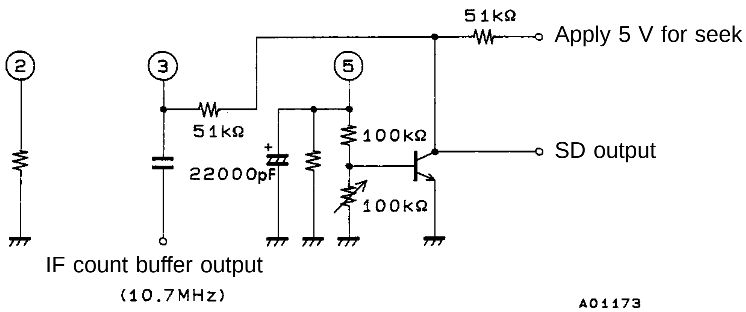
The logical AND of the S-meter output and pin 3 control voltage generates the output 10.7 MHz IF count signal.

SD Output

1. To obtain SD output, attach an external NPN transistor to pin 5 as shown in the following figure.
2. The resistor connected between the base and ground is for adjusting the SD sensitivity.
3. The transient response characteristic of the resulting SD circuit on pin 5 is, like that for the IF count buffer, determined by the time constants for pins 1, 4, 5 and 29. Raising the seek speed requires decreasing the time constants. Decreasing them too far, however, reduces muting transient response and risks introducing beat noise and other distortion.

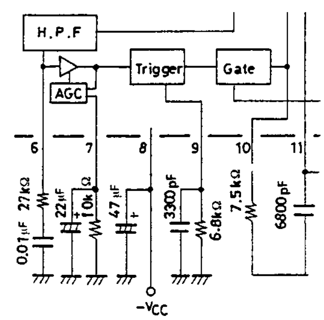


4. The following figure illustrates one possible circuit design using both the IF count buffer and the SD output circuit.



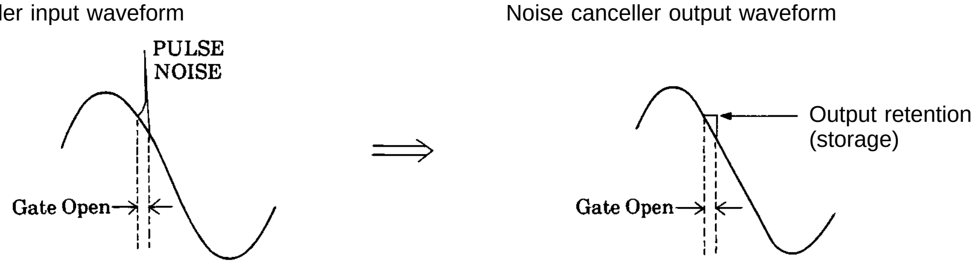
Noise Canceller Block

1. The resistor and capacitor connected to pin 6 determine the noise canceller sensitivity.
2. The resistor and capacitor connected to pin 7 determine the noise AGC.
3. Pin 9 is the gate trigger output. The resistor and capacitor connected to pin 9 determine the length of time that the gate is open.
4. The resistor and capacitor connected to pins 10 and 11 are for holding the input signal level when the noise canceller gate operates. The storage time depends on the time that the gate is open. The time constant for the RC circuit on pins 10 and 11 must, therefore, be such that the output retention signal level does not drop during this interval.



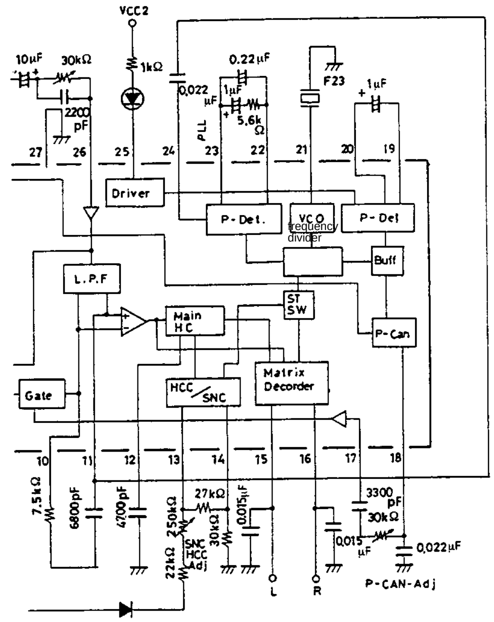
Noise canceller input waveform

Noise canceller output waveform



5. Pin 26 is the noise canceller input. An appropriate input level is 250 mVrms for 100% dev and fm = 1 kHz. Excessive input can exceed the noise canceller dynamic range, increasing the THD. Insufficient input, on the other hand, lowers the signal-to-noise ratio and reduces pilot lamp sensitivity.

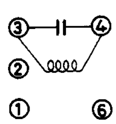
MPX Block



1. The variable resistor between pins 26 and 28 is for adjusting separation.
2. The ceramic oscillator must be a Murata F23. The use of other oscillators leads to frequency discrepancies and spurious oscillations.
3. Pin 14 is the SNC control input. It uses the S-meter output from pin 1 to automatically vary the stereo separation with the input signal strength. It is also possible to reduce noise resulting from weak stereo signals.
4. Pin 13 is the HCC control input. It uses the S-meter output from pin 1 to automatically vary the multiplexer output high-frequency characteristic with the input signal strength. The capacitor at pin 12 determines the maximum attenuation for this band. Too big a capacitance, however, will degrade music quality and make the audibility unstable during reception.
5. Pin 24 is the 19 kHz pilot signal input. Capacitively couple the 19 kHz component from pin 11 to pin 24.
6. Pin 25 is the stereo lamp signal. Current flows only for stereo signals. Leaving the pin open forces monaural operation.
7. The VCO always operates during both stereo and monaural operation.
8. Pins 15 and 16 are the left- and right-channel outputs. The capacitors at these pins determine the amount of deemphasis — 50 µs using 0.015 µF, and 75 µs using 0.022 µF.
9. Pin 18 is the pilot cancel signal output. Adjust the variable resistor between pins 17 and 18 to minimize the 19 kHz pilot signal components in the left- and right-channel outputs for correct channel balance.
10. When adjusting the pilot cancel signal output, connect a 20 kHz lowpass filter (for example, a DIN audio filter) to the multiplexer output to remove the 38 kHz component and prevent its affect on the process of minimizing the 19 kHz component.
11. The capacitor connected to pin 34 is used to detect the pilot cancel signal. It should be connected to V_{CC} or GND. In the case of V_{CC}, use a capacitor with no DC leakage.

Coil Specifications

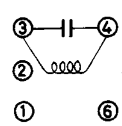
600YEAS-6889GW (Toko)



For European markets

C = 100 pF internal

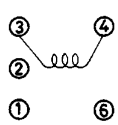
600YEAS-6890GW (Toko)



For North American and Japanese markets

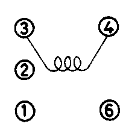
C = 51 pF Internal

M7-T1-31301 (Mitsumi)



YD-0214
For European markets

C = 100 pF External

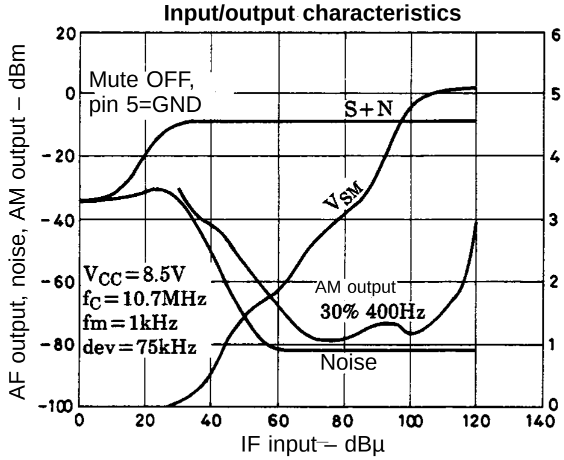


YD-9493-3
For North American and Japanese markets

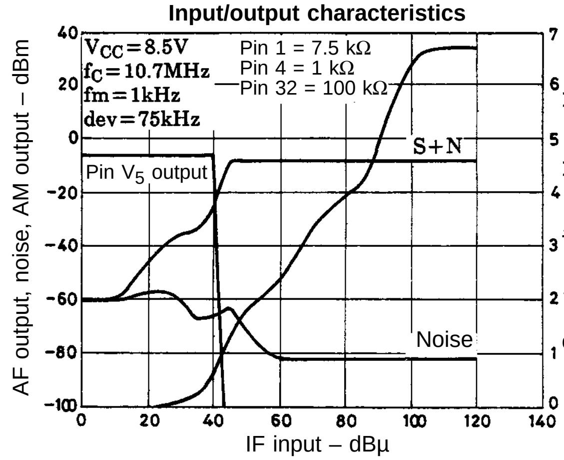
C = 51 pF External

Note: The dotted lines in the characteristics diagrams on the following pages represent device operation outside the device specifications.

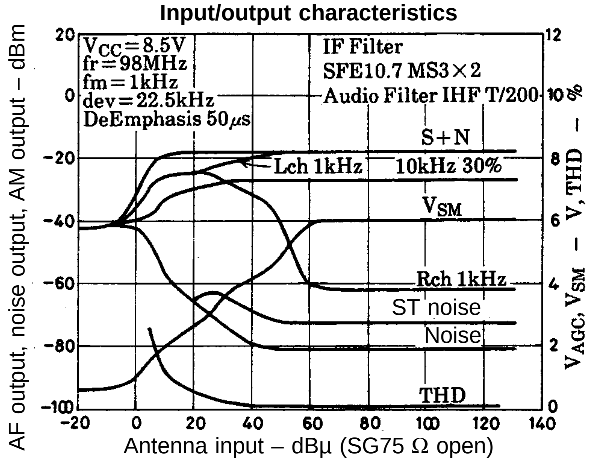
Input/output characteristics



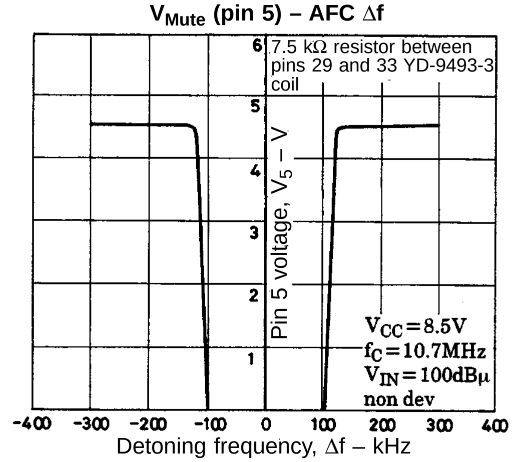
Input/output characteristics



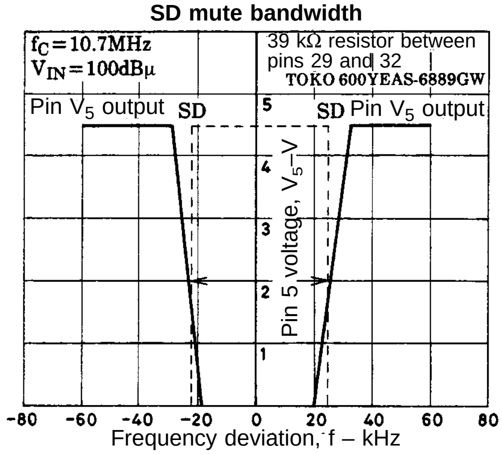
Input/output characteristics



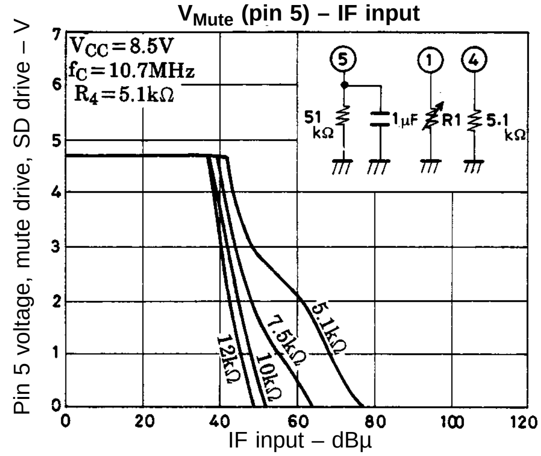
V_{Mute} (pin 5) – AFC Δf



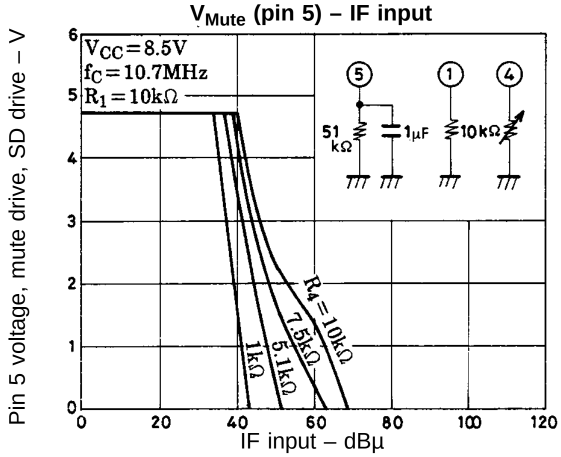
SD mute bandwidth



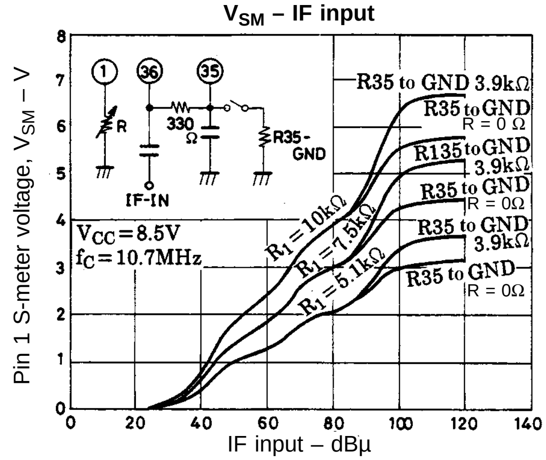
V_{Mute} (pin 5) – IF input



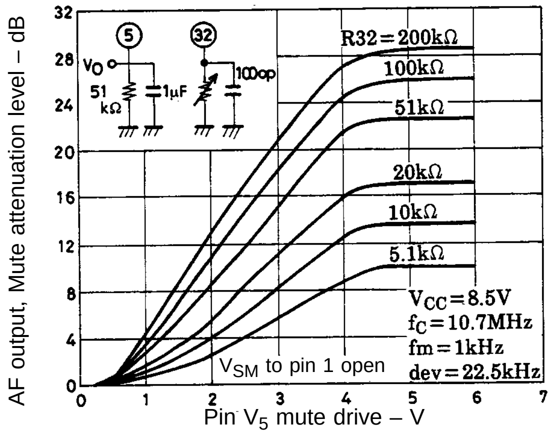
V_{Mute} (pin 5) – IF input



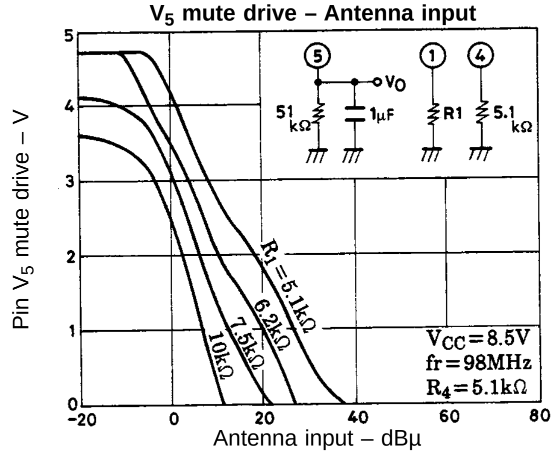
V_{SM} – IF input



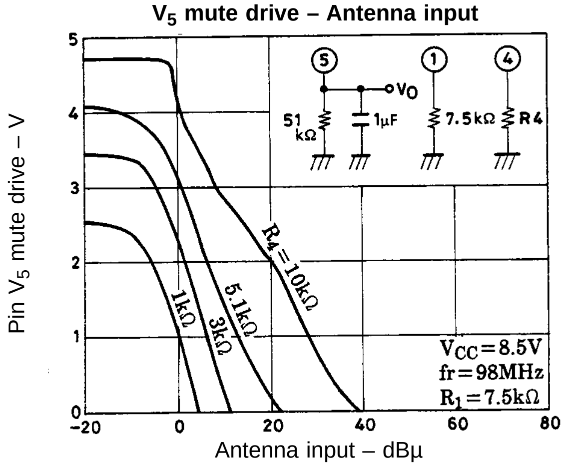
Mute-Att – Mute Drive



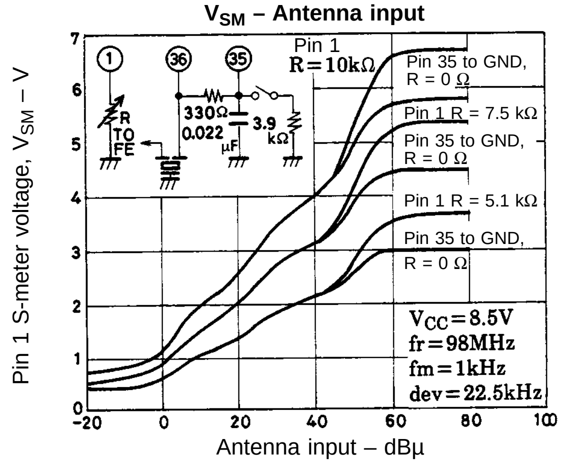
V_5 mute drive – Antenna input



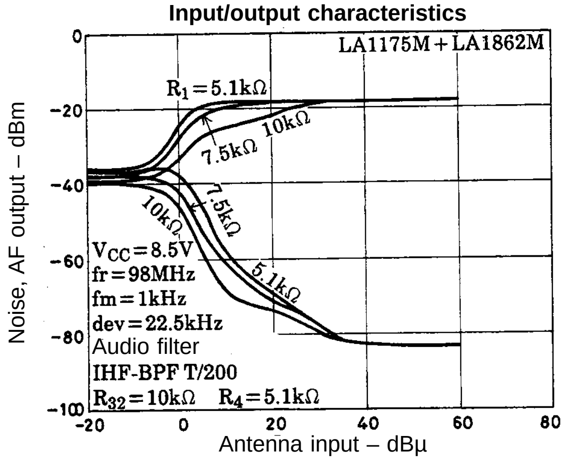
V_5 mute drive – Antenna input



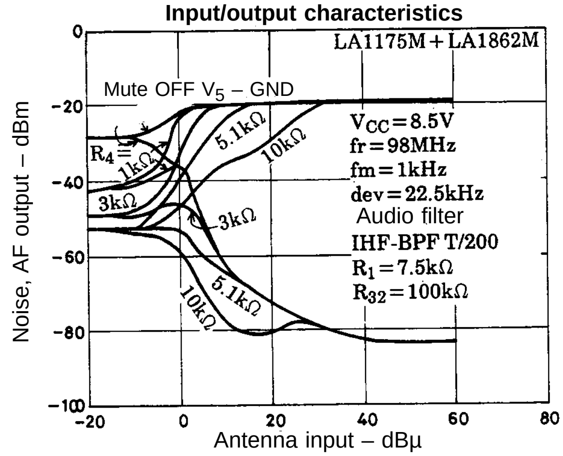
V_{SM} – Antenna input



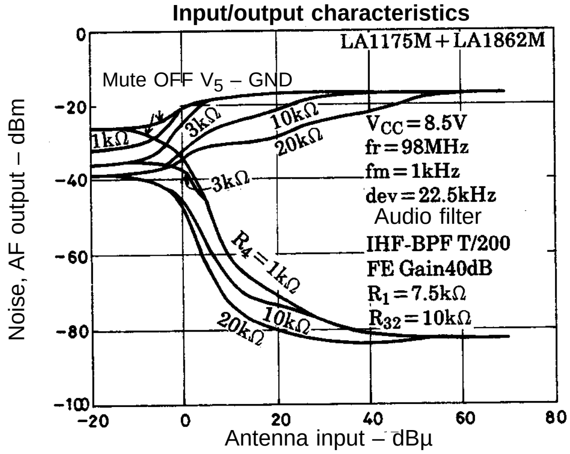
Input/output characteristics



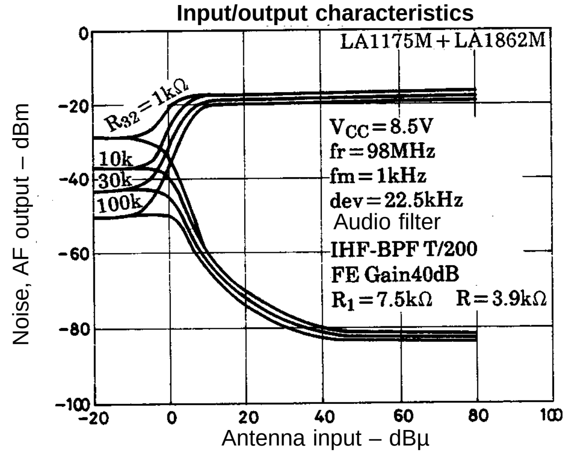
Input/output characteristics



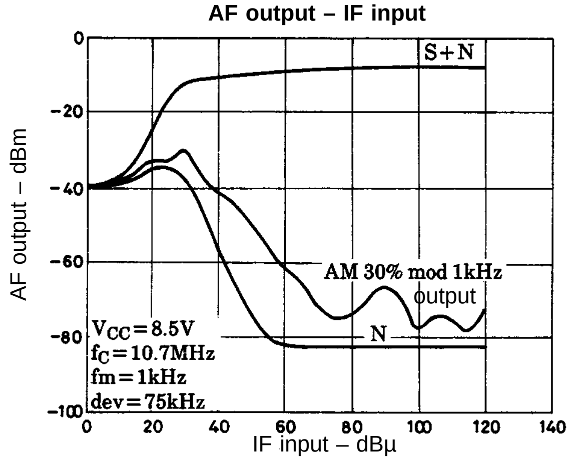
Input/output characteristics



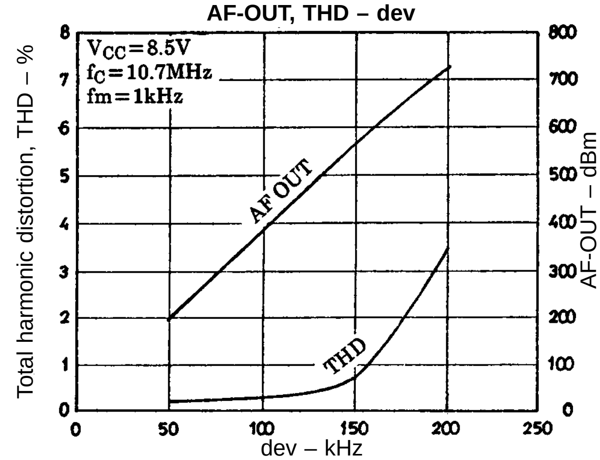
Input/output characteristics



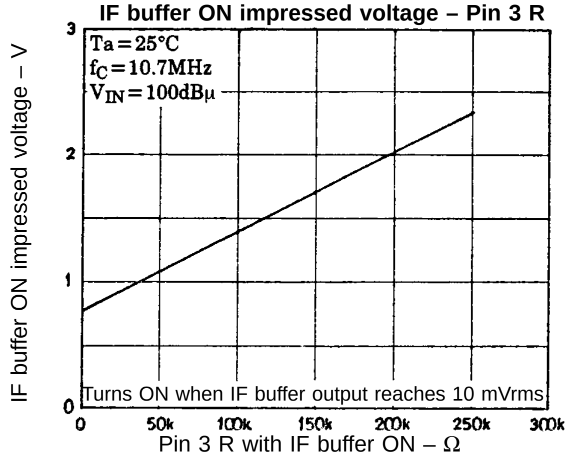
AF output – IF input



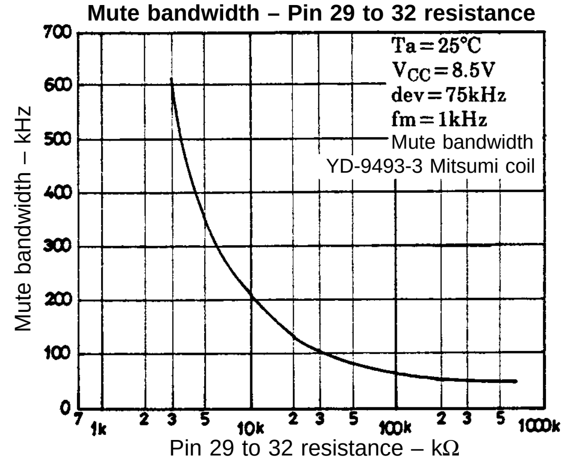
AF-OUT, THD – dev



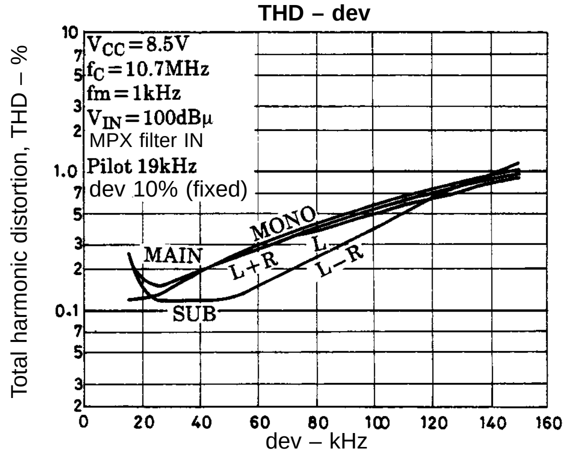
IF buffer ON impressed voltage – Pin 3 R



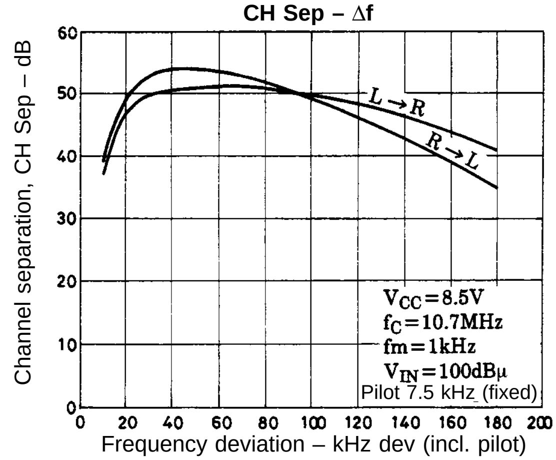
Mute bandwidth – Pin 29 to 32 resistance



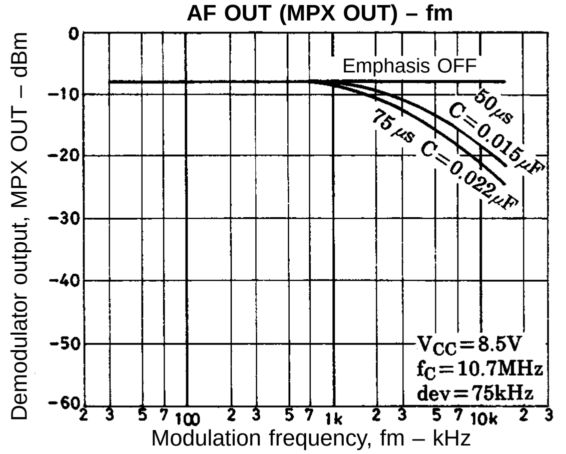
THD – dev



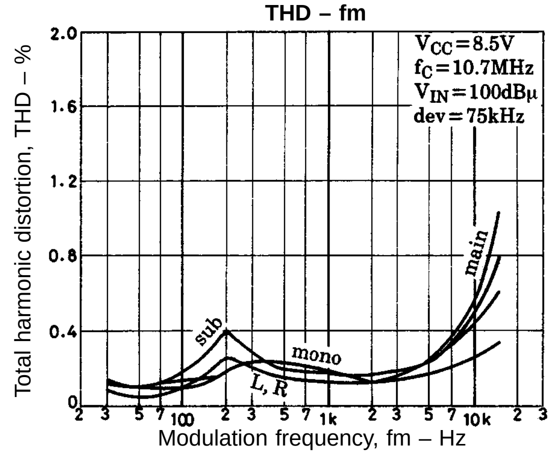
CH Sep – Δf



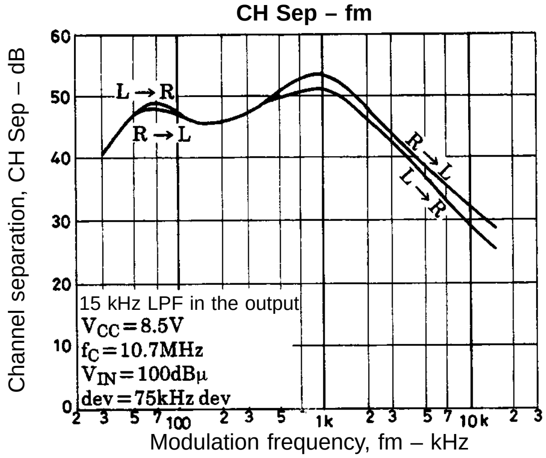
AF OUT (MPX OUT) – fm



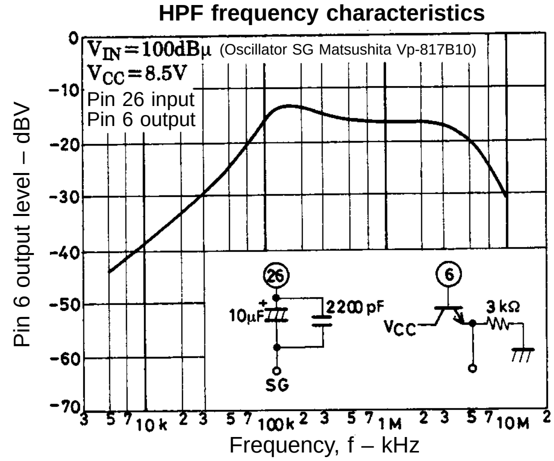
THD – fm



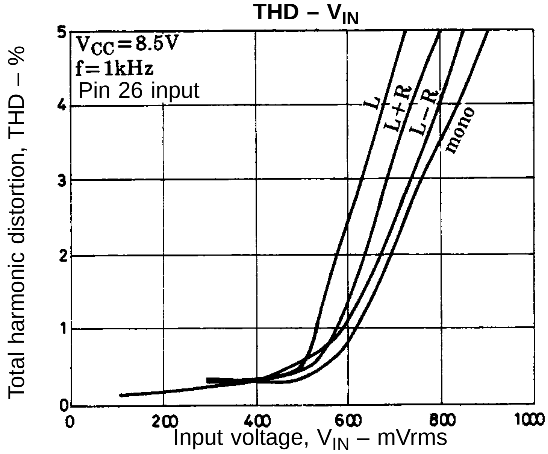
CH Sep – fm



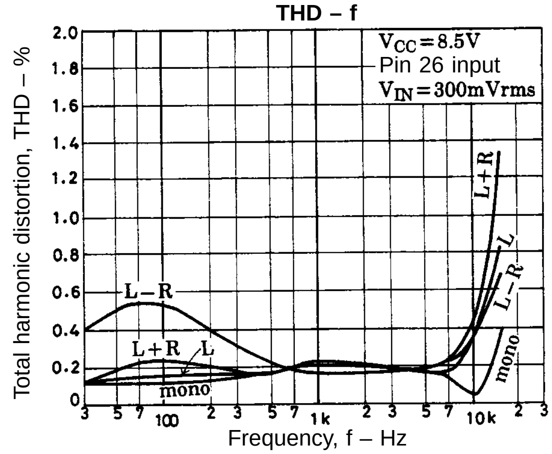
HPF frequency characteristics



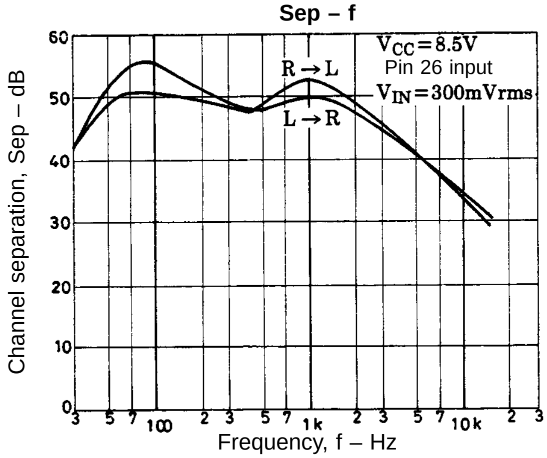
THD – V_{IN}



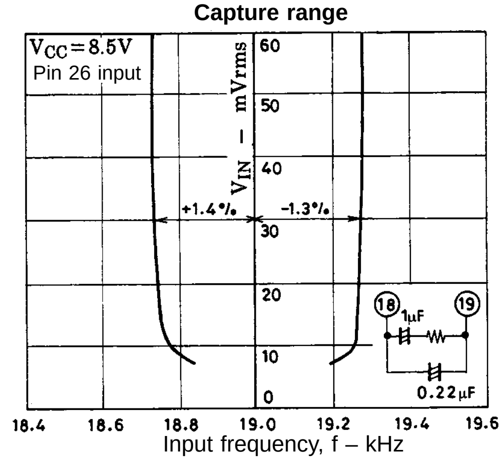
THD – f



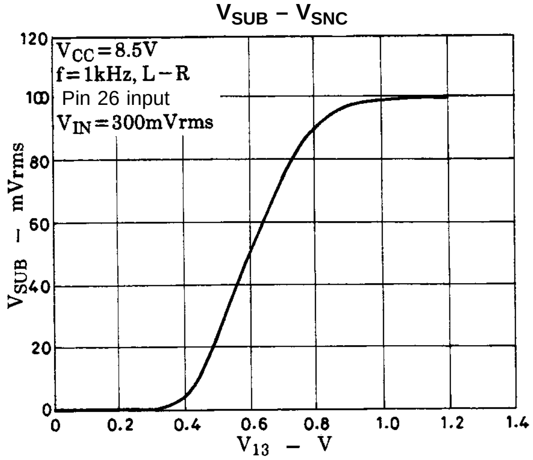
Sep – f



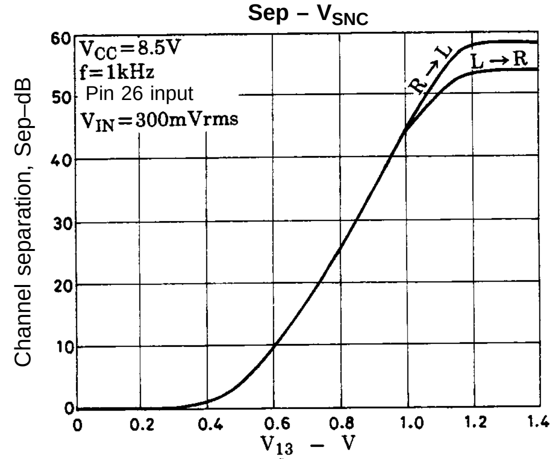
Capture range



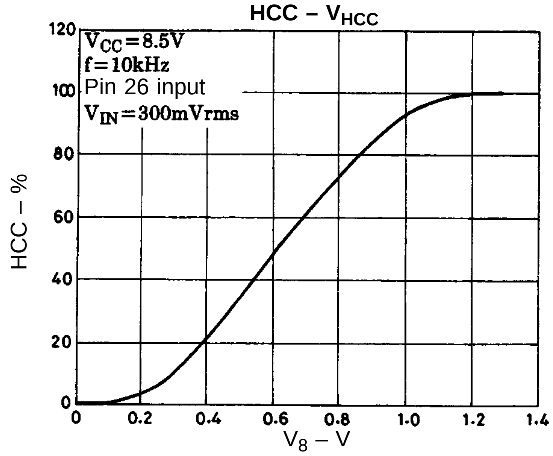
V_{SUB} – V_{SNC}



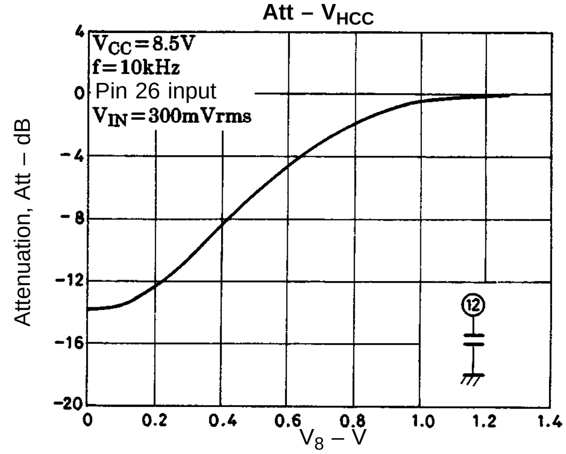
Sep – V_{SNC}



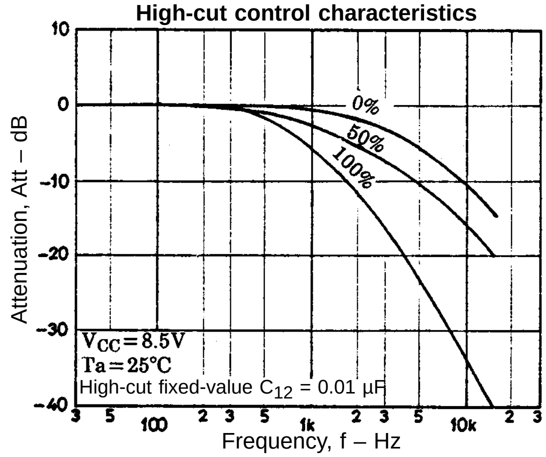
HCC – V_{HCC}



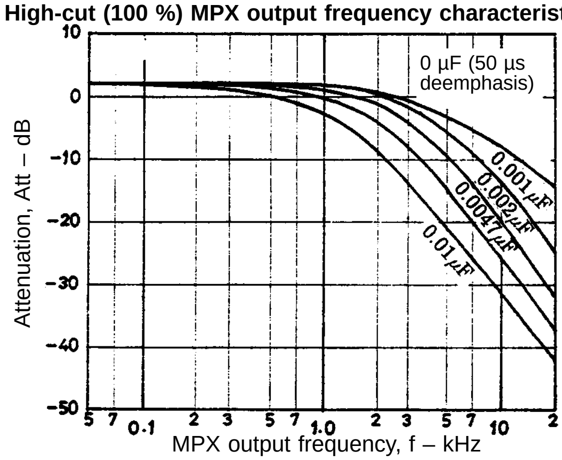
Att – V_{HCC}



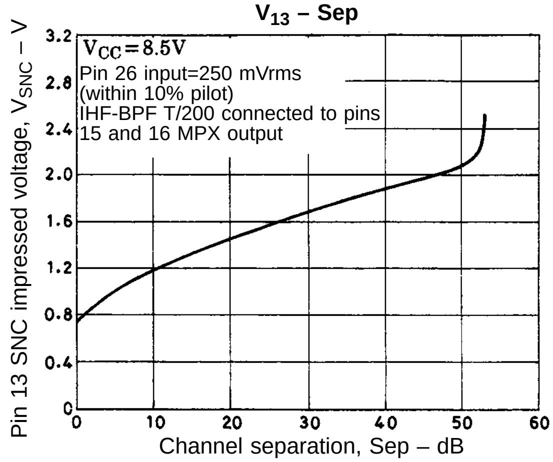
High-cut control characteristics



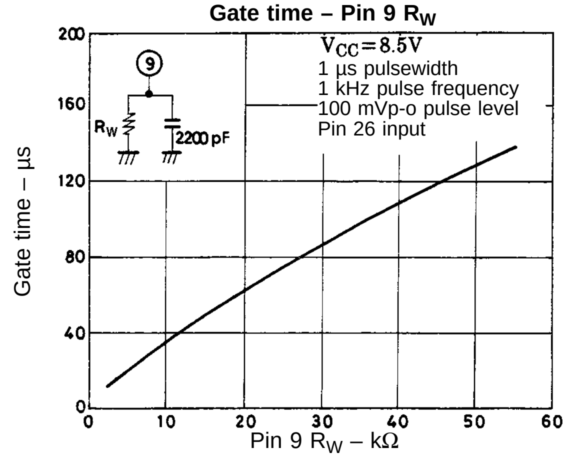
High-cut (100 %) MPX output frequency characteristics



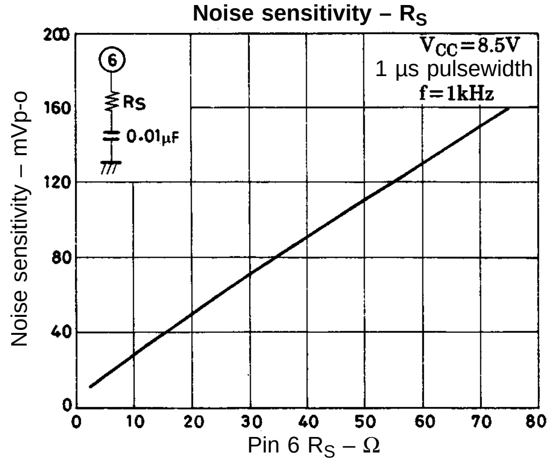
V_{13} – Sep



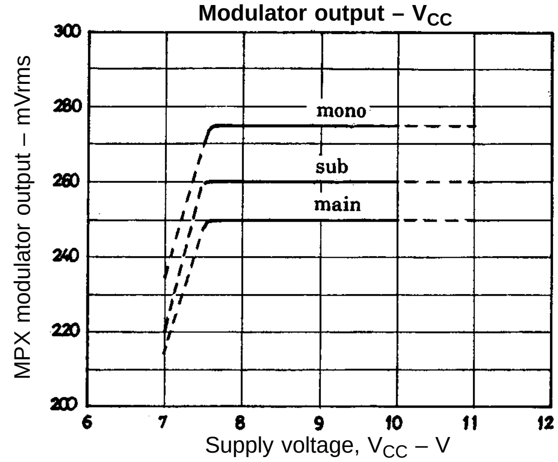
Gate time – Pin 9 R_W



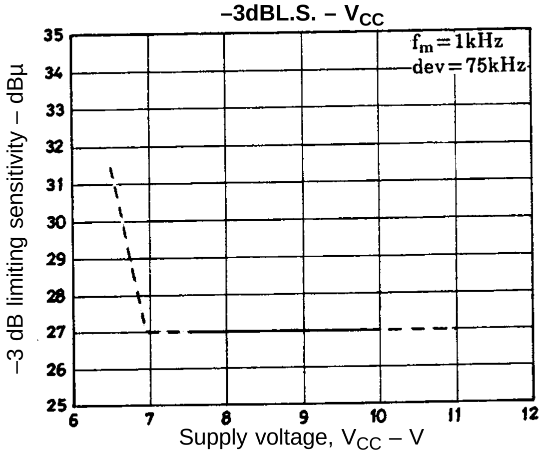
Noise sensitivity – R_S



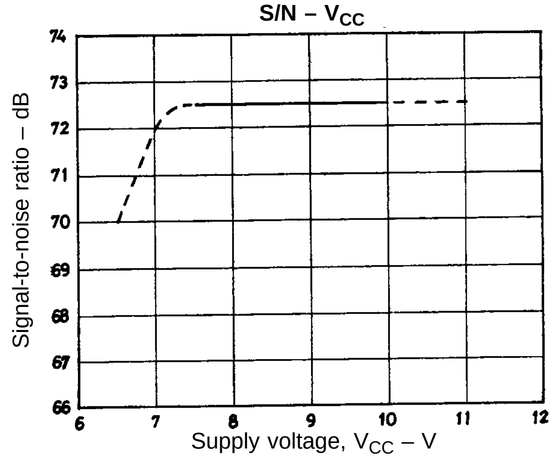
Modulator output – V_{CC}



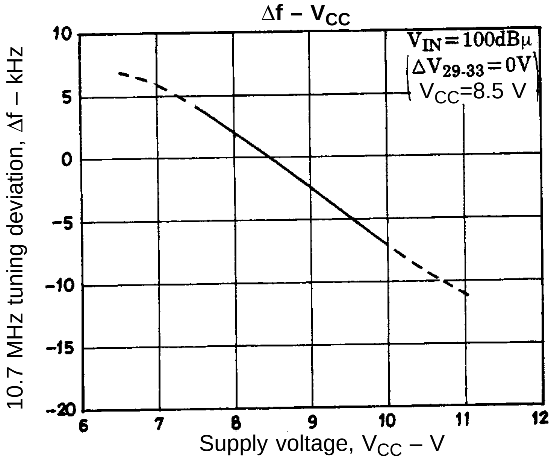
–3dBL.S. – V_{CC}



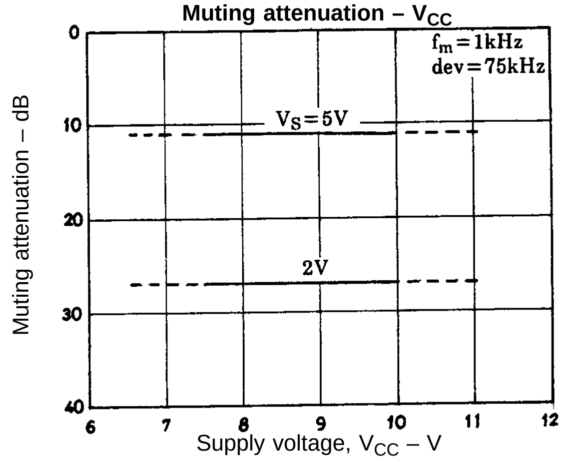
S/N – V_{CC}



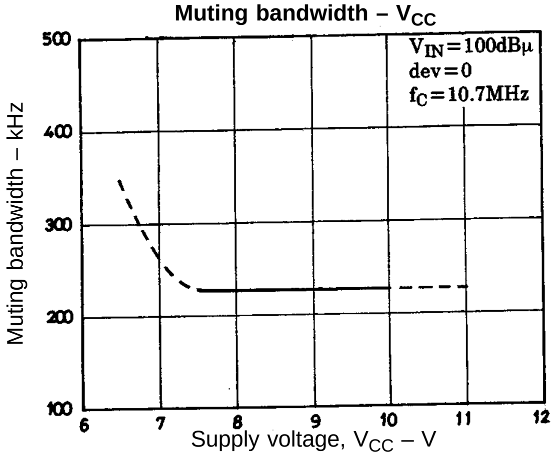
Δf – V_{CC}



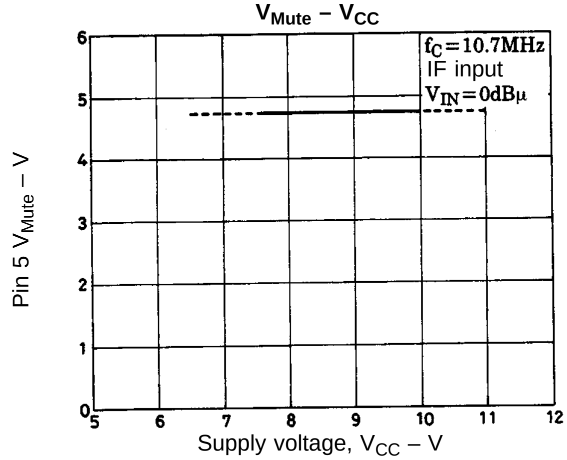
Muting attenuation – V_{CC}



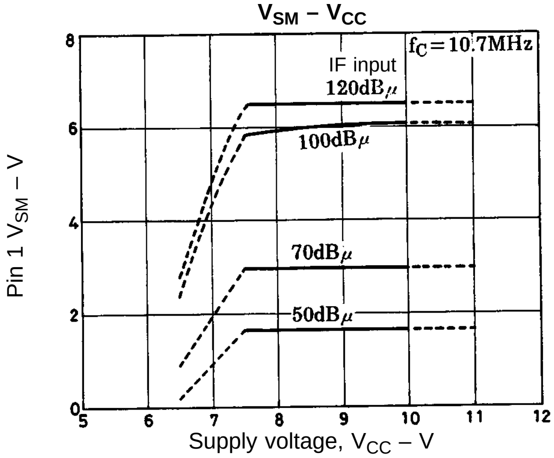
Muting bandwidth – V_{CC}



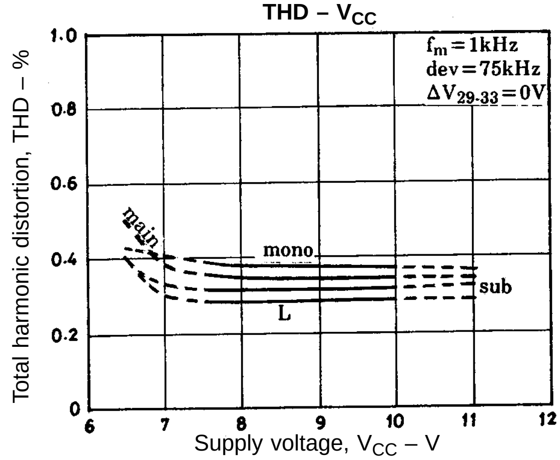
V_{Mute} – V_{CC}



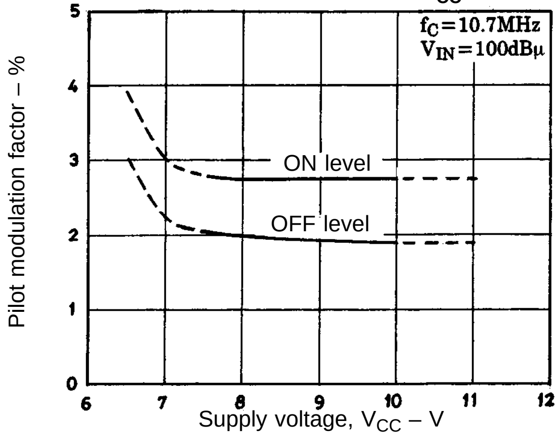
V_{SM} – V_{CC}



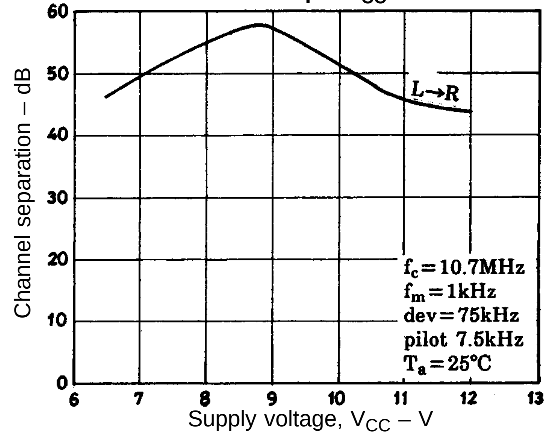
THD – V_{CC}



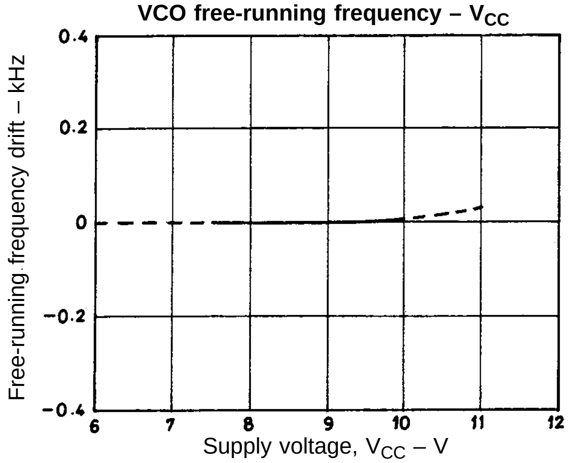
Pilot indicator level – V_{CC}



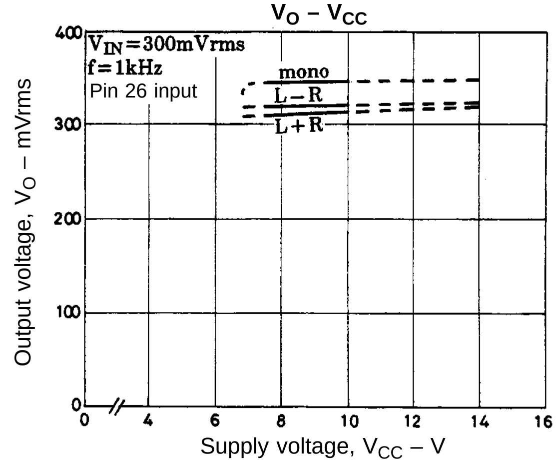
CH Sep – V_{CC}



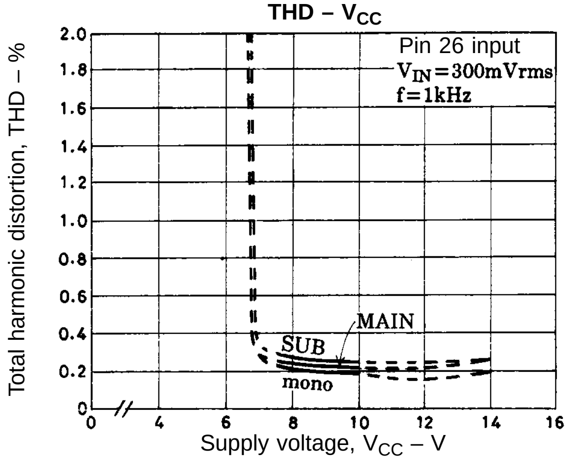
VCO free-running frequency – V_{CC}



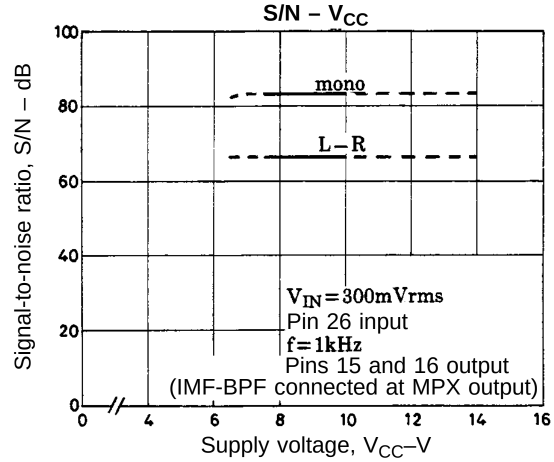
V_O – V_{CC}



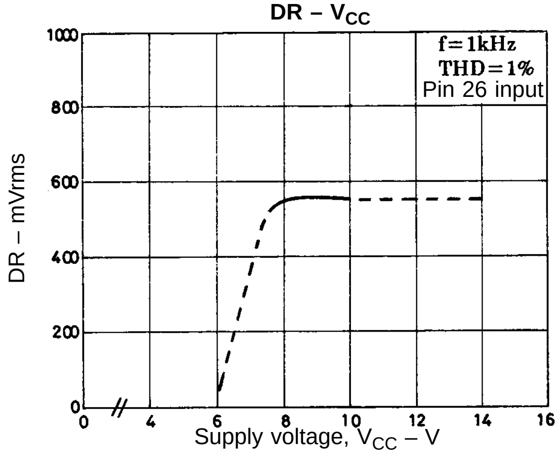
THD – V_{CC}



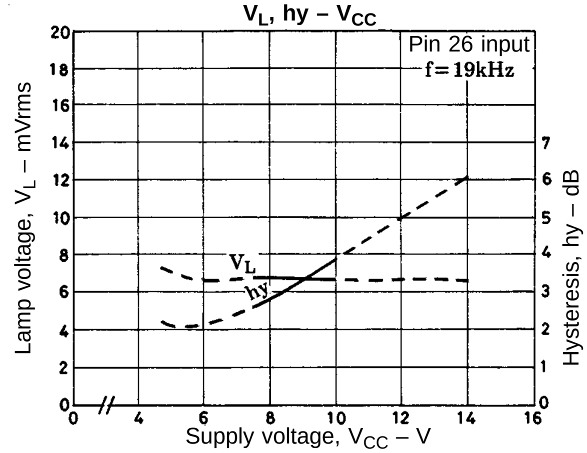
S/N – V_{CC}



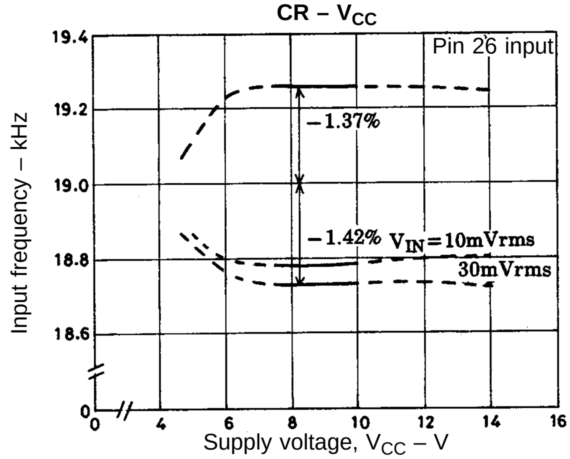
DR – V_{CC}



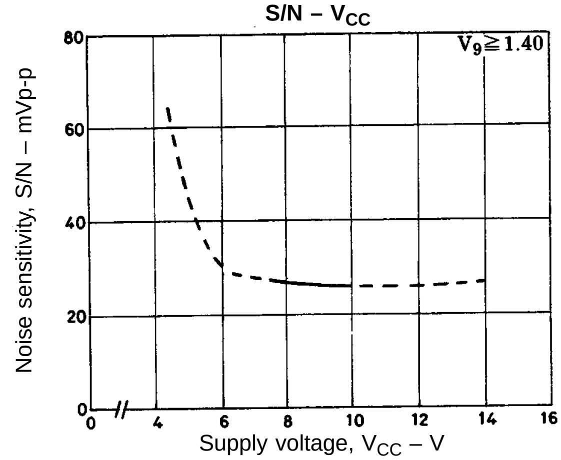
V_L, hy – V_{CC}



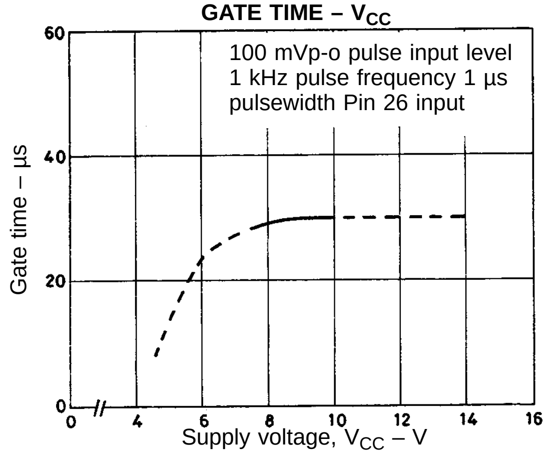
CR – V_{CC}



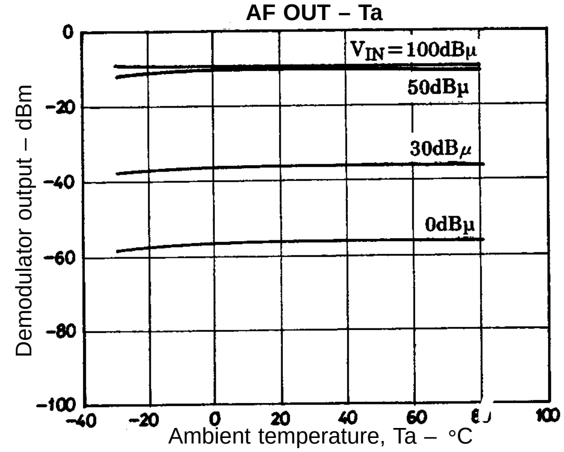
S/N – V_{CC}



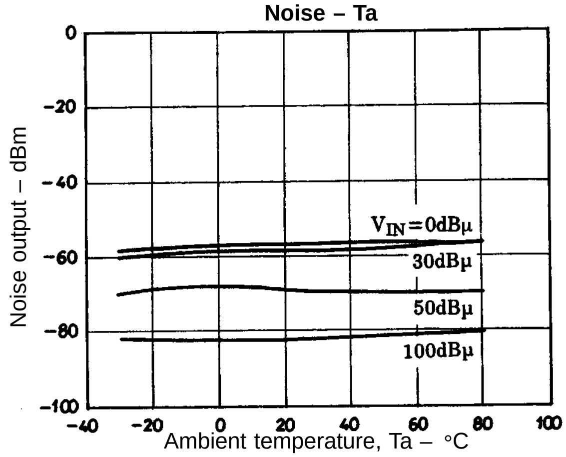
GATE TIME – V_{CC}



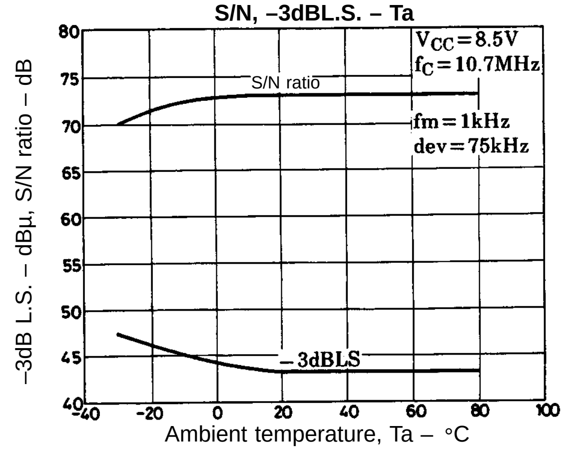
AF OUT – Ta



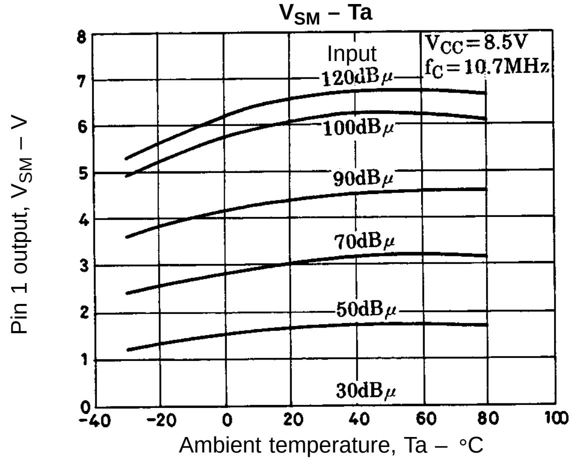
Noise – Ta



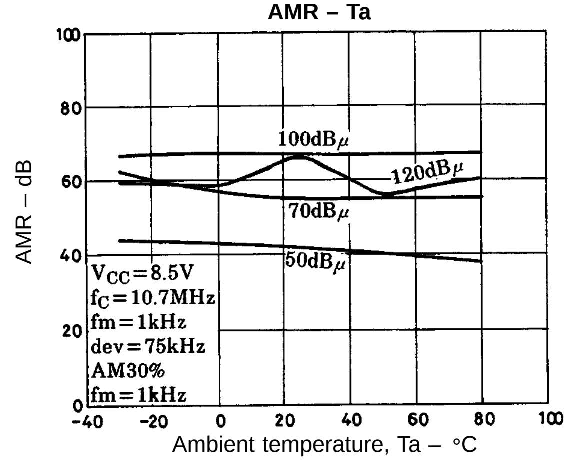
S/N, –3dBL.S. – Ta



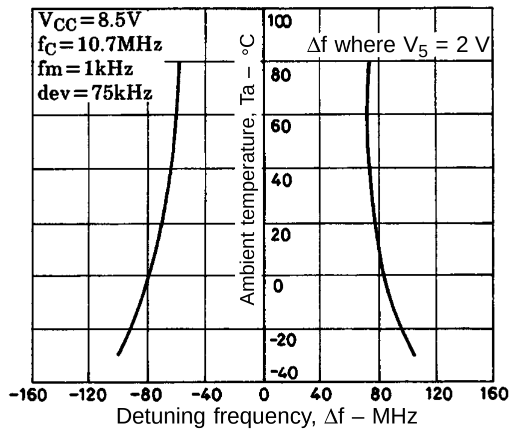
V_{SM} – Ta



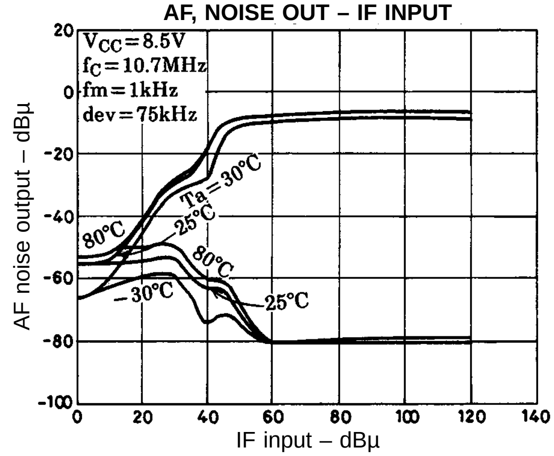
AMR – Ta



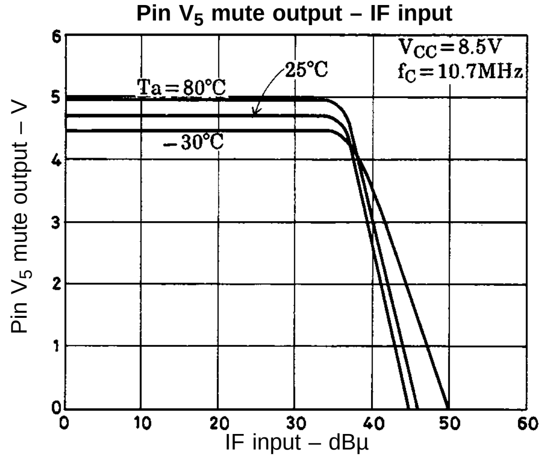
Ta – Δf



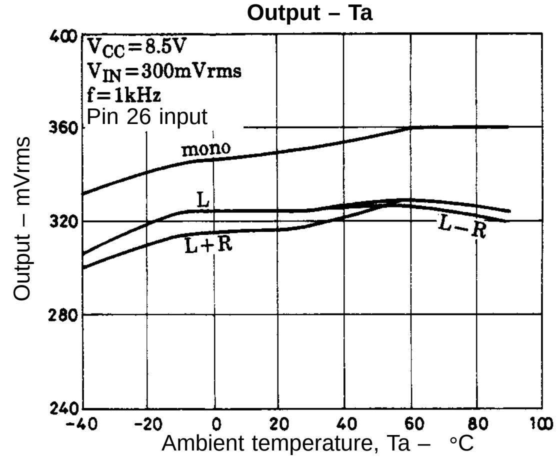
AF, NOISE OUT – IF INPUT



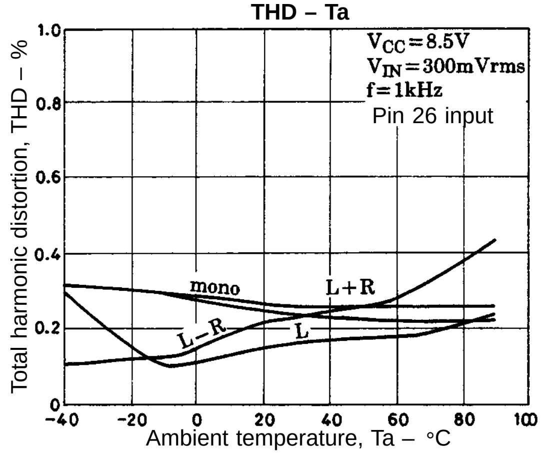
Pin V5 mute output – IF input



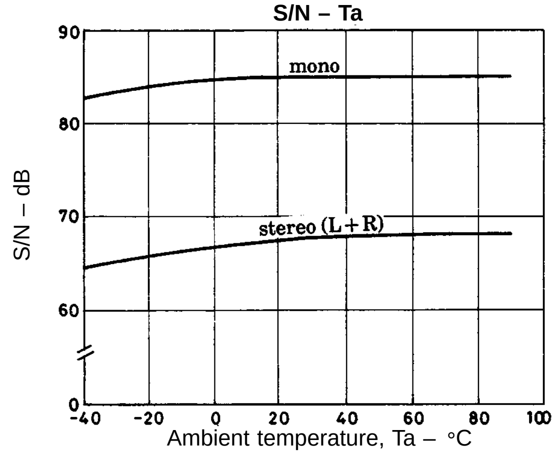
Output – Ta



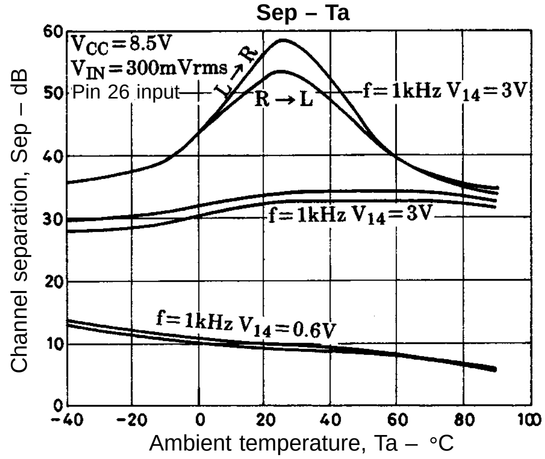
THD – Ta



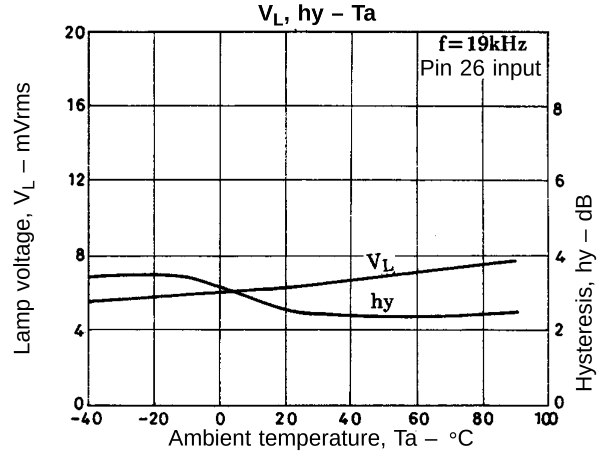
S/N – Ta



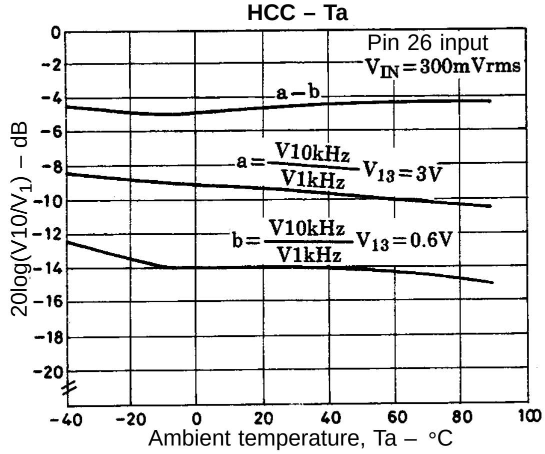
Sep – Ta



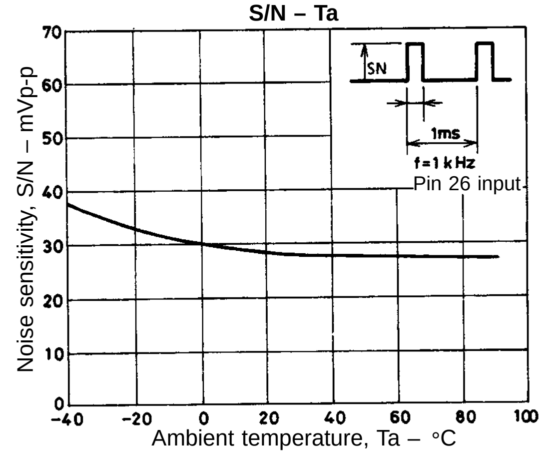
V_L, hy – Ta



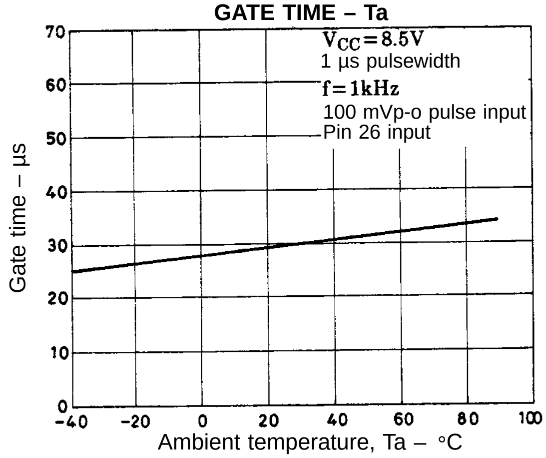
HCC – Ta



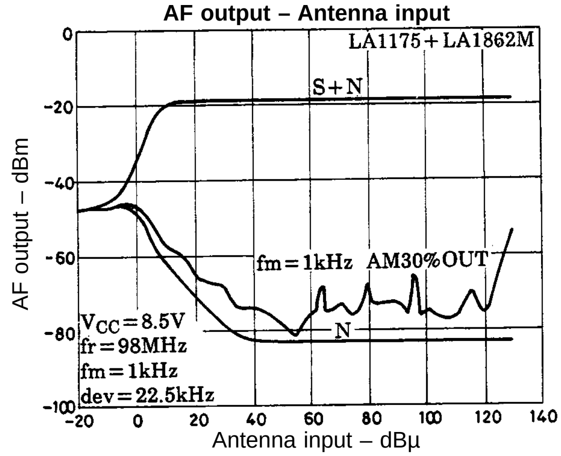
S/N – Ta



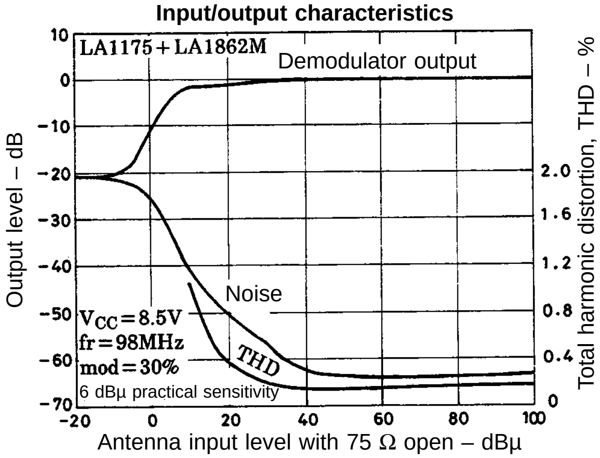
GATE TIME – Ta



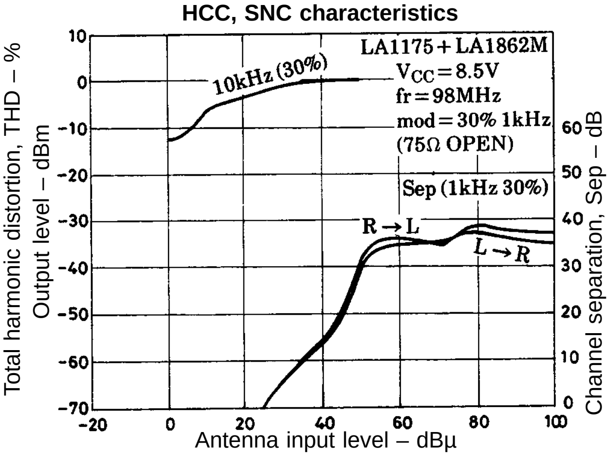
AF output – Antenna input



Input/output characteristics



HCC, SNC characteristics



V_{CC} – Input level