Ordering number : EN8137A

SANYO Semiconductors
DATA SHEET

LC74152B — CMOS IC For digital TV TS+Audio+Video decoder LSI with built-in OSD

Overview

The LC74152B is TS+Audio+Video decoder LSI with built-in OSD for digital TV.

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Features

- MULTI2 type descrambler, TS-Demultiplexer, video decoder, and audio decoder functions incorporated
- Video decoder converts the HDTV (MPEFG MP@HL) stream input to 480P/480i for output.
  Audio decoder compatible with MPEG-AAC and MPEG-BC
- OSD compatible with data broadcasting standard of BS digital broadcast
- NTSC video encoder incorporated (compatible with Microvision)
- Compatible with the 16bit Intel/Power PC bus type host CPU interface
- SDRAM 128Mbit (32bit × 2M × 2 pieces, 135MHz, CL=3) externally incorporated
- Supply voltage: 1.8V(Internal), 3.3V(I/O)

Functions

[Ts decoder block]

- Compatible with two TS channel inputs
- 8bit parallel TS input
- Internal/external synchronization selectable
- Compatible with 55 INDICES, enabling setting of PID and channel No, for each INDEX.
- Compatible with the video filter PID and splicing of channel No.
- Two independent PCR filters incorporated
- Automatic load function incorporated to enable automatic setting to the reference counter each time PCR is received.
- 27MHz count-down timer incorporated
- 27MHz system clock PWM control possible

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- "Multi2" type descrambling function incorporated
- 32 independent data filters incorporated
- Compatible with the duplicate packet
- Three independent video filters and two independent audio filters incorporated

[Video decoder block]

- HD stream down-decoded to 480i/480p
- HD 2ch down replay, HD down and 480p normal 2ch replay, and 480p 3ch normal replay possible
- Compatible with special replay (trick mode), enabling smooth double-speed replay and smooth reverse replay.
- Four operation modes; 2ch mode, 3ch mode, trick 1ch mode, trick 2ch mode.

Operation mode(SDRAM mapping)	2ch	3ch	Trick 1ch	Trick 2ch
HD(1080i/720p) down replay	○	×	○	×
HD×2ch down replay	○	×	×	×
HD down and 480p/SD normal 2ch replay	○	×	×	×
480p/SD×3ch normal replay	×	○	×	×
480p/SD×2ch normal replay	○	○	×	×
480p/SD normal replay	○	○	○	○
HD/480p/SD normal replay+external SD input	○	×	×	×
Double-speed and slow replays	○	○	○	○
Reverse and forward replays	×	×	○	○

[Audio decoder block]

- MPEG-AAC 5.1ch decoding possible. (2ch output through down mixing)
- MPEG-BC decoding possible
- Two DAC interfaces. (Normal output and output for recording)
- DIT 5.1ch output or 2ch output
- Compatible with double-speed replay function

[OSD block]

- Compatible with 480i/480p display
- Compatible with YUV422 format of 16bit/pixel and CLUT8 format of 8 bit/pixel
- BMP drawing of transmitted picture, copy between planes, and rectangular painting in single color possible
- Setting possible of either the ON mode in which only the set data is drawn or the OFF mode in which data other than set ones is drawn.
- Plane setting and overlapping of a total of maximum five planes possible, including one plane of still picture of half-HD resolution, two planes of CLUT 8 picture, and two planes of CLUT 8 picture.
- CLUT table value of 2561 INDEX setting possible for the half HD resolution and SD resolution respectively
- Blending by pixel possible for CLUT8 picture
- Scaling (reduced) display possible for drawn plane picture
- Compatible with OSD two pictures

[Scaler block]

- Two scalers incorporated to enable two-plane composition or recording output
- Multi-view three screen display possible for BS digital broadcast
- Picture scaling possible from magnification by 2048 to reduction by 1/31
- Digital single-channel input/output I/F (16bit: YUV422) and single-channel output I/F (8bit: YUV422) available
- For the digital single-channel input/output I/F, SD video input/main output selectable

[Encoder block]

- Compatible with interlaced video encode of NTSC
- Picture output of two systems possible
- Composite (Y, C, CVBS) and component (Y, Pb, Pr) picture output possible
- Compatible with MACROVISION Revision7.1.L1
- Compatible with CGMS/A, Closed Caption (NTSC) overlap

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Power supply voltage	V_{DD}		-0.5		2.2	V
I/O power supply voltage	V_D33		-0.5		4.0	V
Input voltage	V_I		-0.5		6.0	V
Output voltage	V_O		-0.5		6.0	V
Operation temperature	Topr		-30		70	°C
Storage temperature	Tstg		-65		150	°C

Allowable Operating Range

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Power supply voltage	V_{DD}		1.77		1.98	V
I/O power supply voltage	V_D33		3.0		3.6	V
Input low voltage	V_{IL}		-0.3		0.8	V
Input high voltage	V_{IH}		2.0		5.5	V
Threshold point	V_T			1.58		V
Schmidt trig. Low to high threshold point	V_T+			1.50		V
Schmidt trig. high to low threshold point	V_T-			0.93		V

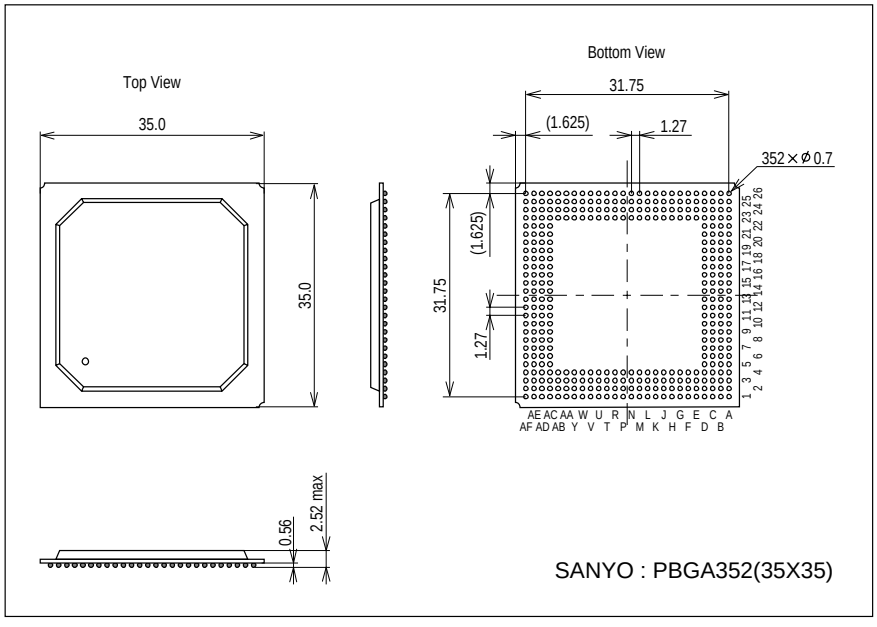
Electrical Characteristics

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Input leakage current	I_L	V_I=3.3V or 0V		±0.01	±1	μA
Tri-stage output leakage current	I_{OZ}	V_O=3.3V or 0V		±0.01	±1	μA
Pull-up resistor	R_{PU}			70		kΩ
Pull-down resistor	R_{PD}			58		kΩ
Output low voltage	V_{OL}	I_{OL}=4mA			0.4	V
Output high voltage	V_{OH}	I_{OH}=4mA	2.4			V

Package Dimensions

unit : mm (typ)

3294

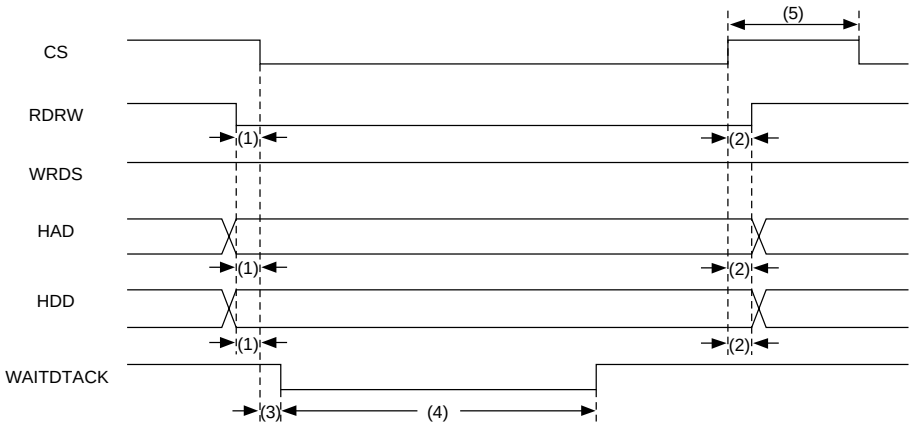


Input/output timing

(1) Host Interface timing

- Power PC system timing

[WRITE operation]



(1) 0ns or more (for fall of CS)
(2) 0ns or more (for rise of CS)
(3) Max 5ns (for fall of CS)
(4) 50ns to 130ns
(5) 10ns or more (up to the next fall of CS)

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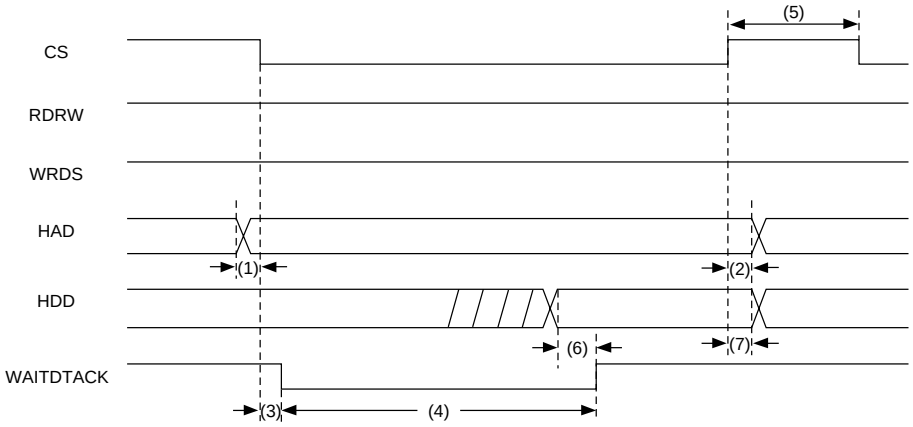
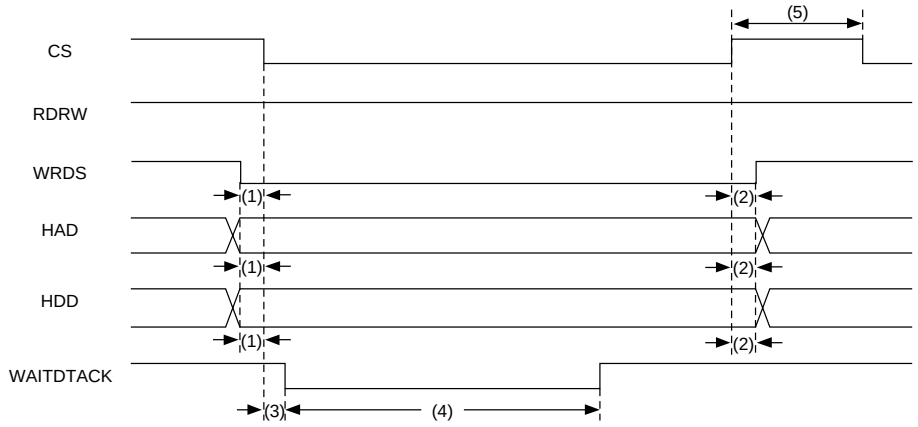
[READ operation]



(1) 0ns or more (for fall of CS)
(2) 0ns or more (for rise of CS)
(3) Max 5ns (for fall of CS)
(4) 60ns to 160ns
(5) 10ns or more (up to the next fall of CS)
(6) Max 10ns (for rise of WAITDTACK)
(7) Max 0ns (for rise of CS)

ILC05555

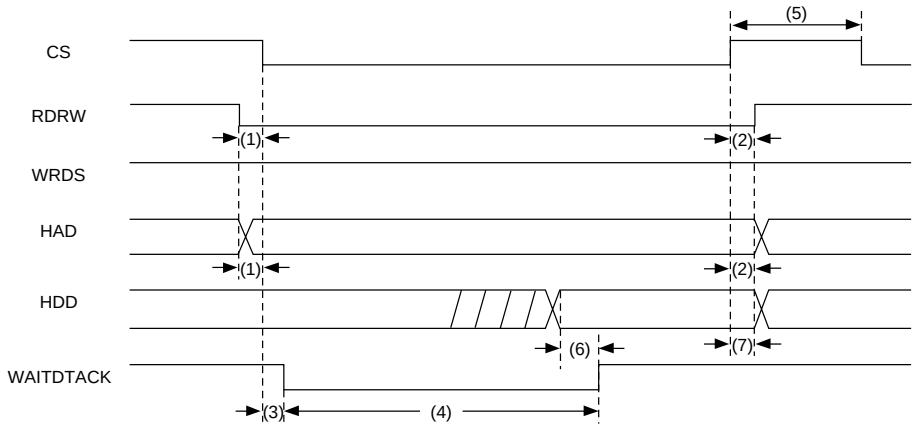
• Intel system timing
[WRITE operation]



(1) 0ns or more (for fall of CS)
(2) 0ns or more (for rise of CS)
(3) Max 5ns (for fall of CS)
(4) 50ns to 130ns
(5) 10ns or more (up to the next fall of CS)

ILC05556

[READ operation]



(1) 0ns or more (for fall of CS)
(2) 0ns or more (for rise of CS)
(3) Max 5ns (for fall of CS)
(4) 60ns to 160ns
(5) 10ns or more (up to the next fall of CS)
(6) Max 10ns (for rise of WAITDTACK)
(7) Max 0ns (for rise of CS)

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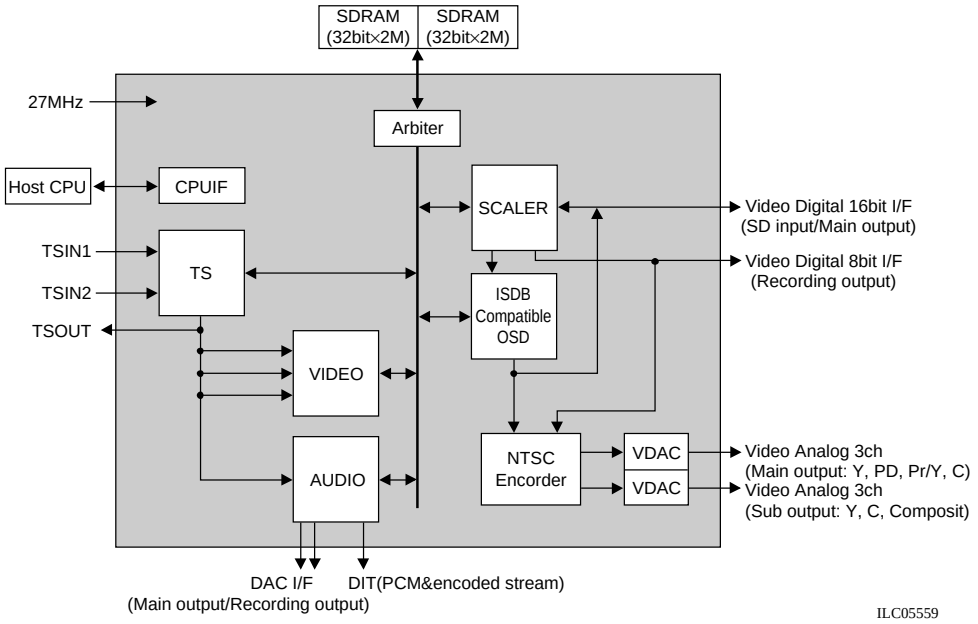
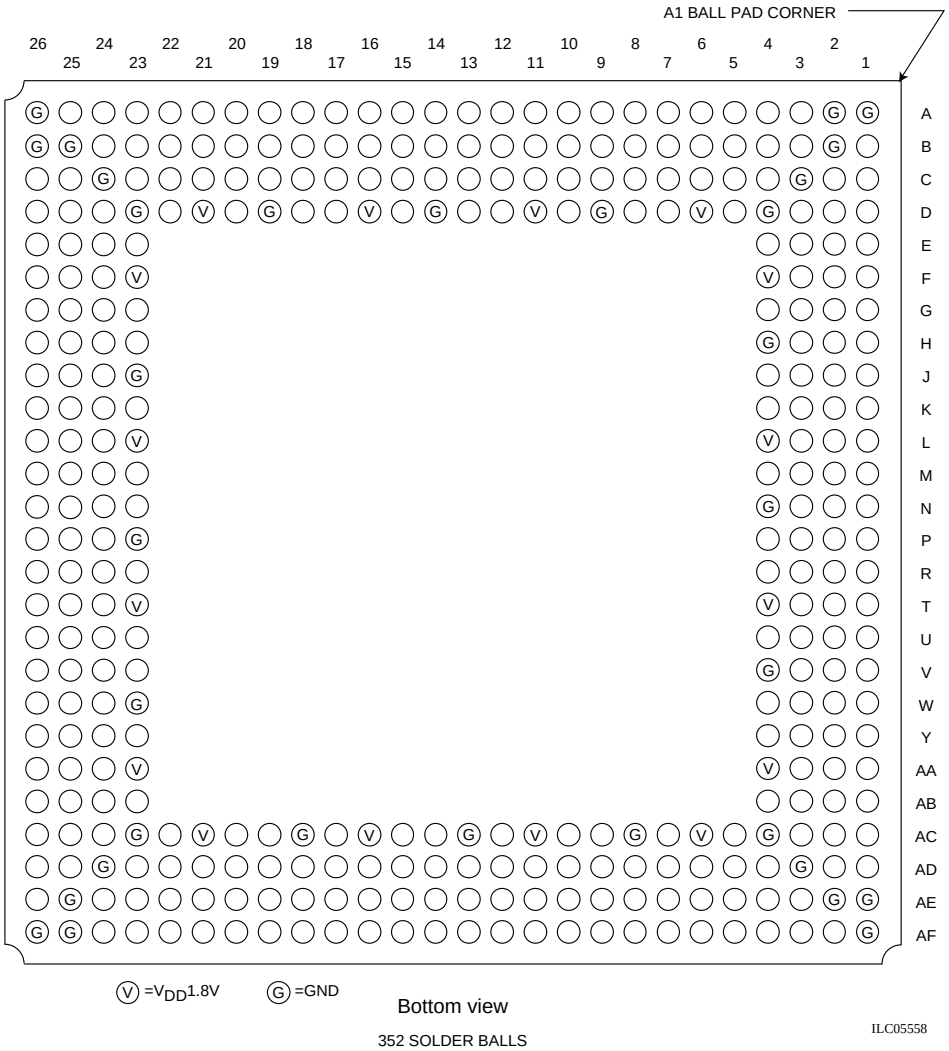
Internal Block Diagram



Pin Assignment



Pin Functions

BALL	Pin Name	I/O	Functions
C2	TS2IN0	IN	TS data input 2
C1	TS2IN1	IN	TS data input 2
D2	TS2IN2	IN	TS data input 2
D3	TS2IN3	IN	TS data input 2
D1	TS2IN4	IN	TS data input 2
E2	TS2IN5	IN	TS data input 2
E4	TS2IN6	IN	TS data input 2
E3	TS2IN7	IN	TS data input 2
E1	TS2CK	IN	TS clock input 2
F2	$V_{DD}2$	-	$V_{DD}3.3V$
G4	TS2SYNC	IN	TS Sync input 2
F3	TS2RDY	OUT	TS Ready output 2
F1	TS2VALID	IN	TS Valid input 2
G2	TS2ERR	IN	TS error flag input 2
G1	TSOUT0	OUT	TS data output
G3	TSOUT1	OUT	TS data output
H2	TSOUT2	OUT	TS data output
J4	TSOUT3	OUT	TS data output
H1	TSOUT4	OUT	TS data output
H3	TSOUT5	OUT	TS data output
J2	$V_{DD}2$	-	$V_{DD}3.3V$
J1	TSOUT6	OUT	TS data output
K2	TSOUT7	OUT	TS data output
J3	TSOCKO	OUT	TS clock output
K1	TSOVALID	OUT	TS data Valid flag output
K4	TSOSYNC	OUT	TS data Sync flag output
L2	ASVALID	OUT	TS Audio data Valid flag output
K3	ASSYNC	OUT	TS Audio data Sync flag output
L1	DASCLK	IN/OUT	Audio system clock output for Audio DAC
M2	DABCK	OUT	Audio system bit clock output for Audio DAC
M1	$V_{DD}2$	-	$V_{DD}3.3V$
L3	DALRCK	OUT	Audio LR clock output for Audio DAC
N2	DAO1	OUT	Audio serial data output (normal output) for Audio DAC
M4	DAOR	OUT	Audio serial data output (for recording) for Audio DAC
N1	SPDOUT	OUT	Audio S/P DIF output
M3	RSTN	IN	Hard reset (Low Active)
P2	INT	OUT	External CPU interrupt request output
P4	VCXO_CNT	OUT	PWM output for 27MHz PLL control
P1	CLK	IN	System clock 27MHz
N3	$V_{DD}2$	-	$V_{DD}3.3V$
R2	CPUTYPE	IN	External CPU bus type setting (L: Intel H: PowerPC)
P3	TEST7	IN	TEST pin (Normally L)
R1	HDD15	IN/OUT	External CPU data bus
T2	HDD14	IN/OUT	External CPU data bus
R3	HDD13	IN/OUT	External CPU data bus
T1	HDD12	IN/OUT	External CPU data bus
R4	HDD11	IN/OUT	External CPU data bus
U2	HDD10	IN/OUT	External CPU data bus
T3	HDD9	IN/OUT	External CPU data bus
U1	HDD8	IN/OUT	External CPU data bus
U4	HDD7	IN/OUT	External CPU data bus
V2	$V_{DD}2$	-	$V_{DD}3.3V$

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BALL	Pin Name	I/O	Functions
U3	HDD6	IN/OUT	External CPU data bus
V1	HDD5	IN/OUT	External CPU data bus
W2	HDD4	IN/OUT	External CPU data bus
W1	HDD3	IN/OUT	External CPU data bus
V3	HDD2	IN/OUT	External CPU data bus
Y2	HDD1	IN/OUT	External CPU data bus
W4	$V_{DD}2$	-	V_{DD}3.3V
Y1	HDD0	IN/OUT	External CPU data bus
W3	CS	IN	External CPU bus chip set select
AA2	RDRW	IN	External CPU bus Read (Intel), R/W (PowerPC)
Y4	WRDS	IN	External CPU bus Write (Intel), “H” (PowerPC)
AA1	WAITDTACK	OUT	External CPU bus Wait (Intel), Ready (PowerPC)
Y3	HAD0	IN	External CPU address bus
AB2	VDD2	-	V_{DD}3.3V
AB1	HAD1	IN	External CPU address bus
AA3	HAD2	IN	External CPU address bus
AC2	HAD3	IN	External CPU address bus
AB4	HAD4	IN	External CPU address bus
AC1	HAD5	IN	External CPU address bus
AB3	HAD6	IN	External CPU address bus
AD2	HAD7	IN	External CPU address bus
AE3	HAD8	IN	External CPU address bus
AF2	HAD9	IN	External CPU address bus
AF3	$PLL2AV_{DD}$	-	PLL2 analog V_{DD}1.8V
AE4	$PLL2AV_{SS}$	-	PLL2 analog GND
AD4	$PLL2DV_{DD}$	-	PLL2 V_{DD}1.8V
AF4	$PLL2DV_{SS}$	-	PLL2 GND
AE5	$VD11V_{SS}$	-	VideoDAC1 analog GND
AC5	VD1VOUT	OUT	VideoDAC1 Pr/CVBS output
AD5	$VD11AV_{DD}2$	-	VideoDAC1 analog V_{DD}3.3V
AF5	VD1UOUT	OUT	VideoDAC1 Pb/C output
AE6	$VD12V_{SS}$	-	VideoDAC1 analog GND
AC7	VD1YOUT	OUT	VideoDAC1 Y/Y output
AD6	$VD12AV_{DD}2$	-	VideoDAC1 analog V_{DD}3.3V
AF6	VD1COMP	OUT	VideoDAC1 COMP pin
AE7	VDRSET	IN/OUT	VideoDAC1 RESET pin
AF7	VD1VREFOUT	OUT	VideoDAC1 VREFOUT pin
AD7	VD1VREFIN	IN	VideoDAC1 VREFIN pin
AE8	$VD1DV_{SS}$	-	VideoDAC1 digital GND
AC9	$VD1DV_{DD}$	-	VideoDAC1 digital V_{DD}1.8V
AF8	$VD21V_{SS}$	-	VideoDAC2 analog GND
AD8	VD2VOUT	OUT	VideoDAC2 Pr/CVBS output
AE9	$VD21AV_{DD}2$	-	VideoDAC2 analog V_{DD}3.3V
AF9	VD2UOUT	OUT	VideoDAC2 Pb/C output
AE10	$VD22V_{SS}$	-	VideoDAC2 analog GND
AD9	VD2YOUT	OUT	VideoDAC2 Y/Y output
AF10	$VD22AV_{DD}2$	-	VideoDAC2 analog V_{DD}3.3V
AC10	VD2COMP	OUT	VideoDAC2 COMP pin
AE11	VD2RSET	IN/OUT	VideoDAC2 RESET pin
AD10	VD2VREFOUT	OUT	VideoDAC2 VREFOUT pin
AF11	VD2VREFIN	IN	VideoDAC2 VREFIN pin
AE12	$VD2DV_{SS}$	-	VideoDAC2 digital GND

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BALL	Pin Name	I/O	Functions
AF12	$VD2DV_{DD}$	-	VideoDAC2 digital V_{DD}1.8V
AD11	XDACK	OUT	AudioDSP debug I/F ACK
AE13	DSOD	OUT	AudioDSP debug I/F serial output
AC12	DCK	IN	AudioDSP debug I/F serial clock
AF13	YDA0	IN/OUT	Videol digital Y data input/output/AudioDSP debug I/F DSL
AD12	YDA1	IN/OUT	Videol digital Y data input/output/AudioDSP debug I/F DS ID
AE14	YDA2	IN/OUT	Video1 digital Y data input/output
AC14	YDA3	IN/OUT	Video1 digital Y data input/output
AF14	YDA4	IN/OUT	Video1 digital Y data input/output
AD13	YDA5	IN/OUT	Video1 digital Y data input/output
AE15	YDA6	IN/OUT	Video1 digital Y data input/output
AD14	YDA7	IN/OUT	Video1 digital Y data input/output
AF15	$V_{DD}2$	-	V_{DD}3.3V
AE16	CDA0	IN/OUT	Video1 digital C data input/output
AD15	CDA1	IN/OUT	Video1 digital C data input/output
AF16	CDA2	IN/OUT	Video1 digital C data input/output
AC15	CDA3	IN/OUT	Video1 digital C data input/output
AE17	CDA4	IN/OUT	Video1 digital C data input/output
AD16	CDA5	IN/OUT	Video1 digital C data input/output
AF17	CDA6	IN/OUT	Video1 digital C data input/output
AC17	CDA7	IN/OUT	Video1 digital C data input/output
AE18	$V_{DD}2$	-	V_{DD}3.3V
AD17	HSYNCA	IN/OUT	Hsync1 input/output
AF18	VSYNCA	IN/OUT	Vsync1 input/output
AE19	PCLKA	IN/OUT	Pixel clock 1 input/output
AF19	DASEL	IN	Video1 digital data input/output select (L: output H: input)
AD18	YCDBO	OUT	Video2 digital YC data output
AE20	$V_{DD}2$	-	V_{DD}3.3V
AC19	YCDB1	OUT	Video2 digital YC data output
AF20	YCDB2	OUT	Video2 digital YC data output
AD19	YCDB3	OUT	Video2 digital YC data output
AE21	YCDB4	OUT	Video2 digital YC data output
AC20	YCDB5	OUT	Video2 digital YC data output
AF21	$V_{DD}2$	-	V_{DD}3.3V
AD20	YCDB6	OUT	Video2 digital YC data output
AE22	YCDB7	OUT	Video2 digital YC data output
AF22	HSYNCB	OUT	Hsync2 output
AD21	VSYNCB	OUT	Vsync2 output
AE23	PCLKB	OUT	Pixel clock 2 output
AC22	TEST0	IN	TEST pin(Normally L)
AF23	TEST1	IN	TEST pin(Normally L)
AD22	$PLL1AV_{DD}2$	-	PLL1 analog V_{DD}3.3V
AE24	$PLL1AV_{SS}$	-	PLL1 analog GND
AD23	$PLL1DV_{DD}$	-	PLL1 V_{DD}1.8V
AF24	$PLL1DV_{SS}$	-	PLL1 GND
AD26	TEST2	IN	TEST pin(Normally L)
AD25	TEST3	IN	TEST pin(Normally L)
AC25	TEST4	IN	TEST pin(Normally L)
AC24	TEST5	IN	TEST pin(Normally L)
AC26	TEST6	IN	TEST pin(Normally L)
AB25	SDADQ31	IN/OUT	SDRAM-A data bus
AB23	$V_{DD}2$	-	V_{DD}3.3V

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BALL	Pin Name	I/O	Functions
AB24	SDADQ30	IN/OUT	SDRAM-A data bus
AB26	SDADQ29	IN/OUT	SDRAM-A data bus
AA25	SDADQ28	IN/OUT	SDRAM-A data bus
Y23	SDADQ27	IN/OUT	SDRAM-A data bus
AA24	SDADQ26	IN/OUT	SDRAM-A data bus
AA26	SDADQ25	IN/OUT	SDRAM-A data bus
Y25	$V_{DD}2$	-	$V_{DD}3.3V$
Y26	SDADQ24	IN/OUT	SDRAM-A data bus
Y24	SDADQ23	IN/OUT	SDRAM-A data bus
W25	SDADQ22	IN/OUT	SDRAM-A data bus
V23	SDADQ21	IN/OUT	SDRAM-A data bus
W26	SDADQ20	IN/OUT	SDRAM-A data bus
W24	SDADQ19	IN/OUT	SDRAM-A data bus
V25	SDADQ18	IN/OUT	SDRAM-A data bus
V26	SDADQ17	IN/OUT	SDRAM-A data bus
U25	$V_{DD}2$	-	$V_{DD}3.3V$
V24	SDADQ16	IN/OUT	SDRAM-A data bus
U26	SDADQ15	IN/OUT	SDRAM-A data bus
U23	SDADQ14	IN/OUT	SDRAM-A data bus
T25	SDADQ13	IN/OUT	SDRAM-A data bus
U24	SDADQ12	IN/OUT	SDRAM-A data bus
T26	SDADQ11	IN/OUT	SDRAM-A data bus
R25	SDADQ10	IN/OUT	SDRAM-A data bus
R26	SDADQ9	IN/OUT	SDRAM-A data bus
T24	SDADQ8	IN/OUT	SDRAM-A data bus
P25	$V_{DD}2$	-	$V_{DD}3.3V$
R23	SDADQ7	IN/OUT	SDRAM-A data bus
P26	SDADQ6	IN/OUT	SDRAM-A data bus
R24	SDADQ5	IN/OUT	SDRAM-A data bus
N25	SDADQ4	IN/OUT	SDRAM-A data bus
N23	SDADQ3	IN/OUT	SDRAM-A data bus
N26	SDADQ2	IN/OUT	SDRAM-A data bus
P24	SDADQ1	IN/OUT	SDRAM-A data bus
M25	$V_{DD}2$	-	$V_{DD}3.3V$
N24	SDADQ0	IN/OUT	SDRAM-A data bus
M26	SDADQM3	OUT	SDRAM-A data mask
L25	SDADQM2	OUT	SDRAM-A data mask
M24	SDADQM1	OUT	SDRAM-A data mask
L26	SDADQM0	OUT	SDRAM-A data mask
M23	SDACLK	OUT	SDRAM-A clock
K25	SDACS	OUT	SDRAM-A CS
L24	SDARAS	OUT	SDRAM-A RAS
K26	$V_{DD}2$	-	$V_{DD}3.3V$
K23	SDACAS	OUT	SDRAM-A CAS
J25	SDAWE	OUT	SDRAM-A WE
K24	SDAAD0	OUT	SDRAM-A address bus
J26	SDAAD1	OUT	SDRAM-A address bus
H25	$V_{DD}2$	-	$V_{DD}3.3V$
H26	SDAAD2	OUT	SDRAM-A address bus
J24	SDAAD3	OUT	SDRAM-A address bus
G25	SDAAD4	OUT	SDRAM-A address bus
H23	SDAAD5	OUT	SDRAM-A address bus

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BALL	Pin Name	I/O	Functions
G26	SDAAD6	OUT	SDRAM-A address bus
H24	SDAAD7	OUT	SDRAM-A address bus
F25	SDAAD8	OUT	SDRAM-A address bus
G23	SDAAD9	OUT	SDRAM-A address bus
F26	SDAAD10	OUT	SDRAM-A address bus
G24	$V_{DD}2$	-	$V_{DD}3.3V$
E25	SDABA0	OUT	SDRAM-A bank address
E26	SDABA1	OUT	SDRAM-A bank address
F24	SDBDQ31	IN/OUT	SDRAM-B data bus
D25	SDBDQ30	IN/OUT	SDRAM-B data bus
E23	SDBDQ29	IN/OUT	SDRAM-B data bus
D26	SDBDQ28	IN/OUT	SDRAM-B data bus
E24	$V_{DD}2$	-	$V_{DD}3.3V$
C25	SDBDQ27	IN/OUT	SDRAM-B data bus
B24	SDBDQ26	IN/OUT	SDRAM-B data bus
A24	SDBDQ25	IN/OUT	SDRAM-B data bus
B23	SDBDQ24	IN/OUT	SDRAM-B data bus
C23	SDBDQ23	IN/OUT	SDRAM-B data bus
A23	SDBDQ22	IN/OUT	SDRAM-B data bus
B22	SDBDQ21	IN/OUT	SDRAM-B data bus
D22	SDBDQ20	IN/OUT	SDRAM-B data bus
C22	$V_{DD}2$	-	$V_{DD}3.3V$
A22	SDBDQ19	IN/OUT	SDRAM-B data bus
B21	SDBDQ18	IN/OUT	SDRAM-B data bus
D20	SDBDQ17	IN/OUT	SDRAM-B data bus
C21	SDBDQ16	IN/OUT	SDRAM-B data bus
A21	$V_{DD}2$	-	$V_{DD}3.3V$
B20	SDBDQ15	IN/OUT	SDRAM-B data bus
A20	SDBDQ14	IN/OUT	SDRAM-B data bus
C20	SDBDQ13	IN/OUT	SDRAM-B data bus
B19	SDBDQ12	IN/OUT	SDRAM-B data bus
D18	SDBDQ11	IN/OUT	SDRAM-B data bus
A19	SDBDQ10	IN/OUT	SDRAM-B data bus
C19	SDBDQ9	IN/OUT	SDRAM-B data bus
B18	SDBDQ8	IN/OUT	SDRAM-B data bus
A18	$V_{DD}2$	-	$V_{DD}3.3V$
B17	SDBDQ7	IN/OUT	SDRAM-B data bus
C18	SDBDQ6	IN/OUT	SDRAM-B data bus
A17	SDBDQ5	IN/OUT	SDRAM-B data bus
D17	SDBDQ4	IN/OUT	SDRAM-B data bus
B16	SDBDQ3	IN/OUT	SDRAM-B data bus
C17	SDBDQ2	IN/OUT	SDRAM-B data bus
A16	SDBDQ1	IN/OUT	SDRAM-B data bus
B15	SDBDQ0	IN/OUT	SDRAM-B data bus
A15	$V_{DD}2$	-	$V_{DD}3.3V$
C16	SDBDQM3	OUT	SDRAM-B data mask
B14	SDBDQM2	OUT	SDRAM-B data mask
D15	SDBDQM1	OUT	SDRAM-B data mask
A14	SDBDQM0	OUT	SDRAM-B data mask
C15	$V_{DD}2$	-	$V_{DD}3.3V$
B13	SDBCLK	OUT	SDRAM-B clock
D13	SDBCS	OUT	SDRAM-B CS

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BALL	Pin Name	I/O	Functions
A13	SDBRAS	OUT	SDRAM-B RAS
C14	SDBCAS	OUT	SDRAM-B CAS
B12	SDBWE	OUT	SDRAM-B WE
C13	SDBAD0	OUT	SDRAM-B address bus
A12	SDBAD1	OUT	SDRAM-B address bus
B11	SDBAD2	OUT	SDRAM-B address bus
C12	$V_{DD}2$	-	$V_{DD}3.3V$
A11	SDBAD3	OUT	SDRAM-B address bus
D12	SDBAD4	OUT	SDRAM-B address bus
B10	SDBAD5	OUT	SDRAM-B address bus
C11	SDBAD6	OUT	SDRAM-B address bus
A10	SDBAD7	OUT	SDRAM-B address bus
D10	SDBAD8	OUT	SDRAM-B address bus
B9	SDBAD9	OUT	SDRAM-B address bus
C10	SDBAD10	OUT	SDRAM-B address bus
A9	SDBBA0	OUT	SDRAM-B bank address
B8	$V_{DD}2$	-	$V_{DD}3.3V$
A8	SDBBA1	OUT	SDRAM-B bank address
C9	TS1IN0	IN	TS data input 1
B7	TS1IN1	IN	TS data input 1
D8	TS1IN2	IN	TS data input 1
A7	TS1IN3	IN	TS data input 1
C8	TS1IN4	IN	TS data input 1
B6	TS1IN5	IN	TS data input 1
D7	TS1IN6	IN	TS data input 1
A6	TS1IN7	IN	TS data input 1
C7	TS1CK	IN	TS clock input 1
B5	$V_{DD}2$	-	$V_{DD}3.3V$
A5	TS1SYNC	IN	TS Sync input 1
C6	TS1RDY	OUT	TS Ready output 1
B4	TS1VALID	IN	TS Valid input 1
D5	TS1ERR	IN	TS air flag input 1
A4	PLL3AVDD	-	PLL3 analog VDD1.8V
C5	PLL3AVSS	-	PLL3 analog GND
B3	PLL3DVDD	-	PLL3 VDD1.8V
C4	PLL3DVSS	-	PLL3 GND
F4	V_{DD}		$V_{DD}1.8V$
L4	V_{DD}		$V_{DD}1.8V$
T4	V_{DD}		$V_{DD}1.8V$
AA4	V_{DD}		$V_{DD}1.8V$
AC6	V_{DD}		$V_{DD}1.8V$
AC11	V_{DD}		$V_{DD}1.8V$
AC16	V_{DD}		$V_{DD}1.8V$
AC21	V_{DD}		$V_{DD}1.8V$
AA23	V_{DD}		$V_{DD}1.8V$
T23	V_{DD}		$V_{DD}1.8V$
L23	V_{DD}		$V_{DD}1.8V$
F23	V_{DD}		$V_{DD}1.8V$
D21	V_{DD}		$V_{DD}1.8V$
D16	V_{DD}		$V_{DD}1.8V$
D11	V_{DD}		$V_{DD}1.8V$
D6	V_{DD}		$V_{DD}1.8V$

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BALL	Pin name	I/O	Functions
A1	GND		GND
A2	GND		GND
B2	GND		GND
C3	GND		GND
D4	GND		GND
H4	GND		GND
N4	GND		GND
V4	GND		GND
AF1	GND		GND
AE1	GND		GND
AE2	GND		GND
AD3	GND		GND
AC4	GND		GND
AC8	GND		GND
AC13	GND		GND
AC18	GND		GND
AF26	GND		GND
AF25	GND		GND
AE25	GND		GND
AD24	GND		GND
AC23	GND		GND
W23	GND		GND
P23	GND		GND
J23	GND		GND
A26	GND		GND
B26	GND		GND
B25	GND		GND
C24	GND		GND
D23	GND		GND
D19	GND		GND
D14	GND		GND
D9	GND		GND