Ordering number : EN5159B

CMOS LSI

LC74772V

Camcorder On-Screen Display LSI

Overview

The LC74772V is a CMOS LSI that implements on-screen display for camcorders. It displays characters and patterns in a camcorder viewfinder under microprocessor control. The LC74772V displays a 12 × 18 dot font with 256 characters.

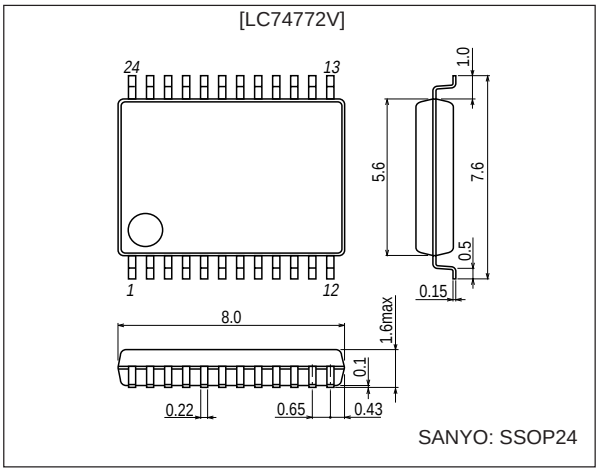
Features

- Screen format: 12 lines × 24 characters (up to 288 characters)
- Number of characters displayed: Up to 288 characters
- Character format: 12 (horizontal) × 18 (vertical) dots
- Number of characters in font: 256 characters
- Character sizes: Normal and double, specified in line units
- Display start position
  - — Horizontal: 64 positions
  - — Vertical: 64 positions
- Character reverse video function: Individual characters can be displayed in reverse video.
- Types of blinking: Two types with periods of 1.0 and 0.5 seconds, specifiable on a per character basis. (Blinking has a 60% display on duty.)
  (Four divisors: 1/25, 1/30, 1/50, 1/60)
- Outputs: R, G, B plus 2 output systems
  Or: 4 output systems (character data and blanking data: 4 outputs each)
- External control input: 8-bit serial data input format.

Package Dimensions

unit: mm

3175A-SSOP24



Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	V_{SS} – 0.3 to V_{SS} + 7.0	V
Input voltage	V_{IN}	All input pins	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}	CK_{OUT}, CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	300	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

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Allowable Operating Ranges at Ta = –30 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7	5.0	5.5	V
Input high-level voltage	V_{IH}	CTRL1, $TEST_{IN}$, $\overline{CS}$, SCLK, SIN, OUT_{MOD}, $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{RST}$	0.8 V_{DD}		V_{DD} + 0.3	V
Input low-level voltage	V_{IL}	CTRL1, $TEST_{IN}$, $\overline{CS}$, SCLK, SIN, OUT_{MOD}, $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{RST}$	V_{SS} – 0.3		0.2 V_{DD}	V
Oscillator frequency	F_{OSC}	OSC_{IN}, OSC_{OUT} (LC oscillator)	6	(8)	10	MHz

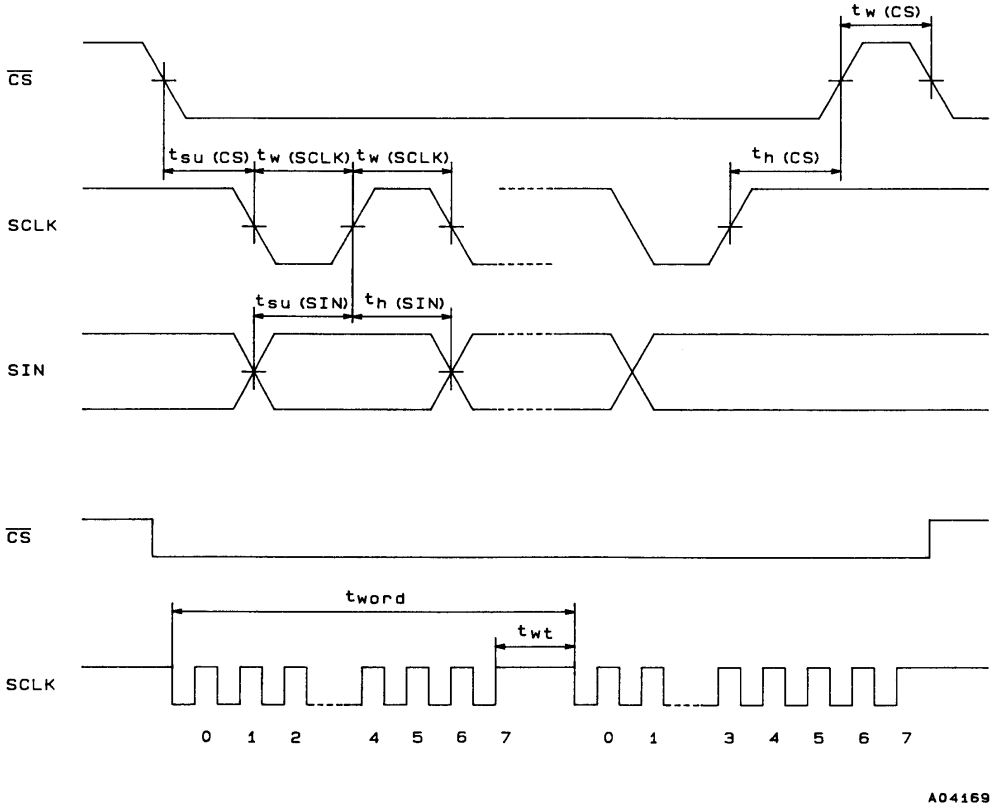
Electrical Characteristics at Ta = –30 to +70°C, unless otherwise specified V_{DD} = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output high-level voltage	V_{OH}	CK_{OUT}, CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK: V_{DD} = 5.5 to 4.5 V (V_{DD} = 4.4 to 2.7 V), I_{OH} = –1.0 mA (–0.5 mA)	0.9 V_{DD}			V
Output low-level voltage	V_{OL}	CK_{OUT}, CHA4, BLK4, CHA3, BLK3, B, G, R, BLANK: V_{DD} = 5.5 to 4.5 V (V_{DD} = 4.4 to 2.7 V), I_{OL} = 1.0 mA (0.5 mA)			0.1 V_{DD}	V
Input current	I_{IH}	CTRL1, $TEST_{IN}$, $\overline{CS}$, SCLK, SIN, OUT_{MOD}, $\overline{HSYNC}$, $\overline{VSYNC}$: V_{IN} = V_{DD}			1	µA
	I_{IL}	CTRL1, $TEST_{IN}$, $\overline{HSYNC}$, $\overline{VSYNC}$: V_{IN} = V_{SS}	–1			µA
Operating current drain	I_{DD}	V_{DD} pin; all outputs open, LC oscillator: 8 MHz			10	mA

Timing Characteristics at Ta = –30 to +70°C, V_{DD} = 5 ± 0.5 V

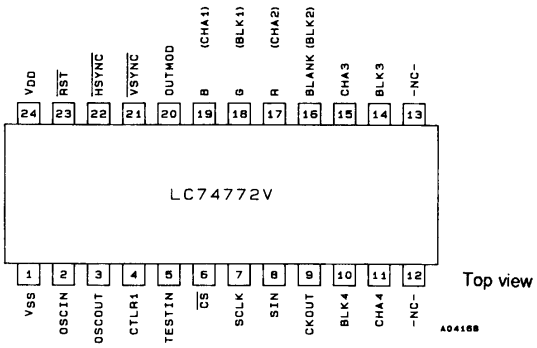
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_{W\ (SCLK)}$	SCLK	200			ns
	$t_{W\ (CS)}$	$\overline{CS}$ (the period that $\overline{CS}$ is high)	1			µs
Data setup time	$t_{SU\ (CS)}$	$\overline{CS}$	200			ns
	$t_{SU\ (SIN)}$	SIN	200			ns
Data hold time	$t_{h\ (CS)}$	$\overline{CS}$	2			µs
	$t_{h\ (SIN)}$	SIN	200			ns
One-word write time	t_{word}	The time to write 8 bits of data	4.2			µs
	t_{wt}	The RAM data write time	1			µs

Serial Data Input Timing



Pin Assignment

The signal names in parentheses indicate the output pin functions when 4-system output mode is used.

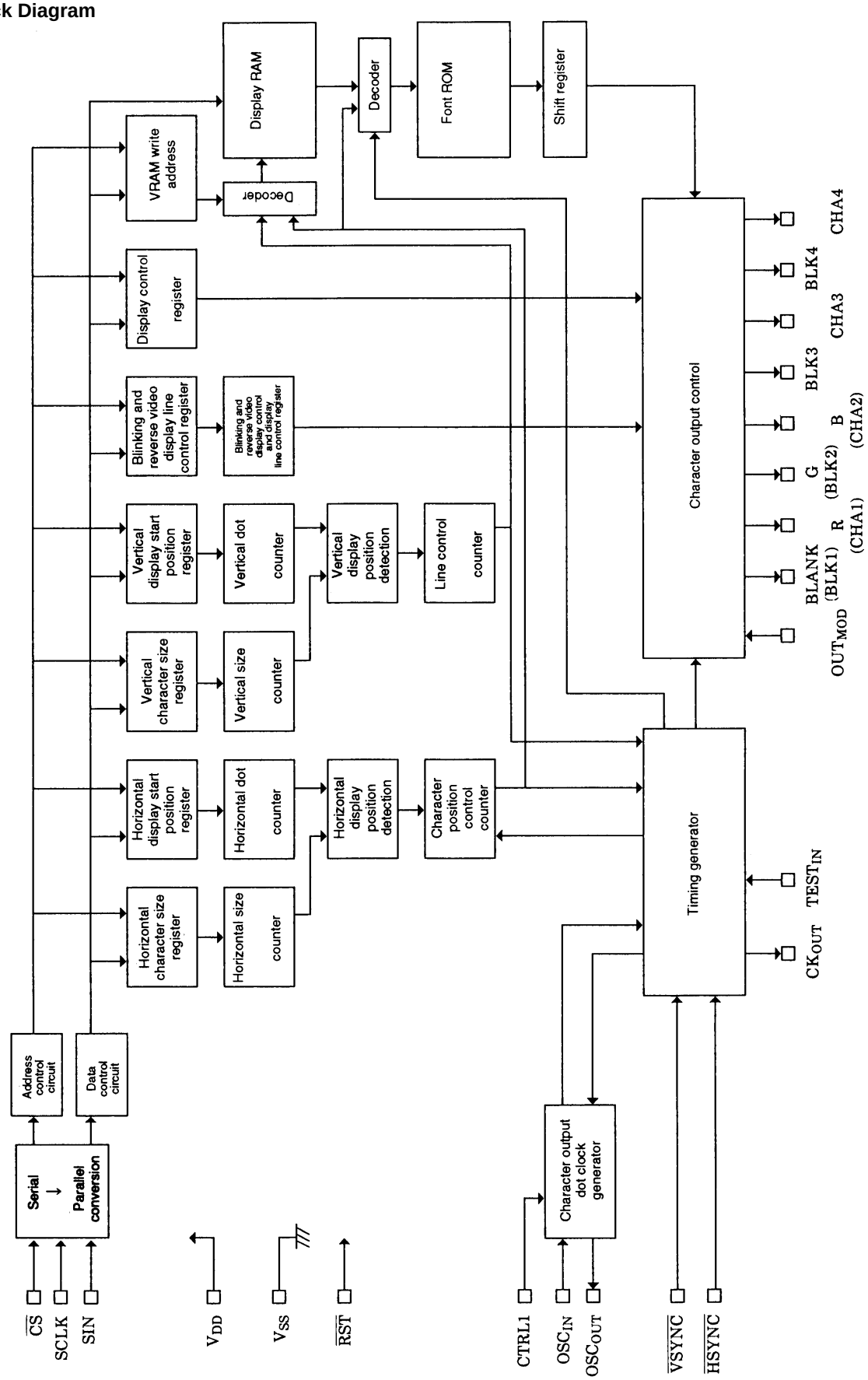


Pin Functions

PinNo.	Symbol	Function	Description
1	V_{SS}	Ground	Ground connection
2	OSC_{IN}	LC oscillator	Connections for the coil and capacitor that form the oscillator that generates the character output horizontal dot clock.
3	OSC_{OUT}		
4	CTRL1	Clock input control	Control input that switches between LC oscillator mode and clock input mode Low: LC oscillator mode, high: clock input mode
5	$TEST_{IN}$	Test control input	Test mode control input (The IC operates in test mode when this input is high.)
6	$\overline{CS}$	Enable input	Serial data input enable input Low: active (This input has hysteresis characteristics.)
7	SCLK	Clock input	Serial data input clock input (This input has hysteresis characteristics.)
8	SIN	Data input	Serial data input (This input has hysteresis characteristics.)
9	CK_{OUT}	Clock output	LC oscillator clock monitor output This signal is output when $\overline{RST}$ is low.
10	BLK4	Blanking signal output	Blanking signal output (system 2) Functions as the system 4 blanking data signal output in 4-system mode.
11	CHA4	Character data output	Character data signal output (system 2) Functions as the system 4 character data signal output in 4-system mode.
12	NC	Unused	Must be left open or tied to ground in normal operation.
13	NC	Unused	Must be left open or tied to ground in normal operation.
14	BLK3	Blanking signal output	Blanking signal output (system 1) Functions as the system 3 blanking data signal output in 4-system mode.
15	CHA3	Character data output	Character data signal output (system 1) Functions as the system 3 character data signal output in 4-system mode.
16	BLANK	Blanking signal output	Blanking signal output (blanking signal for RGB output) Functions as the system 2 blanking data signal output in 4-system mode.
17	R	Character data output	Character data (R) signal output Functions as the system 2 character data signal output in 4-system mode.
18	G	Character data output	Character data (G) signal output Functions as the system 1 blanking data signal output in 4-system mode.
19	B	Character data output	Character data (B) signal output Functions as the system 1 character data signal output in 4-system mode.
20	OUT_{MOD}	Output control input	Control input that switches between RGB output and 4-system output Low: RGB output, high 4-system output
21	$\overline{VSYNC}$	Vertical synchronizing signal input	Vertical synchronizing signal input (This input has hysteresis characteristics.)
22	$\overline{HSYNC}$	Horizontal synchronizing	Horizontal synchronizing signal input (This input has hysteresis characteristics.) signal input
23	$\overline{RST}$	Reset input	System reset signal input (This input has hysteresis characteristics.)
24	V_{DD}	Power supply	Power supply connection (+5 V)

Note: 1. Built-in pull-up resistors can be specified for inclusion in the $\overline{CS}$ (pin 6), SCLK (pin 7), SIN (pin 8), and $\overline{RST}$ (pin 23) pins as mask options.
2. In clock input mode (when CTRL1 is high), the function that holds the OSC_{IN} (pin 2) pin high during an oscillator reset is stopped.

Block Diagram



Display Control Commands

The display control commands have an 8-bit serial input format. Data is input LSB first.

Display Control Command Table

Command	First byte								Second byte							
	Command code				Data				Data							
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND 0 System setup 1	0	0	0	0	RST SYS	RAM CLR	OSC STP	TST MOD	—	—	—	—	—	—	—	—
COMMAND 1 System setup 2	0	0	0	1	CSYN MOD	CLK POLT	CLK MOD1	CLK MOD0	—	—	—	—	—	—	—	—
COMMAND 2 Input control setup	0	0	1	0	VSYN POLT	HSYN POLT	DATA FMT	ART FMT	—	—	—	—	—	—	—	—
COMMAND 3 General-purpose port control	0	0	1	1	PORT SET	OUT P11	OUT P10	OUT P9	—	—	—	—	—	—	—	—
COMMAND 4 Display operation control: reverse video and blinking	0	1	0	0	RVS ON	BLK ON	BLK 1	BLK 0	—	—	—	—	—	—	—	—
COMMAND 5 Display control: on/off settings for each output	0	1	0	1	DSP 4	DSP 3	DSP 2	DSP 1	—	—	—	—	—	—	—	—
COMMAND 6 Output control: systems 3 and 4	0	1	1	0	DSPF SL34	DSP RSG	DSP GSG	DSP BSG	—	—	—	—	—	—	—	—
COMMAND 8 Display control: border	1	0	0	0	0	BKC R	BKC G	BKC B	BKO4 F1	BKO4 F0	BKO3 F1	BKO3 F0	BKO2 F1	BKO2 F0	BKO1 F1	BKO1 F0
COMMAND 9 Display start position	1	0	0	1	VP5	VP4	VP3	VP2	VP1	VP0	HP5	HP4	HP3	HP2	HP1	HP0
COMMAND 10 Display line control	1	0	1	0	LNF SZ	LNF OT4	LNF OT3	LN SEL	0	0	LIN 126	LIN 115	LIN 104	LIN 93	LIN 82	LIN 71
COMMAND 11 RAM write address	1	0	1	1	VADR 3	VADR 2	VADR 1	VADR 0	0	0	0	HADR 4	HADR 3	HADR 2	HADR 1	HADR 0
COMMAND 14 Display RAM setup data	1	1	1	BLK	RV	R	G	B	C7	C6	C5	C4	C3	C2	C1	C0

① ②

① Command code: (These 4 bits in the first byte identify the command.)
Command 14 is recognized by the upper 3 bits.

② Command data: (These bits specify the data for each command.)
- For commands 0 through 7, 8 bits of data are read in.
- For commands 8 through 14, 16 bits of data are read in.
- If the command 2 data-1 bit (DATAFMT) was set to 1, after the first byte of a command 14 is read in, the system goes to continuous transfer mode for reading in a series of following bytes.

Note: 1. If the $\overline{CS}$ pin is set high, the command state is set to the command 0 (system control setup) state.
2. If a system reset is executed from the $\overline{RST}$ pin or by a command reset, the command register is set tot 0.

① COMMAND 0 (System control setup 1)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Command 0 identification code	
6	—	0		
5	—	0		
4	—	0		
3	RST SYS	0	Normal operation	If $\overline{CS}$ is low, the reset is executed, but if $\overline{CS}$ is high this command will be excluded.
		1	System reset	
2	RAM CLR	0	Normal operation	The VRAM clear operation is not executed when the oscillator is stopped.
		1	Normal operation VRAM clear (All data is set to FE (hexadecimal))	
1	OSC STP	0	The LC oscillator operating state is maintained.	Valid when the display is off. VRAM write is not possible when the oscillator is stopped.
		1	The LC oscillator is stopped.	
0	TST MOD	0	Normal operation	Illegal setting. This bit must always be set to 0.
		1	Test mode	

Note: This register is set to 0 on a reset (either by the $\overline{RST}$ pin or by a command reset).

Notes on command settings

1. RSTSYS: A command reset is executed immediately after the data is read.
   The reset is cleared by returning the $\overline{CS}$ pin to high to reset this register. The reset is also cleared if this command is executed consecutively or if this register is set to 0.
2. RAMCLR: The RAM can only be erased when display is off. This operation is not executed during display. This operation cannot be executed if the LC oscillator is stopped. Only use this command when the LC oscillator is operating.
   - This command bit is automatically cleared when the RAM erase operation completes.
   - Once the RAM erase command has been read in, the following time is required to complete the operation.
     — Tclear = 5 [μs] + $4/f_{OSC}$ (LC-oscillator) × 288
3. OSCSTP: The LC oscillator stop command stops the LC oscillator connected to pins 2 and 3 (OSC_{IN} and OSC_{OUT}).
   The oscillator stop command is only executed when display is off. It is not executed if display is in progress.
   - In external clock input mode, this command stops the acquisition of that clock signal.
4. TSTMOD: The test mode command is executed if the $TEST_{IN}$ pin (pin 5) is high. This command should not be used by applications in normal operation.

② COMMAND 1 (System control setup 2)

First byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>0</td><td rowspan="4">Command 1 identification code</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>0</td></tr>
<tr><td>5</td><td>—</td><td>0</td></tr>
<tr><td>4</td><td>—</td><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">CSYN
MOD</td><td>0</td><td>HSYNC (pin 22) functions as the horizontal synchronizing signal input</td><td rowspan="2">The VSYNC pin (pin 21) must be tied to ground or V_{DD} in composite synchronizing signal input mode.</td></tr>
<tr><td>1</td><td>HSYNC (pin 22) functions as the composite synchronizing signal input</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">CLK
POLT</td><td>0</td><td>The system clock has a positive polarity.</td><td rowspan="2">This sets the clock polarity for system operation when pin 2 is used as a clock input.</td></tr>
<tr><td>1</td><td>The system clock has a negative polarity.</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">CLK
MOD1</td><td>0</td><td rowspan="4"><table><tr><th>MOD1</th><th>MOD0</th><th>Operation</th></tr><tr><td>0</td><td>0</td><td>LC oscillator mode</td></tr><tr><td>0</td><td>1</td><td>Clock input (1 dot)</td></tr><tr><td>1</td><td>0</td><td>Clock input (NTSC)</td></tr><tr><td>1</td><td>1</td><td>Clock input (PAL)</td></tr></table></td><td rowspan="4">Valid when the CTRL1 pin (pin 4) is high.
The input clock frequency in clock input mode is either 4fsc or the dot clock frequency.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">CLK
MOD0</td><td>0</td></tr>
<tr><td>1</td></tr>
</table>

③ COMMAND 2 (Input control)

First byte

<table>
<tr><th rowspan="2">DA0 to DA7</th><th rowspan="2">Register name</th><th colspan="2">Register content</th><th rowspan="2">Note</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>0</td><td rowspan="4">Command 2 identification code</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>0</td></tr>
<tr><td>5</td><td>—</td><td>1</td></tr>
<tr><td>4</td><td>—</td><td>0</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">VSYN
POLT</td><td>0</td><td>The vertical synchronizing signal input polarity is low active.</td><td rowspan="2">Sets the pin 21 (VSYNC) signal input polarity.</td></tr>
<tr><td>1</td><td>The vertical synchronizing signal input polarity is high active.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">HSYN
POLT</td><td>0</td><td>The horizontal synchronizing signal input polarity is low active.</td><td rowspan="2">Sets the pin 22 (HSYNC) signal input polarity.</td></tr>
<tr><td>1</td><td>The horizontal synchronizing signal input polarity is high active.</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">DATA
FMT</td><td>0</td><td>Data is transferred in 16-bit units.</td><td rowspan="2">Sets the COMMAND 14 data transfer format.</td></tr>
<tr><td>1</td><td>Continuous transfers with the upper 8 bits input first and then the lower 8 bits</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">ATR
FMT</td><td>0</td><td>RV specifies the reverse video display function.</td><td rowspan="2">COMMAND-14 Data 11: Valid in RV RGB output mode.</td></tr>
<tr><td>1</td><td>RV specifies system 3 output control.</td></tr>
</table>

Note: This register is set to 0 on a reset (either by the $\overline{RST}$ pin or by a command reset).

④ COMMAND 3 (General-purpose port control)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Command 3 identification code	
6	—	0		
5	—	1		
4	—	1		
3	PORT SET	0	System 4 functions as a normal character and border outputs.	Controls the pin 10 (BLK4) and pin 11 (CHA4) outputs.
		1	System 4 functions as general-purpose ports.	
2	OUT P11	0	The pin 11 output is set to low.	Sets the output when PORTSET is set to 1.
		1	The pin 11 output is set to high.	
1	OUT P10	0	The pin 10 output is set to low.	Sets the output when PORTSET is set to 1.
		1	The pin 10 output is set to high.	
0	OUT P9	0	The pin 9 output is set to low.	Sets the output for pin 9 during normal operation (other than during a reset).
		1	The pin 9 output is set to high.	

⑤ COMMAND 4 (Display control: reverse video and blinking)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Command 4 identification code	
6	—	1		
5	—	0		
4	—	0		
3	RVS ON	0	—	
		1	Characters for which the attribute is specified are displayed in reverse video.	
2	BLK ON	0	—	
		1	Characters for which the attribute is specified are displayed blinking.	
1	BLK1	0		The blinking period setting The duty is 60% for all types. Character display on: 60% Character display off: 40% V: Vertical period
		1		
0	BLK0	0		
		1		

BLK1	BLK0	Operation
0	0	V × 25 (PAL: 0.5 s)
0	1	V × 30 (NTSC: 0.5 s)
1	0	V × 50 (PAL: 1.0 s)
1	1	V × 60 (NTSC: 1.0 s)

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

⑥ COMMAND 5 (Display control: on/off settings for each output system)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Command 5 identification code	
6	—	1		
5	—	0		
4	—	1		
3	DSP4	0	System 4 output off	Pin 10 (BLK4) and pin 11 (CHA4) output control
		1	System 4 output on	
2	DSP3	0	System 3 output off	Pin 14 (BLK3) and pin 15 (CHA3) output control
		1	System 3 output on	
1	DSP2	0	System 2 output off	Pin 16 (BLK2) and pin 17 (CHA2) output control
		1	System 2 output on	Invalid in RGB output mode.
0	DSP1	0	System 1 (RGB) output off	Pin 18 (BLK1) and pin 19 (CHA1) output control
		1	System 1 (RGB) output on	Functions as the RGB output control in RGB output mode.

⑦ COMMAND 6 (Output control: systems 3 and 4 output control settings)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	Command 6 identification code	
6	—	1		
5	—	1		
4	—	0		
3	DSPF SL34	0	Sets the system 3 output conditions according to the command described below.	Only system 4 is valid in 4-system output mode. System 4 cannot be set when the general-purpose output port usage is specified.
		1	Sets the system 4 output conditions according to the command described below.	
2	DSP RSG	0	See table below	Note: The following registers are set to 1 during a reset. DSPRSG DSPGSG DSPBSG As a result, the “All of R, G, B are output” state is selected during a reset.
		1		
1	DSP GSG	0		
		1		
0	DSP BSG	0		
		1		

DSPRSG	DSPGSG	DSPBSG	Output selection
0	0	0	Signals other than R, G, B are output.
0	0	1	B is output.
0	1	0	G is output.
0	1	1	G and B are output.
1	0	0	R is output.
1	0	1	R and B are output.
1	1	0	R and G are output.
1	1	1	All of R, G, B are output.

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

⑧ COMMAND 8 (Output control: background color setting: RGB output mode)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 8 identification code	
6	—	0		
5	—	0		
4	—	0		
3		0	—	
2	BKCR	0	See table below	Background color setting in RGB output mode This command is invalid in 4-system output mode. • Invalid when pin 20 (OUT_{MOD}) is high. • Valid when pin 20 (OUT_{MOD}) is low.
		1		
1	BKCG	0		
		1		
0	BKCB	0		
		1		

BKCR	BKCG	BKCB	Background color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	BKO4 F1	0	See table below	The system 4 output border setting
		1		
6	BKO4 F0	0		
		1		
5	BKO3 F1	0	See table below	The system 3 output border setting
		1		
4	BKO3 F0	0		
		1		
3	BKO2 F1	0	See table below	The system 2 output border setting This command is invalid in RGB output mode. • Invalid when pin 20 (OUT_{MOD}) is low. • Valid when pin 20 (OUT_{MOD}) is high.
		1		
2	BKO2 F0	0		
		1		
1	BKO1 F1	0	See table below	The system 1 or RGB output border setting
		1		
0	BKO1 F0	0		
		1		

BKO4F1	BKO4F0	Operation function
0	0	No background or border
0	1	Font size (black characters)
1	0	Border
1	1	Areas other than the font (all filled)

BKO3F1	BKO3F0	Operation function
0	0	No background or border
0	1	Font size (black characters)
1	0	Border
1	1	Areas other than the font (all filled)

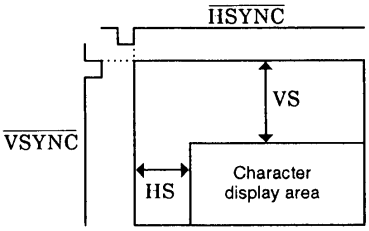
BKO2F1	BKO2F0	Operation function
0	0	No background or border
0	1	Font size (black characters)
1	0	Border
1	1	Areas other than the font (all filled)

BKO1F1	BKO1F0	Operation function
0	0	No background or border
0	1	Font size
1	0	Border
1	1	Areas other than the font (all filled)

Note: This register is set to 0 on a reset (either by the $\overline{RST}$ pin or by a command reset).

⑨ COMMAND 9 (Display start position setting)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 9 identification code	
6	—	0		
5	—	0		
4	—	1		
3	VP5	0	If VS is the vertical display start position then: $VS = H \times (\sum_{n=0}^{5} 2^n VP_n) + 16H$ Where H is horizontal period pulse period.  	
		1		
2	VP4	0		
		1		
1	VP3	0		
		1		
0	VP2	0		
		1		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	VP1	0		
		1		
6	VP0	0		
		1		
5	HP5	0	If VS is the horizontal display start position then: $HS = Tc \times (\sum_{n=0}^{5} 2^n HP_n) + 12Tc$ Where Tc is a single period of the LC oscillator connected to pins 2 and 3 (OSC_{IN} and OSC_{OUT}), or: Tc is the period of the input clock (4fsc input) if CTRL1 (pin 4) is high. NTSC mode: 7.159 MHz = 4fsc × 1/2 PAL mode: 7.094 MHz = 4fsc × 2/5	
		1		
4	HP4	0		
		1		
3	HP3	0		
		1		
2	HP2	0		
		1		
1	HP1	0		
		1		
0	HP0	0		
		1		

Note: This register is set to 0 on a reset (either by the $\overline{RST}$ pin or by a command reset).

⑩ COMMAND 10 (Display line control)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 10 identification code	
6	—	0		
5	—	1		
4	—	0		
3	LNF SZ	0	—	
		1	Sets the character size.	
2	LNF OT4	0	—	Invalid in general-purpose port mode.
		1	Sets the system 4 display line.	
1	LNF OT3	0	—	Invalid in system 4 output setup mode.
		1	Sets the system 3 display line.	
0	LNF SEL	0	The line specified by the next 6 bits is one of lines 1 to 6.	Controls the line switching specified by the six bits in the second byte.
		1	The line specified by the next 6 bits is one of lines 7 to 12.	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	—	
6	—	0	—	
5	LIN 126	0	Clears the line 6 (12) setting.	The character size or display line setting 0: Character size specification = normal Display line specification = off 1: Character size specification = double size Display line specification = on
		1	Sets line 6 (12).	
4	LIN 115	0	Clears the line 5 (11) setting.	
		1	Sets line 5 (11).	
3	LIN 104	0	Clears the line 4 (10) setting.	
		1	Sets line 4 (10).	
2	LIN 93	0	Clears the line 3 (9) setting.	
		1	Sets line 3 (9).	
1	LIN 82	0	Clears the line 2 (8) setting.	
		1	Sets line 2 (8).	
0	LIN 71	0	Clears the line 1 (7) setting.	
		1	Sets line 1 (7).	

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

⑪ COMMAND 11 (Display RAM write address setting)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 11 identification code	
6	—	0		
5	—	1		
4	—	1		
3	VADR 3	0	The range of the display RAM vertical address (line address) setting is from 0 to B (hexadecimal) (12 lines). Values of C (hexadecimal) or larger are not allowed.	
		1		
2	VADR 2	0		
		1		
1	VADR 1	0		
		1		
0	VADR 0	0		
		1		

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	0	—	
6	—	0	—	
5	—	0	—	
4	HADR 4	0	The range of the display RAM horizontal address (character address) setting is from 00 to 17 (hexadecimal) (24 characters). Values of 18 (hexadecimal) or larger are not allowed.	
		1		
3	HADR 3	0		
		1		
2	HADR 2	0		
		1		
1	HADR 1	0		
		1		
0	HADR 0	0		
		1		

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

⑫ COMMAND 14 (Display RAM setup data)

First byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	—	1	Command 14 identification code	
6	—	1		
5	—	1		
4	BLK	0	—	
		1	Blinking character specification	
3	RV	0	—	
		1	Reverse video character specification	
2	R	0	—	
		1	R output specification (system 3 output in 4-system output mode)	
1	G	0	—	
		1	G output specification (system 2 output in 4-system output mode)	
0	B	0	—	
		1	B output specification (system 1 output in 4-system output mode)	

Second byte

DA0 to DA7	Register name	Register content		Note
		State	Function	
7	C7	0	Character code setting There are 256 characters (00 to FF hexadecimal). FE hexadecimal is handled as blank data. Nothing is displayed, whatever the other conditions are set to. FF hexadecimal functions as the transfer termination code for character-code-only continuous transfers. Continuous transfer mode is set up by setting the data 0 bit (DATAFMT) in COMMAND 2 to 1.	
		1		
6	C6	0		
		1		
5	C5	0		
		1		
4	C4	0		
		1		
3	C3	0		
		1		
2	C2	0		
		1		
1	C1	0		
		1		
0	C0	0		
		1		

Note: This register is set to 0 on a reset (either by the $\overline{\text{RST}}$ pin or by a command reset).

Display Screen Organization

The display screen consists of 12 lines of 24 characters each.
Thus the maximum number of characters that can be displayed is 288 characters.
The display memory address consists of a line address (VADR0, VADR1, VADR2, and VADR3 representing values from 0 to B (hexadecimal)), and a column (character position) address (HADR0, HADR1, HADR2, HADR3, and HADR4 representing values from 0 to 17 (hexadecimal)).

Display Screen Organization (Display memory address)

	24 characters																							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	00h 00h	01h 00h	02h 00h	03h 00h	04h 00h	05h 00h	06h 00h	07h 00h	08h 00h	09h 00h	0Ah 00h	0Bh 00h	0Ch 00h	0Dh 00h	0Eh 00h	0Fh 00h	10h 00h	11h 00h	12h 00h	13h 00h	14h 00h	15h 00h	16h 00h	17h 00h
2	00h 01h	01h 01h	02h 01h	03h 01h	04h 01h	05h 01h	06h 01h	07h 01h	08h 01h	09h 01h	0Ah 01h	0Bh 01h	0Ch 01h	0Dh 01h	0Eh 01h	0Fh 01h	10h 01h	11h 01h	12h 01h	13h 01h	14h 01h	15h 01h	16h 01h	17h 01h
3	00h 02h	01h 02h	02h 02h	03h 02h	04h 02h	05h 02h	06h 02h	07h 02h	08h 02h	09h 02h	0Ah 02h	0Bh 02h	0Ch 02h	0Dh 02h	0Eh 02h	0Fh 02h	10h 02h	11h 02h	12h 02h	13h 02h	14h 02h	15h 02h	16h 02h	17h 02h
4	00h 03h	01h 03h	02h 03h	03h 03h	04h 03h	05h 03h	06h 03h	07h 03h	08h 03h	09h 03h	0Ah 03h	0Bh 03h	0Ch 03h	0Dh 03h	0Eh 03h	0Fh 03h	10h 03h	11h 03h	12h 03h	13h 03h	14h 03h	15h 03h	16h 03h	17h 03h
5	00h 04h	01h 04h	02h 04h	03h 04h	04h 04h	05h 04h	06h 04h	07h 04h	08h 04h	09h 04h	0Ah 04h	0Bh 04h	0Ch 04h	0Dh 04h	0Eh 04h	0Fh 04h	10h 04h	11h 04h	12h 04h	13h 04h	14h 04h	15h 04h	16h 04h	17h 04h
6	00h 05h	01h 05h	02h 05h	03h 05h	04h 05h	05h 05h	06h 05h	07h 05h	08h 05h	09h 05h	0Ah 05h	0Bh 05h	0Ch 05h	0Dh 05h	0Eh 05h	0Fh 05h	10h 05h	11h 05h	12h 05h	13h 05h	14h 05h	15h 05h	16h 05h	17h 05h
7	00h 06h	01h 06h	02h 06h	03h 06h	04h 06h	05h 06h	06h 06h	07h 06h	08h 06h	09h 06h	0Ah 06h	0Bh 06h	0Ch 06h	0Dh 06h	0Eh 06h	0Fh 06h	10h 06h	11h 06h	12h 06h	13h 06h	14h 06h	15h 06h	16h 06h	17h 06h
8	00h 07h	01h 07h	02h 07h	03h 07h	04h 07h	05h 07h	06h 07h	07h 07h	08h 07h	09h 07h	0Ah 07h	0Bh 07h	0Ch 07h	0Dh 07h	0Eh 07h	0Fh 07h	10h 07h	11h 07h	12h 07h	13h 07h	14h 07h	15h 07h	16h 07h	17h 07h
9	00h 08h	01h 08h	02h 08h	03h 08h	04h 08h	05h 08h	06h 08h	07h 08h	08h 08h	09h 08h	0Ah 08h	0Bh 08h	0Ch 08h	0Dh 08h	0Eh 08h	0Fh 08h	10h 08h	11h 08h	12h 08h	13h 08h	14h 08h	15h 08h	16h 08h	17h 08h
10	00h 09h	01h 09h	02h 09h	03h 09h	04h 09h	05h 09h	06h 09h	07h 09h	08h 09h	09h 09h	0Ah 09h	0Bh 09h	0Ch 09h	0Dh 09h	0Eh 09h	0Fh 09h	10h 09h	11h 09h	12h 09h	13h 09h	14h 09h	15h 09h	16h 09h	17h 09h
11	00h 0Ah	01h 0Ah	02h 0Ah	03h 0Ah	04h 0Ah	05h 0Ah	06h 0Ah	07h 0Ah	08h 0Ah	09h 0Ah	0Ah 0Ah	0Bh 0Ah	0Ch 0Ah	0Dh 0Ah	0Eh 0Ah	0Fh 0Ah	10h 0Ah	11h 0Ah	12h 0Ah	13h 0Ah	14h 0Ah	15h 0Ah	16h 0Ah	17h 0Ah
12	00h 0Bh	01h 0Bh	02h 0Bh	03h 0Bh	04h 0Bh	05h 0Bh	06h 0Bh	07h 0Bh	08h 0Bh	09h 0Bh	0Ah 0Bh	0Bh 0Bh	0Ch 0Bh	0Dh 0Bh	0Eh 0Bh	0Fh 0Bh	10h 0Bh	11h 0Bh	12h 0Bh	13h 0Bh	14h 0Bh	15h 0Bh	16h 0Bh	17h 0Bh

12 rows

H-address (horizontal address: in hexadecimal)
V-address (vertical address: in hexadecimal)