



# LC74793, 74793JM

## VPS / PDC Slicer IC

### Preliminary

### Overview

The LC74793/JM is a CMOS IC that provides PDS, VPS, and UDT data acquisition functions. The LC74793/JM supports microprocessor control of its operating modes and microprocessor read out of data acquired in any of its operating modes.

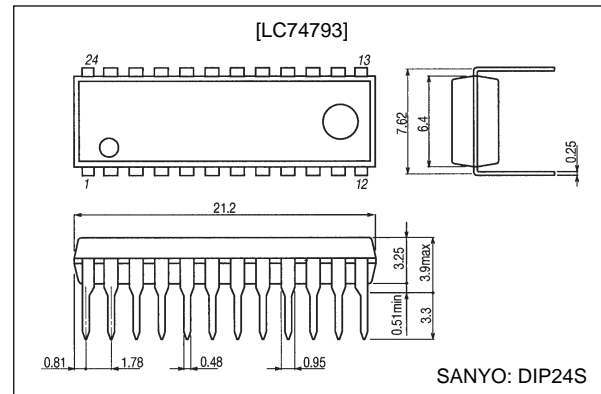
### Features

- VPS data acquisition (5 or 11 to 15 bytes)  
VPS: Video Program System
- PDC (8/30/2) data acquisition (13 to 25 bytes)  
PDC: Program Delivery Control
- UDT (8/30/1) data acquisition (13 to 25 bytes)  
UDT: Unified Date and Time
- Header (X/00) data acquisition (14 to 45 bytes)
- Status display (8/30/1, 8/30/2) data acquisition (26 to 45 bytes)
- Automatic VPS/PDC discrimination mode
- Built-in AFC and sync separator circuits
- Synchronization discrimination circuit
- I<sup>2</sup>C bus support

### Package Dimensions

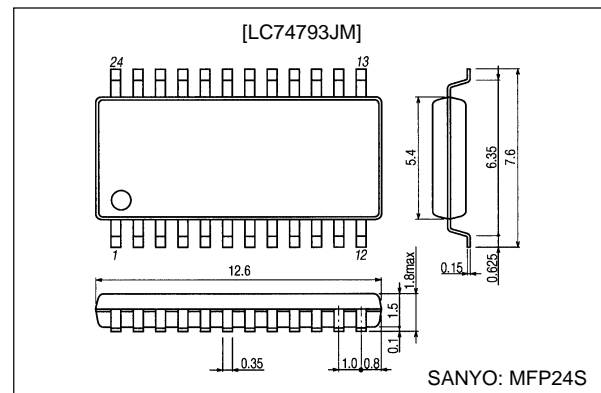
unit: mm

#### 3067-DIP24S



unit: mm

#### 3112-MFP24S



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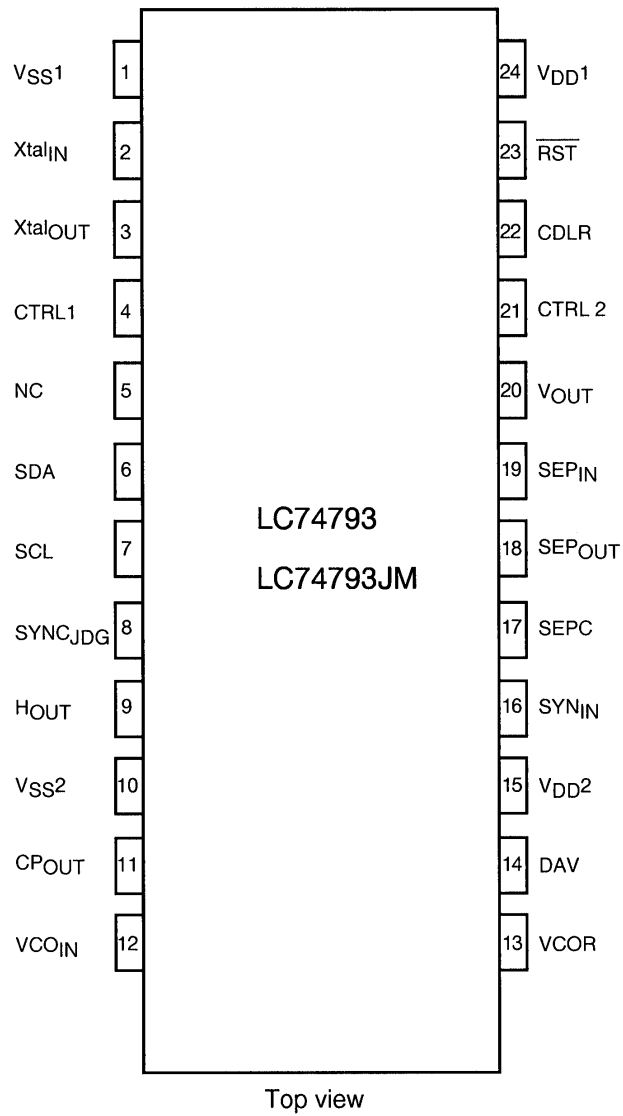
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D1898RM (OT) No. 5966-1/24

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## Pin Assignment



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Pin Functions

Pin No.	Pin	Function	Description
1	V <sub>SS1</sub>	Ground	Digital system ground
2	Xtal <sub>in</sub>	Crystal oscillator connections	Connections for the crystal element and capacitors that form the crystal oscillator. Also used for external clock input (fsc, 2fsc, or 4fsc).
3	Xtal <sub>out</sub>		
4	CTRL1	Crystal element switching	Switches between external clock input mode and crystal oscillator mode. Set this pin low for crystal oscillator, and high for external clock input.
5	NC		
6	SDA	Data I/O I <sup>2</sup> C bus	PDC/VPS data I/O. I <sup>2</sup> C bus write address: 01111100 I <sup>2</sup> C bus read address: 01111101
7	SCL	Clock input I <sup>2</sup> C bus	PDC/VPS data clock input. I <sup>2</sup> C bus
8	SYNC <sub>JDG</sub>	External synchronizing signal discrimination output	External synchronizing signal presence/absence discrimination status output. A high level is output when synchronizing signals are present. This pin outputs the crystal oscillator clock when the RST pin is low. (This reset state output can be disabled with command input.)
9	Hout	Horizontal synchronizing signal output	Horizontal synchronizing signal output
10	VSS2	Ground	Ground. (VCO circuit ground)
11	CP <sub>OUT</sub>	Charge pump output	Charge pump output. Connect a low-pass filter to this pin.
12	VCO <sub>IN</sub>	Oscillator control voltage input	VCO oscillation control voltage input
13	VCOR	Oscillator range adjustment	VCO oscillation range adjustment resistor connection
14	DAV	Data acquisition output	Outputs a low level when PDC/VPS data has been discriminated
15	V <sub>DD2</sub>	Power supply (+5 V)	Power supply (+5 V) (VCO system power supply)
16	SYN <sub>in</sub>	Sync separator circuit input	Internal sync separator circuit video signal input
17	SEPC	Slice level output	Slice level verification
18	SEP <sub>OUT</sub>	Composite synchronizing signal output	Internal sync separator circuit composite synchronizing signal output
19	SEP <sub>IN</sub>	Vertical synchronizing signal input	Inputs the vertical synchronizing signal by integrating the SEP out pin output signal. Applications must connect the SEP out pin to this pin through an integration circuit. If unused, connect this pin to VDD1. (This pin is enabled when CTRL2 is high.)
20	Vout	Vertical synchronizing signal output	Vertical synchronizing signal output This pin outputs the VCO clock when the RST pin is low. (This reset state output can be disabled with command input.)
21	CTRL2	SEPin input control	Controls whether or not the VSYNC vertical synchronizing signal is input to the SEPin input. When low: The VSYNC signal is not input. (The internal vertical separation circuit is used.) When high: The VSYNC signal is input.
22	CDLR	Clock phase adjustment	Connection for the clock phase adjustment resistor.
23	RST	Reset input	System reset input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
24	V <sub>DD1</sub>	Power supply (+5 V)	Power supply. (+5 V: digital system power supply)

## Specifications

### Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$	$V_{DD1}$ and $V_{DD2}$	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Input voltage	$V_{IN}$	All input pins	$V_{SS} - 0.3$ to $V_{DD1} + 0.3$	V
Output voltage	$V_{OUT}$	SDA, SYNCJDG, SEPOUT, DAV, HOUT, and VOUT	$V_{SS} - 0.3$ to $V_{DD1} + 0.3$	V
Allowable power dissipation	Pd max	$T_a = 25^{\circ}\text{C}$	350	mW
Operating temperature	Topr		-30 to +70	$^{\circ}\text{C}$
Storage temperature	Tstg		-40 to +125	$^{\circ}\text{C}$

### Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ	max		
Supply voltage	$V_{DD1}$	$V_{DD1}$ and $V_{DD2}$	4.5	5.0	5.5	V	
High-level input voltage	$V_{IH1}$	SDA and SCL	$0.8 V_{DD1}$		5.5	V	
	$V_{IH2}$	$\overline{\text{RST}}$	$0.8 V_{DD1}$		$V_{DD1} + 0.3$	V	
	$V_{IH3}$	CTRL1 and CTRL2	$0.7 V_{DD1}$		$V_{DD1} + 0.3$	V	
Low-level input voltage	$V_{IL1}$	$\overline{\text{RST}}$ , SDA, and SCL	$V_{SS} - 0.3$		$0.2 V_{DD1}$	V	
	$V_{IL2}$	CTRL1 and CTRL2	$V_{SS} - 0.3$		$0.3 V_{DD1}$	V	
Pull-up resistance	RPU	$\overline{\text{RST}}$	25	50	90	$\text{k}\Omega$	
Composite video signal input voltage	$V_{IN1}$	SYNIN	$V_{DD1} = 5\text{ V}$	1.5	2.0	2.25	Vp-p
Input voltage	$V_{IN2}$	XtalIN (in external clock input mode) $f_{in} = \text{fsc}, 2\text{fsc}, \text{ or } 4\text{fsc}$	$V_{DD1} = 5\text{ V}$	0.10		5.0	Vp-p
Oscillator frequency	FOSC1	The XtalIN and XtalOUT oscillator pins (4fsc: PAL)		17.734		MHz	
	FOSC2	The XtalIN and XtalOUT oscillator pins (2fsc: PAL)		8.867		MHz	
	FOSC3	The XtalIN and XtalOUT oscillator pins (fsc: PAL)		4.433		MHz	

Note: Note that adequate measure must be taken to prevent noise from entering the XtalIN pin when it is used in clock input mode.

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**Electrical Characteristics at Ta = -30 to +70°C, V<sub>DD1</sub> = 5 V unless otherwise specified.**

Parameter	Symbol	Applicable pins	Conditions	Ratings			Unit
				min	typ	max	
Output off leakage current	I <sub>leak2</sub>	SDA and DAV				1	μA
High-level output voltage	V <sub>OH1</sub>	SEPOUT, CPOUT, SYNCJDG, HOUT, and VOUT	V <sub>DD1</sub> = 4.5 V, I <sub>OH</sub> = -1.0 mA	3.5			V
Low-level output voltage	V <sub>OL1</sub>	SEPOUT, CPOUT, SYNCJDG, DAV, HOUT, and VOUT	V <sub>DD1</sub> = 4.5 V I <sub>OL</sub> = 1.0 mA			1.0	V
	V <sub>OL2</sub>	SDA	V <sub>DD1</sub> = 5.0 V I <sub>OL</sub> = 3.0 mA			0.4	V
Input current	I <sub>IH</sub>	RST, SDA, SCL, CTRL1, CTRL2, VCOIN	V <sub>IN</sub> = V <sub>DD1</sub>			1	μA
	I <sub>IL</sub>	SDA, SCL, CTRL1, CTRL2, VCOIN	V <sub>IN</sub> = V <sub>SS1</sub>	-1			μA
Operating current drain	I <sub>DD1</sub>	V <sub>DD1</sub> and V <sub>DD2</sub>	With all outputs open and a 17.734 MHz crystal			40	mA

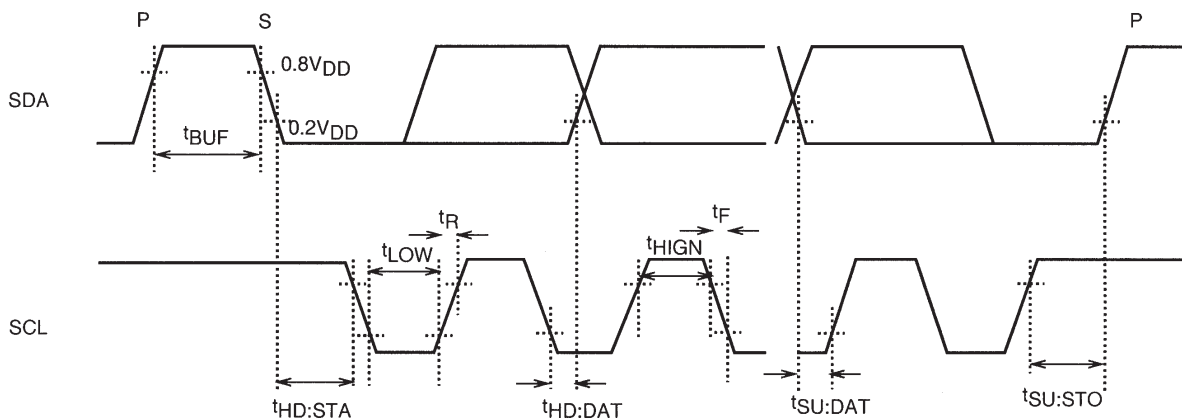
### Timing Characteristics

**PDC and VPS Read and Write (I<sup>2</sup>C bus timing) at Ta = -30 to +70°C, V<sub>DD1</sub> = 5±0.5 V**

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SCL frequency	f <sub>SCL</sub>				100	kHz
Bus release time	t <sub>BUF</sub>		4.7			μs
Start hold time	t <sub>HD</sub> ; STA		4.0			μs
SCL low-level period	t <sub>LOW</sub>		4.7			μs
SCL high-level period	t <sub>HIGN</sub>		4.0			μs
Data hold time	t <sub>HD</sub> ; DAT		0			μs
Data setup time	t <sub>SU</sub> ; DAT		250			ns
Rise time	t <sub>R</sub>				1000	ns
Fall time	t <sub>F</sub>				300	ns
Stop setup time	t <sub>SU</sub> ; STO		4.0			μs

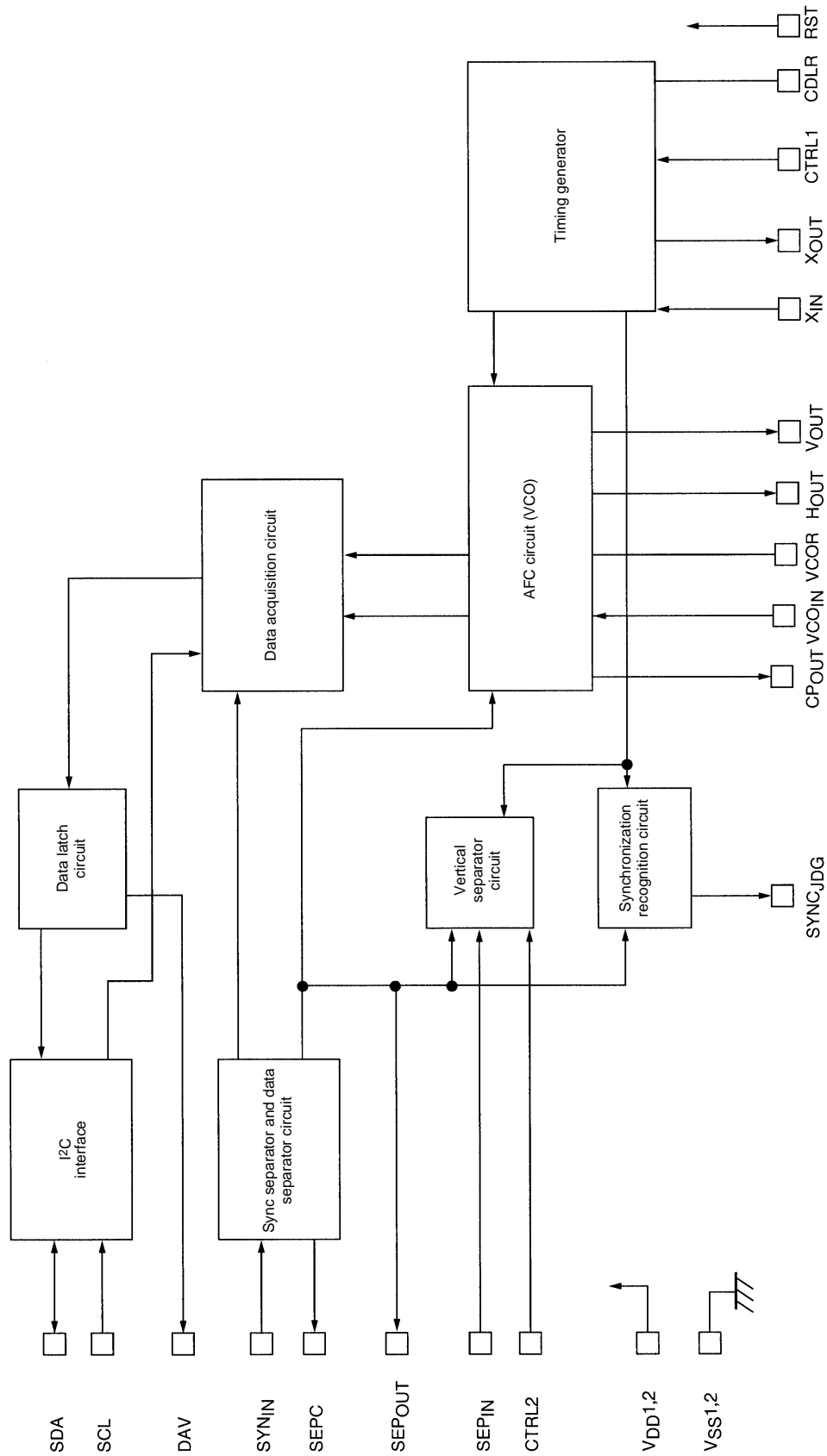
### Supplementary Documentation

- PDC and VPS serial timing (I<sup>2</sup>C bus timing)



S: Start condition  
P: Stop condition

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LC74793/M System Block Diagram

**Control Commands**

The control commands have an 8-bit serial input format. Commands consist of a command identification code in the first byte and data in the following bytes.

- Command 0: Clock control command
- Command 1: VPS/PDC control command 1
- Command 2: VPS/PDC control command 2
- Command 3: Synchronizing signal detection command 1
- Command 4: Synchronizing signal detection command 2
- Command 5: Output control command 1
- Command 6: Output control command 2
- Command 7: VPS/PDC control command 3
- Command 8: VPS/PDC control command 4
- Command 9: VPS/PDC control command 5
- Command 10: VPS/PDC control command 6

**Display Control Commands: I<sup>2</sup>C Write**

Command	First byte								Second byte							
	Command ID code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 (Clock control)	1	1	1	1	0	0	0	0	0	FS	FS2	FS3	O	TST	O	SYS
COMMAND1 (VPS/PDC control 1)	1	1	1	1	0	0	0	1	0	CPA	CPA	CPA	VPM	VPM	VPM	VPM
COMMAND2 (VPS/PDC control 2)	1	1	1	1	0	0	1	0	0	VMW	VMW	HBS	HBS	BMS	EMS	DCE
COMMAND3 (Synchronizing signal detection 1)	1	1	1	1	0	0	1	1	0	RN	RN	RN	SN	SN	SN	SN
COMMAND4 (Synchronizing signal detection 2)	1	1	1	1	0	1	0	0	0	0	RNE	SJN	SJN	SJN	SJC	SJC
COMMAND5 (Output control 1)	1	1	1	1	0	1	0	1	0	SP0	SP0	SP0	SJ0	SJ0	VNP	VSP
COMMAND6 (Output control 2)	1	1	1	1	0	1	1	0	0	0	NP1	NP0	VI0	HI0	V0T	H0T
COMMAND7 (VPS/PDC control 3)	1	1	1	1	0	1	1	1	0	0	ECV	ECV	ECV	ECV	ECV	ECV
COMMAND8 (VPS/PDC control 4)	1	1	1	1	1	0	0	0	0	ECP	ECP	ECP	ECP	ECP	ECP	ECP
COMMAND9 (VPS/PDC control 5)	1	1	1	1	1	0	0	1	0	0	ECP	ECP	ECP	ECP	ECP	ECP
COMMAND10 (VPS/PDC control 6)	1	1	1	1	1	0	1	0	0	HXA	LKA	MSK	KMW	SLH	SLH	SLH
										LL2	SLC	H1		3	2	1

Once written, the first byte command identification code is retained until the next first byte is written.  
Data is written in second byte only continuous mode. (Automatic increment)

**Command 0 (Clock Settings Command)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 0 identification code.	
5	—	1	Clock settings.	
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents				Notes																				
		Status	Function																							
7	—	0	Second byte identification bit			Setting for the frequency input to the Xtal <sub>IN</sub> pin (pin 2). CDLR can be deleted: The resistor connected to the CDLR pin may be removed.																				
6	FS	0	<table border="1"> <thead> <tr> <th>FS</th> <th>FS2</th> <th>FS3</th> <th>Setting</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>2FSC</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>4FSC (CDLR can be deleted)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>FSC</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>2FSC (CDLR can be deleted)</td> </tr> </tbody> </table>				FS	FS2	FS3	Setting	0	0	0	2FSC	1	0	0	4FSC (CDLR can be deleted)	0	1	1	FSC	0	0	1	2FSC (CDLR can be deleted)
		FS					FS2	FS3	Setting																	
0	0	0	2FSC																							
1	0	0	4FSC (CDLR can be deleted)																							
0	1	1	FSC																							
0	0	1	2FSC (CDLR can be deleted)																							
5	FS2	0																								
		1																								
4	FS3	0																								
		1																								
3	—	0																								
2	TSTMOD	0	Normal operating mode			This bit must be set to 0.																				
		1	Test mode																							
1	—	0																								
0	SYSRST	0																								
		1	All registers are reset																							



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### Command 1 (VPS/PDC control command 1)

#### • First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 1 identification code.	
5	—	1	VPS/PDC control settings 1.	
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	—	1		

#### • Second byte

DA 0 to 7	Register	Contents				Notes	
		Status	Function				
7	—	0	Second byte identification bit			Data acquisition clock selection. The clock can be shifted relative to the data in units of 8 clock cycles.	
6	CPA1	0	CPA2	CPA1	CPA0		Clock
		1	0	0	0		NO1
5	CPA2	0	0	0	1		NO2
		1	0	1	0		NO3
4	CPA0	0	0	1	1		NO4
		1	1	0	0		NO5
3	VPM3	0	1	0	1		NO6
		1	1	1	0		NO7
2	VPM2	0	1	1	1		NO8
		1	1	1	1		NO8
1	VPM1	0	M3	M2	M1	MO	Operating mode
		1	0	0	0	0	VPS
0	VPM0	0	0	0	0	1	8/30/2 (PDC)
		1	0	0	1	0	PDC and VPS automatic recognition 1
3	VPM3	0	0	0	1	1	8/30/1 (UDT)
		1	0	1	0	0	Header time 1
2	VPM2	0	0	1	0	1	Header time 2
		1	0	1	1	0	Header time 3
1	VPM1	0	0	1	1	1	Header time 4
		1	1	0	0	0	Status display 1
0	VPM0	0	1	0	0	1	Status display 2
		1	1	0	1	0	Status display 3
3	VPM3	0	1	0	1	1	Status display 4
		1	1	1	0	0	PAL PULSE
2	VPM2	0	1	1	0	1	PDC and VPS automatic recognition 2
		1	1	1	1	0	PDC and VPS automatic recognition 3
1	VPM1	0	1	1	1	1	PDC and VPS automatic recognition 4
		1	1	1	1	1	PDC and VPS automatic recognition 4

Note: All registers are cleared to 0 when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 2 (VPS/PDC control command 2)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 2 identification code.	
5	—	1	VPS/PDC control settings 2.	
4	—	1		
3	—	0		
2	—	0		
1	—	1		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	0	Second byte identification bit	
6	VMWSE2	0	From the vertical mask period start return period	CPOUT pin vertical mask period switching 2
		1	From 10H before the vertical mask period start return period	
5	VMWSEL	0	The vertical mask period is the return period	CPOUT pin vertical mask period switching
		1	The vertical mask period is 9H	
4	HBS2	0	Clock run discrimination 1 (2 times)	Clock run discrimination circuit setting
		1	Clock run discrimination 2 (4 times)	
3	HBS1	0	Framing code discrimination 1	Framing code discrimination selection
		1	Framing code discrimination 2 (A single bad bit is ignored)	
2	BMS	0	Error check enabled (The error check can be turned on or off on per-byte basis.)	When set to 0: If there are no errors in bytes for which the error check is turned on, those bytes will be written to P-S (COM7-9). When set to 1: Data is written to P-S regardless of whether or not errors occurred.
		1	Error check disabled (Applications can select whether data with errors is held or written for each byte.)	
1	EMS	0	Data hold	When error checking is enabled, specifies the processing when an error occurs in a byte for which error checking was turned off
		1	Data write (Error bits are set to 0 in VPS mode)	
0	DCE	0	Error check turned on for unused bytes VPS: bytes 3, 4, and 6 to 10, PDC: bytes 7 to 12 Header 1: bytes 14 to 37, 2: 14 to 29, 3 14 to 21. Status 1 (3): bytes 7 to 25, status 2 (4) bytes 7 to 35.	Error check setting for unused data bytes Biphase (VPS), Hamming (PDC), Odd parity (header)
		1	Error check turned off for unused bytes VPS: bytes 3, 4, and 6 to 10, PDC: bytes 7 to 12 Header 1: bytes 14 to 37, 2: 14 to 29, 3 14 to 21. Status 1 (3): bytes 7 to 25, status 2 (4) bytes 7 to 35.	

Note: All registers are cleared to 0 when the IC is reset by the RST pin.

**Command 3 (Synchronizing signal detection command 1)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 3 identification code.	
5	—	1	Synchronizing signal detection settings 1.	
4	—	1		
3	—	0		
2	—	0		
1	—	1		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents		Notes																														
		Status	Function																															
7	—	0	Second byte identification bit																															
6	RN2	0	<table border="1"> <thead> <tr> <th>RN2</th> <th>RN1</th> <th>RN0</th> <th>Number of HSYNC detections</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0 (32)</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>4 (64)</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>8 (128)</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>16 (256)</td> </tr> </tbody> </table>	RN2	RN1	RN0	Number of HSYNC detections	0	0	0	0 (32)	0	0	1	4 (64)	0	1	0	8 (128)	1	0	0	16 (256)	External synchronizing signal detection control. Signal absent → present discrimination. Sets the sampling period during which SYNC is continuously detected in the horizontal synchronizing signal period (1H). Values in parentheses apply when RNE0 (COM4) is set to 1.										
		RN2		RN1	RN0	Number of HSYNC detections																												
0	0	0	0 (32)																															
0	0	1	4 (64)																															
0	1	0	8 (128)																															
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5	RN1	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SNO</th> <th>Number of HSYNC detections</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>No detection performed</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256</td> </tr> </tbody> </table>	SN3	SN2	SN1	SNO	Number of HSYNC detections	0	0	0	0	No detection performed	0	0	0	1	32	0	0	1	0	64	0	1	0	0	128	1	0	0	0	256	External synchronizing signal detection control. Signal present → absent discrimination. Sets the sampling period during which SYNC cannot be detected consecutively in the horizontal synchronizing signal period (1H).
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4	RN0	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SNO</th> <th>Number of HSYNC detections</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>No detection performed</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256</td> </tr> </tbody> </table>	SN3	SN2	SN1	SNO	Number of HSYNC detections	0	0	0	0	No detection performed	0	0	0	1	32	0	0	1	0	64	0	1	0	0	128	1	0	0	0	256	External synchronizing signal detection control. Signal present → absent discrimination. Sets the sampling period during which SYNC cannot be detected consecutively in the horizontal synchronizing signal period (1H).
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0	1	0	0	128																														
1	0	0	0	256																														
1																																		
3	SN3	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SNO</th> <th>Number of HSYNC detections</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>No detection performed</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256</td> </tr> </tbody> </table>	SN3	SN2	SN1	SNO	Number of HSYNC detections	0	0	0	0	No detection performed	0	0	0	1	32	0	0	1	0	64	0	1	0	0	128	1	0	0	0	256	External synchronizing signal detection control. Signal present → absent discrimination. Sets the sampling period during which SYNC cannot be detected consecutively in the horizontal synchronizing signal period (1H).
		SN3		SN2	SN1	SNO	Number of HSYNC detections																											
0	0	0	0	No detection performed																														
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0	0	1	0	64																														
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		SN3		SN2	SN1	SNO	Number of HSYNC detections																											
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0	0	1	0	64																														
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1	0	0	0	256																														
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		SN3		SN2	SN1	SNO	Number of HSYNC detections																											
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0	0	1	0	64																														
0	1	0	0	128																														
1	0	0	0	256																														
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0	SN0	0	<table border="1"> <thead> <tr> <th>SN3</th> <th>SN2</th> <th>SN1</th> <th>SNO</th> <th>Number of HSYNC detections</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>No detection performed</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>32</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>64</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>128</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>256</td> </tr> </tbody> </table>	SN3	SN2	SN1	SNO	Number of HSYNC detections	0	0	0	0	No detection performed	0	0	0	1	32	0	0	1	0	64	0	1	0	0	128	1	0	0	0	256	External synchronizing signal detection control. Signal present → absent discrimination. Sets the sampling period during which SYNC cannot be detected consecutively in the horizontal synchronizing signal period (1H).
		SN3		SN2	SN1	SNO	Number of HSYNC detections																											
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0	0	1	0	64																														
0	1	0	0	128																														
1	0	0	0	256																														
1																																		

Note: All registers are cleared to 0 when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 4 (Synchronizing signal detection command 2)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 4 identification code.	
5	—	1	Synchronizing signal detection settings 2.	
4	—	1		
3	—	0		
2	—	1		
1	—	0		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes																																				
		Status	Function																																					
7	—	0	Second byte identification bit																																					
6	—	0																																						
5	RNE0	0	Synchronization signal discrimination absent → preset: Normal values	Changes the values used for synchronizing signal discrimination in the absent → preset direction (COM3).																																				
		1	Synchronization signal discrimination absent → preset: Values in parentheses																																					
4	SJNS3	0	<table border="1"> <thead> <tr> <th>SJNS3</th> <th>SJNS2</th> <th>SJNS1</th> <th>Count</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>None</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>4</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>8</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>16</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>32</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>64</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>128</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>256</td> </tr> </tbody> </table>	SJNS3	SJNS2	SJNS1	Count	0	0	0	None	0	0	1	4	0	1	0	8	0	1	1	16	1	0	0	32	1	0	1	64	1	1	0	128	1	1	1	256	Setting for the noise exclusion circuit used for synchronizing signal discrimination in the absent → preset direction. If the number of H signal inputs during a 1H period is greater than or equal to the value listed in the table, the IC determines that the signal is absent.
		SJNS3		SJNS2	SJNS1	Count																																		
0	0	0	None																																					
0	0	1	4																																					
0	1	0	8																																					
0	1	1	16																																					
1	0	0	32																																					
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3	SJNS1	0	<table border="1"> <thead> <tr> <th>SJCS1</th> <th>SJCS0</th> <th>PAL</th> <th>NTSC</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>677 ns (1/3)</td> <td>448 ns (1/2)</td> </tr> <tr> <td>0</td> <td>1</td> <td>903 ns (1/4)</td> <td>838 ns (1/3)</td> </tr> <tr> <td>1</td> <td>0</td> <td>450 ns (1/2)</td> <td>1117 ns (1/4)</td> </tr> </tbody> </table>	SJCS1	SJCS0	PAL	NTSC	0	0	677 ns (1/3)	448 ns (1/2)	0	1	903 ns (1/4)	838 ns (1/3)	1	0	450 ns (1/2)	1117 ns (1/4)	Synchronization discrimination. HSYNI signal switching clock selection.																				
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Note: All registers are cleared to 0 when the IC is reset by the RST pin.

**Command 5 (Output control command 1)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 5 identification code.	
5	—	1	Output control settings 1	
4	—	1		
3	—	0		
2	—	1		
1	—	0		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents				Notes		
		Status	Function					
7	—	0	Second byte identification bit					
6	SPO2	0	SPO2	SPO1	SPO0	SEPOut pin	SEPOUT (pin 18) output switching	
		1	0	0	0	CSYNC		
5	SPO1	0	0	0	1	Slice data amplitude		
		1	0	1	0	O/E		
4	SPO0	0	0	1	1	CLK (acquisition)		
		1	1	0	0	VCO 1/1		
3	SJO1	0	1	0	1	VCO 1/2		
		1	1	0	0	VCO 1/3		
2	SJO0	0	1	1	1	VCO 1/4		
		1	1	1	1	VCO 1/4		
3	SJO1	0	SJO1	SJO0	SYNCJDG pin			SYNCJDG (pin 8) output switching
		1	0	0	SYNCjdg			
2	SJO0	0	0	1	LOCK			
		1	1	0	SYNCdet			
1	VNPSEL	0	Vertical signal falling edge detection			Vertical signal acquisition polarity switching. Only valid when internal vertical separation used.		
		1	Vertical signal rising edge detection					
0	VSPSEL	0	VSEP: About 8.9 μs (NTSC)			Internal vertical separation time switching		
		1	VSEP: About 17.8 μs (NTSC)					

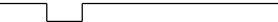
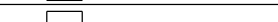
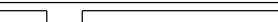

Note: All registers are cleared to 0 when the IC is reset by the RST pin.

**Command 6 (Output control command 2)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 6 identification code.	
5	—	1	Output control settings 2.	
4	—	1		
3	—	0		
2	—	1		
1	—	1		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	NP1	0	PAL	
		1	NTSC	
4	NP0	0	625	Number of scan lines
		1	525	
3	VIOSET	0	VSYNC signal output	VOUT mode setting
		1	Set up as a general-purpose port	
2	HIOSET	0	HSYNC signal output	HOUT mode setting
		1	Set up as a general-purpose port	
1	VOTKST	0	Negative polarity  (Lo)	VOUT polarity selection. Level in parentheses applies when set up as a general-purpose port.
		1	Positive polarity  (Hi)	
0	HOTKST	0	Negative polarity  (Lo)	HOUT polarity selection. Level in parentheses applies when set up as a general-purpose port.
		1	Positive polarity  (Hi)	

Note: All registers are cleared to 0 when the IC is reset by the RST pin.

**Command 7 (VPS/PDC control command 3)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 7 identification code.	
5	—	1	VPS/PDC control settings 3.	
4	—	1		
3	—	0		
2	—	1		
1	—	1		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	ECV15	0	Byte 15 biphas error check: on (data retained)	VPS data specification when BMS is 0. Items in parentheses are the specification when BMS is 1.
		1	Byte 15 biphas error check: off (data written)	
4	ECV14	0	Byte 14 biphas error check: on (data retained)	
		1	Byte 14 biphas error check: off (data written)	
3	ECV13	0	Byte 13 biphas error check: on (data retained)	
		1	Byte 13 biphas error check: off (data written)	
2	ECV12	0	Byte 12 biphas error check: on (data retained)	
		1	Byte 12 biphas error check: off (data written)	
1	ECV11	0	Byte 11 biphas error check: on (data retained)	
		1	Byte 11 biphas error check: off (data written)	
0	ECV5	0	Byte 5 biphas error check: on (data retained)	
		1	Byte 5 biphas error check: off (data written)	

Note: All registers are cleared to 0 when the IC is reset by the RST pin.

**Command 8 (VPS/PDC control command 4)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 8 identification code.	
5	—	1	VPS/PDC control settings 4.	
4	—	1		
3	—	1		
2	—	0		
1	—	0		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	0	Second byte identification bit	PDC data specification when BMS is 0. Items in parentheses are the specification when BMS is 1. Items in curly braces are the bytes for which the odd parity check is turned on or off for headers 1, 2, 3, and 4, and for status 1, 2, 3, and 4.
6	ECP19	0	Byte 19 Hamming error check on (Data retained) {Bytes 44, 28, 36, 20, 32, 42, 32, 42}	
		1	Byte 19 Hamming error check off (Data written) {Bytes 44, 28, 36, 20, 32, 42, 32, 42}	
5	ECP18	0	Byte 18 Hamming error check on (Data retained) {Bytes 43, 27, 35, 19, 31, 41, 31, 41}	
		1	Byte 18 Hamming error check off (Data written) {Bytes 43, 27, 35, 19, 31, 41, 31, 41}	
4	ECP17	0	Byte 17 Hamming error check on (Data retained) {Bytes 42, 26, 34, 18, 30, 40, 30, 40}	
		1	Byte 17 Hamming error check off (Data written) {Bytes 42, 26, 34, 18, 30, 40, 30, 40}	
3	ECP16	0	Byte 16 Hamming error check on (Data retained) {Bytes 41, 25, 33, 17, 29, 39, 29, 39}	
		1	Byte 16 Hamming error check off (Data written) {Bytes 41, 25, 33, 17, 29, 39, 29, 39}	
2	ECP15	0	Byte 15 Hamming error check on (Data retained) {Bytes 40, 24, 32, 16, 28, 38, 28, 38}	
		1	Byte 15 Hamming error check off (Data written) {Bytes 40, 24, 32, 16, 28, 38, 28, 38}	
1	ECP14	0	Byte 14 Hamming error check on (Data retained) {Bytes 39, 23, 31, 15, 27, 37, 27, 37}	
		1	Byte 14 Hamming error check off (Data written) {Bytes 39, 23, 31, 15, 27, 37, 27, 37}	
0	ECP13	0	Byte 13 Hamming error check on (Data retained) {Bytes 38, 22, 30, 14, 26, 36, 26, 36}	
		1	Byte 13 Hamming error check off (Data written) {Bytes 38, 22, 30, 14, 26, 36, 26, 36}	

Note: All registers are cleared to 0 when the IC is reset by the RST pin.



**Command 9 (VPS/PDC control command 5)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command 9 identification code.	
5	—	1	VPS/PDC control settings 5.	
4	—	1		
3	—	1		
2	—	0		
1	—	0		
0	—	1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	0	Second byte identification bit	
6	—	0		
5	ECP25	0	Byte 25 Hamming error check on (Data retained)	PDC data specification when BMS is 0. Items in parentheses are the specification when BMS is 1. Items in curly braces are the bytes for which the odd parity check is turned on or off for headers 1, 2, 3, and 4, and for status 1, 2, 3, and 4.
		1	Byte 25 Hamming error check off (Data written)	
4	ECP24	0	Byte 24 Hamming error check on (Data retained)	
		1	Byte 24 Hamming error check off (Data written)	
3	ECP23	0	Byte 23 Hamming error check on (Data retained)	
		1	Byte 23 Hamming error check off (Data written)	
2	ECP22	0	Byte 22 Hamming error check on (Data retained) {Bytes , , , , 35, 45, 35, 45}	
		1	Byte 22 Hamming error check off (Data written) {Bytes , , , , 35, 45, 35, 45}	
1	ECP21	0	Byte 21 Hamming error check on (Data retained) {Bytes , , , , 34, 44, 34, 44}	
		1	Byte 21 Hamming error check off (Data written) {Bytes , , , , 34, 44, 34, 44}	
0	ECP20	0	Byte 20 Hamming error check on (Data retained) {Bytes 45, 29, 37, 21, 33, 43, 33, 43}	
		1	Byte 20 Hamming error check off (Data written) {Bytes 45, 29, 37, 21, 33, 43, 33, 43}	

Note: All registers are cleared to 0 when the IC is reset by the  $\overline{\text{RST}}$  pin.

**Command 10 (VPS/PDC control command 6)**

• First byte

DA 0 to 7	Register	Contents		Notes
		Status	Function	
7	—	1	First byte identification bit	
6	—	1	Command A identification code.	
5	—	1	VPS/PDC control settings 6.	
4	—	1		
3	—	1		
2	—	0		
1	—	1		
0	—	0		

• Second byte

DA 0 to 7	Register	Contents		Notes																											
		Status	Function																												
7	—	0	Second byte identification bit																												
6	HXALL2	0	Slice data discrimination time: Normal	VPS/PDC data discrimination period setting																											
		1	Discriminates the vertical return period data in all modes																												
5	LKASLC	0	Normal operation																												
		1	Always in the locked state																												
4	MSKH1	0																													
		1	AFC: A mask is applied to the horizontal signal																												
3	KMW	0																													
		1	Forcibly set to high or low only during the CSYNC period																												
2	SLH3	0	<table border="1"> <thead> <tr> <th>MODE</th> <th>S321</th> <th>Clock discrimination</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0 0 0</td> <td>1 1 1 1 1 1 x x 0 0 0 0 0 0 x x</td> </tr> <tr> <td>1</td> <td>0 0 1</td> <td>0 0 0 0 0 0 x x 1 1 1 1 1 1 x x</td> </tr> <tr> <td>2</td> <td>0 1 0</td> <td>1 1 1 1 1 x x x 0 0 0 0 0 x x x</td> </tr> <tr> <td>3</td> <td>0 1 1</td> <td>0 0 0 0 0 x x x 1 1 1 1 1 x x x</td> </tr> <tr> <td>4</td> <td>1 0 0</td> <td>x x 1 1 1 1 1 1 0 0 0 0 0 0 x x</td> </tr> <tr> <td>5</td> <td>1 0 1</td> <td>x x 0 0 0 0 0 0 1 1 1 1 1 1 x x</td> </tr> <tr> <td>6</td> <td>1 1 0</td> <td>1 1 1 x 0 0 0 x</td> </tr> <tr> <td>7</td> <td>1 1 1</td> <td>0 0 0 x 1 1 1 x</td> </tr> </tbody> </table>	MODE	S321	Clock discrimination	0	0 0 0	1 1 1 1 1 1 x x 0 0 0 0 0 0 x x	1	0 0 1	0 0 0 0 0 0 x x 1 1 1 1 1 1 x x	2	0 1 0	1 1 1 1 1 x x x 0 0 0 0 0 x x x	3	0 1 1	0 0 0 0 0 x x x 1 1 1 1 1 x x x	4	1 0 0	x x 1 1 1 1 1 1 0 0 0 0 0 0 x x	5	1 0 1	x x 0 0 0 0 0 0 1 1 1 1 1 1 x x	6	1 1 0	1 1 1 x 0 0 0 x	7	1 1 1	0 0 0 x 1 1 1 x	Clock discrimination method switching
		MODE	S321	Clock discrimination																											
0	0 0 0	1 1 1 1 1 1 x x 0 0 0 0 0 0 x x																													
1	0 0 1	0 0 0 0 0 0 x x 1 1 1 1 1 1 x x																													
2	0 1 0	1 1 1 1 1 x x x 0 0 0 0 0 x x x																													
3	0 1 1	0 0 0 0 0 x x x 1 1 1 1 1 x x x																													
4	1 0 0	x x 1 1 1 1 1 1 0 0 0 0 0 0 x x																													
5	1 0 1	x x 0 0 0 0 0 0 1 1 1 1 1 1 x x																													
6	1 1 0	1 1 1 x 0 0 0 x																													
7	1 1 1	0 0 0 x 1 1 1 x																													
1	1																														
1	SLH2	0																													
		1																													
0	SLH1	0																													
		1																													

Note: All registers are cleared to 0 when the IC is reset by the  $\overline{\text{RST}}$  pin.

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**PDC/VPS Output Data Format**

Data is read out in order starting with bit 7 of byte 1.

Output data		PDC 8/30/mode				VPS mode		Header time mode 1 (3)		Header time mode 2 (4)		
		Format1		Format2								
Byte1	Bit7	byte15	bit0	byte16	bit0	byte11	bit0	byte38	bit0	byte22	bit0	
	6		1		1		(30)		1		(14)	1
	5		2		2				2			2
	4		3		3				3			3
	3		4		byte17		bit0		4			4
	2		5						5			5
	1		6						6			6
	0		7						7			7
Byte2	Bit7	byte16	bit0	byte18	bit0	byte12	bit0	byte39	bit0	byte23	bit0	
	6		1		1		(31)		1		(15)	1
	5		2		2				2			2
	4		3		3				3			3
	3		4		byte19		bit0		4			4
	2		5						5			5
	1		6						6			6
	0		7						7			7
Byte3	Bit7	byte17	bit0	byte20	bit0	byte13	bit0	byte40	bit0	byte24	bit0	
	6		1		1		(32)		1		(16)	1
	5		2		2				2			2
	4		3		3				3			3
	3		4		byte21		bit0		4			4
	2		5						5			5
	1		6						6			6
	0		7						7			7
Byte4	Bit7	byte18	bit0	byte22	bit0	byte14	bit0	byte41	bit0	byte25	bit0	
	6		1		1		(33)		1		(17)	1
	5		2		2				2			2
	4		3		3				3			3
	3		4		byte23		bit0		4			4
	2		5						5			5
	1		6						6			6
	0		7						7			7
Byte5	Bit7	byte19	bit0	byte14	bit0	byte5	bit0	byte42	bit0	byte26	bit0	
	6		1		1		(34)		1		(18)	1
	5		2		2				2			2
	4		3		3				3			3
	3		4		byte15		bit0		4			4
	2		5						5			5
	1		6						6			6
	0		7						7			7
Byte6	Bit7	byte20	bit0	byte24	bit0	byte15	bit0	byte43	bit0	byte27	bit0	
	6		1		1		(35)		1		(19)	1
	5		2		2				2			2
	4		3		3				3			3
	3		4		byte25		bit0		4			4
	2		5						5			5
	1		6						6			6
	0		7						7			7

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Continued from preceding page.

Output data		PDC 8/30/mode				VPS mode		Header time mode 1 (3)		Header time mode 2 (4)							
		Format1		Format2													
Byte7	Bit7	byte21	bit0	byte13	bit0	1	1	byte44	bit0	byte28	bit0						
	6		1		1							(36)	1	(20)	1		
	5		2		1							2	2	2	2		
	4		3		1							3	1	3	3		
	3		4		1							4	1	4	4		
	2		5		1							5	1	5	5		
	1		6		1							6	1	6	6		
	0		7		1							7	0	7	7		
Byte8	Bit7	byte13	bit0	Error information 1	byte16	Error information	byte11	byte45	bit0	byte29	bit0						
	6		1									17	12	(37)	1	(21)	1
	5		2									18	13	2	2	2	
	4		3									19	14	3	3	3	
	3		4									20	5	4	4	4	
	2		5									21	15	5	5	5	
	1		6									22	0	6	6	6	
	0		7									23	0	7	7	7	
Byte9	Bit7	byte14	bit0	Error information 2	byte14			Error information	byte38 (30)	Error information	byte22 (14)						
	6		1									15	39 (31)	23 (15)			
	5		2									24	40 (32)	24 (16)			
	4		3									25	41 (33)	25 (17)			
	3		4									13	42 (34)	26 (18)			
	2		5									0	43 (35)	27 (19)			
	1		6									0	44 (36)	28 (20)			
	0		7									0	45 (37)	29 (21)			
Byte10	Bit7	byte22	bit0														
	6		1														
	5		2														
	4		3														
	3		4														
	2		5														
	1		6														
	0		7														
Byte11	Bit7	byte23	bit0														
	6		1														
	5		2														
	4		3														
	3		4														
	2		5														
	1		6														
	0		7														
Byte12	Bit7	byte24	bit0														
	6		1														
	5		2														
	4		3														
	3		4														
	2		5														
	1		6														
	0		7														
Byte13	Bit7	byte25	bit0														
	6		1														
	5		2														
	4		3														
	3		4														
	2		5														
	1		6														
	0		7														

Note: Data with the value 1 is output for sections for which there is no output data setting.

**LC74793, 74793JM**

**Data is read out in order starting with bit 7 of byte 1.**

Status display 1 and 2: 8/30/2    Status display 1 and 2: 8/30/1

Output data		Status display mode 1 (3)		Status display mode 2 (4)		PAL Puls
Byte1	Bit7	byte26	bit0	byte36	bit0	bit0
	6	(26)	1	(36)	1	1
	5		2		2	2
	4		3		3	3
	3		4		4	4
	2		5		5	5
	1		6		6	6
	0		7		7	7
Byte2	Bit7	byte27	bit0	byte37	bit0	bit8
	6	(27)	1	(37)	1	9
	5		2		2	10
	4		3		3	11
	3		4		4	12
	2		5		5	13
	1		6		6	0
	0		7		7	0
Byte3	Bit7	byte28	bit0	byte38	bit0	
	6	(28)	1	(38)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte4	Bit7	byte29	bit0	byte39	bit0	
	6	(29)	1	(39)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte5	Bit7	byte30	bit0	byte40	bit0	
	6	(30)	1	(40)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	
Byte6	Bit7	byte31	bit0	byte41	bit0	
	6	(31)	1	(41)	1	
	5		2		2	
	4		3		3	
	3		4		4	
	2		5		5	
	1		6		6	
	0		7		7	

Note: Data with the value 1 is output for sections for which there is no output data setting.

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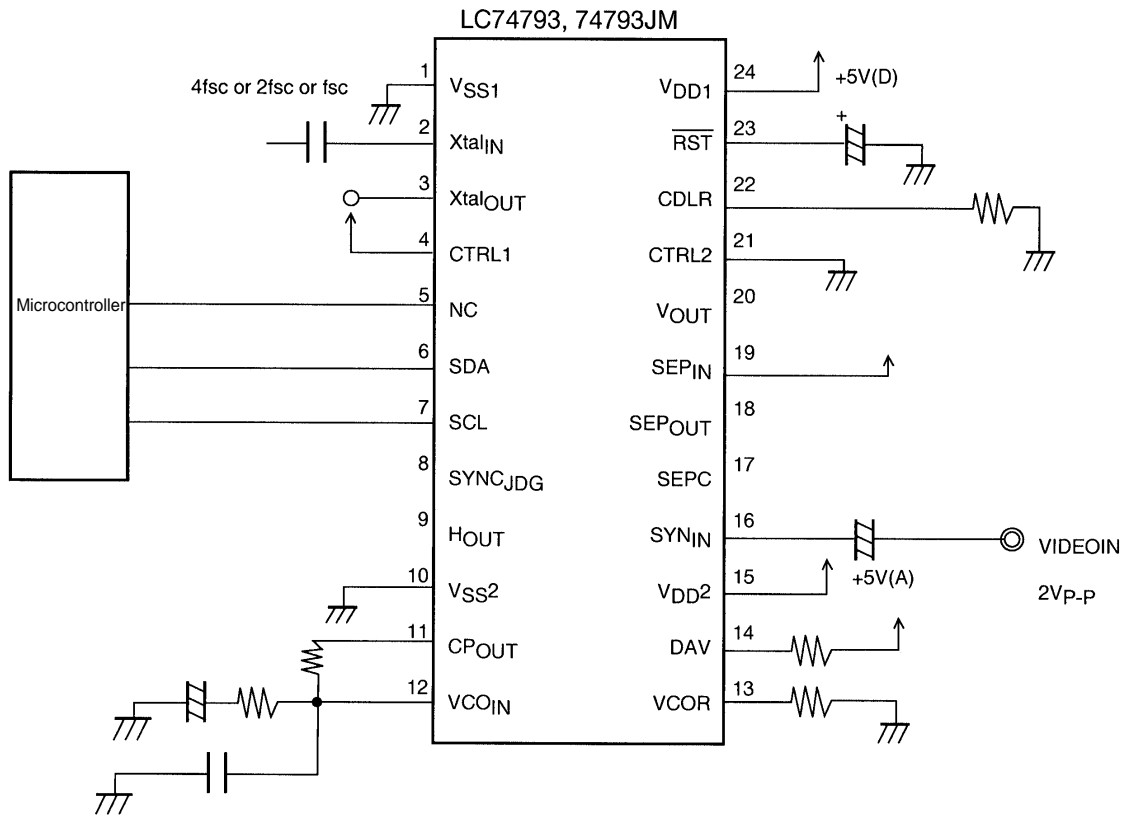
Output data		Status display mode 1 (3)		Status display mode 2 (4)		PAL Puls
Byte7	Bit7 6 5 4 3 2 1 0	byte32 (32)	bit0 1 2 3 4 5 6 7	byte42 (42)	bit0 1 2 3 4 5 6 7	
Byte8	Bit7 6 5 4 3 2 1 0	byte33 (33)	bit0 1 2 3 4 5 6 7	byte43 (43)	bit0 1 2 3 4 5 6 7	
Byte9	Bit7 6 5 4 3 2 1 0	byte34 (34)	bit0 1 2 3 4 5 6 7	byte44 (44)	bit0 1 2 3 4 5 6 7	
Byte10	Bit7 6 5 4 3 2 1 0	byte35 (35)	bit0 1 2 3 4 5 6 7	byte45 (45)	bit0 1 2 3 4 5 6 7	
Byte11	Bit7 6 5 4 3 2 1 0	Error information 1	byte26 (26) 27 (27) 28 (28) 29 (29) 30 (30) 31 (31) 32 (32) 33 (33)	Error information 1	byte36 (36) 37 (37) 38 (38) 39 (39) 40 (40) 41 (41) 42 (42) 43 (43)	
Byte12	Bit7 6 5 4 3 2 1 0	Error information 2	byte34 (34) 35 (35)	Error information 1	byte44 (44) 45 (45)	
Byte13	Bit7 6 5 4 3 2 1 0					

Note: Data with the value 1 is output for sections for which there is no output data setting.

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## Sample Application Circuit

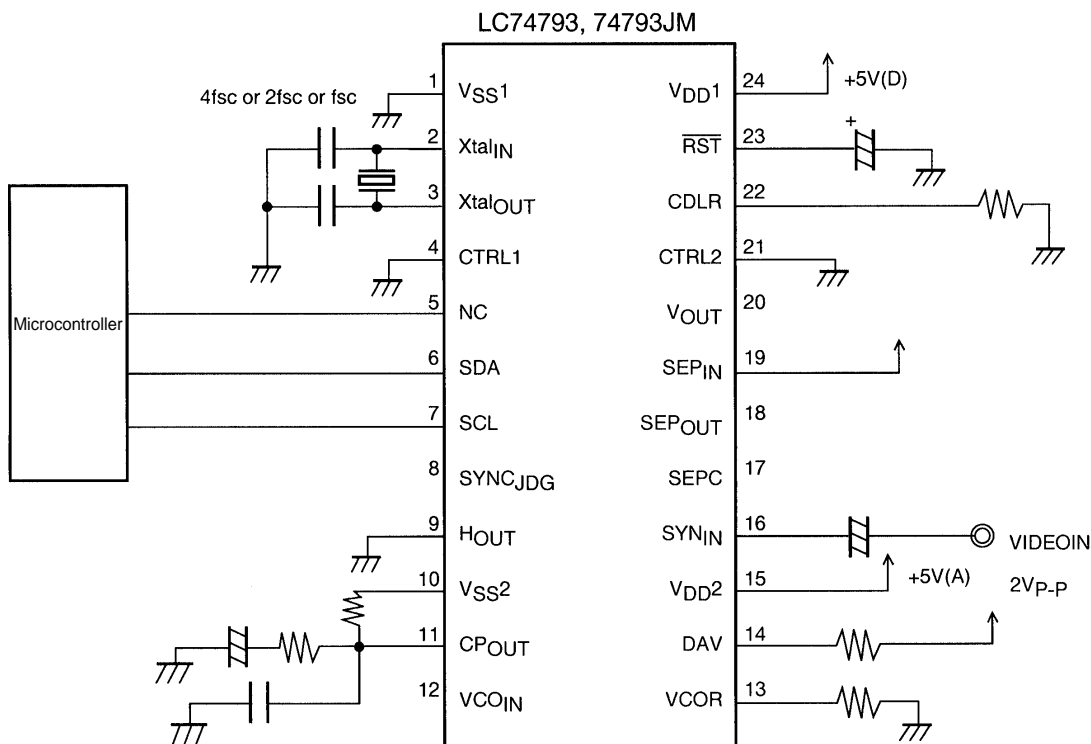
- Using an external system clock



A11053

## LC74793, 74793JM

- Using a crystal oscillator



A11054

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