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Status	Product Specification
Memory Products	

82LS135
2K-bit TTL bipolar PROM

DESCRIPTION

The 82LS135 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82LS135 includes on-chip decoding and two Chip Enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

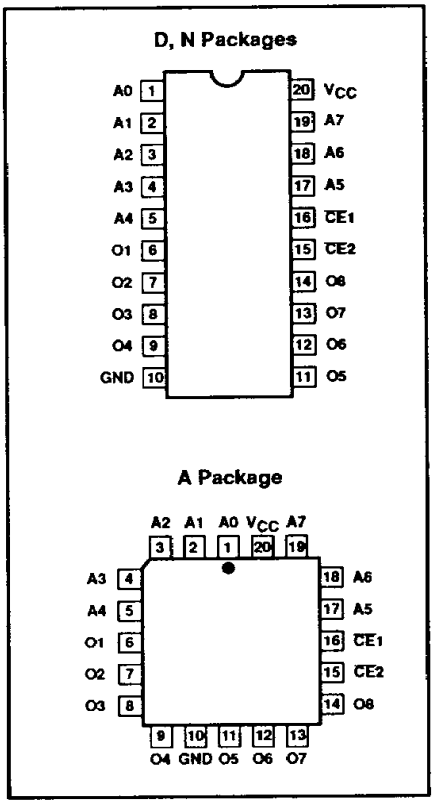
FEATURES

- Address access time: 100ns max
- Power dissipation: 200µW/bit typ
- Input loading: -100µA max
- Two Chip Enable inputs
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Unprogrammed outputs are Low level
- Outputs: 3-State

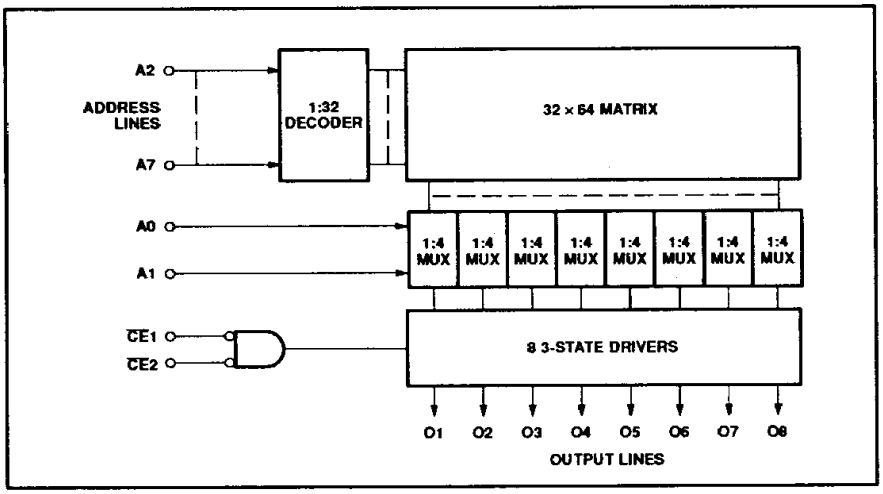
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATIONS



BLOCK DIAGRAM



2K-bit TTL bipolar PROM (256 × 8) — 82LS135

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	N82LS135 N
20-Pin Plastic Small Outline 300mil-wide	N82LS135 D
20-Pin Plastic Leaded Chip Carrier 350mil-square	N82LS135 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	I_{IN} = -12mA			-1.2	V
Output voltage						
V_{OL}	Low	I_{OUT} = 16mA			0.5	V
V_{OH}	High	I_{OUT} = -2mA, High stored	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
I_{OZ}	Hi-Z state	$\overline{CE}1$, $\overline{CE}2$ = High, V_{OUT} = 0.5V			-40	µA
		$\overline{CE}1$, $\overline{CE}2$ = High, V_{OUT} = 5.5V			40	µA
I_{OS}	Short circuit[4]	$\overline{CE}1$, $\overline{CE}2$ = Low, V_{OUT} = 0V, High stored	-15		-75	mA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V		80	100	mA
Capacitance						
		V_{CC} = 5.0V, $\overline{CE}$ = High				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Typical values are at V_{CC} = 5V, T_{amb} = +25°C.
4. Duration of short circuit should not exceed 1 second.
5. Measured with all inputs grounded and all outputs open.

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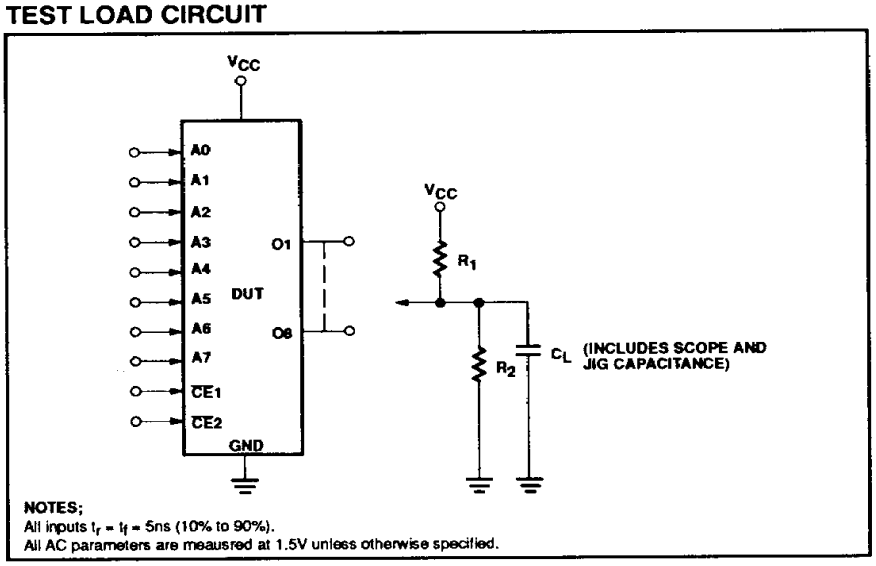
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_{amb} \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ[1]	LIMITS Max	UNIT
Access time[2]							
t_{AA}		Output	Address		70	100	ns
t_{CE}		Output	Chip Enable		30	50	ns
Disable time[3]							
t_{CD}		Output	Chip Disable		30	60	ns

NOTES:
1. Typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
2. Tested at an address cycle time of 1µs.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$, $C_L = 5pF$.

TEST LOAD CIRCUIT



NOTES;
All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are meausred at 1.5V unless otherwise specified.

VOLTAGE WAVEFORMS