Rev 0; 2/08

MAXIM

I²C Gamma and VCOM Buffer with EEPROM

DS3510

General Description

The DS3510 is a programmable gamma and VCOM voltage generator which supports both real-time updating as well as multibyte storage of gamma/VCOM data in on-chip EEPROM memory. An independent 8-bit DAC, two 8-bit data registers, and 4 bytes of EEPROM memory are provided for each individually addressable gamma or VCOM channel. High-performance buffer amplifiers are integrated on-chip, providing rail-to-rail, low-power (400µA/gamma channel) operation. The VCOM channel features a high-current drive (> 250mA peak) and a fast-settling buffer amplifier optimized to drive the VCOM node of a wide range of TFT-LCD panels.

Programming occurs through an I²C-compatible serial interface. Interface performance and flexibility are enhanced by a pair of independently loaded data registers per channel, as well as support for I²C speeds up to 400kHz. The multitable EEPROM memory enables a rich variety of display system enhancements, including support for temperature or light-level-dependent gamma tables, enabling of factory or field automated display adjustment, and support for backlight dimming algorithms to reduce system power. Upon power-up and depending on mode, DAC data is selected from EEPROM by the S0/S1 pads or from a fixed memory address.

Applications

TFT-LCD Gamma and VCOM Buffer

Adaptive Gamma and VCOM Adjustment (Real-Time by I²C, Select EEPROM Through I²C or S0/S1 Pads)

Industrial Process Control

Features

- **8-Bit Gamma Buffers, 10 Channels**
- **8-Bit VCOM Buffer, 1 Channel**
- **4 EEPROM Bytes per Channel**
- **Low-Power 400µA/ch Gamma Buffers**
- **I²C-Compatible Serial Interface**
- **Flexible Control from I²C or Pins**
- **9.0V to 15.0V Analog Supply**
- **2.7V to 5.5V Digital Supply**
- **48-Pin Package (TQFN 7mm x 7mm)**

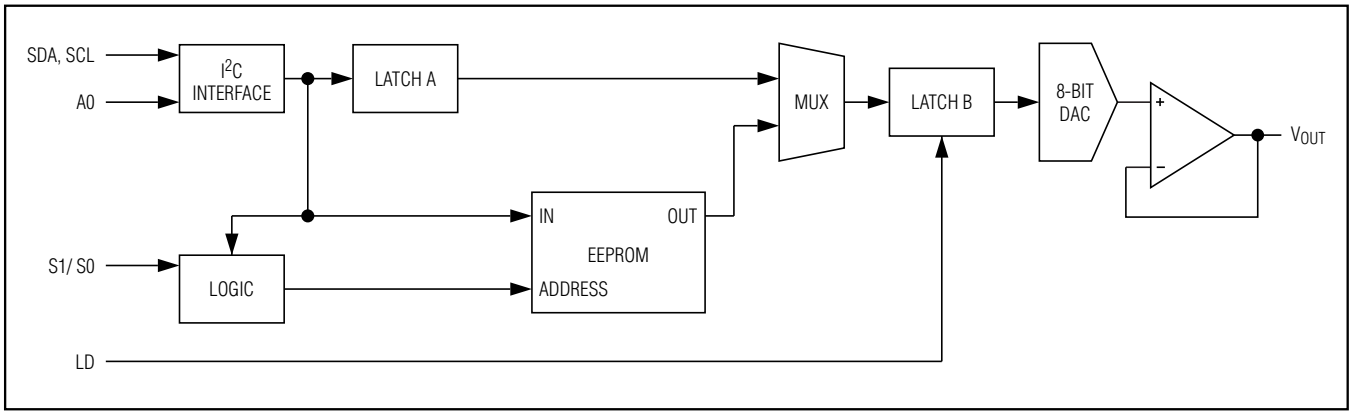
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3510T+	-45°C to +95°C	48 TQFN-EP*
DS3510T+T&R	-45°C to +95°C	48 TQFN-EP*

+Denotes a lead-free package.
T&R = Tape and reel.
**EP = Exposed pad.*

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

Gamma or VCOM Channel Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

I²C Gamma and VCOM Buffer with EEPROM

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{DD} Relative to GND .....-0.5V to +16V
Voltage on VRL, VRH, GHH, GHM, GLM, GLL
Relative to GND.....-0.5V to (V_{DD} + 0.5V), not to exceed 16V
Voltage on V_{CC} Relative to GND .....-0.5V to +6V
Voltage on SDA, SCL, A0, LD, S0,
S1 Relative to GND ....-0.5V to (V_{CC} + 0.5V), not to exceed 6V

Junction Temperature .....+125°C
Operating Temperature Range .....-45°C to +95°C
Programming Temperature Range .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -45°C to +95°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Voltage	V_{CC}	(Note 1)	+2.7		+5.5	V
Analog Supply Voltage	V_{DD}	(Note 1)	+9.0		+15.0	V
VRH, VRL Voltage	V_{VCOM}	Applies to V_{COM} output	+2.0		V_{DD} - 2.0	V
GHH, GHM, GLM, GLL Voltage	$V_{GM1–10}$	Applies to GM1–GM10	GND + 0.2		V_{DD} - 0.2	V
Input Logic 1 (SCL, SDA, A0, S0, S1, LD)	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0 (SCL, SDA, A0, S0, S1, LD)	V_{IL}		-0.3		0.3 x V_{CC}	V
V_{COM} Load Capacitor	C_D		1			µF
V_{CAP} Compensation Capacitor	C_{COMP}		0.1			µF

INPUT ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (SDA, SCL, S0, S1, LD)	I_L		-1		+1	µA
Input Leakage (A0)	$I_{L:A0}$				2	mA
V_{DD} Supply Current	I_{DD}	(Notes 2, 3)		6.7	15.0	mA
V_{CC} Supply Current, Nonvolatile Read or Write	I_{CC}	(Note 4)		0.2	1.0	mA
V_{CC} Standby Supply Current	I_{CCQ}	(Note 5)		1.8	10.0	µA
V_{DD} Standby Supply Current	I_{DDQ}	(Note 6)		2	4	mA
I/O Capacitance (SDA, SCL, A0)	$C_{I/O}$	(Note 7)		5	10	pF
End-to-End Resistance (VRH to VRL)	R_{TOTAL}			16		kΩ

INPUT ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
R_{TOTAL} Tolerance		T_A= +25°C	-20		+20	%
Input Resistance (GHH, GHM, GLM, GLL)				75		kΩ
Input Resistance Tolerance		T_A= +25°C	-20		+20	%

OUTPUT ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, VRL = GLL = +0.2V, GLM = +4.8V, GHM = +10.2V, VRH = GHH = +14.8V, T_A = -45°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{COM}/GM1–10 DAC resolution				8			Bits
Integral Nonlinearity Error	INL	(Note 8)	V_{COM}	-0.75		+0.75	LSB
			Gamma	-0.4		+0.4	
Differential Nonlinearity Error	DNL	V_{COM}/gamma (Note 9)		-0.3		+0.3	LSB
Output Voltage Range (V_{COM})				2.0		V_{DD} - 2.0	V
Output Voltage Range (GM1–10)				0.2		V_{DD} - 0.2	V
Output Accuracy (V_{COM}, GM1–10)		T_A= +25°C	V_{COM}	-25		+25	mV
			Gamma	-50		+50	
Voltage Gain (GM1–10)		(Note 10)			0.995		V/V
Load Regulation (V_{COM}, GM1–10)					0.5		mV/mA
Short-Circuit Current (V_{COM})		To V_{DD} or GND		250			mA
S0/S1 to LD Setup Time	t_{SU}	Figure 1 or 2		200			ns
S0/S1 to LD Hold Time	t_{HD}	Figure 1 or 2		200			ns
V_{COM} Settling Time from LD Low to High (S0/S1 Meet t_{SU})	t_{SET-V}	Settling to 0.1% (see Figure 1) (Notes 3, 11)			2		µs
GM1–10 Settling Time from LD Low to High	t_{SET-G}	4 tau settled with I_{LOAD}= ±20mA (see Figure 2) (Notes 3, 11, 12)				6.7	µs
S0, S1 to V_{COM} or GM1–10 Output 10% Settled	t_{SEL}	10% settling (see Figure 3), LD = V_{CC} (asynchronous) (Note 12)				450	ns

I²C ELECTRICAL CHARACTERISTICS (See Figure 4)

(V_{CC} = +2.7V to +5.5V, T_A = -45°C to +95°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 13)	0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
START Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 14)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 14)	$20 + 0.1C_B$		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 14)			400	pF
EEPROM Write Time	t_W	(Note 15)			20	ms
Pulse-Width Suppression Time at SDA and SCL Inputs	t_{IN}	(Note 16)			50	ns
A0 Setup Time	$t_{SU:A}$	Before START	0.6			µs
A0 Hold Time	$t_{HD:A}$	After STOP	0.6			µs
SDA and SCL Input Buffer Hysteresis			$0.05 \times V_{CC}$			V
Low-Level Output Voltage (SDA)	V_{OL}	4mA sink current			0.4	V
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling through $0.3V_{CC}$ to SDA exit $0.3V_{CC}$ ~$0.7V_{CC}$ window			900	ns
Output Data Hold	t_{DH}	SCL falling through $0.3V_{CC}$ until SDA in $0.3V_{CC}$ ~$0.7V_{CC}$ window	0			ns

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
EEPROM Write Cycles		T_A = +70°C	50,000		Writes
EEPROM Write Cycles		T_A = +25°C	200,000		Writes

Note 1: All voltages are referenced to ground. Currents entering the IC are specified positive and currents exiting the IC are negative.
Note 2: I_{DD} supply current is specified with V_{DD} = 15.0V and no load on V_{COM} or GM1–10 outputs.
Note 3: Specified with the V_{COM} and gamma bias currents set to 100%.
Note 4: I_{CC} is specified with the following conditions: SCL = 400kHz, SDA = V_{CC} = 5.5V, and V_{COM} and GM1–10 floating.
Note 5: I_{CCQ} is specified with the following conditions: SCL = SDA = V_{CC} = 5.5V, and V_{COM} and GM1–10 floating.
Note 6: I_{DDQ} is specified with the following conditions: SCL = SDA = V_{CC} = 5.5V and V_{COM} and GM1–10 floating.
Note 7: Guaranteed by design.
Note 8: Integral nonlinearity is the deviation of a measured value from the expected values at each particular setting. Expected value is calculated by connecting a straight line from the measured minimum setting to the measured maximum setting. INL = $[V(RW)_i - (V(RW)_0]$/LSB(measured) - i, for i = 0...255.
Note 9: Differential nonlinearity is the deviation of the step size change between two LSB settings from the expected step size. The expected LSB step size is the slope of the straight line from measured minimum position to measured maximum position. DNL = $[V(RW)_{i+1} - (V(RW)_i]$/LSB(measured) - 1, for i = 0...254.
Note 10: Tested at VRL = VRH = 6.5V/7.5V/8.5V, GLL = GLM = 0.5V/6.5V/8.5V/14.5V, GHM = GHH = 0.5V/6.5V/8.5V/14.5V.
Note 11: EEPROM data is assumed already settled at input of Latch B. LD transitions after EEPROM byte has been selected.
Note 12: Rising transition from 5V to 10V; falling transition from 10V to 5V.
Note 13: I²C interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with I²C standard mode timing.
Note 14: C_B—total capacitance of one bus line in picofarads.
Note 15: EEPROM write time begins after a STOP condition occurs.
Note 16: Pulses narrower than max are suppressed.

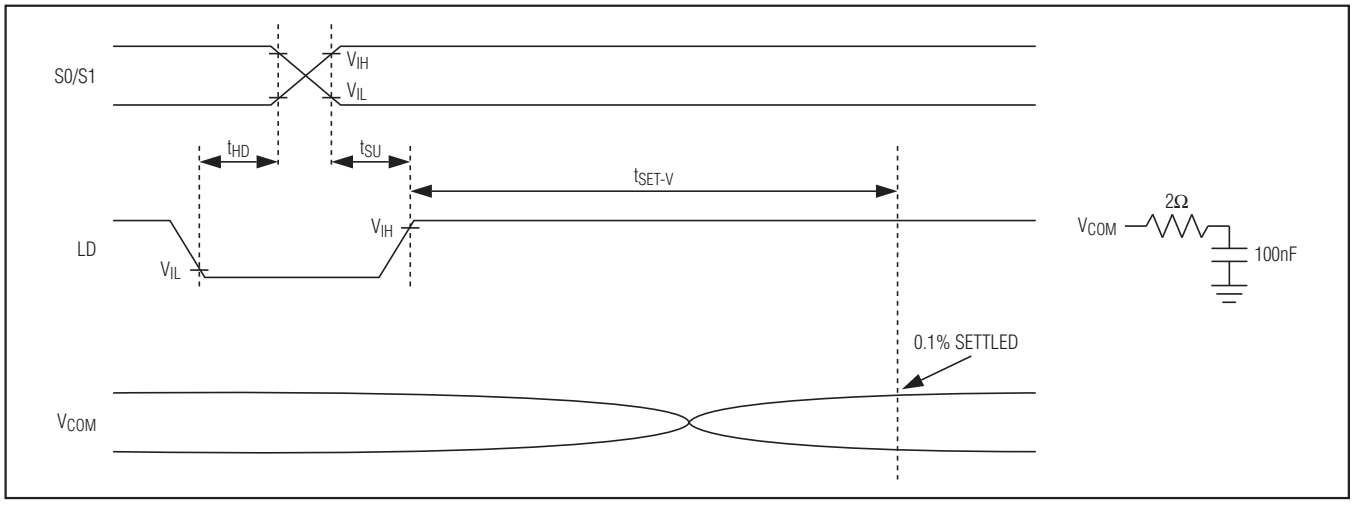


Figure 1. V_{COM} Settling Timing Diagram

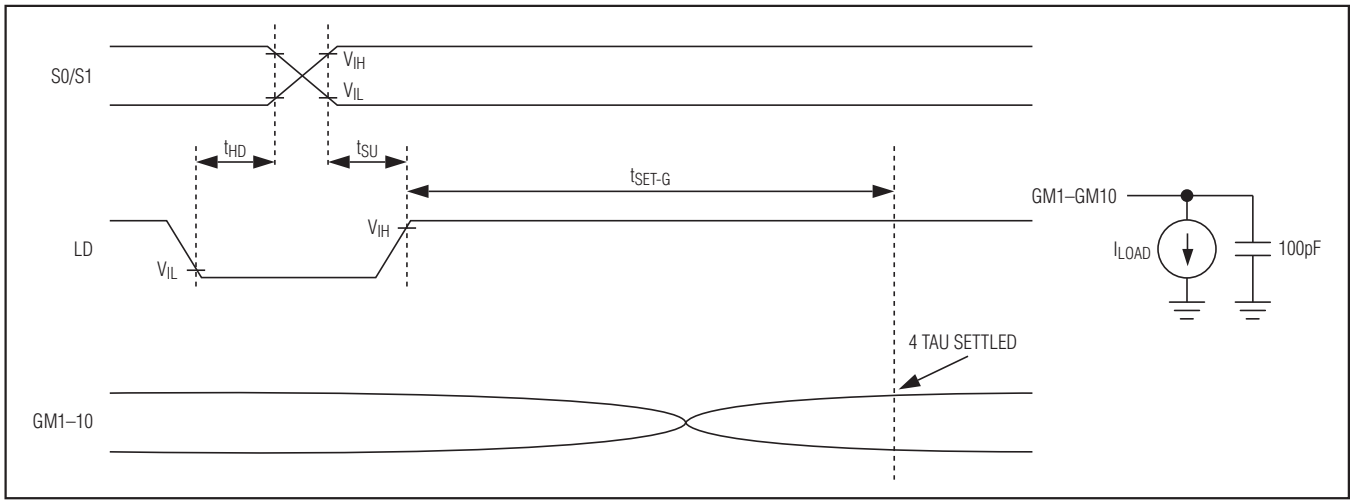


Figure 2. GM1–10 Settling Timing Diagram

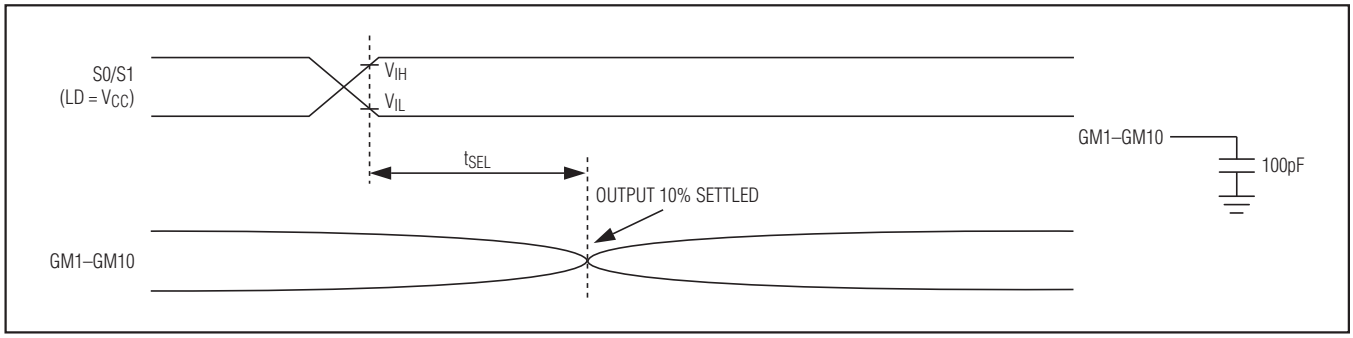


Figure 3. Input Pin to Output Change Timing Diagram

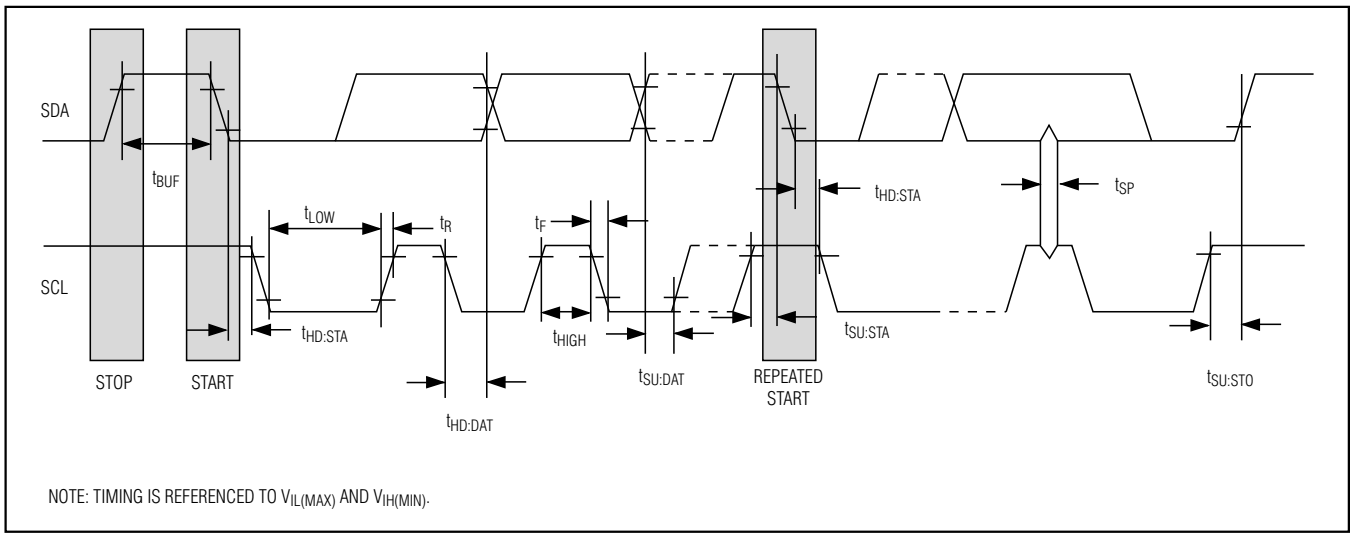
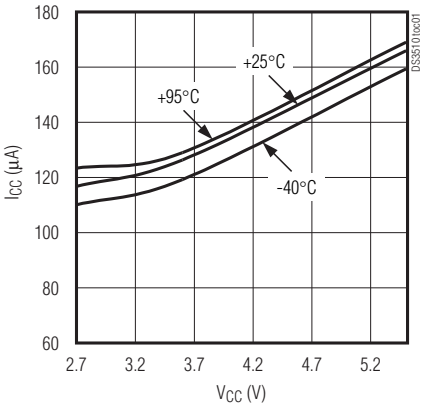


Figure 4. I²C Timing Diagram

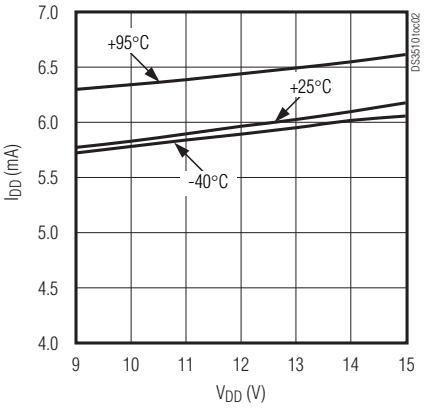
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

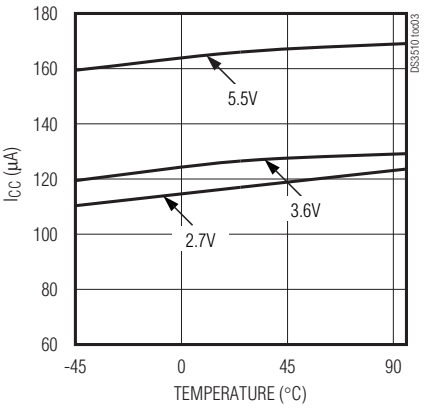
ICC vs. VCC



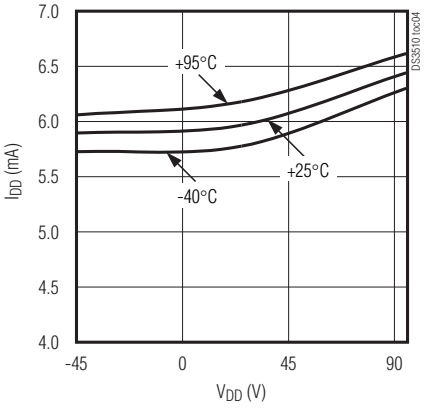
IDD vs. VDD



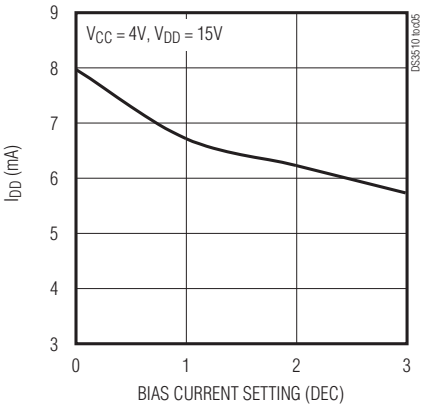
ICC vs. TEMPERATURE



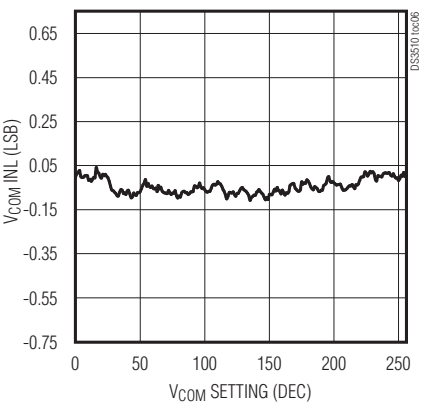
IDD vs. VDD



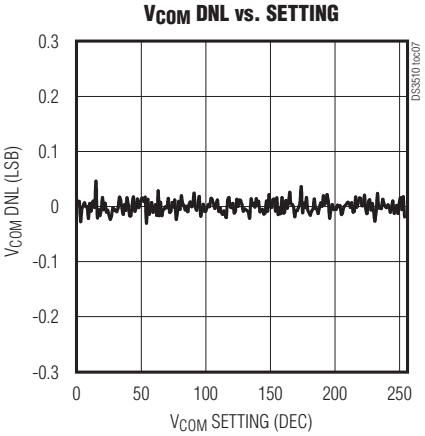
IDD vs. BIAS CURRENT SETTING



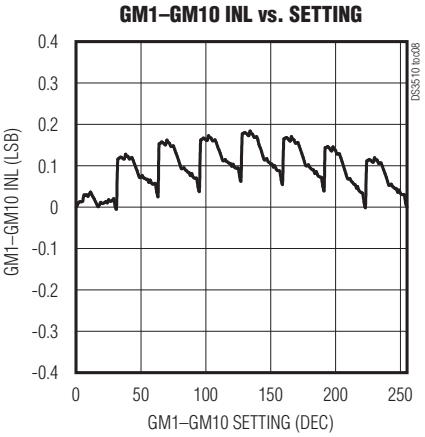
VCOM INL vs. SETTING



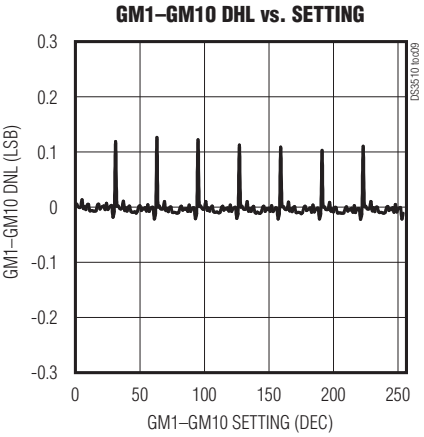
VCOM DNL vs. SETTING



GM1–GM10 INL vs. SETTING



GM1–GM10 DHL vs. SETTING

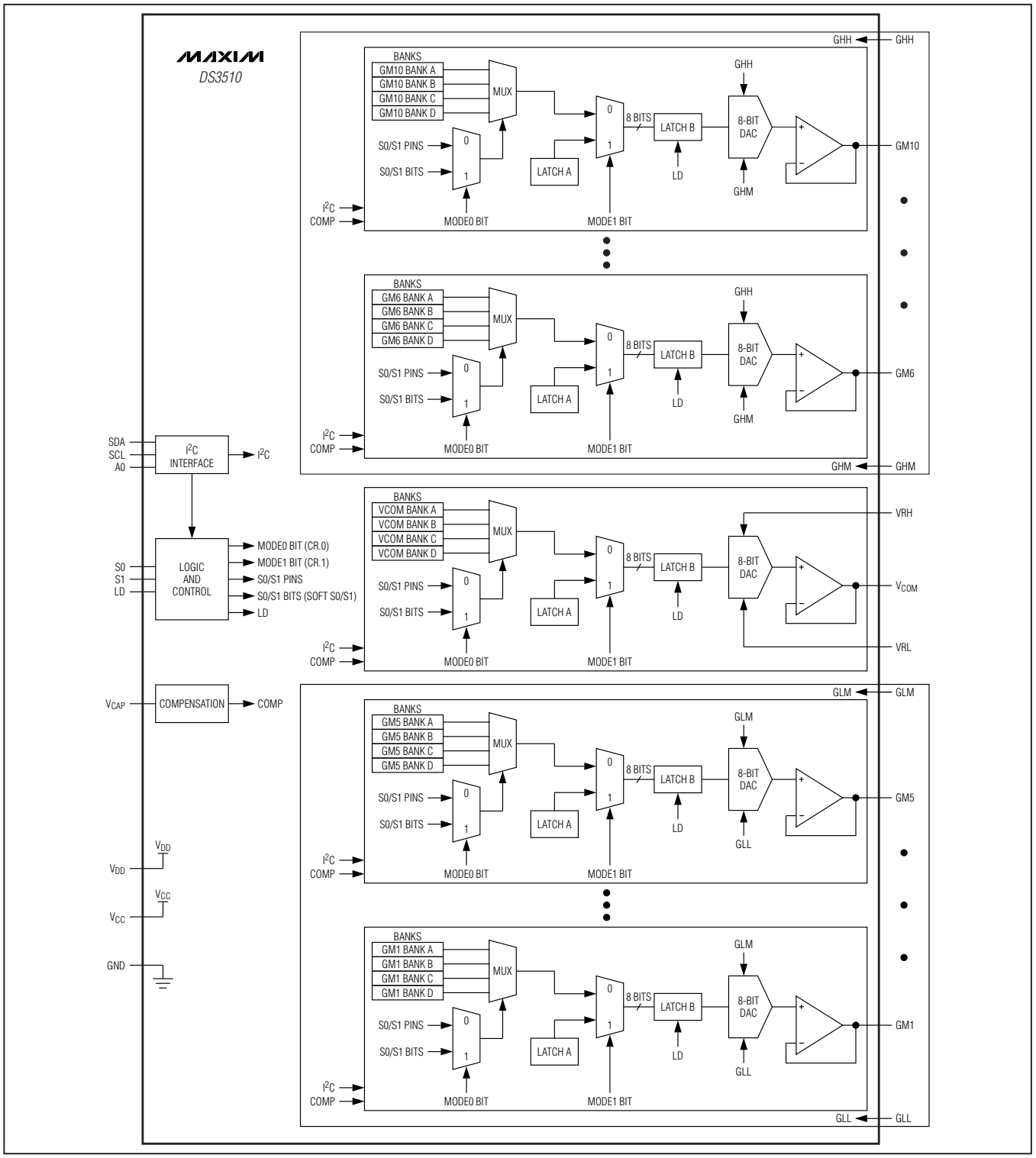


I²C Gamma and VCOM Buffer with EEPROM

Pin Description

NAME	PIN	TYPE	FUNCTION
V_{DD}	1, 19, 20, 24	Power	Analog Supply (9.0V to 15.5V)
GND	2, 38, 40, 42, 43	Power	Ground
LD	3	Input	Latch Data Input. When LD is low, Latch B retains existing data (acts as a latch). When LD is high, the input to Latch B data flows through to the output and updates the DACs asynchronously.
S1	4	Input	Select Inputs. When Control register [1,0] = 00, S0 and S1 pins are used to select DAC input data from EEPROM.
S0	5		
SCL	6	Input	I²C Serial Clock Input
SDA	7	Input/Output	I²C Serial Data Input/Output
A0	8	Input	Address Input. This pin determines I²C slave address of the DS3510.
V_{CC}	9	Power	Digital Supply (2.7V to 5.5V)
VRH, VRL	10, 11	Reference Input	V_{COM} Reference Inputs. High-voltage reference for V_{COM} DAC.
N.C.	12–17, 23, 36, 37, 44–48	—	No Connection
V_{CAP}	18	Input	Compensation Capacitor Input. Connect VCAP to GND through a 0.1µF capacitor.
GLL, GLM	21, 22	Reference Input	References for Low-Voltage Gamma DAC
GM1–GM5	25–29	Output	Low-Voltage Gamma Analog Outputs
V_{COM}	30	Output	V_{COM} Analog Output. This output requires a 1µF capacitor to GND.
GM6–GM10	31–35	Output	High-Voltage Gamma Analog Outputs
GHM, GHH	41, 39	Reference Input	References for High-Voltage Gamma DAC
GND	EP	—	Ground. Exposed pad. Connect to GND.

Block Diagram



I²C Gamma and VCOM Buffer with EEPROM

Detailed Description

The DS3510 operates in one of three modes which determine how the V_{COM} and gamma DACs are controlled/updated. The first two modes allow "banked" control of the 10 gamma channels and 1 V_{COM} channel. Depending on the mode, one of four banks (in EEPROM) can be selected using either the S0/S1 pins or using the SOFT S0/S1 bits in the Soft S0/S1 register. Once a bank is selected, the LD pin can then be used to simultaneously update each channel's DAC output. The third and final mode is not banked. It allows I²C control of each channel's Latch A register which is SRAM (volatile), allowing quick and unlimited updates. In this mode, the LD pin can also be used to simultaneously update each channel's DAC output. A detailed description of the three modes as well as additional features of the DS3510 follows.

Mode Selection

The DS3510 mode of operation is determined by 2 bits located in the Control register (60h), which is nonvolatile (NV) (EEPROM). In particular, the mode is determined by the MODE0 bit (CR.0) and the MODE1 bit (CR.1). Table 1 illustrates how the 2 control bits are used to select the operating mode. When shipped from the factory, the DS3510 is programmed with both MODE bits set to zero.

Table 1. DS3510 Operating Modes

MODE1 BIT (CR.1)	MODE0 BIT (CR.0)	MODE
0	0	S0/S1 Pin-Controlled Bank Updating (Factory Default)
0	1	S0/S1 Bit-Controlled Bank Updating
1	X	I²C Individual Channel Control

S0/S1 Pin-Controlled Bank Updating Mode

As shown in the block diagram, each channel contains 4 bytes of EEPROM, which are used to implement the "banking" functionality. Each "bank" contains unique DAC settings for each channel. When the DS3510 is configured in this operating mode, the desired bank is selected using the S0 and S1 pins as shown in Table 2 where 0 is ground and 1 is V_{CC}. For example, if S0 and S1 are both connected to ground, then the first bank (Bank A) is selected. Once a bank is selected, the timing of the DAC update depends on the state of LD pin. When LD is high, Latch B functions as a flow-through latch, so the amplifier will respond asynchronously to changes in the state of S0/S1 to meet the t_{SEL} specification. Conversely, when LD is low, Latch B functions as a latch, holding its previous data. A low-to-high transition on LD allows the Latch B input data to flow through and update the DACs with the EEPROM bank selected by S0/S1. A high-to-low transition on LD latches the selected DAC data into Latch B.

Table 2. DS3510 Bank Selection Table

S1	S0	VCOM CHANNEL	GAMMA CHANNELS
0	0	V_{COM} Bank A	GM1–10 Bank A
0	1	V_{COM} Bank B	GM1–10 Bank B
1	0	V_{COM} Bank C	GM1–10 Bank C
1	1	V_{COM} Bank D	GM1–10 Bank D

SOFT S0/S1 (Bit) Controlled Bank Updating Mode

This mode also features "banked" operation with the only difference being how the desired bank is selected. In particular, the bank is selected using the SOFT S0 (bit 0) and SOFT S1 (bit 1) bits contained in the Soft S0/S1 register (50h). The S0 and S1 pins are ignored in this mode. Table 2 illustrates the relationship between the bit settings and the selected bank. For example, if both bits, S0 and S1, are written to zero, then the first bank (Bank A) is selected. Once a bank is selected, the timing of the DAC update depends on the state of the LD pin. When LD is high, Latch B functions as a flow-through latch, so the amplifier will respond asynchronously to changes in the state of the S0/S1 bits. These are changed by an I²C write. Conversely, when LD is low, Latch B functions as a latch, holding its previous data. A low-to-high transition on LD allows the Latch B input data to flow through and update the DACs with the EEPROM bank selected by the S0/S1 bits. A high-to-low transition on LD latches the selected DAC data into Latch B.

Since the Soft S0/S1 register is SRAM, subsequent power-ups result in the SOFT S0 and SOFT S1 bits being cleared to 0 and, hence, powering up to Bank A.

I²C Individual Channel Control Mode

In this mode the I²C master writes directly to individual channel Latch A registers to update a single DAC (i.e., not banked). The Latch A registers are SRAM and not EEPROM. This allows an unlimited number of write cycles as well as quicker write times since t_W only applies to EEPROM writes. As shown in the *Memory Map*, the Latch A registers for each channel are accessed through memory addresses 00–0Ah. Then,

Table 3. DAC Voltage/Data Relationship for Selected Codes

SETTING (HEX)	V_{COM} OUTPUT VOLTAGE	GM1–GM5 OUTPUT VOLTAGE	GM6–GM10 OUTPUT VOLTAGE
00h	VRL	GLL	GHM + (255/256) x (GHH - GHM)
01h	VRL + (1/255) x (VRH - VRL)	GLL + (1/256) x (GLM - GLL)	GHM + (254/256) x (GHH - GHM)
02h	VRL + (2/255) x (VRH - VRL)	GLL + (2/256) x (GLM - GLL)	GHM + (253/256) x (GHH - GHM)
03h	VRL + (3/255) x (VRH - VRL)	GLL + (3/256) x (GLM - GLL)	GHM + (252/256) x (GHH - GHM)
0Fh	VRL + (15/255) x (VRH - VRL)	GLL + (15/256) x (GLM - GLL)	GHM + (240/256) x (GHH - GHM)
3Fh	VRL + (63/255) x (VRH - VRL)	GLL + (63/256) x (GLM - GLL)	GHM + (192/256) x (GHH - GHM)
7Fh	VRL + (127/255) x (VRH - VRL)	GLL + (127/256) x (GLM - GLL)	GHM + (128/256) x (GHH - GHM)
FDh	VRL + (253/255) x (VRH - VRL)	GLL + (253/256) x (GLM - GLL)	GHM + (2/256) x (GHH - GHM)
FEh	VRL + (254/255) x (VRH - VRL)	GLL + (254/256) x (GLM - GLL)	GHM + (1/256) x (GHH - GHM)
FFh	VRH	GLL + (255/256) x (GLM - GLL)	GHM

like the other modes, the LD pin determines when the DACs get updated. If the LD signal is high, Latch B is flow-through and the DAC is updated immediately. If LD is low, Latch B will be loaded from Latch A after a low-to-high transition on the LD pin. This latter method allows the timing of the DAC update to be controlled by an external signal pulse.

V_{COM}/Gamma Channel Outputs

As illustrated in the *Block Diagram*, the V_{COM} and gamma channel outputs are equivalent to an 8-bit digital potentiometer (DAC) with a buffered output. The V_{COM} channel's digital potentiometer is comprised of 255 equal resistive elements. The relationship between output voltage and DAC setting is illustrated in Table 3. Unlike the gamma channels, the V_{COM} channel is capable of outputting a range of voltages including both references (VRH and VRL). Each of the gamma channel digital potentiometers, on the other hand, are comprised of 256 equal resistive elements. The extra resistive element prohibits one of the rails from being reached. In particular, gamma channel outputs GM1–GM5 can span from (and including) GLL to 1 LSB away from GLM. Likewise, gamma channel outputs GM6–GM10 span from (and including) GHM to 1 LSB away from GHH. The relationship between output voltage and DAC setting for the gamma channels is also illustrated in Table 3.

Standby Mode

Standby mode (not to be confused with the three DS3510 operating modes) can be used to minimize current consumption. Standby mode is entered by setting the standby bit, which is the LSB of register 51h. The V_{COM} and gamma outputs are placed in a high-impedance state. Current drawn from the V_{DD} supply in this state is specified as I_{DDQ}.

The DS3510 continues to respond to I²C commands, and thus draws some current from V_{CC} when I²C activity is occurring. When the I²C interface is inactive, current drawn from the V_{CC} supply is specified as I_{CCQ}.

Thermal Shutdown

As a safety feature, the DS3510 goes into a thermal shutdown state if the junction temperature ever reaches or exceeds +150°C. In this state, the V_{COM} buffer is disabled (output goes high impedance) until the junction temperature falls below +150°C.

Slave Address Byte and Address Pin

The slave address byte consists of a 7-bit slave address plus a R/$\overline{W}$ bit (see Figure 5). The DS3510's slave address is determined by the state of the A0 pin. This pin allows up to two devices to reside on the same I²C bus. Connecting A0 to GND results in a 0 in the corresponding bit position in the slave address. Conversely, connecting A0 to V_{CC} results in a 1 in the corresponding bit position. For example, the DS3510's slave address byte is C0h when A0 is grounded. I²C communication is described in detail in the *I²C Serial Interface Description* section.

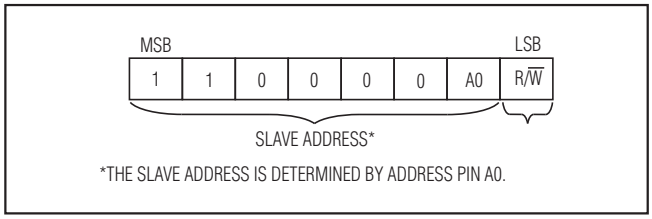


Figure 5. DS3510 Slave Address Byte

I²C Gamma and VCOM Buffer with EEPROM

Memory Organization

Memory Description

The list of registers/memory contained in the DS3510 is shown in the *Memory Map*. Also shown for each of the registers is the memory type and accessibility, as well as the power-up default values for volatile locations and factory-programmed defaults for the NV locations. Detailed register descriptions for the registers shown in **bold** follow in the *Detailed Register Descriptions* section. Furthermore, additional information regarding reading and writing the memory is located in the *I²C Serial Interface Description* section.

Memory Map

NAME	ADDR (HEX)	DESCRIPTION	MEMORY TYPE	I²C ACCESS	DEFAULT (HEX)
V_{COM} Latch A	00	Data for I²C Control of V_{COM}	Volatile	R/W	00
GM1 Latch A	01	Data for I²C Control of GM1	Volatile	R/W	00
GM2 Latch A	02	Data for I²C Control of GM2	Volatile	R/W	00
GM3 Latch A	03	Data for I²C Control of GM3	Volatile	R/W	00
GM4 Latch A	04	Data for I²C Control of GM4	Volatile	R/W	00
GM5 Latch A	05	Data for I²C Control of GM5	Volatile	R/W	00
GM6 Latch A	06	Data for I²C Control of GM6	Volatile	R/W	00
GM7 Latch A	07	Data for I²C Control of GM7	Volatile	R/W	00
GM8 Latch A	08	Data for I²C Control of GM8	Volatile	R/W	00
GM9 Latch A	09	Data for I²C Control of GM9	Volatile	R/W	00
GM10 Latch A	0A	Data for I²C Control of GM10	Volatile	R/W	00
Reserved	0B–0F	Reserved	—	—	—
V_{COM} Bank A–D	10–13	V_{COM} EEPROM Data (4 Bytes)	NV	R/W	80
GM1 Bank A–D	14–17	GM1 EEPROM Data (4 Bytes)	NV	R/W	80
GM2 Bank A–D	18–1B	GM2 EEPROM Data (4 Bytes)	NV	R/W	80
GM3 Bank A–D	1C–1F	GM3 EEPROM Data (4 Bytes)	NV	R/W	80
GM4 Bank A–D	20–23	GM4 EEPROM Data (4 Bytes)	NV	R/W	80
GM5 Bank A–D	24–27	GM5 EEPROM Data (4 Bytes)	NV	R/W	80
GM6 Bank A–D	28–2B	GM6 EEPROM Data (4 Bytes)	NV	R/W	80
GM7 Bank A–D	2C–2F	GM7 EEPROM Data (4 Bytes)	NV	R/W	80
GM8 Bank A–D	30–33	GM8 EEPROM Data (4 Bytes)	NV	R/W	80
GM9 Bank A–D	34–37	GM9 EEPROM Data (4 Bytes)	NV	R/W	80
GM10 Bank A–D	38–3B	GM10 EEPROM Data (4 Bytes)	NV	R/W	80
Reserved	3C–4F	Reserved	—	—	—
Soft S0/S1	50	Software Bank Select Bits	Volatile	R/W	00
Standby	51	Standby (xxxxxxx, Standby)	Volatile	R/W	00
Reserved	52–56	Reserved	—	—	—
Status	57	Status Bits (LD, xxxxx, S1, S0)	Status	R	N/A
Reserved	58–5F	Reserved	—	—	—
Control Register (CR)	60	Control Register	NV	R/W	10
Reserved	61–FF	Reserved	—	—	—

Detailed Register Descriptions

SOFT S0/S1 50h: SOFT S1/S0 Bits

FACTORY DEFAULT 00h

MEMORY TYPE Volatile

50h	x	x	x	x	x	x	SOFT S1	SOFT S0
	bit7							bit0

bit7:2	Reserved
bit1, bit0	These bits are used when in SOFT S0/S1 (bit) Controlled Bank Updating Mode (MODE1 = 0, MODE0 = 1) SOFT S1, SOFT S0: 00 = Selects V_{COM} and GM1–GM10 Bank A 01 = Selects V_{COM} and GM1–GM10 Bank B 10 = Selects V_{COM} and GM1–GM10 Bank C 11 = Selects V_{COM} and GM1–GM10 Bank D

STANDBY 51h: Standby Mode Enable

FACTORY DEFAULT 00h

MEMORY TYPE Volatile

51h	x	x	x	x	x	x	x	Standby
	bit7							bit0

bit7:1	Reserved
bit0	Standby: 0 = Standby Mode Disabled 1 = Standby Mode Enabled

STATUS 57h: Real-Time Indicator of Logic State on LD, S1, and S0 Pins

FACTORY DEFAULT —

MEMORY TYPE Read Only

57h	LD	x	x	x	x	x	S1	S0
	bit7							bit0

I²C Gamma and V_{COM} Buffer with EEPROM

CONTROL REGISTER 60h: Control Register (CR)

FACTORY DEFAULT 10h

MEMORY TYPE NV

60h	x	x	BIAS1	BIAS0	x	x	MODE1	MODE0
	bit7							bit0

bit7:6	Reserved
bit5:4	V_{COM} and Gamma Bias Current Control Bits: 00 = 150% 01 = 100% (default) 10 = 80% 11 = 60%
bits3:2	Reserved
bits1:0	DS3510 Mode: 00 = S0/S1 Pins are Used to Select the Desired Bank (A–D) (Default) 01 = Soft S0/S1 (Bits) Are Used to Select the Desired Bank (A–D) 1X = Latch A Is Used to Control the DACs

I²C Serial Interface Description

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. (See Figure 4 and *I²C Electrical Characteristics* for additional information.)

Master device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave devices: Slave devices send and receive data at the master's request.

Bus idle or not busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition.

STOP condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition.

Repeated START condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition.

Bit write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An Acknowledge (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a 0 during the 9th bit. A device performs a NACK by transmitting a 1 during the 9th bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or indicates that the device is not receiving data.

Byte write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.

Byte read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition above, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a start condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The DS3510's slave address is determined by the state of the A0 address pin as shown in Figure 5. An address pin connected to GND results in a 0 in the corresponding bit position in the slave address. Conversely, an address pin connected to V_{CC} results in a 1 in the corresponding bit position.

When the R/$\overline{W}$ bit is 0 (such as in C0h), the master is indicating it will write data to the slave. If R/$\overline{W}$ is set to a 1, (C1h in this case), the master is indicating it wants to read from the slave.

If an incorrect (non-matching) slave address is written, the DS3510 will assume the master is communicating with another I²C device and ignore the communication until the next start condition is sent.

Memory address: During an I²C write operation to the DS3510, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

Writing a single byte to a slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte write operations.

When writing to the DS3510 (and if LD = 1), the DAC will adjust to the new setting once it has acknowledged the new data that is being written, and the EEPROM (used to make the setting nonvolatile) will be written following the STOP condition at the end of the write command.

Writing multiple bytes to a slave: To write multiple bytes to a slave in one transaction, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The DS3510 is capable of writing 1 to 8 bytes (1 page or row) in a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). The first page begins at address 00h and subsequent pages begin at multiples of 8 (08h, 10h, 18h, etc). Attempts to write to additional pages of memory without sending a STOP condition between pages results in the address counter wrapping around to the beginning of the present row. To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM-write time to elapse. Then the master can generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge polling: Any time a EEPROM byte is written, the DS3510 requires the EEPROM write time (t_W) after the STOP condition to write the contents of the byte to EEPROM. During the EEPROM write time, the device will not acknowledge its slave address because it is busy. It is possible to take advantage of this phenomenon by repeatedly addressing the DS3510, which allows communication to continue as soon as the DS3510 is ready. The alternative to acknowledge polling is to wait for a maximum period of t_W to elapse before attempting to access the device.

I²C Gamma and VCOM Buffer with EEPROM

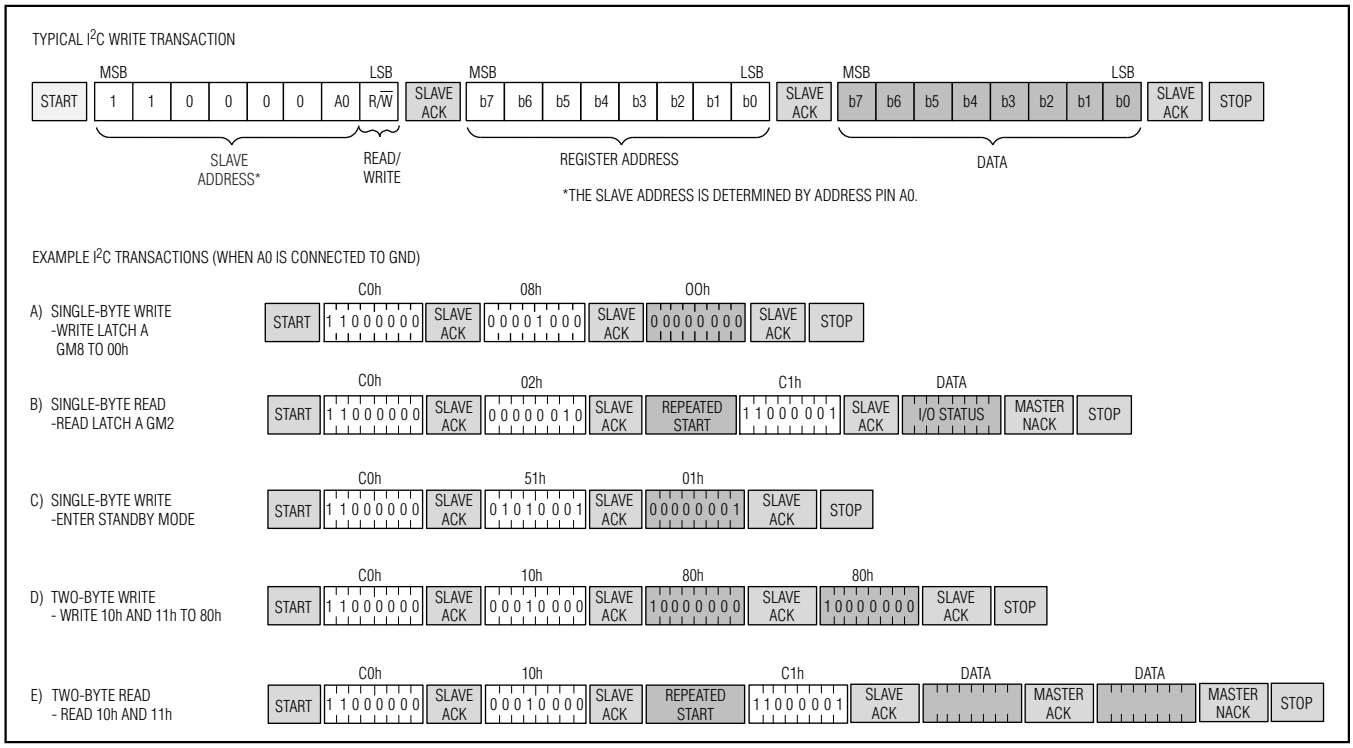


Figure 6. I²C Communication Examples

EEPROM write cycles: The DS3510's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature (hot) as well as at room temperature.

Reading a single byte from a slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location.

Manipulating the address counter for reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. Recall that the master must NACK the last byte to inform the slave that no additional bytes will be read.

See Figure 6 for I²C communication examples.

Reading multiple bytes from a slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte, it must NACK to indicate the end of the transfer and generates a STOP condition.

I²C Gamma and VCOM Buffer with EEPROM

Applications Information

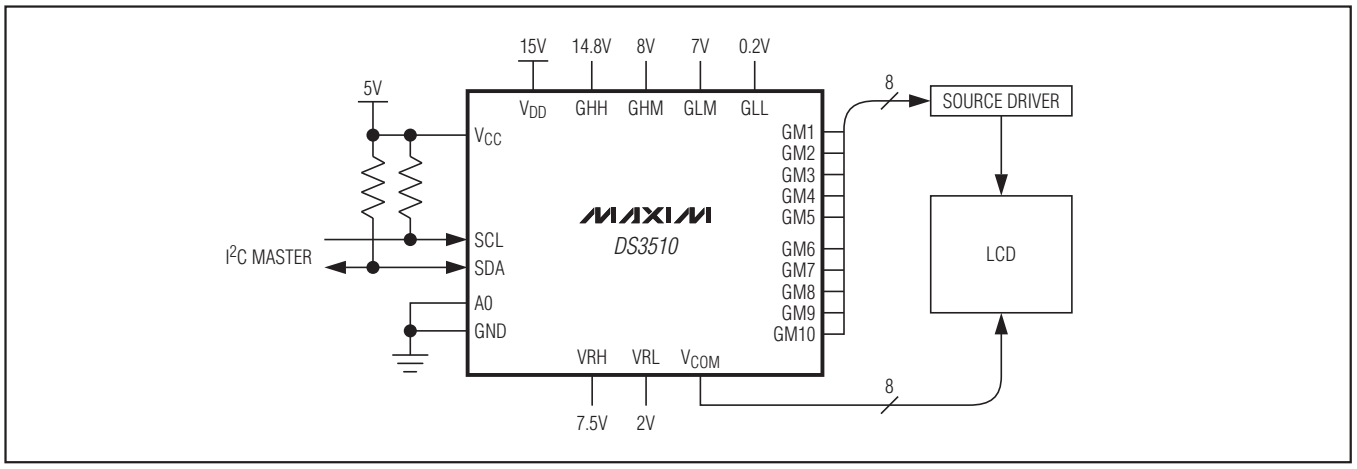
Power-Supply Decoupling

To achieve the best results when using the DS3510, decouple all the power-supply pins (V_{CC} and V_{DD}) with a 0.01µF or 0.1µF capacitor. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

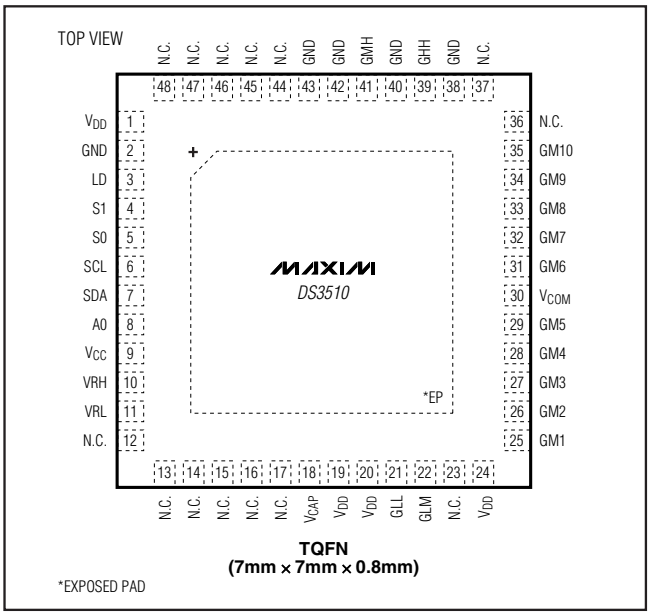
SDA and SCL Pullup Resistors

SDA is an I/O with an open-collector output that requires a pullup resistor to realize high-logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I²C Electrical Characteristics* are within specification. A typical value for the pullup resistors is 4.7kΩ.

Typical Operating Circuit



Pin Configuration



Package Information

(For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN-EP	T4877+6	**21-0144**

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