



# CMOS OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE, 3-STATE OUT- PUTS, 5 VOLT TOLERANT I/O

**IDT74LVCC3245A**

## FEATURES:

- 0.5 MICRON CMOS Technology
- $V_{CCA} = 2.3V$  to  $3.6V$
- $V_{CCB} = 3V$  to  $5.5V$
- CMOS power levels ( $0.4\mu W$  typ. static)
- Rail-to-rail output swing for increased noise margin
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SOIC, SSOP, QSOP, and TSSOP packages

## DRIVE FEATURES:

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

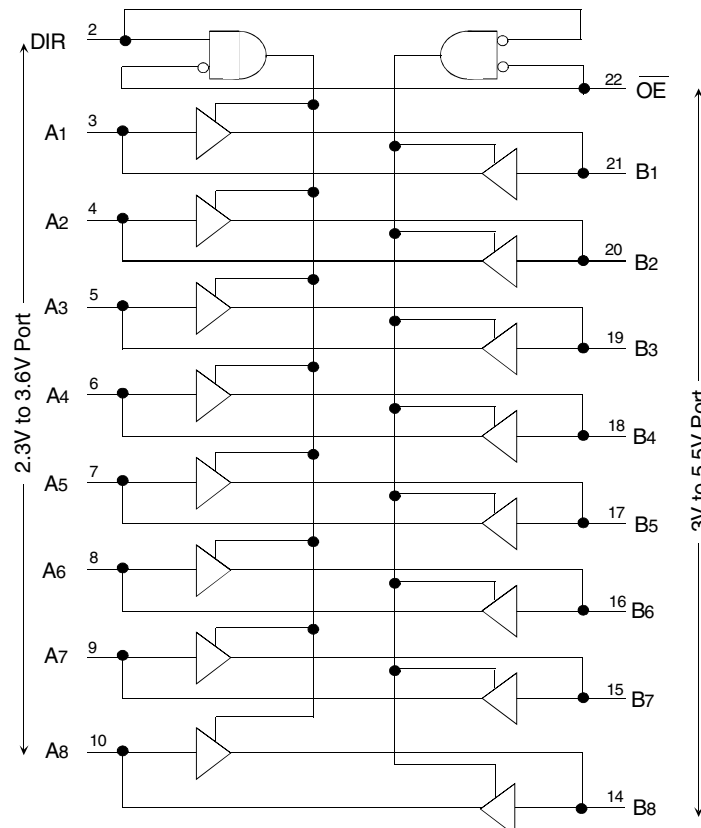
## DESCRIPTION:

The LVCC3245A is manufactured using advanced dual metal CMOS technology. This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track  $V_{CCB}$ , which accepts voltages from 3V to 5.5V, and the A port is designed to track  $V_{CCA}$ , which operates at 2.3V to 3.6V. This allows for translation from a 3.3V to a 5V system environment and vice-versa, or from a 2.5V to a 3.3V system environment, and vice-versa.

This LVCC3245A is ideal for asynchronous communication between two data buses (A and B). The device transmits data from A to B or from B to A, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

The LVCC3245A has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

## FUNCTIONAL BLOCK DIAGRAM

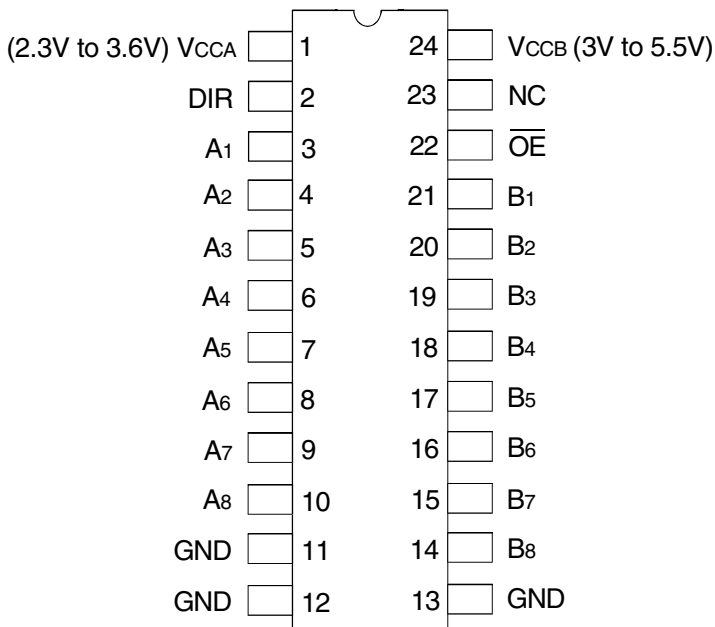


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

INDUSTRIAL TEMPERATURE RANGE

JULY 2000

## PIN CONFIGURATION



SOIC/ SSOP/ QSOP/ TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS FOR V<sub>CCB</sub> OR V<sub>CCB</sub>(<sup>1</sup>)

Symbol	Description	Max	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +6	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

**NOTE:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	11	pF

**NOTE:**

- As applicable to the device type.

## PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
DIR	Direction Control Input
A <sub>x</sub>	Port A Inputs or 3-State Outputs
B <sub>x</sub>	Port B Inputs or 3-State Outputs
NC	No Internal Connection

## FUNCTION TABLE<sup>(1)</sup>

Inputs		Outputs
$\overline{OE}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z state

**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT)

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CCA} = 2.3\text{V}$  to  $3.6\text{V}^{(1)}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{OB} \leq 0.1\text{V}$ $V_{OB} \geq V_{CCB} - 0.1\text{V}$	$V_{CCA} = 2.3\text{V}$ , $V_{CCB} = 3\text{V}$	1.7	—	—	V
			$V_{CCA} = 2.7\text{V}$ to $3.6\text{V}$	2	—	—	
$V_{IL}$	Input LOW Voltage Level		$V_{CCA} = 2.3\text{V}$ , $V_{CCB} = 3\text{V}$	—	—	0.7	V
			$V_{CCA} = 2.7\text{V}$ to $3.6\text{V}$	—	—	0.8	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CCA} = 3.6\text{V}$	$V_I = 0$ to $5.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CCA} = 3.6\text{V}$	$V_O = V_{CCA}$ or GND	—	—	$\pm 5$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CCA} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_H$	Input Hysteresis	$V_{CCA} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CCA} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or $V_{CC}$	—	—	50	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CCA} - 0.6$ , other inputs at $V_{CCA}$ or GND		—	—	500	$\mu\text{A}$

### NOTES:

- $V_{CCB} = 3\text{V}$  to  $5.5\text{V}$ .
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This applies in the disabled state only.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (B PORT)

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CCB} = 3\text{V}$  to  $5.5\text{V}^{(1)}$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage Level	$V_{OA} \leq 0.1\text{V}$ $V_{OA} \geq V_{CCA} - 0.1\text{V}$	$V_{CCB} = 3\text{V}$ to $3.6\text{V}$	2	—	—	V
			$V_{CCB} = 5.5\text{V}$	3.85	—	—	
$V_{IL}$	Input LOW Voltage Level		$V_{CCB} = 3\text{V}$ to $3.6\text{V}$	—	—	0.8	V
			$V_{CCB} = 5.5\text{V}$	—	—	1.65	
$I_{IH}$ $I_{IL}$	Input Leakage Current	$V_{CCB} = 3.6\text{V}$	$V_I = 0$ to $5.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZH}$ $I_{OZL}$	High Impedance Output Current (3-State Output pins)	$V_{CCB} = 3.6\text{V}$	$V_O = V_{CCB}$ or GND	—	—	$\pm 5$	$\mu\text{A}$
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CCB} = 0\text{V}$ , $V_{IN}$ or $V_O \leq 5.5\text{V}$		—	—	$\pm 50$	$\mu\text{A}$
$V_H$	Input Hysteresis	$V_{CCB} = 3.3\text{V}$		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CCB} = 3.6\text{V}$	$V_{IN} = \text{GND}$ or $V_{CC}$	—	—	50	$\mu\text{A}$
		$V_{CCB} = 5.5\text{V}$		—	—	80	
$\Delta I_{CC}$	Quiescent Power Supply Current Variation	One input at $V_{CCB} - 2.1$ other inputs at $V_{CCB}$ or GND		—	—	1.5	mA

### NOTES:

- $V_{CCA} = 2.3\text{V}$  to  $3.6\text{V}$ .
- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS,  $V_{CCA} = 2.3V$  TO  $3.6V$  (A PORT)

Symbol	Parameter	Test Conditions <sup>(1)</sup>			Min.	Max.	Unit
VOHA	Output HIGH Voltage (B port to A port)	$V_{CCA} = 3V$	$V_{CCB} = 3V$	$I_{OH} = -0.1mA$	2.9	—	V
		$V_{CCA} = 2.3V$	$V_{CCB} = 3V$	$I_{OH} = -8mA$	2	—	
		$V_{CCA} = 2.7V$	$V_{CCB} = 3V$	$I_{OH} = -12mA$	2.2	—	
		$V_{CCA} = 3V$	$V_{CCB} = 3V$		2.4	—	
		$V_{CCA} = 3V$	$V_{CCB} = 3V$	$I_{OH} = -24mA$	2.2	—	
		$V_{CCA} = 2.7V$	$V_{CCB} = 4.5V$		2	—	
VOLA	Output LOW Voltage (B port to A port)	$V_{CCA} = 3V$	$V_{CCB} = 3V$	$I_{OL} = 0.1mA$	—	0.1	V
		$V_{CCA} = 2.3V$	$V_{CCB} = 3V$	$I_{OL} = 8mA$	—	0.6	
		$V_{CCA} = 2.7V$	$V_{CCB} = 3V$	$I_{OL} = 12mA$	—	0.5	
		$V_{CCA} = 3V$	$V_{CCB} = 3V$	$I_{OL} = 24mA$	—	0.5	
		$V_{CCA} = 2.7V$	$V_{CCB} = 4.5V$		—	0.5	

NOTE:  
1.  $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{CC}$  range.  
 $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $V_{CCB} = 3V$  to  $5.5V$ .

OUTPUT DRIVE CHARACTERISTICS,  $V_{CCB} = 3V$  TO  $5.5V$  (B PORT)

Symbol	Parameter	Test Conditions <sup>(1)</sup>			Min.	Max.	Unit
VOHB	Output HIGH Voltage (A port to B port)	$V_{CCB} = 3V$	$V_{CCA} = 3V$	$I_{OH} = -0.1mA$	2.9	—	V
		$V_{CCB} = 3V$	$V_{CCA} = 2.3V$	$I_{OH} = -12mA$	2.4	—	
		$V_{CCB} = 3V$	$V_{CCA} = 2.7V$		2.4	—	
		$V_{CCB} = 3V$	$V_{CCA} = 3V$	$I_{OH} = -24mA$	2.2	—	
		$V_{CCB} = 4.5V$	$V_{CCA} = 2.7V$		3.2	—	
VOLB	Output LOW Voltage (A port to B port)	$V_{CCB} = 3V$	$V_{CCA} = 3V$	$I_{OL} = 0.1mA$	—	0.1	V
		$V_{CCB} = 3V$	$V_{CCA} = 2.3V$	$I_{OL} = 12mA$	—	0.4	
		$V_{CCB} = 3V$	$V_{CCA} = 3V$	$I_{OL} = 24mA$	—	0.5	
		$V_{CCB} = 4.5V$	$V_{CCA} = 3V$		—	0.5	

NOTE:  
1.  $V_{IH}$  and  $V_{IL}$  must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate  $V_{CC}$  range.  
 $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $V_{CCA} = 2.3V$  to  $3.6V$ .

OPERATING CHARACTERISTICS,  $T_A = 25^{\circ}C$

Symbol	Parameter	Test Conditions	$V_{CCA} = 3.3V, V_{CCB} = 5V$	Unit
			Typical	
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled A to B	$C_L = 0pF, f = 10Mhz$	38	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled B to A		36.5	

SWITCHING CHARACTERISTICS<sup>(1)</sup>

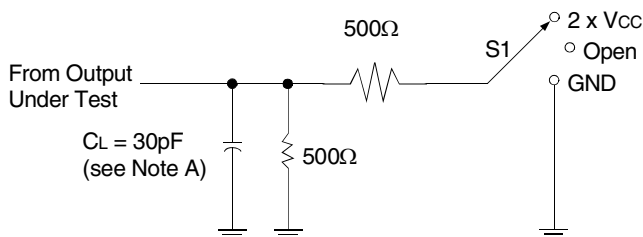
Symbol	Parameter	VCCA = 2.5V ± 0.2V		VCCA = 2.7V to 3.6V				Unit
		VCCB = 3.3V ± 0.3V		VCCB = 5V ± 0.5V		VCCB = 3.3V ± 0.3V		
		Min.	Max.	Min.	Max.	Min.	Max.	
tPHL	Propagation Delay	1	9.4	1	6	1	7.1	ns
tPLH	Ax to Bx	1	9.1	1	5.3	1	7.2	
tPHL	Propagation Delay	1	11.2	1	5.8	1	6.4	ns
tPLH	Bx to Ax	1	9.9	1	7	1	7.6	
tPZL	Output Enable Time	1	13	1	8.1	1	9.2	ns
tPLZ	$\overline{OE}$ to Bx	1	12.8	1	8.4	1	9.9	
tPZL	Output Enable Time	1	14.5	1	9.2	1	9.7	ns
tPLZ	$\overline{OE}$ to Ax	1	12.9	1	9.5	1	9.5	
tPLZ	Output Disable Time	1	7.1	1	5.5	1	6.6	ns
tPHZ	$\overline{OE}$ to Ax	1	6.9	1	7.8	1	6.9	
tPLZ	Output Disable Time	1	8.8	1	7.3	1	7.5	ns
tPHZ	$\overline{OE}$ to Bx	1	8.9	1	7	1	7.9	

NOTE:

1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.

## LOAD CIRCUIT AND VOLTAGE WAVEFORMS PARAMETER MEASUREMENT INFORMATION (A PORT)

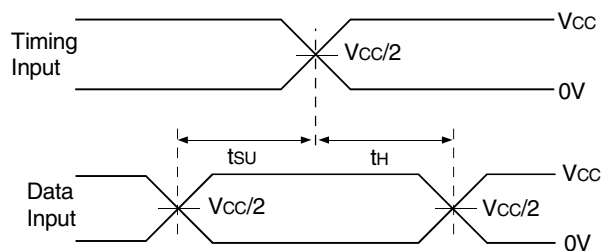
$$V_{CCA} = 2.5V \pm 0.2V \text{ and } V_{CCB} = 3.3V \pm 0.3V$$



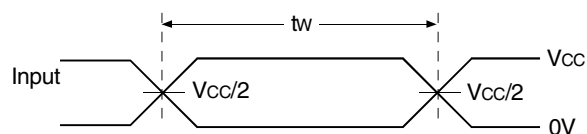
*Load Circuit*

### TEST CONDITIONS

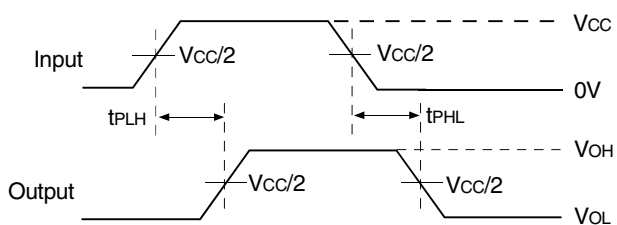
TEST	S1
$t_{PD}$	Open
$t_{PLZ}/t_{PZL}$	2 x $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



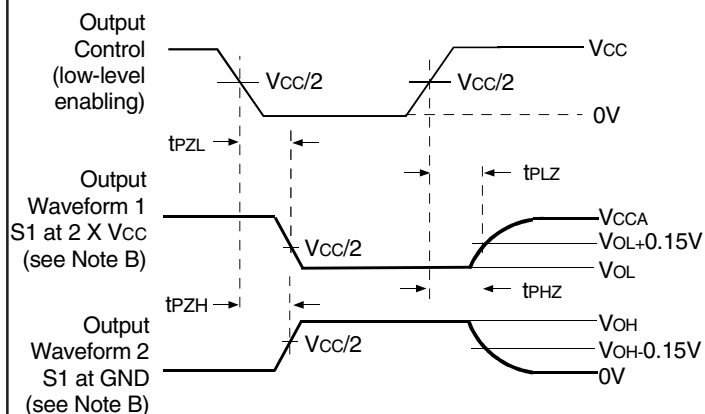
*Voltage Waveforms Setup and Hold Times*



*Voltage Waveforms Pulse Duration*



*Voltage Waveforms Propagation Delay Times*



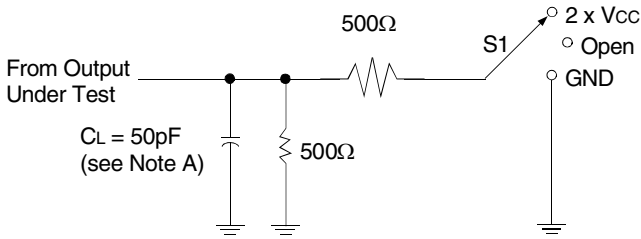
*Voltage Waveforms Enable and Disable Times*

#### NOTES:

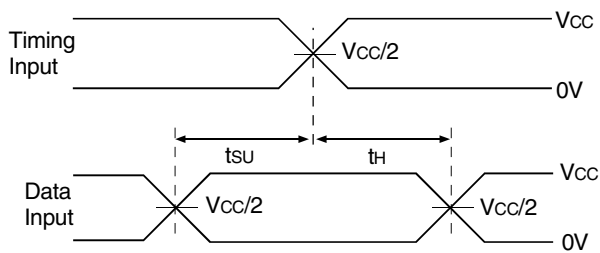
- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{MHz}$ ;  $Z_o = 50\Omega$ ;  $t_r \leq 2\text{ns}$ ;  $t_f \leq 2\text{ns}$ .
- The outputs are measured one at a time with one transition per measurement.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS  
PARAMETER MEASUREMENT INFORMATION (B PORT)

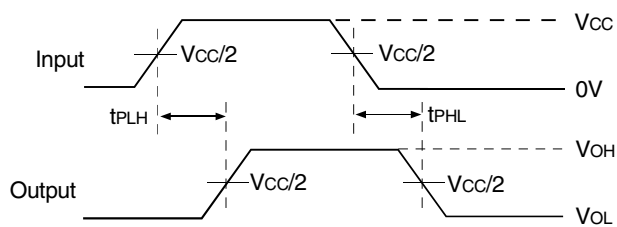
$V_{CCA} = 2.5V \pm 0.2V$  and  $V_{CCB} = 3.3V \pm 0.3V$



Load Circuit



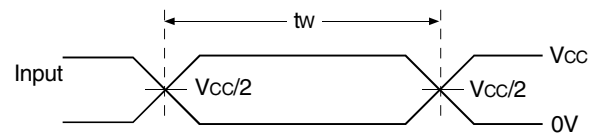
Voltage Waveforms Setup and Hold Times



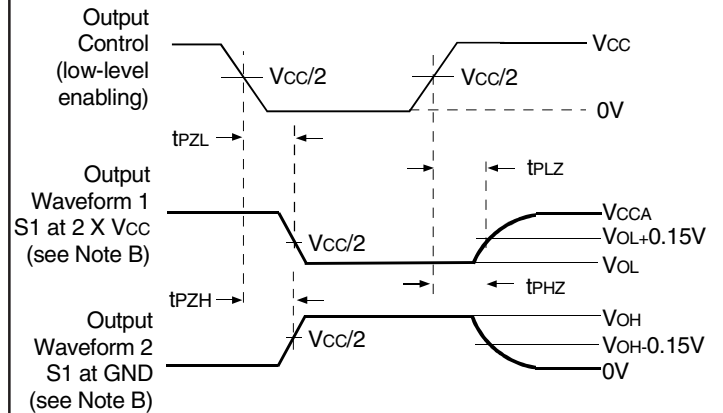
Voltage Waveforms Propagation Delay Times

TEST CONDITIONS

TEST	S1
$t_{PD}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PHL}$	GND



Voltage Waveforms Pulse Duration



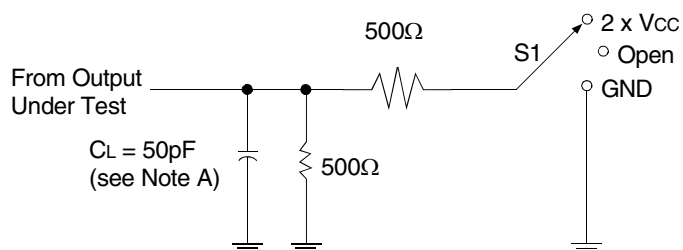
Voltage Waveforms Enable and Disable Times

NOTES:

- CL includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10MHz; Zo = 50Ω; tr  $\leq$  2ns; tr  $\leq$  2ns.
- The outputs are measured one at a time with one transition per measurement.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS  
PARAMETER MEASUREMENT INFORMATION (A PORT)

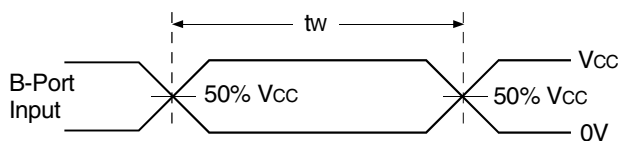
$V_{CCA} = 3.6V$  and  $V_{CCB} = 5.5V$



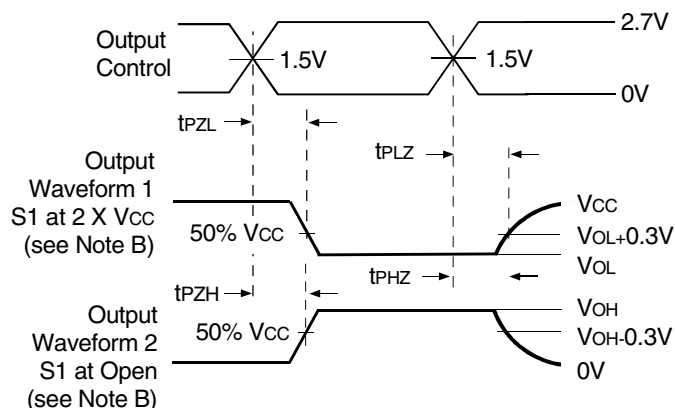
Load Circuit

TEST CONDITIONS

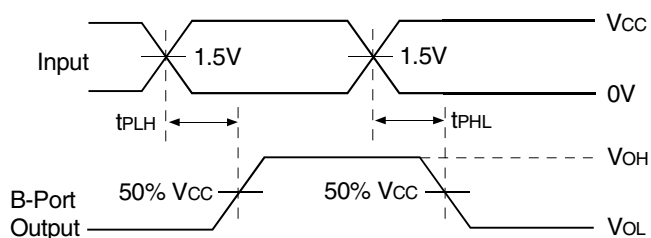
TEST	S1
$t_{PLH} / t_{PHL}$	Open
$t_{PLZ} / t_{PZL}$	2 x $V_{CC}$
$t_{PHZ} / t_{PZH}$	GND



Voltage Waveforms Pulse Duration



Voltage Waveforms Enable and Disable Times  
Low- and High-Level Enabling



Voltage Waveforms Propagation Delay Times  
Noninverting Outputs

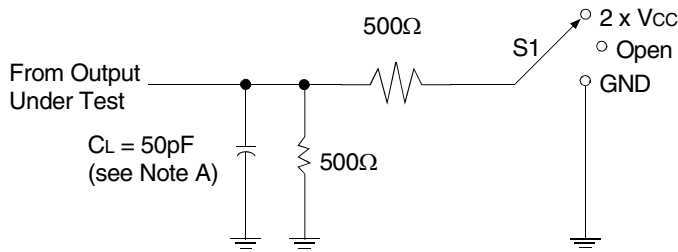
NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10MHz$ ;  $Z_o = 50\Omega$ ;  $t_f \leq 2.5ns$ ;  $t_r \leq 2.5ns$ .
- D. The outputs are measured one at a time with one transition per measurement.



LOAD CIRCUIT AND VOLTAGE WAVEFORMS  
PARAMETER MEASUREMENT INFORMATION (B PORT)

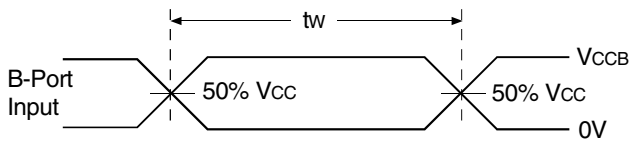
$V_{CCA} = 3.6V$  and  $V_{CCB} = 5.5V$



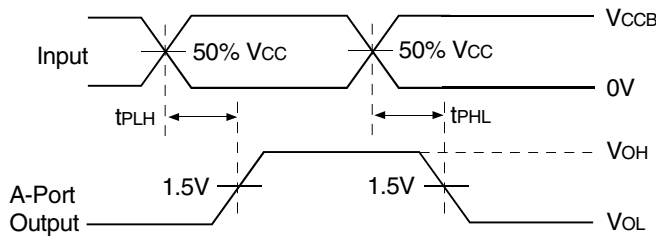
Load Circuit

TEST CONDITIONS

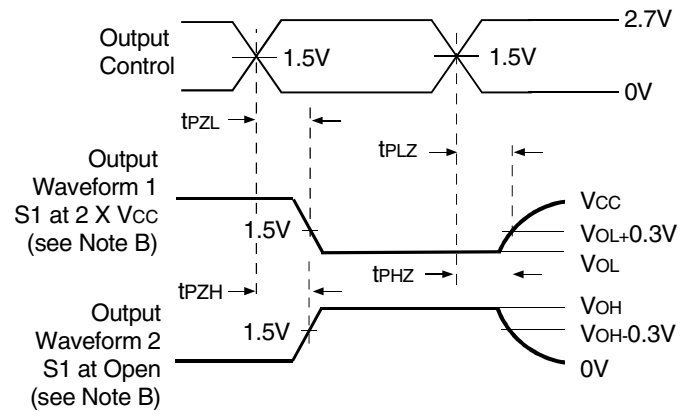
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 x $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times  
Noninverting Outputs



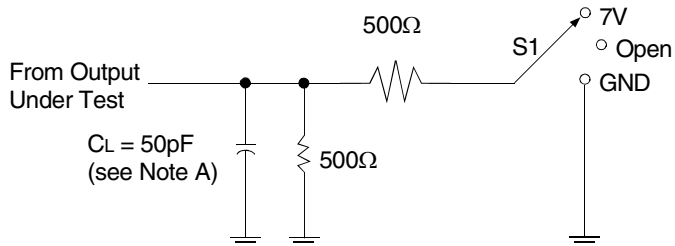
Voltage Waveforms Enable and Disable Times  
Low- and High-Level Enabling

NOTES:

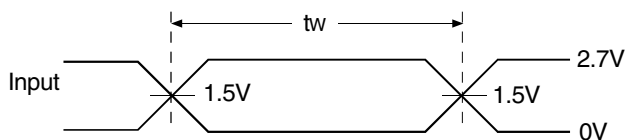
- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10MHz$ ;  $Z_o = 50\Omega$ ;  $t_r \leq 2.5ns$ ;  $t_f \leq 2.5ns$ .
- D. The outputs are measured one at a time with one transition per measurement.

LOAD CIRCUIT AND VOLTAGE WAVEFORMS  
PARAMETER MEASUREMENT INFORMATION (A AND B PORT)

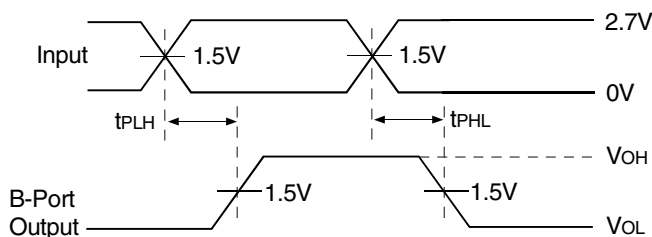
$V_{CCA} = \text{and } V_{CCB} = 3.6V$



Load Circuit



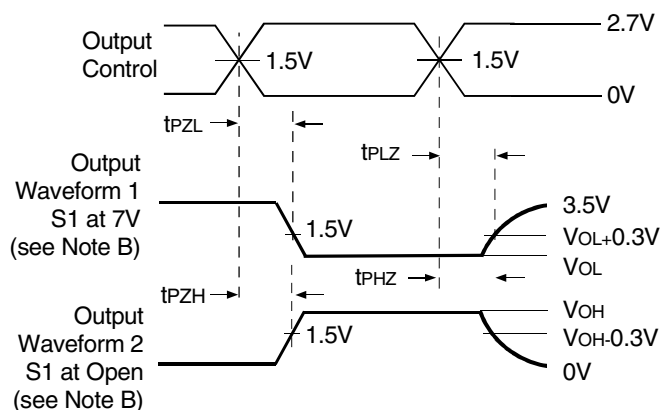
Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times  
Noninverting Outputs

TEST CONDITIONS

TEST	S1
$t_{PLH} / t_{PHL}$	Open
$t_{PLZ} / t_{PZL}$	7V
$t_{PHZ} / t_{PZH}$	GND



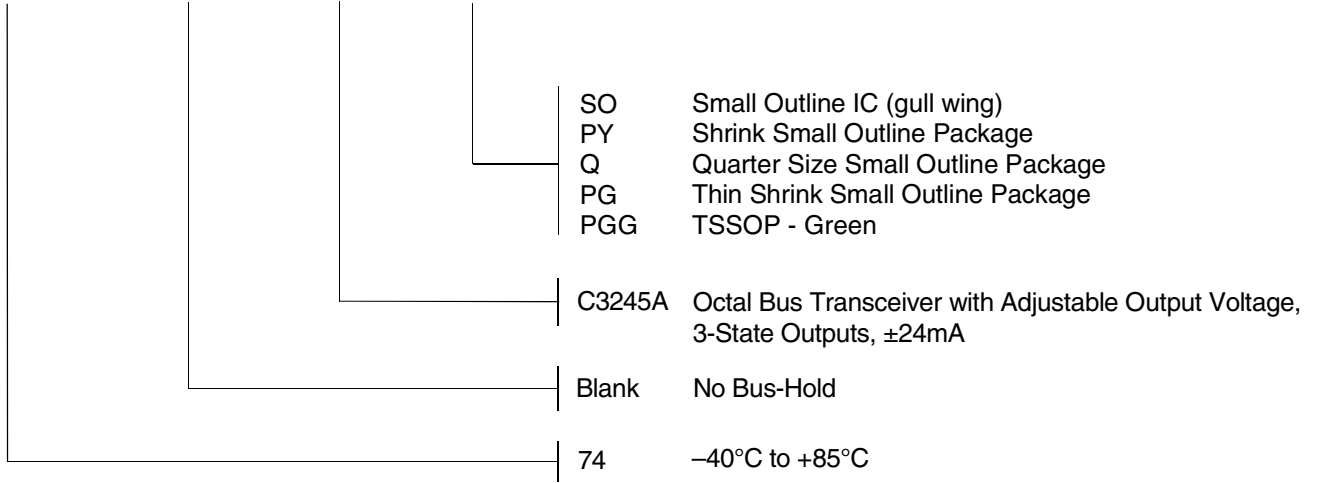
Voltage Waveforms Enable and Disable Times  
Low- and High-Level Enabling

NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{MHz}$ ;  $Z_o = 50\Omega$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

ORDERING INFORMATION

IDT XX LVC X XXXX XX  
Temp. Range Bus-Hold Device Type Package



**CORPORATE HEADQUARTERS**  
2975 Stender Way  
Santa Clara, CA 95054

**for SALES:**  
800-345-7015 or 408-727-6116  
fax: 408-492-8674  
www.idt.com

**for Tech Support:**  
logichelp@idt.com  
(408) 654-6459