November 2000

National Semiconductor

DS34LV87T
Enhanced CMOS Quad Differential Line Driver

General Description

The DS34LV87T is a high speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS34LV87T features low static I_{CC} of 100 µA max which makes it ideal for battery powered and power conscious applications. The TRI-STATE® enable, EN, allows the device to be disabled when the device is not in use to minimize power. The dual enable scheme allows for flexibility in turning devices on or off.

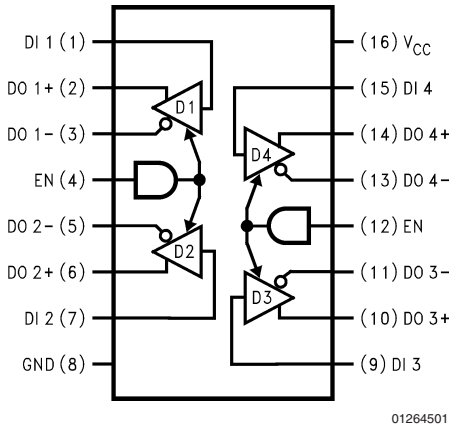
Protection diodes protect all the driver inputs against electrostatic discharge. The driver and enable inputs (DI and EN) are compatible with LVTTL and LVCMOS devices. Differential outputs have the same V_{OD} (≥2V) guarantee as the 5V version. The outputs have enhanced ESD Protection providing greater than 7 kV tolerance.

Features

- Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 recommendation
- Interoperable with existing 5V RS-422 networks
- Guaranteed V_{OD} of 2V min over operating conditions
- Balanced output crossover for low EMI (typical within 40 mV of 50% voltage level)
- Low power design (330 µW @ 3.3V static)
- ESD ≥ 7 kV on cable I/O pins (HBM)
- Industrial temperature range
- Guaranteed AC parameter:
  — Maximum driver skew: 2 ns
  — Maximum transition time: 10 ns
- Pin compatible with DS26C31
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS34LV87TM
See NS Package Number M16A

Truth Table

Enables	Input	Outputs	
EN	DI	DO+	DO−
L	X	Z	Z
H	H	H	L
H	L	L	H

L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7V
Enable Input Voltage (EN)	−0.5V to V_{CC} + 0.5V
Driver Input Voltage (D_I)	−0.5V to V_{CC} + 0.5V
Clamp Diode Current	±20 mA
DC Output Current, per pin	±150 mA
Driver Output Voltage	
(Power Off: DO+, DO−)	−0.5V to +7V
Maximum Package Power Dissipation @+25˚C	
M Package	1226 mW
Derate M Package	9.8 mW/˚C above +25˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range	
(Soldering, 4 sec.)	+260˚C
ESD Ratings	
(HBM, 1.5k, 100 pF)	
Driver Outputs	≥ 7 kV
Other Pins	≥ 2.5 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature Range (T_A)				
DS34LV87T	−40	25	+85	˚C
Input Rise and Fall Time			500	ns

Electrical Characteristics (Notes 2, 3)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Output Differential Voltage	R_L= ∞, (No Load)	DO+, DO−		3.3	4.0	V
V_{OD2}	Output Differential Voltage	R_L = 100Ω *Figure 1*		2	2.6		V
ΔV_{OD2}	Change in Magnitude of Output Differential Voltage			−400	7	400	mV
V_{OD3}	Output Differential Voltage	R_L = 3900Ω (V.11), *Figure 1* (Note 7)			3.2	3.5	V
V_{OC}	Common Mode Voltage	R_L = 100Ω *Figure 1*			1.5	2	V
ΔV_{OC}	Change in Magnitude of Common Mode Voltage			−400	6	400	mV
I_{OZ}	TRI-STATE Leakage Current	V_{OUT} = V_{CC} or GND Drivers Disabled			±0.5	±20	µA
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V V_{IN} = V_{CC} or GND (Note 4)		−40	−70	−150	mA
I_{OFF}	Output Leakage Current	V_{CC}= 0V, V_{OUT} = 3V			0.03	100	µA
		V_{CC} = 0V, V_{OUT} = −0.25V			−0.08	−100	µA
V_{IH}	High Level Input Voltage		DI, EN	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IN}= V_{CC}				10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND		−10			µA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA				−1.5	V
I_{CC}	Power Supply Current	No Load, V_{IN} (all) = V_{CC} or GND	V_{CC}			100	µA

Switching Characteristics (Notes 5, 6)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 50 pF (*Figures 2, 3*)	6	10.5	16	ns
t_{PLHD}	Differential Propagation Delay Low to High		6	11	16	ns
t_{SKD}	Differential Skew $\|t_{PHLD}-t_{PLHD}\|$			0.5	2.0	ns
t_{SK1}	Skew, Pin to Pin (same device)			1.0	2.0	ns
t_{SK2}	Skew, Part to Part (Note 8)			3.0	5.0	ns
t_{TLH}	Differential Transition Time Low to High (20% to 80%)			4.2	10	ns
t_{THL}	Differential Transition Time High to Low (80% to 20%)			4.7	10	ns
t_{PHZ}	Disable Time High to Z	(*Figures 4, 5*)		12	20	ns
t_{PLZ}	Disable Time Low to Z			9	20	ns
t_{PZH}	Enable Time Z to High			22	32	ns
t_{PZL}	Enable Time Z to Low			22	32	ns
f_{MAX}	Maximum Operating Frequency (Note 9)			32		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages V_{OD1}, V_{OD2}, V_{OD3}.

Note 3: All typical values are given for V_{CC}= 3.3V and T_A = +25˚C.

Note 4: Only one output shorted at a time. The output (true or complement) is configured High.

Note 5: f = 1 MHz, t_r and $t_f \leq$ 6 ns (10% to 90%).

Note 6: See TIA/EIA-422-B specifications for exact test conditions.

Note 7: This specification limit is for compliance with TIA/EIA-422-B and ITU-T V.11.

Note 8: Devices are at the same V_{CC} and within 5˚C within the operating temperature range.

Note 9: All channels switching, output duty cycle criteria is 40%/60% measured at 50%. This parameter is guaranteed by design and characterization.

Parameter Measurement Information

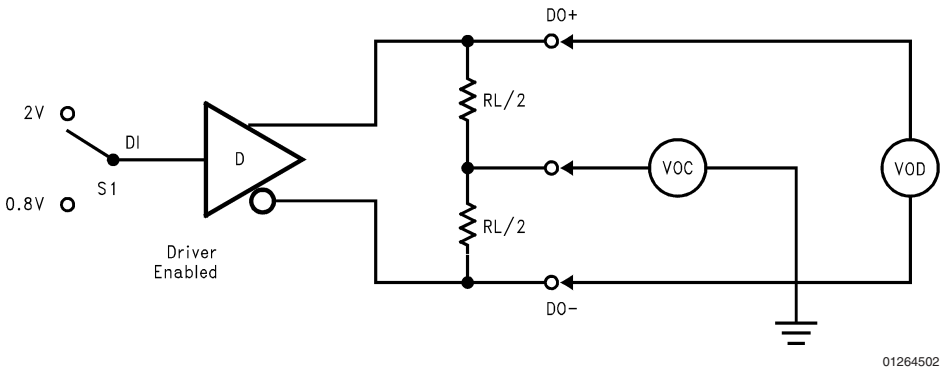


FIGURE 1. Differential Driver DC Test Circuit

Parameter Measurement Information (Continued)

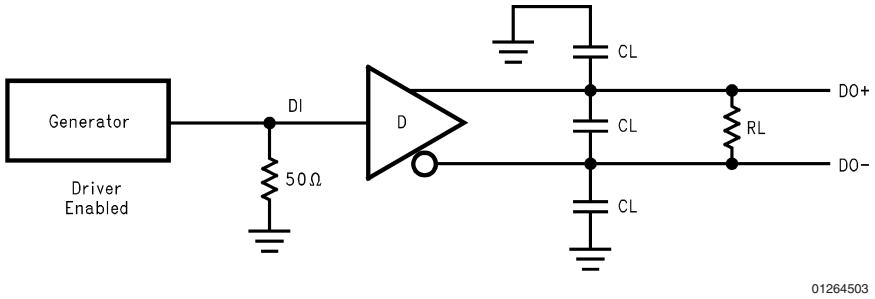


FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

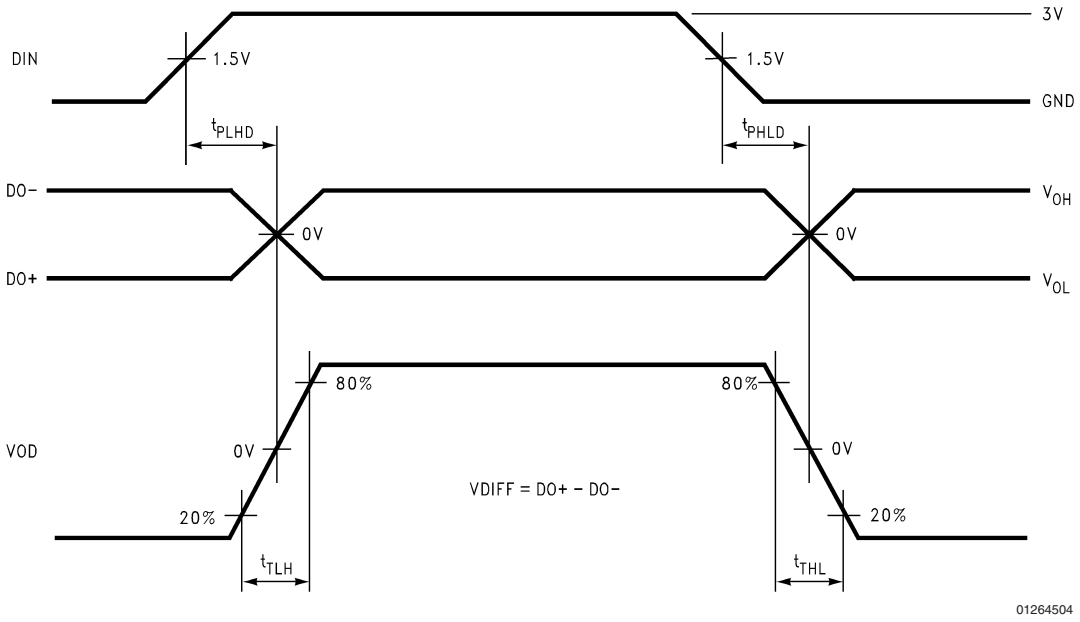


FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms

Note 10: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_o = 50Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note 11: C_L includes probe and fixture capacitance.

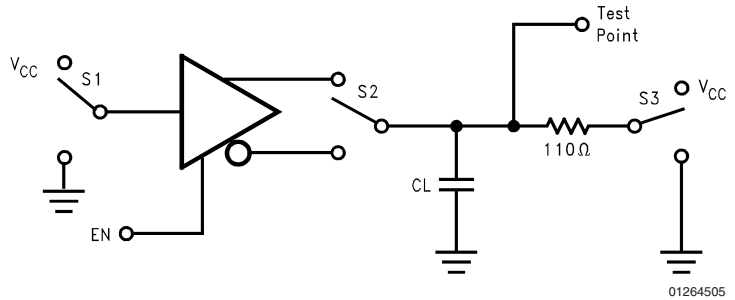


FIGURE 4. Driver Single-Ended TRI-STATE Test Circuit

Parameter Measurement Information (Continued)

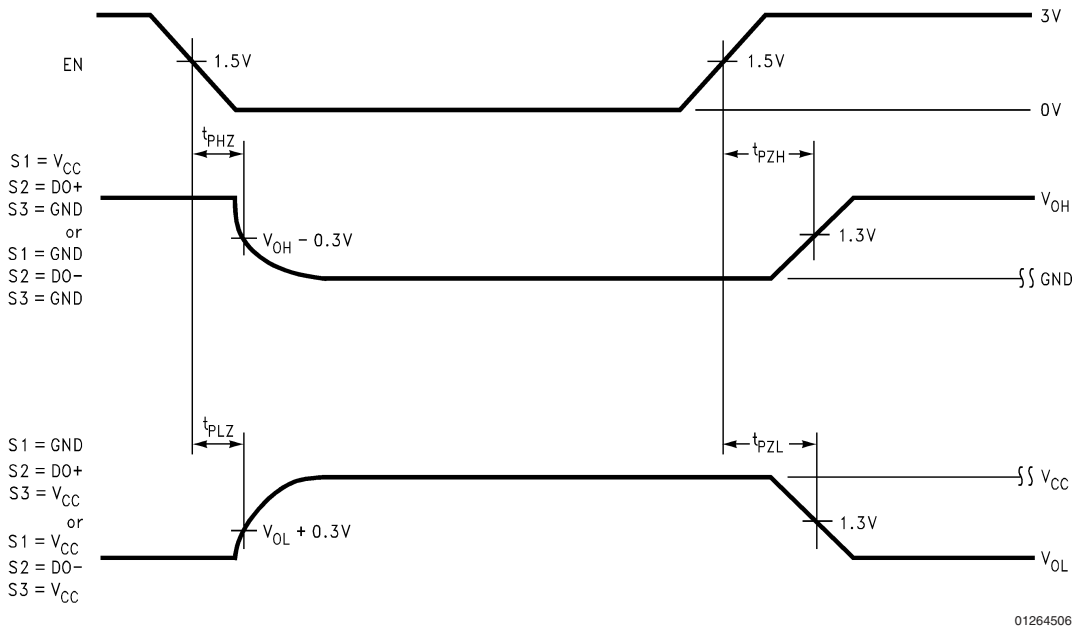


FIGURE 5. Driver Single-Ended TRI-STATE Waveforms

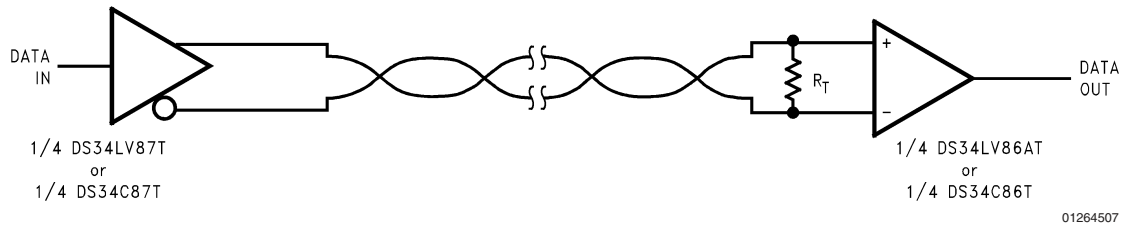
Typical Application Information

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

AN-214, AN-457, AN-805, AN-847, AN-903, AN-912, AN-916.

Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 µF in parallel with 0.01 µF at the power supply pin. A 10 µF or greater tantalum or electrolytic should be connected at the power entry point on the printed circuit board.



R_T is optional although highly recommended to reduce reflection

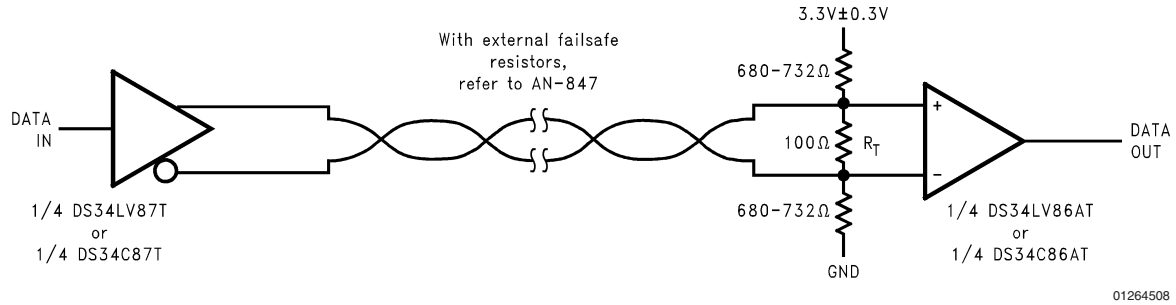


FIGURE 6. Typical Driver Connection

Typical Application Information (Continued)

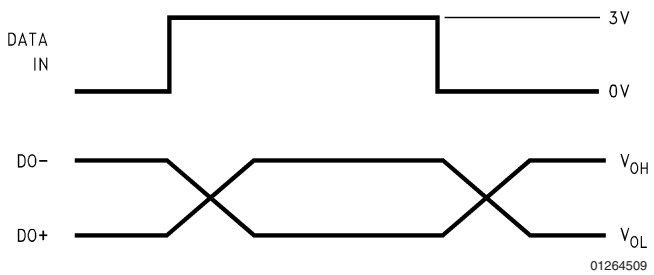
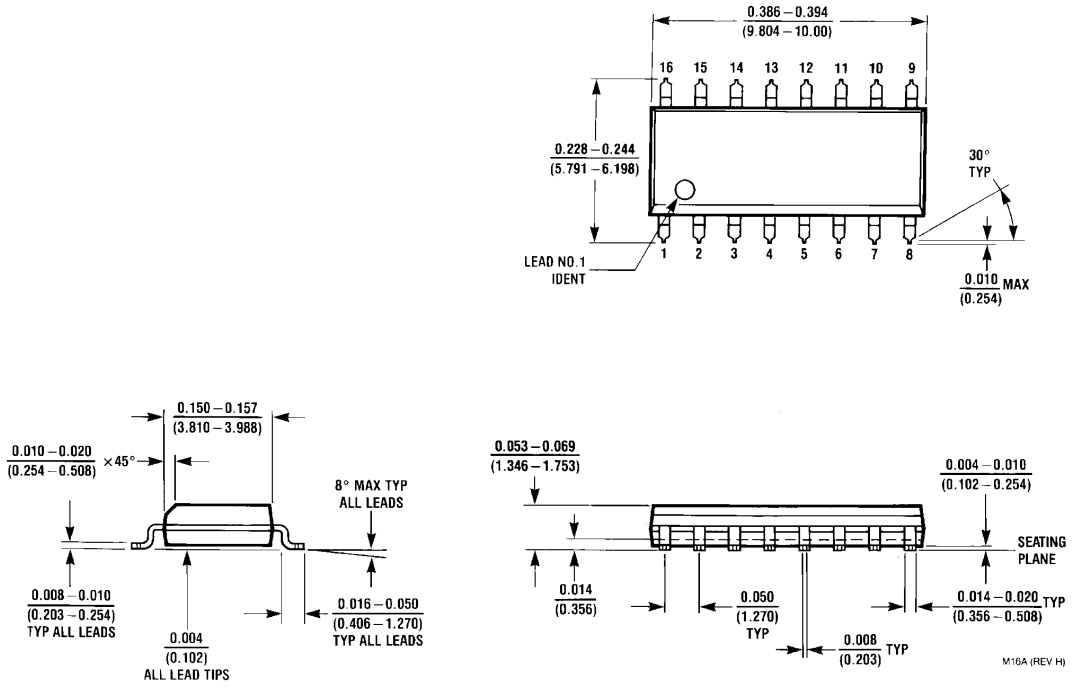


FIGURE 7. Typical Driver Output Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Molded Small Outline Package (M)
Order Number DS34LV87TM
NS Package Number M16A

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