19-5312; Rev 0; 6/10

MAXIM

±5ppm, I²C Real-Time Clock

DS3231M

General Description

The DS3231M is a low-cost, extremely accurate, I²C real-time clock (RTC). The device incorporates a battery input and maintains accurate timekeeping when main power to the device is interrupted. The integration of the microelectromechanical systems (MEMS) resonator enhances the long-term accuracy of the device and reduces the piece-part count in a manufacturing line. The DS3231M is available in the same footprint as the popular DS3231 RTC.

The RTC maintains seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an $\overline{AM}$/PM indicator. Two programmable time-of-day alarms and a 1Hz output are provided. Address and data are transferred serially through an I²C bidirectional bus. A precision temperature-compensated voltage reference and comparator circuit monitors the status of V_{CC} to detect power failures, to provide a reset output, and to automatically switch to the backup supply when necessary. Additionally, the $\overline{RST}$ pin is monitored as a pushbutton input for generating a microprocessor reset. See the *Block Diagram* for more details.

Applications

Power Meters

Industrial Applications

Ordering Information

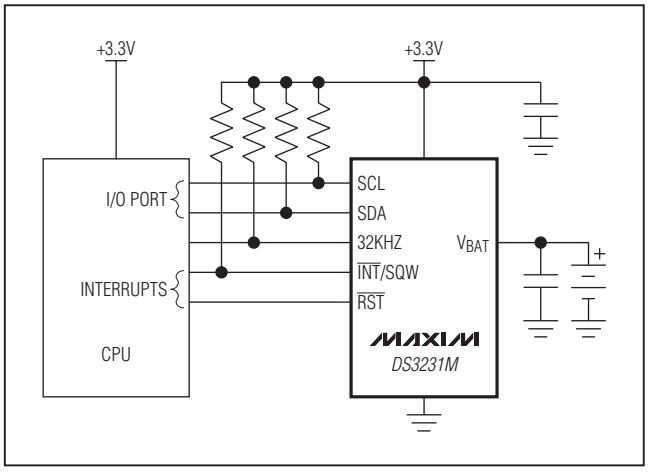
PART	TEMP RANGE	PIN-PACKAGE
DS3231MZ+*	-40°C to +85°C	8 SO
DS3231M+	-40°C to +85°C	16 SO

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Future product—contact factory for availability.*

Features

- **Timekeeping Accuracy ±5ppm (±0.432 Second/Day) from -40°C to +85°C**
- **Battery Backup for Continuous Timekeeping**
- **Low Power Consumption**
- **Footprint and Functionally Compatible to DS3231**
- **Complete Clock Calendar Functionality Including Seconds, Minutes, Hours, Day, Date, Month, and Year with Leap Year Compensation Up to Year 2100**
- **Two Time-of-Day Alarms**
- **1Hz and 32.768kHz Outputs**
- **Reset Output and Pushbutton Input with Debounce**
- **Fast (400kHz) I²C-Compatible Serial Bus**
- **+2.3V to +5.5V Supply Voltage**
- **Digital Temp Sensor with ±3°C Accuracy**
- **-40°C to +85°C Temperature Range**
- **16-Pin SO (300 mils) Package**
- **Underwriters Laboratories (UL) Recognized**

Typical Operating Circuit



Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: **www.maxim-ic.com/errata**.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to GND .....-0.3V to +6.0V
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.3	3.3	5.5	V
	V_{BAT}		2.3	3.0	5.5	
Logic 1	V_{IH}		0.7 x V_{CC}		V_{CC} + 0.3	V
Logic 0	V_{IL}		-0.3		0.3 x V_{CC}	V

ELECTRICAL CHARACTERISTICS—FREQUENCY AND TIMEKEEPING

(V_{CC} or V_{BAT} = +3.3V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_{BAT} = +3.0V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1Hz Frequency Tolerance	$\Delta f/f_{OUT}$	Measured over ≥ 10s interval			±5	ppm
1Hz Frequency Stability vs. V_{CC} Voltage	$\Delta f/V$			±1		ppm/V
Timekeeping Accuracy	tK_A				±0.432	Seconds/ Day
32kHz Frequency Tolerance	$\Delta f/f_{OUT}$				±2.5	%

DC ELECTRICAL CHARACTERISTICS—GENERAL

(V_{CC} = +2.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_{BAT} = +3.0V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Supply Current (I²C Active: Includes Temperature Conversion Current)	I_{CCA}	V_{CC} = +3.63V			200	µA
		V_{CC} = V_{CCMAX}			300	
Standby Supply Current (I²C Inactive: Includes Temperature Conversion Current)	I_{CCS}	V_{CC} = +3.63V			130	µA
		V_{CC} = V_{CCMAX}			200	
Temperature Conversion Current (I²C Inactive)	$I_{CCSCONV}$	V_{CC} = +3.63V			575	µA
		V_{CC} = V_{CCMAX}			650	

DC ELECTRICAL CHARACTERISTICS—GENERAL (continued)

(V_{CC} = +2.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_{BAT} = +3.0V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Fail Voltage	V_{PF}		2.45	2.575	2.70	V
Logic 0 Output (32KHZ, $\overline{INT}$/SQW, SDA)	V_{OL}	I_{OL} = 3mA			0.4	V
Logic 0 Output ($\overline{RST}$)	V_{OL}	I_{OL} = 1mA			0.4	V
Output Leakage (32KHZ, $\overline{INT}$/SQW, SDA)	I_{LO}		-0.1		+0.1	µA
Input Leakage (SCL)	I_{LI}		-0.1		+0.1	µA
$\overline{RST}$ I/O Leakage	I_{OL}		-200		+10	µA
V_{BAT} Leakage	I_{BATLKG}			25	100	nA
Temperature Accuracy	$TEMP_{ACC}$	V_{CC} or V_{BAT} = +3.3V			±3	°C
Temperature Conversion Time	t_{CONV}			10		ms
Pushbutton Debounce	PB_{DB}			250		ms
Reset Active Time	t_{RST}			250		ms
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 2)		125	200	ms

DC ELECTRICAL CHARACTERISTICS—V_{BAT} CURRENT CONSUMPTION

(V_{CC} = 0V, V_{BAT} = +2.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 0V, V_{BAT} = +3.0V, and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Battery Current (I²C Active) (Note 3)	I_{BATA}	V_{BAT} = +3.63V			70	µA
		V_{BAT} = V_{BATMAX}			150	
Timekeeping Battery Current (I²C Inactive) (Note 3)	I_{BATT}	V_{BAT} = +3.63V, EN32KHZ = 0		2	3.0	µA
		V_{BAT} = V_{BATMAX}, EN32KHZ = 0		2	3.5	
Temperature Conversion Current (I²C Inactive)	I_{BATTC}	V_{BAT} = +3.63V			575	µA
		V_{BAT} = V_{BATMAX}			650	
Data Retention Current (Oscillator Stopped and I²C Inactive)	I_{BATDR}	T_A = +25°C			100	nA

AC ELECTRICAL CHARACTERISTICS—POWER SWITCH

(T_A = -40°C to +85°C, unless otherwise noted.) (Figure 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Fall Time, V_{PFMAX} to V_{PFMIN}	t_{VCCF}		300			µs
V_{CC} Rise Time, V_{PFMIN} to V_{PFMAX}	t_{VCCR}		0			µs
Recovery at Power-Up	t_{REC}	(Note 4)		250	300	ms

AC ELECTRICAL CHARACTERISTICS—I²C INTERFACE

(V_{CC} or V_{BAT} = +2.3V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_{BAT} = +3.0V, and T_A = +25°C, unless otherwise noted.) (Note 5, Figure 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Set-Up Time	$t_{SU:DAT}$		100			ns
START Set-Up Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 6)	$20 + 0.1C_B$		300	ns
SDA and SCL Fall Time	t_F	(Note 6)	$20 + 0.1C_B$		300	ns
STOP Set-Up Time	$t_{SU:STO}$		0.6			µs
SDA, SCL Input Capacitance	C_{BIN}			10		pF

Note 1: All voltages are referenced to ground.

Note 2: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set.

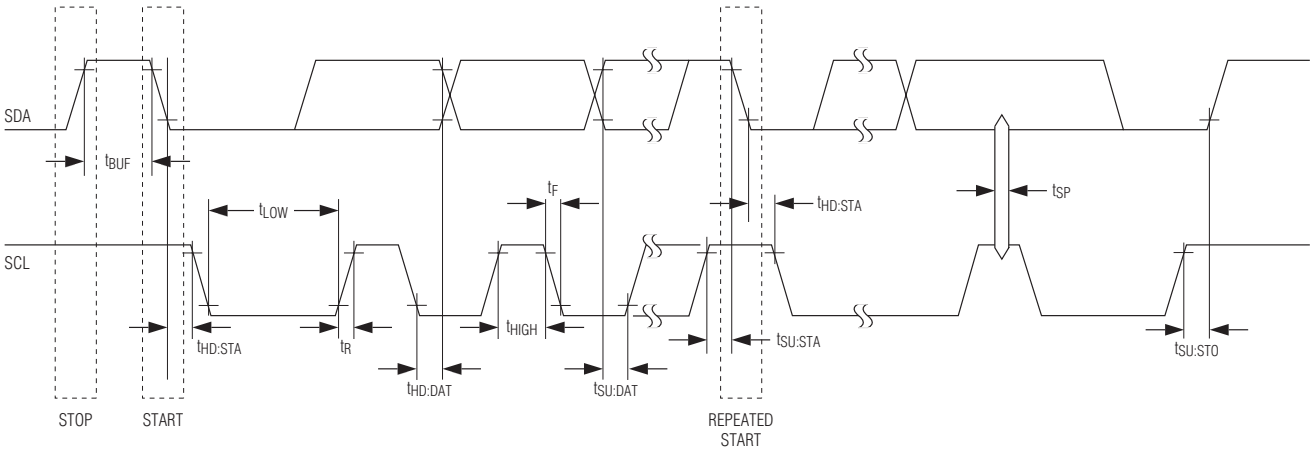
Note 3: Includes the temperature conversion current (averaged).

Note 4: This delay applies only if the oscillator is enabled. If the $\overline{EOSC}$ bit is 1, t_{REC} is bypassed and $\overline{RST}$ immediately goes high. The state of $\overline{RST}$ does not affect the I²C interface or RTC functions.

Note 5: Interface timing shown is for fast-mode (400kHz) operation. This device is also backward-compatible with standard mode I²C timing.

Note 6: C_B: Total capacitance of one bus line in picofarads.

Timing Diagrams



NOTE: TIMING IS REFERENCED TO V_{ILMAX} AND V_{IHMIN}.

Figure 1. I²C Timing

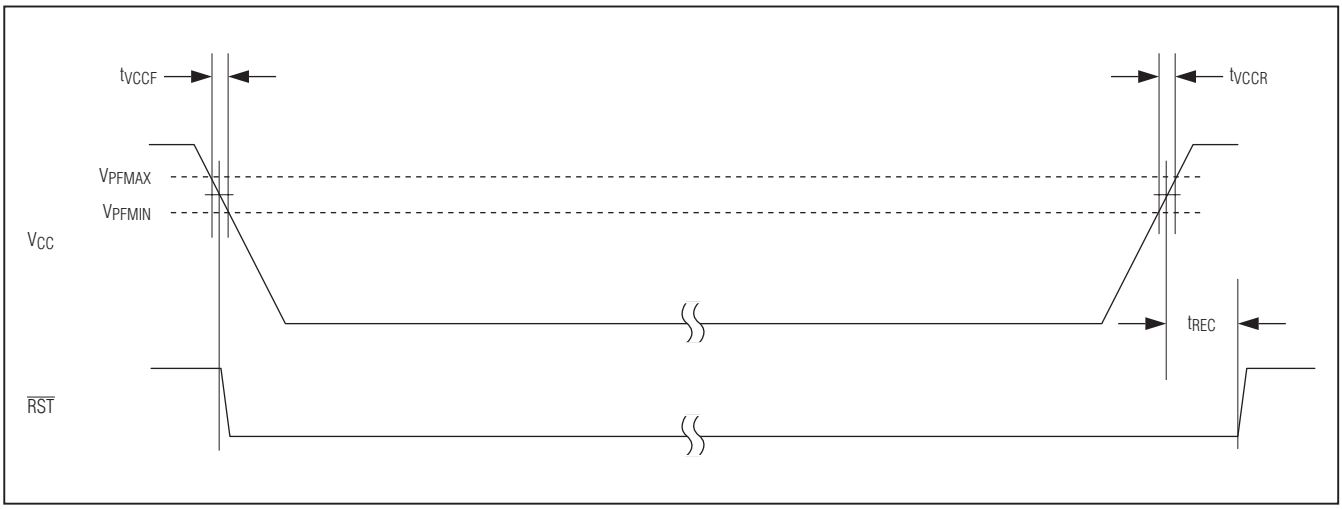


Figure 2. Power Switch Timing

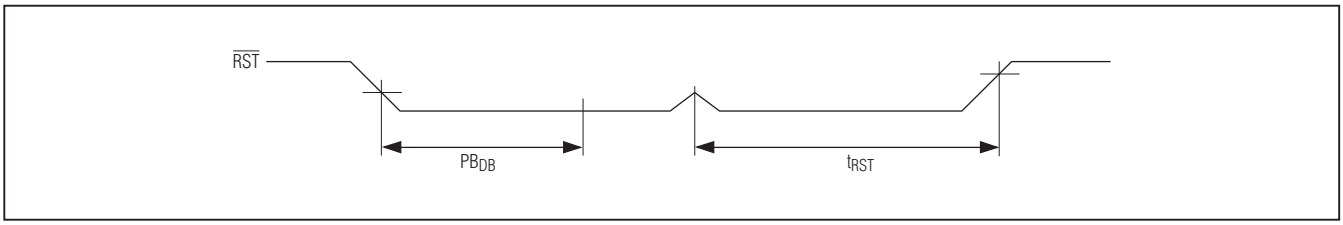
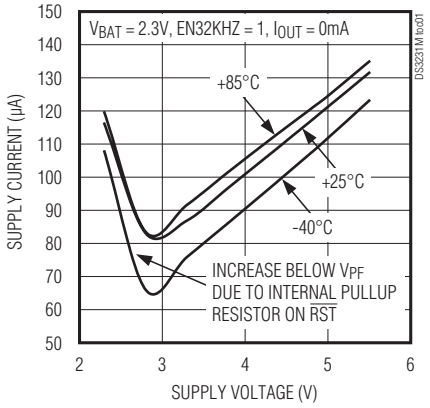


Figure 3. Pushbutton Reset Timing

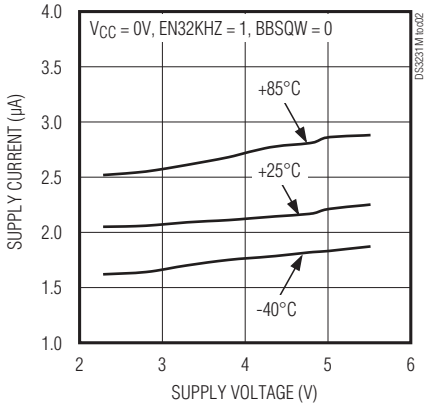
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

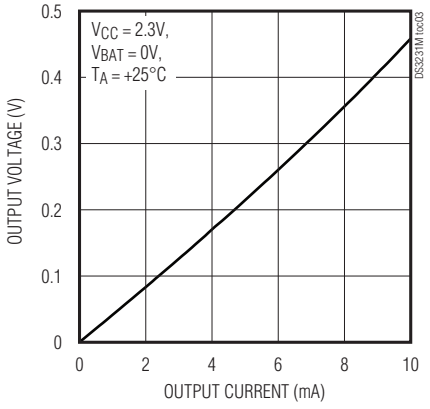
POWER-SUPPLY CURRENT vs. POWER-SUPPLY VOLTAGE



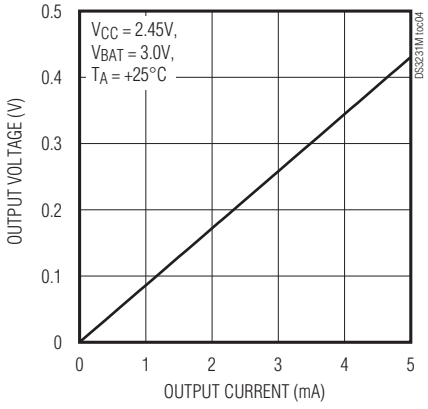
BATTERY-SUPPLY CURRENT vs. BATTERY-SUPPLY VOLTAGE



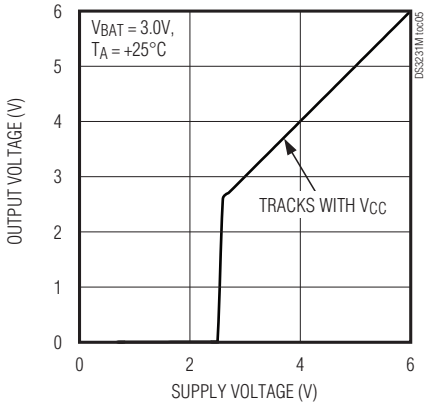
INT/SQW OUTPUT VOLTAGE vs. OUTPUT CURRENT



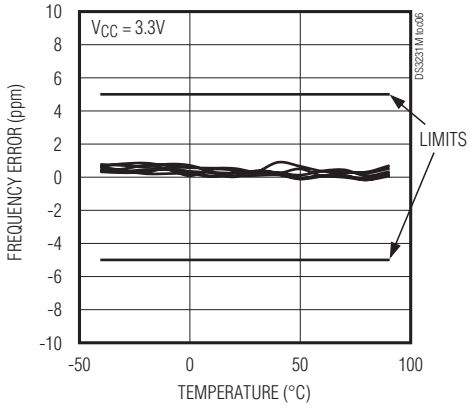
RST OUTPUT VOLTAGE vs. OUTPUT CURRENT



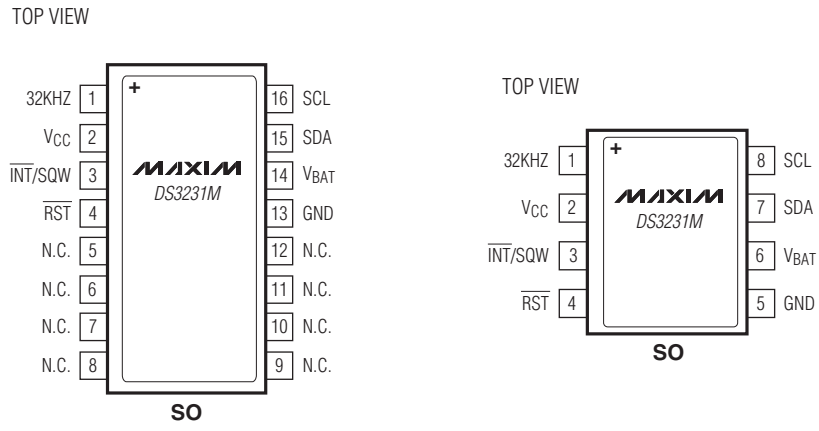
RST OUTPUT VOLTAGE vs. POWER SUPPLY VOLTAGE



FREQUENCY ERROR vs. TEMPERATURE



Pin Configuration



Pin Description

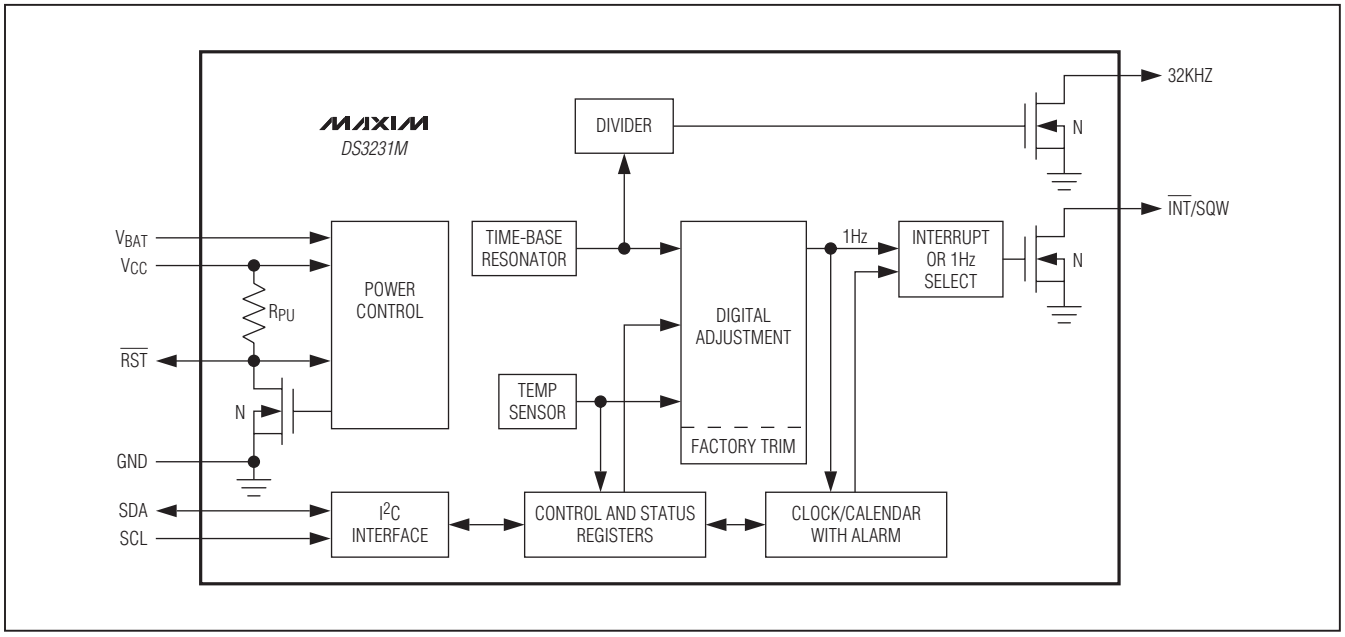
PIN		NAME	FUNCTION
8 SO	16 SO		
1	1	32KHZ	32.768kHz Output (50% Duty Cycle). This open-drain pin requires an external pullup resistor. When enabled with the EN32KHZ bit in the Status register (0Fh), this output operates on either power supply. This pin can be left open circuit if not used.
2	2	V_{CC}	DC Power Pin for Primary Power Supply. This pin should be decoupled using a 0.1µF to 1.0µF capacitor. Connect to ground if not used.
3	3	$\overline{INT}$/ SQW	Active-Low Interrupt or 1Hz Square-Wave Output. This open-drain pin requires an external pullup resistor connected to a supply at 5.5V or less. It can be left open if not used. This multifunction pin is determined by the state of the INTCN bit in the Control register (0Eh). When INTCN is set to logic 0, this pin outputs a 1Hz square wave. When INTCN is set to logic 1, a match between the timekeeping registers and either of the alarm registers activates the $\overline{INT}$/SQW pin (if the alarm is enabled). Because the INTCN bit is set to logic 1 when power is first applied, the pin defaults to an interrupt output with alarms disabled.
4	4	$\overline{RST}$	Active-Low Reset. This pin is an open-drain input/output. It indicates the status of V_{CC} relative to the V_{PF} specification. As V_{CC} falls below V_{PF}, the $\overline{RST}$ pin is driven low. When V_{CC} exceeds V_{PF}, for t_{RST}, the $\overline{RST}$ pin is pulled high by the internal pullup resistor. The active-low, open-drain output is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. It has an internal 50kΩ (R_{PU}) nominal value pullup resistor to V_{CC}. No external pullup resistors should be connected. If the oscillator is disabled, t_{REC} is bypassed and $\overline{RST}$ immediately goes high.
—	5–12	N.C.	No Connection. These pins must be connected to ground.
5	13	GND	Ground
6	14	V_{BAT}	Backup Power-Supply Input. When using the device with the V_{BAT} input as the primary power source, this pin should be decoupled using a 0.1µF to 1.0µF low-leakage capacitor. When using the device with the V_{BAT} input as the backup power source, the capacitor is not required. If V_{BAT} is not used, connect to ground. The device is UL recognized to ensure against reverse charging when used with a primary lithium battery. Go to **www.maxim-ic.com/qa/info/ul** for more information.

±5ppm, I²C Real-Time Clock

Pin Description (continued)

PIN		NAME	FUNCTION
8 SO	16 SO		
7	15	SDA	Serial-Data Input/Output. This pin is the data input/output for the I²C serial interface. This open-drain pin requires an external pullup resistor. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}.
8	16	SCL	Serial-Clock Input. This pin is the clock input for the I²C serial interface and is used to synchronize data movement on the serial interface. The pullup voltage can be up to 5.5V, regardless of the voltage on V_{CC}.

Block Diagram



Detailed Description

The DS3231M is a serial real-time clock (RTC) driven by an internal, temperature-compensated, microelectromechanical systems (MEMS) resonator. The oscillator provides a stable and accurate reference clock and maintains the RTC to within ±0.432 seconds-per-day accuracy from -40°C to +85°C. The RTC is a low-power clock/calendar with two programmable time-of-day alarms. $\overline{INT}$/SQW provides either an interrupt signal due to alarm conditions or a 1Hz square wave. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an $\overline{AM}$/PM indicator. The internal registers are accessible though an I²C bus interface. A temperature-compensated voltage reference and comparator circuit monitors the level of V_{CC} to detect power failures and to automatically switch to the backup supply when necessary. The $\overline{RST}$ pin provides an external pushbutton function and acts as an indicator of a power-fail event.

Operation

The *Block Diagram* shows the device's main elements. Each of the major blocks is described separately in the following sections.

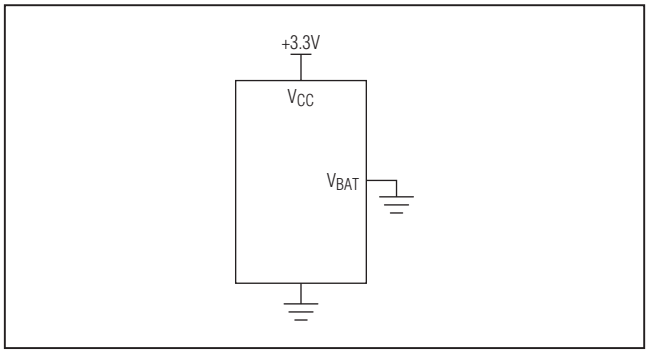


Figure 4. Single Supply (V_{CC} Only)

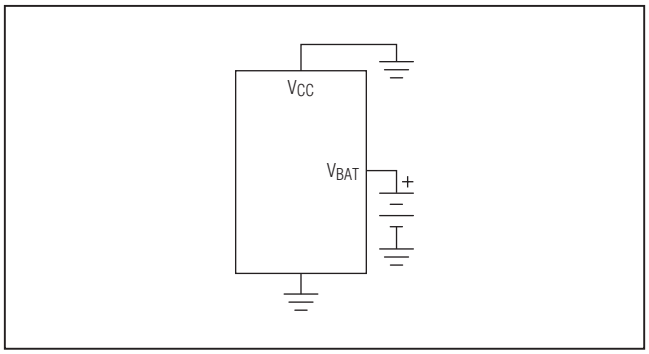


Figure 5. Single Supply (V_{BAT} Only)

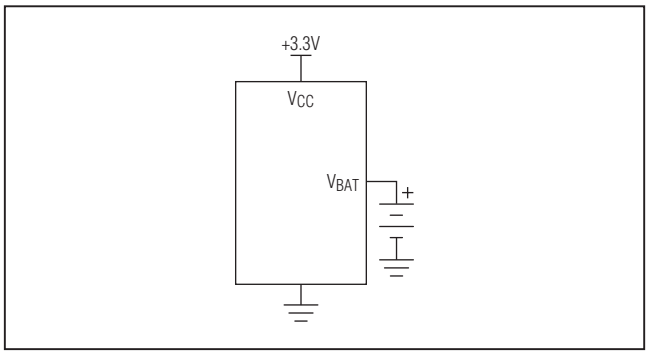


Figure 6. Dual Power Supply

High-Accuracy Time Base

The temperature sensor, oscillator, and digital adjustment controller logic form the highly accurate time base. The controller reads the output of the on-board temperature sensor and adjusts the final 1Hz output to maintain the required accuracy. The device is trimmed at the factory to maintain a tight accuracy over the operating temperature range. When the device is powered by V_{CC}, the adjustment occurs once a second. When the device is powered by V_{BAT}, the adjustment occurs once every 10s to conserve power. Adjusting the 1Hz time base less often does not affect the device's long-term timekeeping accuracy. The device also contains an Aging Offset register that allows a constant offset (positive or negative) to be added to the factory-trimmed adjustment value.

Power-Supply Configurations

The DS3231M can be configured to operate on a single power supply (using either V_{CC} or V_{BAT}) or in a dual-supply configuration, which provides a backup supply source to keep the timekeeping circuits alive during absence of primary system power.

Figure 4 illustrates a single-supply configuration using V_{CC} only, with the V_{BAT} input grounded. When $V_{CC} < V_{PF}$, the $\overline{RST}$ output is asserted (active low). Temperature conversions are executed once per second.

Figure 5 illustrates a single-supply configuration using V_{BAT} only, with the V_{CC} input grounded. The $\overline{RST}$ output is disabled and is held at ground through the connection of the internal pullup resistor. Temperature conversions are executed once every 10s.

Figure 6 illustrates a dual-supply configuration, using the V_{CC} supply for normal system operation and the V_{BAT} supply for backup power. In this configuration, the power-selection function is provided by a temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. When V_{CC} is greater than V_{PF}, the device is powered by V_{CC}. When V_{CC} is less than V_{PF} but greater than V_{BAT}, the device is powered

Table 1. Power Control

CONFIGURATION	CONDITION	I/O ACTIVE		I/O INACTIVE		$\overline{RST}$
V_{CC} Only (Figure 4)	$V_{CC} > V_{PF}$	I_{CCA}		I_{CCS}		Inactive (High)
	$V_{CC} < V_{PF}$					Active (Low)
V_{BAT} Only (Figure 5)	$\overline{EOSC} = 0$	I_{BATA}		I_{BATT}		Disabled (Low)
	$\overline{EOSC} = 1$			I_{BATDR}		
Dual Supply (Figure 6)	$V_{CC} > V_{PF}$	I_{CCA}		I_{CCS}		Inactive (High)
	$V_{CC} < V_{PF}$	$V_{CC} > V_{BAT}$	I_{CCA}	$V_{CC} > V_{BAT}$	I_{CCS}	Active (Low)
		$V_{CC} < V_{BAT}$	I_{BATA}	$V_{CC} < V_{BAT}$	I_{BATT}	

by V_{CC}. If V_{CC} is less than V_{PF} and is less than V_{BAT}, the device is powered by V_{BAT} (see Table 1).

When V_{CC} < V_{PF}, the $\overline{RST}$ output is asserted (active low). When V_{CC} is the presently selected power source, temperature conversions are executed once per second. When V_{BAT} is the presently selected power source, temperature conversions are executed once every 10s.

To preserve the battery, the first time V_{BAT} is applied to the device the oscillator does not start up until V_{CC} exceeds V_{PF} or until a valid I²C address is written to the device. Typical oscillator startup time is less than 1s. Approximately 2s after V_{CC} is applied, or a valid I²C address is written, the device makes a temperature measurement and applies the calculated correction to the oscillator. Once the oscillator is running, it continues to run as long as a valid power source is available (V_{CC} or V_{BAT}), and the device continues to measure the temperature and correct the oscillator frequency. On the first application of V_{CC} power, or (if V_{BAT} powered) when a valid I²C address is written to the device, the time and date registers are reset to 01/01/00 01 00:00:00 (MM/DD/YY DOW HH:MM:SS).

V_{BAT} Operation

There are several modes of operation that affect the amount of V_{BAT} current that is drawn. While the device is powered by V_{BAT} and the serial interface is active, the active battery current I_{BATA} is drawn. When the serial interface is inactive, the timekeeping current I_{BATT} (which includes the averaged temperature-conversion current I_{BATTC}) is used. The temperature-conversion current I_{BATTC} is specified since the system must be able to support the periodic higher current pulse and still maintain a valid voltage level. The data-retention current I_{BATDR} is the current drawn by the device when the oscillator is stopped ($\overline{EOSC}$ = 1). This mode can be used to minimize battery requirements for periods when maintaining time and date information is not necessary, e.g., while the end system is waiting to be shipped to a customer.

Pushbutton Reset Function

The device provides for a pushbutton switch to be connected to the $\overline{RST}$ input/output pin. When the device is not in a reset cycle, it continuously monitors $\overline{RST}$ for a low-going edge. If an edge transition is detected, the device debounces the switch by pulling $\overline{RST}$ low. After the internal timer has expired (PB_{DB}), the device continues to monitor the $\overline{RST}$ line. If the line is still low, the device continuously monitors the line looking for a rising edge. Upon detecting release, the device forces $\overline{RST}$ low and holds it low for t_{RST}. $\overline{RST}$ is also used to indicate a power-fail condition. When V_{CC} is lower than V_{PF}, an internal power-fail signal is generated, which forces $\overline{RST}$ low. When V_{CC} returns to a level above V_{PF}, $\overline{RST}$ is held low for approximately 250ms (t_{REC}) to allow the power supply to stabilize. If the oscillator is not running when V_{CC} is applied, t_{REC} is bypassed and $\overline{RST}$ immediately goes high. Assertion of the $\overline{RST}$ output, whether by pushbutton or power-fail detection, does not affect the device's internal operation. $\overline{RST}$ output operation and pushbutton monitoring are only available if V_{CC} power is available.

Real-Time Clock (RTC)

With the 1Hz source from the temperature-compensated oscillator, the RTC provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or the 12-hour format with an $\overline{AM}$/PM indicator. The clock provides two programmable time-of-day alarms. $\overline{INT}$/SQW can be enabled to generate either an interrupt due to an alarm condition or a 1Hz square wave. This selection is controlled by the INTCN bit in the Control register.

I²C Interface

The I²C interface is accessible whenever either V_{CC} or V_{BAT} is at a valid level. If a microcontroller connected to the device resets because of a loss of V_{CC} or other event, it is possible that the microcontroller and device's I²C communications could become unsynchronized, e.g., the microcontroller resets while reading data from the device. When the microcontroller resets, the device's I²C interface can be placed into a known state by toggling SCL until SDA is observed to be at a high level. At that point the microcontroller should pull SDA low while SCL is high, generating a START condition.

Address Map

Table 2 shows the address map for the device's timekeeping registers. During a multibyte access, when the address pointer reaches the end of the register space (12h), it wraps around to location 00h. On an I²C START or address pointer incrementing to location 00h, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock can continue to run. This eliminates the need to reread the registers in case the main registers update during a read.

Table 2. Timekeeping Registers

ADDRESS	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB	FUNCTION	RANGE
00h	0	10 Seconds			Seconds				Seconds	00–59
01h	0	10 Minutes			Minutes				Minutes	00–59
02h	0	12/$\overline{24}$	$\overline{AM}$/PM 20 Hours	10 Hours	Hour				Hours	1–12 + $\overline{AM}$/PM 00–23
03h	0	0	0	0	0	Day			Day	1–7
04h	0	0	10 Date		Date				Date	01–31
05h	Century	0	0	10 Month	Month				Month/Century	01–12 + Century
06h	10 Year				Year				Year	00–99
07h	A1M1	10 Seconds			Seconds				Alarm 1 Seconds	00–59
08h	A1M2	10 Minutes			Minutes				Alarm 1 Minutes	00–59
09h	A1M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hours	10 Hours	Hour				Alarm 1 Hours	1–12 + $\overline{AM}$/PM 00–23
0Ah	A1M4	DY/$\overline{DT}$	10 Date		Day				Alarm 1 Day	1–7
					Date				Alarm 1 Date	1–31
0Bh	A2M2	10 Minutes			Minutes				Alarm 2 Minutes	00–59
0Ch	A2M3	12/$\overline{24}$	$\overline{AM}$/PM 20 Hours	10 Hours	Hour				Alarm 2 Hours	1–12 + $\overline{AM}$/PM 00–23
0Dh	A2M4	DY/$\overline{DT}$	10 Date		Day				Alarm 2 Day	1–7
					Date				Alarm 2 Date	1–31
0Eh	$\overline{EOSC}$	BBSQW	CONV	NA	NA	INTCN	A2IE	A1IE	Control	—
0Fh	OSF	0	0	0	EN32KHZ	BSY	A2F	A1F	Status	—
10h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Aging Offset	—
11h	SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA	Temperature MSB	—
12h	DATA	DATA	0	0	0	0	0	0	Temperature LSB	—

Note: *Unless otherwise specified, the registers' state is not defined when power is first applied.*

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. Table 2 shows the RTC registers. The time and calendar data are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The device can be run in either 12-hour or 24-hour mode. Bit 6 of the Hours register is defined as the 12-hour or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic-high being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20–23 hours). The century bit (bit 7 of the Month register) is toggled when the Years register overflows from 99

to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. When reading or writing the time and date registers, secondary buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the secondary buffers are synchronized to the internal registers on any I²C START and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read. The countdown chain is reset whenever the seconds register is written. Write transfers occur on the acknowledge from the device. Once the countdown chain is reset, to avoid rollover issues the remaining time and date registers must be written within 1s.

Alarms

The device contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 07h–0Ah. Alarm 2 can be set by writing to registers 0Bh–0Dh. See Table 2. The alarms can be programmed (by the alarm enable and INTCN bits in the Control register) to activate the $\overline{INT}$/SQW output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 2). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 3 shows the possible settings. Configurations not listed in the table result in illogical operation. The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0–5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{DT}$ is written to logic 1, the alarm is the result of a match with day of the week. When the RTC register values match alarm register settings, the corresponding alarm flag A1F or A2F bit is set to logic 1. If the corresponding alarm interrupt enable A1IE or A2IE bit is also set to logic 1, the alarm condition activates the $\overline{INT}$/SQW signal if the INTCN bit is set to logic 1. The match is tested on the once-per-second update of the time and date registers.

Table 3. Alarm Mask Bits

DY/$\overline{DT}$	ALARM 1 REGISTER MASK BITS (BIT 7)				ALARM RATE
	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	Alarm once a second
X	1	1	1	0	Alarm when seconds match
X	1	1	0	0	Alarm when minutes and seconds match
X	1	0	0	0	Alarm when hours, minutes, and seconds match
0	0	0	0	0	Alarm when date, hours, minutes, and seconds match
1	0	0	0	0	Alarm when day, hours, minutes, and seconds match

DY/$\overline{DT}$	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	
X	1	1	1	Alarm once per minute (00 seconds of every minute)
X	1	1	0	Alarm when minutes match
X	1	0	0	Alarm when hours and minutes match
0	0	0	0	Alarm when date, hours, and minutes match
1	0	0	0	Alarm when day, hours, and minutes match

Control Register (0Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{ESOC}}$	BBSQW	CONV	NA	NA	INTCN	A2IE	A1IE
0	0	0	1	1	1	0	0

BIT 7	**$\overline{\text{ESOC}}$:** Enable oscillator. When set to logic 0, the oscillator is started. When set to logic 1, the oscillator is stopped when the device switches to V_{BAT}. This bit is clear (logic 0) when power is first applied. When the device is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{\text{EOSC}}$ bit. When the oscillator is disabled, all register data is static.
BIT 6	**BBSQW:** Battery-backed square-wave enable. When set to logic 1 with INTCN = 0 and $V_{CC} < V_{PF}$, this bit enables the 1Hz square wave. When BBSQW is logic 0, $\overline{\text{INT}}$/SQW goes high impedance when V_{CC} falls below V_{PF}. This bit is disabled (logic 0) when power is first applied.
BIT 5	**CONV:** Convert temperature. Setting this bit to 1 forces the temperature sensor to convert the temperature into digital code and execute the temperature compensate algorithm to update the oscillator's accuracy. The device cannot be forced to execute the temperature-compensate algorithm faster than once per second. A user-initiated temperature conversion does not affect the internal update cycle. The CONV bit remains at a 1 from the time it is written until the temperature conversion is completed, at which time both CONV and BSY go to 0. The CONV bit should be used when monitoring the status of a user-initiated conversion. See Figure 7 for more details.
BITS 4:3	**NA:** Not applicable. These bits have no affect on the device and can be set to either 0 or 1.
BIT 2	**INTCN:** Interrupt control. This bit controls the $\overline{\text{INT}}$/SQW output signal. When the INTCN bit is set to logic 0, a 1Hz square wave is output on $\overline{\text{INT}}$/SQW. When the INTCN bit is set to logic 1, a match between the timekeeping registers and either of the alarm registers activates the $\overline{\text{INT}}$/SQW output (if the alarm is also enabled). The corresponding alarm flag is always set regardless of the state of the INTCN bit. The INTCN bit is set to a logic 1 when power is first applied.
BIT 1	**A2IE:** Alarm 2 interrupt enable. When set to logic 1, this bit permits the alarm 2 flag (A2F) bit in the status register to assert $\overline{\text{INT}}$/SQW (when INTCN = 1). When the A2IE bit is set to logic 0 or INTCN is set to logic 0, the A2F bit does not initiate an interrupt signal. The A2IE bit is disabled (logic 0) when power is first applied.
BIT 0	**A1IE:** Alarm 1 interrupt enable. When set to logic 1, this bit permits the alarm 1 flag (A1F) bit in the status register to assert $\overline{\text{INT}}$/SQW (when INTCN = 1). When the A1IE bit is set to logic 0 or INTCN is set to logic 0, the A1F bit does not initiate an interrupt signal. The A1IE bit is disabled (logic 0) when power is first applied.

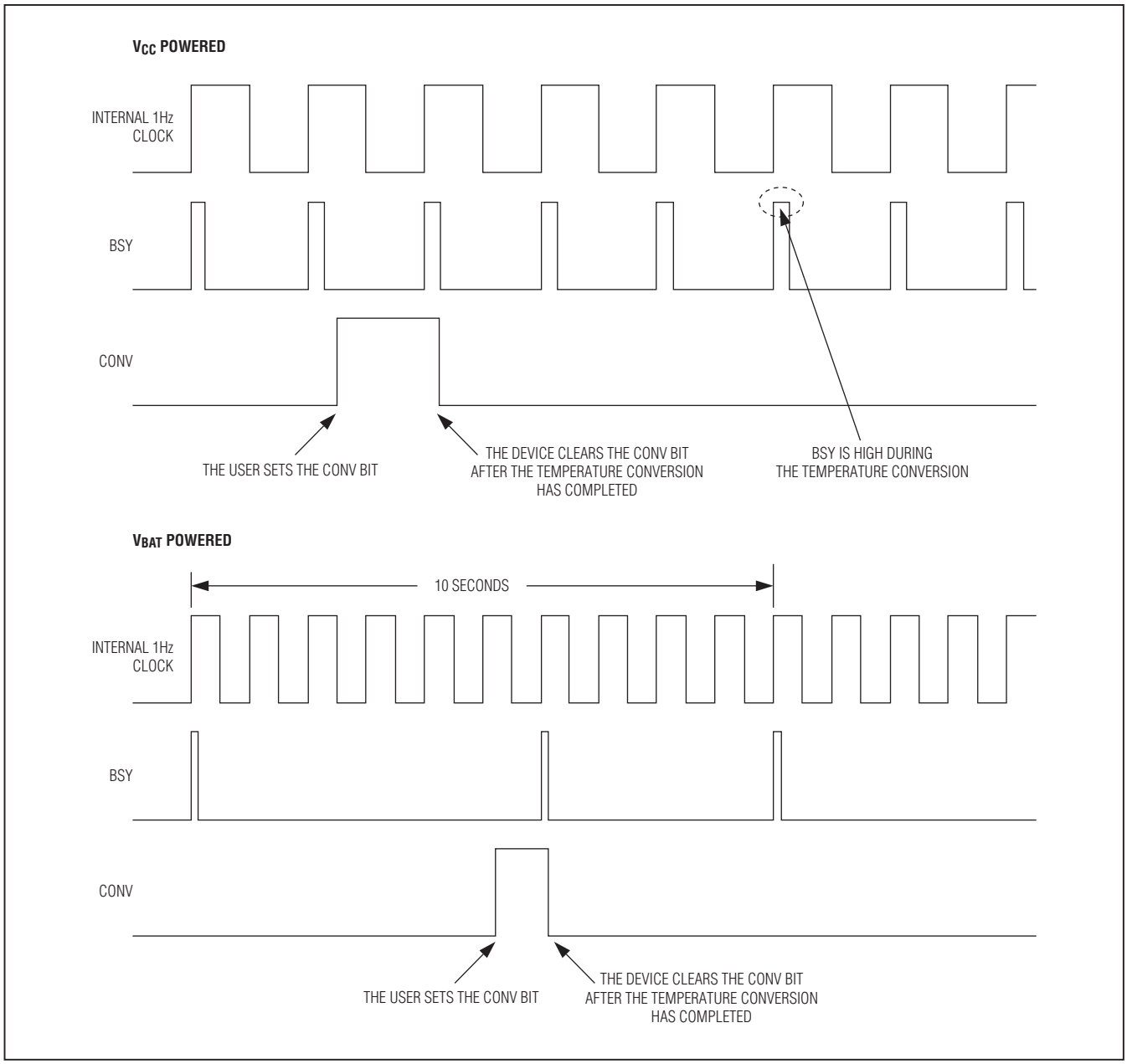


Figure 7. CONV Control Bit and BSY Status Bit Operation

Status Register (0Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OSF	0	0	0	EN32KHZ	BSY	A2F	A1F
1	0	0	0	1	X	X	X

BIT 7	**OSF:** Oscillator stop flag. A logic 1 in this bit indicates that the oscillator either is stopped or was stopped for some period and could be used to judge the validity of the timekeeping data. This bit is set to logic 1 any time that the oscillator stops. This bit remains at logic 1 until written to logic 0. The following are examples of conditions that can cause the OSF bit to be set: 1) The first time power is applied. 2) The voltages present on both V_{CC} and V_{BAT} are insufficient to support the oscillator. 3) The $\overline{EOSC}$ bit is turned off in battery-backed mode. 4) External influences on the oscillator (i.e., noise, leakage, etc.).
BITS 6:4	Unused (0). These bits have no meaning and are fixed at 0 when read.
BIT 3	**EN32KHZ:** Enabled 32.768kHz output. This bit enables and disables the 32KHZ output. When set to a logic 0, the 32KHZ output is high impedance. On initial power-up, this bit is set to a logic 1 and the 32KHZ output is enabled and produces a 32.768kHz square wave if the oscillator is enabled.
BIT 2	**BSY:** Busy. This bit indicates the device is busy executing temperature conversion function. It goes to logic 1 when the conversion signal to the temperature sensor is asserted, and then it is cleared when the device has completed the temperature conversion. See the *Block Diagram* for more details.
BIT 1	**A2F:** Alarm 2 flag. A logic 1 in the alarm 2 flag bit indicates that the time matched the alarm 2 registers. If the A2IE bit is logic 1 and the INTCN bit is set to logic 1, $\overline{INT}$/SQW is also asserted. A2F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.
BIT 0	**A1F:** Alarm 1 flag. A logic 1 in the alarm 1 flag bit indicates that the time matched the alarm 1 registers. If the A1IE bit is logic 1 and the INTCN bit is set to logic 1, $\overline{INT}$/SQW is also asserted. A1F is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Aging Offset Register (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA
0	0	0	0	0	0	0	0

The Aging Offset register takes a user-provided value to add to or subtract from the factory-trimmed value that adjusts the accuracy of the time base. Use of the Aging Offset register is not needed to achieve the accuracy as defined in the *Electrical Characteristics* tables.

The Aging Offset code is encoded in two's complement, with bit 7 representing the SIGN bit. One LSB typically represents a 0.12ppm change in frequency. The change in ppm per LSB is the same over the operating temperature range. Positive offsets slow the time base and negative offsets quicken the time base.

Temperature Registers (11h–12h)

Temperature Register (Upper Byte = 11h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SIGN	DATA	DATA	DATA	DATA	DATA	DATA	DATA
0	0	0	0	0	0	0	0

Temperature Register (Lower Byte = 12h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA	DATA	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Temperature is represented as a 10-bit code with a resolution of 0.25°C and is accessible at location 11h and 12h. The temperature is encoded in two's complement format. The upper 8 bits, the integer portion, are at location 11h and the lower 2 bits, the fractional portion, are at location 12h. For example, 00011001 01b = +25.25°C. Upon power reset, the registers are set to a default temperature of 0°C and the controller starts a temperature conversion. The temperature is read upon initial application of V_{CC} or I²C access on V_{BAT} and once every second afterwards with V_{CC} power or once every 10s with V_{BAT} power. The Temperature registers are also updated after each user-initiated conversion and are read only.

I²C Serial Port Operation

I²C Slave Address

The device's slave address byte is D0h. The first byte sent to the device includes the device identifier, device address, and the R/$\overline{W}$ bit (Figure 8). The device address sent by the I²C master must match the address assigned to the device.

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

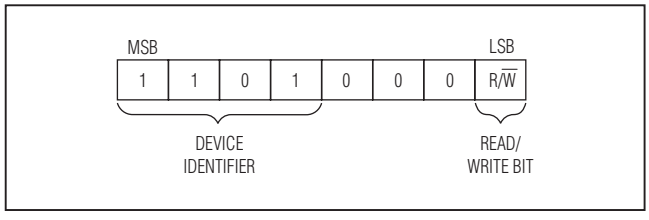


Figure 8. I²C Slave Address Byte

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle, it often initiates a low-power mode for slave devices.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 1 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 1 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it immediately initiates a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 1 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the setup and hold time requirements (see Figure 1). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (see Figure 1) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses including when it is reading bits from the slave.

Acknowledge (ACK and NACK): An acknowledge (ACK) or not acknowledge (NACK) is always the ninth bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a 0 during the ninth bit. A device performs a NACK by transmitting a 1 during the ninth bit. Timing for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgment from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgment is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I²C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit. The device's slave address is D0h and cannot be modified by the user. When the R/$\overline{W}$ bit is 0 (such as in D0h), the master is indicating it writes data to the slave. If R/$\overline{W}$ = 1 (D1h in this case), the master is indicating it wants to read from the slave. If an incorrect slave address is written, the device assumes the master is communicating with another I²C device and ignore the communication until the next START condition is sent.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I²C Communication

See Figure 9 for an I²C communication example.

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember the master must read the slave's acknowledgment during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the starting memory address, writes multiple data bytes, and generates a STOP condition.

Reading a Single Byte from a Slave: Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the master to keep track of the memory address counter is impractical, use the method for manipulating the address counter for reads.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1),

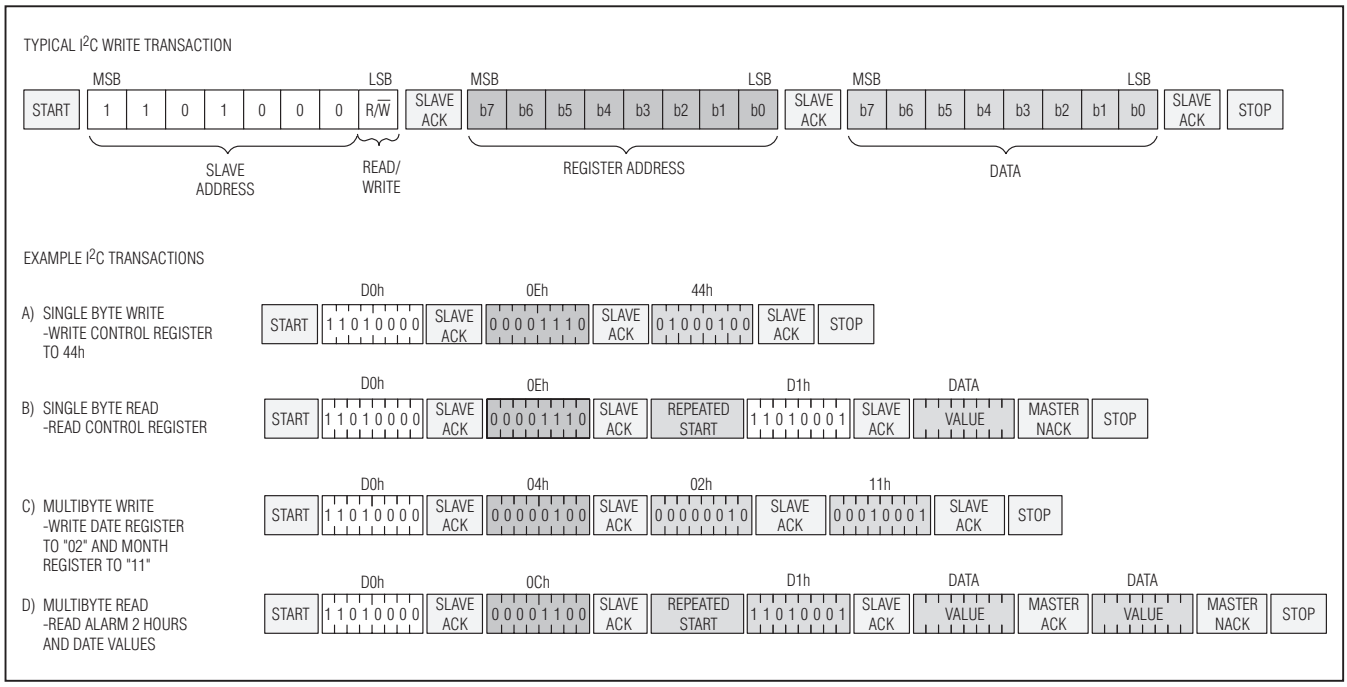


Figure 9. I²C Transactions

reads data with ACK or NACK as applicable, and generates a STOP condition. See Figure 6 for a read example using the repeated START condition to specify the starting memory location.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it must NACK to indicate the end of the transfer and then it generates a STOP condition.

Applications Information

Power-Supply Decoupling

To achieve the best results when using the DS3231M, decouple the V_{CC} and/or V_{BAT} power supplies with 0.1µF and/or 1.0µF capacitors. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

If communications during battery operation are not required, the V_{BAT} decoupling capacitor can be omitted.

Using Open-Drain Outputs

The 32KHZ and $\overline{INT}$/SQW outputs are open drain and therefore require external pullup resistors to realize logic-high output levels. Pullup resistor values between 1kΩ and 10MΩ are typical.

The $\overline{RST}$ output is also open drain, but is provided with an internal 50kΩ pullup resistor (R_{PU}) to V_{CC}. External pullup resistors should not be added.

SDA and SCL Pullup Resistors

SDA is an open-drain output and requires an external pullup resistor to realize a logic-high level.

Because the device does not use clock cycle stretching, a master using either an open-drain output with a pullup resistor or CMOS output driver (push-pull) could be used for SCL.

Battery Charge Protection

The device contains Maxim's redundant battery-charge protection circuit to prevent any charging of the external battery.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SO	W16+2	**21-0042**	**90-0107**
8 SO	S8+4	**21-0041**	**90-0096**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—