

1 Mbit (128K x8) Page-Mode EEPROM

SST29EE010 / SST29LE010 / SST29VE010



Data Sheet

FEATURES:

- **Single Voltage Read and Write Operations**
 - 5.0V-only for SST29EE010
 - 3.0-3.6V for SST29LE010
 - 2.7-3.6V for SST29VE010
- **Superior Reliability**
 - Endurance: 100,000 Cycles (typical)
 - Greater than 100 years Data Retention
- **Low Power Consumption**
 - Active Current: 20 mA (typical) for 5V and 10 mA (typical) for 3.0/2.7V
 - Standby Current: 10 μ A (typical)
- **Fast Page-Write Operation**
 - 128 Bytes per Page, 1024 Pages
 - Page-Write Cycle: 5 ms (typical)
 - Complete Memory Rewrite: 5 sec (typical)
 - Effective Byte-Write Cycle Time: 39 μ s (typical)
- **Fast Read Access Time**
 - 5.0V-only operation: 70 and 90 ns
 - 3.0-3.6V operation: 150 and 200 ns
 - 2.7-3.6V operation: 200 and 250 ns
- **Latched Address and Data**
- **Automatic Write Timing**
 - Internal V_{PP} Generation
- **End of Write Detection**
 - Toggle Bit
 - Data# Polling
- **Hardware and Software Data Protection**
- **Product Identification can be accessed via Software Operation**
- **TTL I/O Compatibility**
- **JEDEC Standard**
 - Flash EEPROM Pinouts and command sets
- **Packages Available**
 - 32-lead PLCC
 - 32-lead TSOP (8mm x 14mm, 8mm x 20mm)
 - 32-pin PDIP

PRODUCT DESCRIPTION

The SST29EE/LE/VE010 are 128K x8 CMOS Page-Write EEPROMs manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST29EE/LE/VE010 write with a single power supply. Internal Erase/Program is transparent to the user. The SST29EE/LE/VE010 conform to JEDEC standard pinouts for byte-wide memories.

Featuring high performance Page-Write, the SST29EE/LE/VE010 provide a typical Byte-Write time of 39 μ sec. The entire memory, i.e., 128 KBytes, can be written page-by-page in as little as 5 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of a Write cycle. To protect against inadvertent write, the SST29EE/LE/VE010 have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST29EE/LE/VE010 are offered with a guaranteed Page-Write endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST29EE/LE/VE010 are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST29EE/LE/VE010 significantly improve performance and reliability, while lowering power consumption. The SST29EE/LE/VE010 improve flexibility while lowering the cost for program, data, and configuration storage applications.

To meet high density, surface mount requirements, the SST29EE/LE/VE010 are offered in 32-lead PLCC and 32-lead TSOP packages. A 600-mil, 32-pin PDIP package is also available. See Figures 1, 2, and 3 for pinouts.

Device Operation

The SST Page-Mode EEPROM offers in-circuit electrical write capability. The SST29EE/LE/VE010 does not require separate Erase and Program operations. The internally timed write cycle executes both erase and program transparently to the user. The SST29EE/LE/VE010 have industry standard optional Software Data Protection, which SST recommends always to be enabled. The SST29EE/LE/VE010 are compatible with industry standard EEPROM pinouts and functionality.



Read

The Read operations of the SST29EE/LE/VE010 are controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the read cycle timing diagram for further details (Figure 4).

Write

The Page-Write to the SST29EE/LE/VE010 should always use the JEDEC Standard Software Data Protection (SDP) three-byte command sequence. The SST29EE/LE/VE010 contain the optional JEDEC approved Software Data Protection scheme. SST recommends that SDP always be enabled, thus, the description of the Write operations will be given using the SDP enabled format. The three-byte SDP Enable and SDP Write commands are identical; therefore, any time a SDP Write command is issued, Software Data Protection is automatically assured. The first time the three-byte SDP command is given, the device becomes SDP enabled. Subsequent issuance of the same command bypasses the data protection for the page being written. At the end of the desired Page-Write, the entire device remains protected. For additional descriptions, please see the application notes, *The Proper Use of JEDEC Standard Software Data Protection and Protecting Against Unintentional Writes When Using Single Power Supply Flash Memories*.

The Write operation consists of three steps. Step 1 is the three-byte load sequence for Software Data Protection. Step 2 is the byte-load cycle to a page buffer of the SST29EE/LE/VE010. Steps 1 and 2 use the same timing for both operations. Step 3 is an internally controlled write cycle for writing the data loaded in the page buffer into the memory array for nonvolatile storage. During both the SDP three-byte load sequence and the byte-load cycle, the addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. The internal write cycle is initiated by the T_{BLC0} timer after the rising edge of WE# or CE#, whichever occurs first. The Write cycle, once initiated, will continue to completion, typically within 5 ms. See Figures 5 and 6 for WE# and CE# controlled Page-Write cycle timing diagrams and Figures 15 and 17 for flowcharts.

The Write operation has three functional cycles: the Software Data Protection load sequence, the page load cycle, and the internal write cycle. The Software Data Protection

consists of a specific three-byte load sequence that allows writing to the selected page and will leave the SST29EE/LE/VE010 protected at the end of the Page-Write. The page load cycle consists of loading 1 to 128 bytes of data into the page buffer. The internal write cycle consists of the T_{BLC0} time-out and the write timer operation. During the Write operation, the only valid reads are Data# Polling and Toggle Bit.

The Page-Write operation allows the loading of up to 128 bytes of data into the page buffer of the SST29EE/LE/VE010 before the initiation of the internal write cycle. During the internal write cycle, all the data in the page buffer is written simultaneously into the memory array. Hence, the Page-Write feature of SST29EE/LE/VE010 allow the entire memory to be written in as little as 5 seconds. During the internal write cycle, the host is free to perform additional tasks, such as to fetch data from other locations in the system to set up the write to the next page. In each Page-Write operation, all the bytes that are loaded into the page buffer must have the same page address, i.e. A₇ through A₁₆. Any byte not loaded with user data will be written to FFH.

See Figures 5 and 6 for the Page-Write cycle timing diagrams. If after the completion of the three-byte SDP load sequence or the initial byte-load cycle, the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 100 μ s, the SST29EE/LE/VE010 will stay in the page load cycle. Additional bytes are then loaded consecutively. The page load cycle will be terminated if no additional byte is loaded into the page buffer within 200 μ s (T_{BLC0}) from the last byte-load cycle, i.e., no subsequent WE# or CE# high-to-low transition after the last rising edge of WE# or CE#. Data in the page buffer can be changed by a subsequent byte-load cycle. The page load period can continue indefinitely, as long as the host continues to load the device within the byte-load cycle time of 100 μ s. The page to be loaded is determined by the page address of the last byte loaded.

Software Chip-Erase

The SST29EE/LE/VE010 provide a Chip-Erase operation, which allows the user to simultaneously clear the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Software Chip-Erase operation is initiated by using a specific six-byte load sequence. After the load sequence, the device enters into an internally timed cycle similar to the Write cycle. During the Erase operation, the only valid read is Toggle Bit. See Table 4 for the load sequence, Figure 10 for timing diagram, and Figure 19 for the flowchart.



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Write Operation Status Detection

The SST29EE/LE/VE010 provide two software means to detect the completion of a Write cycle, in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The end of write detection mode is enabled after the rising WE# or CE# whichever occurs first, which initiates the internal write cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ₇ or DQ₆. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ₇)

When the SST29EE/LE/VE010 are in the internal write cycle, any attempt to read DQ₇ of the last byte loaded during the byte-load cycle will receive the complement of the true data. Once the Write cycle is completed, DQ₇ will show true data. The device is then ready for the next operation. See Figure 7 for Data# Polling timing diagram and Figure 16 for a flowchart.

Toggle Bit (DQ₆)

During the internal write cycle, any consecutive attempts to read DQ₆ will produce alternating 0s and 1s, i.e. toggling between 0 and 1. When the Write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 8 for Toggle Bit timing diagram and Figure 16 for a flowchart. The initial read of the Toggle Bit will typically be a "1".

Data Protection

The SST29EE/LE/VE010 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 2.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST29EE/LE/VE010 provide the JEDEC approved optional Software Data Protection scheme for all data alteration operations, i.e., Write and Chip-Erase. With this scheme, any Write operation requires the inclusion of a series of three byte-load operations to precede the data loading operation. The three byte-load sequence is used to initiate the Write cycle, providing optimal protection from inadvertent write operations, e.g., during the system power-up or power-down. The SST29EE/LE/VE010 are shipped with the Software Data Protection disabled.

The software protection scheme can be enabled by applying a three-byte sequence to the device, during a page-load cycle (Figures 5 and 6). The device will then be automatically set into the data protect mode. Any subsequent Write operation will require the preceding three-byte sequence. See Table 4 for the specific software command codes and Figures 5 and 6 for the timing diagrams. To set the device into the unprotected mode, a six-byte sequence is required. See Table 4 for the specific codes and Figure 9 for the timing diagram. If a write is attempted while SDP is enabled the device will be in a non-accessible state for ~300 μs. SST recommends Software Data Protection always be enabled. See Figure 17 for flowcharts.

The SST29EE/LE/VE010 Software Data Protection is a global command, protecting (or unprotecting) all pages in the entire memory array once enabled (or disabled). Therefore using SDP for a single Page-Write will enable SDP for the entire array. Single pages by themselves cannot be SDP enabled or disabled.

Single power supply reprogrammable nonvolatile memories may be unintentionally altered. SST strongly recommends that Software Data Protection (SDP) always be enabled. The SST29EE/LE/VE010 should be programmed using the SDP command sequence. SST recommends the SDP Disable Command Sequence not be issued to the device prior to writing.

Please refer to the following Application Notes for more information on using SDP:

- *Protecting Against Unintentional Writes When Using Single Power Supply Flash Memories*
- *The Proper Use of JEDEC Standard Software Data Protection*



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Product Identification

The product identification mode identifies the device as the SST29EE/LE/VE010 and manufacturer as SST. This mode is accessed via software. For details, see Table 4, Figure 11 for the software ID entry and read timing diagram and Figure 18, for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

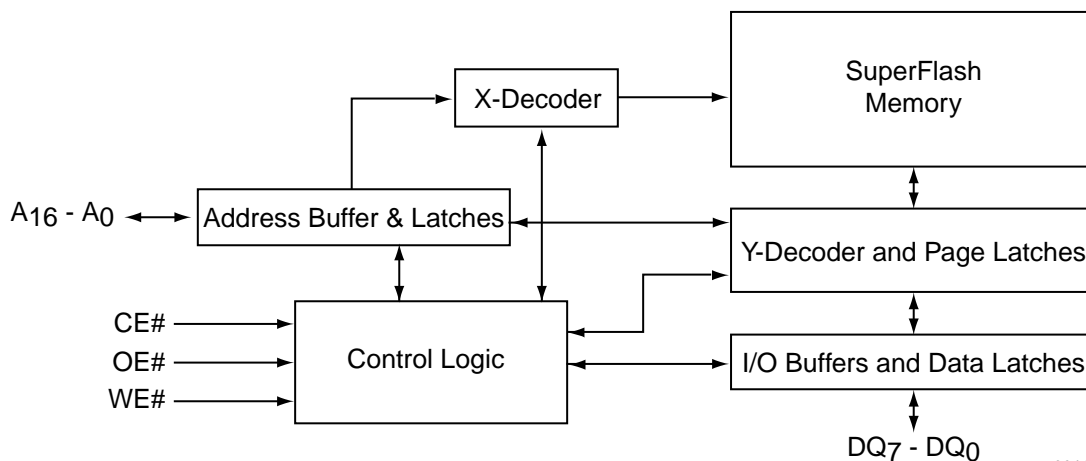
| | Address | Data |
|-------------------|---------|------|
| Manufacturer's ID | 0000H | BFH |
| Device ID | | |
| SST29EE010 | 0001H | 07H |
| SST29LE010 | 0001H | 08H |
| SST29VE010 | 0001H | 08H |

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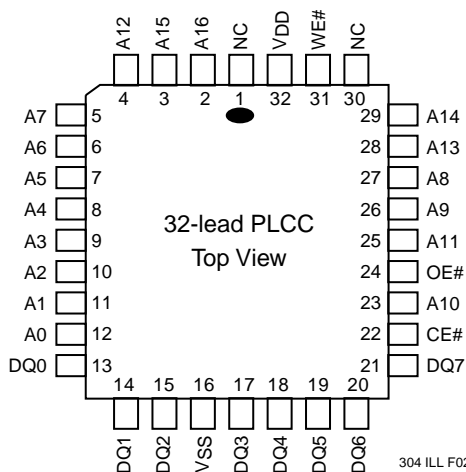
Product Identification Mode Exit

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Software ID Exit (reset) operation, which returns the device to the Read operation. The Reset operation may also be used to reset the device to the Read mode after an inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. See Table 4 for software command codes, Figure 12 for timing waveform, and Figure 18 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM



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FIGURE 1: PIN ASSIGNMENTS FOR 32-LEAD PLCC



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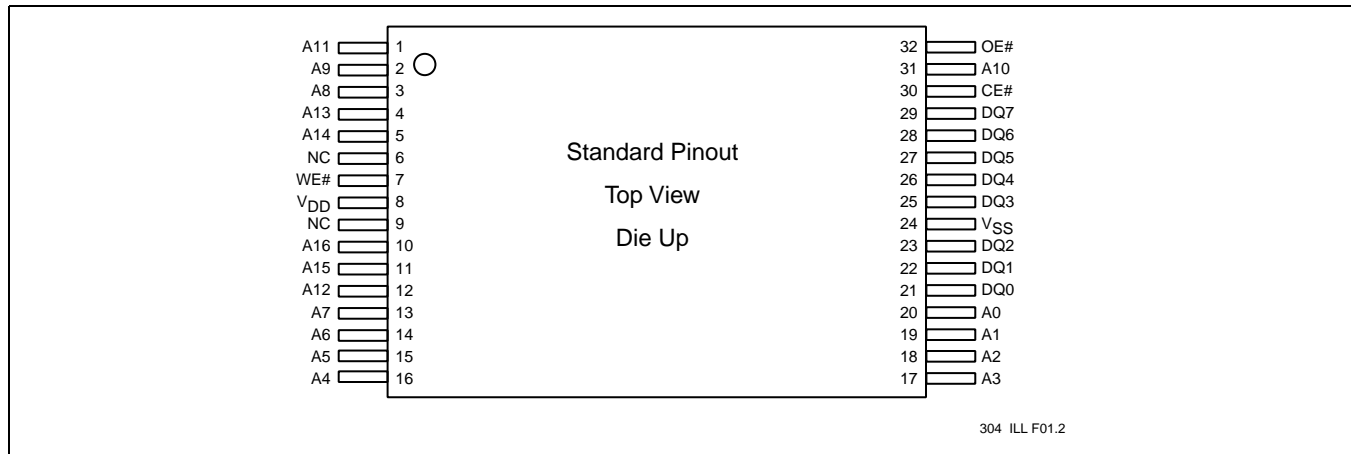


FIGURE 2: PIN ASSIGNMENTS FOR 32-LEAD TSOP

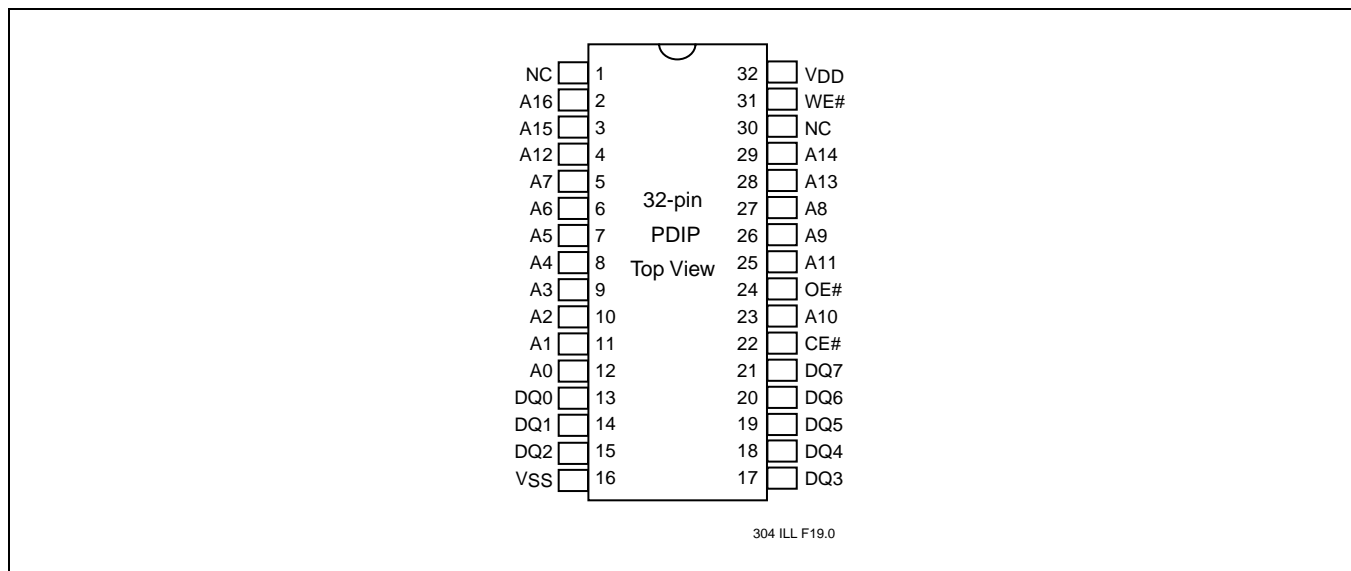


FIGURE 3: PIN ASSIGNMENTS FOR 32-PIN PDIP

TABLE 2: PIN DESCRIPTION

| Symbol | Pin Name | Functions |
|----------------------------------|-----------------------|--|
| A ₁₆ -A ₇ | Row Address Inputs | To provide memory addresses. Row addresses define a page for a Write cycle. |
| A ₆ -A ₀ | Column Address Inputs | Column Addresses are toggled to load page data |
| DQ ₇ -DQ ₀ | Data Input/output | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high. |
| CE# | Chip Enable | To activate the device when CE# is low. |
| OE# | Output Enable | To gate the data output buffers. |
| WE# | Write Enable | To control the Write operations. |
| V _{DD} | Power Supply | To provide: 5.0V supply (±10%) for SST29EE010 3.0V supply (3.0-3.6V) for SST29LE010 2.7V supply (2.7-3.6V) for SST29VE010 |
| V _{SS} | Ground | |
| NC | No Connection | Unconnected pins. |

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TABLE 3: OPERATION MODES SELECTION

| Mode | CE# | OE# | WE# | DQ | Address |
|------------------------|-----------------|-----------------|-----------------|---|-------------------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | D _{OUT} | A _{IN} |
| Page-Write | V _{IL} | V _{IH} | V _{IL} | D _{IN} | A _{IN} |
| Standby | V _{IH} | X ¹ | X | High Z | X |
| Write Inhibit | X | V _{IL} | X | High Z/ D _{OUT} | X |
| | X | X | V _{IH} | High Z/ D _{OUT} | X |
| Software Chip-Erase | V _{IL} | V _{IH} | V _{IL} | D _{IN} | A _{IN} , See Table 4 |
| Product Identification | | | | | |
| Software Mode | V _{IL} | V _{IH} | V _{IL} | Manufacturer's ID (BFH) Device ID ² | See Table 4 |
| SDP Enable Mode | V _{IL} | V _{IH} | V _{IL} | | See Table 4 |
| SDP Disable Mode | V _{IL} | V _{IH} | V _{IL} | | See Table 4 |

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1. X can be V_{IL} or V_{IH}, but no other value.
2. Device ID = 07H for SST29EE010 and 08H for SST29LE/VE010

TABLE 4: SOFTWARE COMMAND SEQUENCE

| Command Sequence | 1st Bus Write Cycle | | 2nd Bus Write Cycle | | 3rd Bus Write Cycle | | 4th Bus Write Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|---|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|---------------------|------|
| | Addr ¹ | Data | Addr ¹ | Data | Addr ¹ | Data | Addr ¹ | Data | Addr ¹ | Data | Addr ¹ | Data |
| Software Data Protect Enable & Page-Write | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | Addr ² | Data | | | | |
| Software Data Protect Disable | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 20H |
| Software Chip-Erase ³ | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| Software ID Entry ^{4,5} | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | | | | | | |
| Software ID Exit | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | | | | | | |
| Alternate Software ID Entry ⁶ | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 60H |

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1. Address format A₁₄-A₀ (Hex), Addresses A₁₅ and A₁₆ can be V_{IL} or V_{IH}, but no other value."
2. Page-Write consists of loading up to 128 Bytes (A₆-A₀)
3. The software Chip-Erase function is not supported by the industrial temperature part. Please contact SST if you require this function for an industrial temperature part.
4. The device does not remain in Software Product ID Mode if powered down.
5. With A₁₄-A₁ = 0; SST Manufacturer's ID= BFH, is read with A₀ = 0,
SST29EE010 Device ID = 07H, is read with A₀ = 1
SST29LE/VE010 Device ID = 08H, is read with A₀ = 1
6. Alternate six-byte Software Product ID Command Code

Note: This product supports both the JEDEC standard three-byte command code sequence and SST's original six-byte command code sequence. For new designs, SST recommends that the three-byte command code sequence be used.



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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

| | |
|---|--------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| D. C. Voltage on Any Pin to Ground Potential | -0.5V to $V_{DD} + 0.5V$ |
| Transient Voltage (<20 ns) on Any Pin to Ground Potential | -1.0V to $V_{DD} + 1.0V$ |
| Voltage on A ₉ Pin to Ground Potential | -0.5V to 14.0V |
| Package Power Dissipation Capability (Ta = 25°C) | 1.0W |
| Through Hold Lead Soldering Temperature (10 Seconds) | 300°C |
| Surface Mount Lead Soldering Temperature (3 Seconds) | 240°C |
| Output Short Circuit Current ¹ | 100 mA |

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE FOR SST29EE010

| Range | Ambient Temp | V _{DD} |
|------------|----------------|-----------------|
| Commercial | 0°C to +70°C | 5.0V±10% |
| Industrial | -40°C to +85°C | 5.0V±10% |

OPERATING RANGE FOR SST29LE010

| Range | Ambient Temp | V _{DD} |
|------------|----------------|-----------------|
| Commercial | 0°C to +70°C | 3.0-3.6V |
| Industrial | -40°C to +85°C | 3.0-3.6V |

OPERATING RANGE FOR SST29VE010

| Range | Ambient Temp | V _{DD} |
|------------|----------------|-----------------|
| Commercial | 0°C to +70°C | 2.7-3.6V |
| Industrial | -40°C to +85°C | 2.7-3.6V |

AC CONDITIONS OF TEST

| | |
|-----------------------|--|
| Input Rise/Fall Time | 10 ns |
| Output Load | 1 TTL Gate and C _L = 100 pF |
| See Figures 13 and 14 | |



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TABLE 5: DC OPERATING CHARACTERISTICS $V_{DD} = 5.0V \pm 10\%$ FOR SST29EE010

| Symbol | Parameter | Limits | | | Test Conditions |
|------------------|---------------------------------------|--------|-----|---------|---|
| | | Min | Max | Units | |
| I _{DD} | Power Supply Current | | | | Address input= V_{IL}/V_{IH} , at $f=1/T_{RC}$ Min, $V_{DD}=V_{DD}$ Max |
| | Read | | 30 | mA | $CE\#=OE\#=V_{IL}$, $WE\#=V_{IH}$, all I/Os open |
| | Write | | 50 | mA | $CE\#=WE\#=V_{IL}$, $OE\#=V_{IH}$, $V_{DD}=V_{DD}$ Max |
| I _{SB1} | Standby V_{DD} Current (TTL input) | | 3 | mA | $CE\#=OE\#=WE\#=V_{IH}$, $V_{DD}=V_{DD}$ Max |
| I _{SB2} | Standby V_{DD} Current (CMOS input) | | 50 | μ A | $CE\#=OE\#=WE\#=V_{DD} - 0.3V$, $V_{DD}=V_{DD}$ Max |
| I _{LI} | Input Leakage Current | | 1 | μ A | $V_{IN} = GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max |
| I _{LO} | Output Leakage Current | | 10 | μ A | $V_{OUT} = GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max |
| V _{IL} | Input Low Voltage | | 0.8 | V | $V_{DD}=V_{DD}$ Min |
| V _{IH} | Input High Voltage | 2.0 | | V | $V_{DD}=V_{DD}$ Max |
| V _{OL} | Output Low Voltage | | 0.4 | V | $I_{OL}=2.1$ mA, $V_{DD}=V_{DD}$ Min |
| V _{OH} | Output High Voltage | 2.4 | | V | $I_{OH}=-400$ μ A, $V_{DD}=V_{DD}$ Min |

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TABLE 6: DC OPERATING CHARACTERISTICS $V_{DD} = 3.0-3.6V$ FOR SST29LE010 AND $2.7-3.0V$ FOR SST29VE010

| Symbol | Parameter | Limits | | | Test Conditions |
|------------------|---------------------------------------|--------|-----|---------|---|
| | | Min | Max | Units | |
| I _{DD} | Power Supply Current | | | | Address input= V_{IL}/V_{IH} , at $f=1/T_{RC}$ Min, $V_{DD}=V_{DD}$ Max |
| | Read | | 12 | mA | $CE\#=OE\#=V_{IL}$, $WE\#=V_{IH}$, all I/Os open |
| | Write | | 15 | mA | $CE\#=WE\#=V_{IL}$, $OE\#=V_{IH}$, $V_{DD}=V_{DD}$ Max |
| I _{SB1} | Standby V_{DD} Current (TTL input) | | 1 | mA | $CE\#=OE\#=WE\#=V_{IH}$, $V_{DD}=V_{DD}$ Max |
| I _{SB2} | Standby V_{DD} Current (CMOS input) | | 15 | μ A | $CE\#=OE\#=WE\#=V_{DD} - 0.3V$, $V_{DD}=V_{DD}$ Max |
| I _{LI} | Input Leakage Current | | 1 | μ A | $V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max |
| I _{LO} | Output Leakage Current | | 10 | μ A | $V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max |
| V _{IL} | Input Low Voltage | | 0.8 | V | $V_{DD}=V_{DD}$ Min |
| V _{IH} | Input High Voltage | 2.0 | | V | $V_{DD}=V_{DD}$ Max |
| V _{OL} | Output Low Voltage | | 0.4 | V | $I_{OL}=100$ μ A, $V_{DD}=V_{DD}$ Min |
| V _{OH} | Output High Voltage | 2.4 | | V | $I_{OH}=-100$ μ A, $V_{DD}=V_{DD}$ Min |

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TABLE 7: RECOMMENDED SYSTEM POWER-UP TIMINGS

| Symbol | Parameter | Minimum | Units |
|------------------|-----------------------------|---------|---------|
| $T_{PU-READ}^1$ | Power-up to Read Operation | 100 | μ s |
| $T_{PU-WRITE}^1$ | Power-up to Write Operation | 5 | ms |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

| Parameter | Description | Test Condition | Maximum |
|-------------|---------------------|----------------|---------|
| $C_{I/O}^1$ | I/O Pin Capacitance | $V_{I/O} = 0V$ | 12 pF |
| C_{IN}^1 | Input Capacitance | $V_{IN} = 0V$ | 6 pF |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|-------------|----------------|-----------------------|--------|---------------------|
| N_{END}^1 | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| T_{DR}^1 | Data Retention | 100 | Years | JEDEC Standard A103 |
| I_{LTH}^1 | Latch Up | 100 | mA | JEDEC Standard 78 |

T9.5 304

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



AC CHARACTERISTICS

TABLE 10: READ CYCLE TIMING PARAMETERS FOR SST29EE010

| Symbol | Parameter | SST29EE010-70 | | SST29EE010-90 | | Units |
|-------------------------------|---------------------------------|---------------|-----|---------------|-----|-------|
| | | Min | Max | Min | Max | |
| T _{RC} | Read Cycle Time | 70 | | 90 | | ns |
| T _{CE} | Chip Enable Access Time | | 70 | | 90 | ns |
| T _{AA} | Address Access Time | | 70 | | 90 | ns |
| T _{OE} | Output Enable Access Time | | 30 | | 40 | ns |
| T _{CLZ} ¹ | CE# Low to Active Output | 0 | | 0 | | ns |
| T _{OLZ} ¹ | OE# Low to Active Output | 0 | | 0 | | ns |
| T _{CHZ} ¹ | CE# High to High-Z Output | | 20 | | 30 | ns |
| T _{OHZ} ¹ | OE# High to High-Z Output | | 20 | | 30 | ns |
| T _{OH} ¹ | Output Hold from Address Change | 0 | | 0 | | ns |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11: READ CYCLE TIMING PARAMETERS FOR SST29LE010

| Symbol | Parameter | SST29LE010-150 | | SST29LE010-200 | | Units |
|-------------------------------|---------------------------------|----------------|-----|----------------|-----|-------|
| | | Min | Max | Min | Max | |
| T _{RC} | Read Cycle Time | 150 | | 200 | | ns |
| T _{CE} | Chip Enable Access Time | | 150 | | 200 | ns |
| T _{AA} | Address Access Time | | 150 | | 200 | ns |
| T _{OE} | Output Enable Access Time | | 60 | | 100 | ns |
| T _{CLZ} ¹ | CE# Low to Active Output | 0 | | 0 | | ns |
| T _{OLZ} ¹ | OE# Low to Active Output | 0 | | 0 | | ns |
| T _{CHZ} ¹ | CE# High to High-Z Output | | 30 | | 50 | ns |
| T _{OHZ} ¹ | OE# High to High-Z Output | | 30 | | 50 | ns |
| T _{OH} ¹ | Output Hold from Address Change | 0 | | 0 | | ns |

T11.1 304

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12: READ CYCLE TIMING PARAMETERS FOR SST29VE010

| Symbol | Parameter | SST29VE010-200 | | SST29VE010-250 | | Units |
|-------------------------------|---------------------------------|----------------|-----|----------------|-----|-------|
| | | Min | Max | Min | Max | |
| T _{RC} | Read Cycle Time | 200 | | 250 | | ns |
| T _{CE} | Chip Enable Access Time | | 200 | | 250 | ns |
| T _{AA} | Address Access Time | | 200 | | 250 | ns |
| T _{OE} | Output Enable Access Time | | 100 | | 120 | ns |
| T _{CLZ} ¹ | CE# Low to Active Output | 0 | | 0 | | ns |
| T _{OLZ} ¹ | OE# Low to Active Output | 0 | | 0 | | ns |
| T _{CHZ} ¹ | CE# High to High-Z Output | | 50 | | 50 | ns |
| T _{OHZ} ¹ | OE# High to High-Z Output | | 50 | | 50 | ns |
| T _{OH} ¹ | Output Hold from Address Change | 0 | | 0 | | ns |

T12.1 304

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



1 Mbit Page-Mode EEPROM

SST29EE010 / SST29LE010 / SST29VE010

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TABLE 13: PAGE-WRITE CYCLE TIMING PARAMETERS

| Symbol | Parameter | SST29EE010 | | SST29LE/VE010 | | Units |
|--------------------------------|----------------------------------|------------|-----|---------------|-----|-------|
| | | Min | Max | Min | Max | |
| T _{WC} | Write Cycle (Erase and Program) | | 10 | | 10 | ms |
| T _{AS} | Address Setup Time | 0 | | 0 | | ns |
| T _{AH} | Address Hold Time | 50 | | 70 | | ns |
| T _{CS} | WE# and CE# Setup Time | 0 | | 0 | | ns |
| T _{CH} | WE# and CE# Hold Time | 0 | | 0 | | ns |
| T _{OES} | OE# High Setup Time | 0 | | 0 | | ns |
| T _{OEH} | OE# High Hold Time | 0 | | 0 | | ns |
| T _{CP} | CE# Pulse Width | 70 | | 120 | | ns |
| T _{WP} | WE# Pulse Width | 70 | | 120 | | ns |
| T _{DS} | Data Setup Time | 35 | | 50 | | ns |
| T _{DH} ¹ | Data Hold Time | 0 | | 0 | | ns |
| T _{BLC} ¹ | Byte Load Cycle Time | 0.05 | 100 | 0.05 | 100 | μs |
| T _{BLCO} ¹ | Byte Load Cycle Time | 200 | | 200 | | μs |
| T _{IDA} ¹ | Software ID Access and Exit Time | | 10 | | 10 | μs |
| T _{SCE} | Software Chip-Erase | | 20 | | 20 | ms |

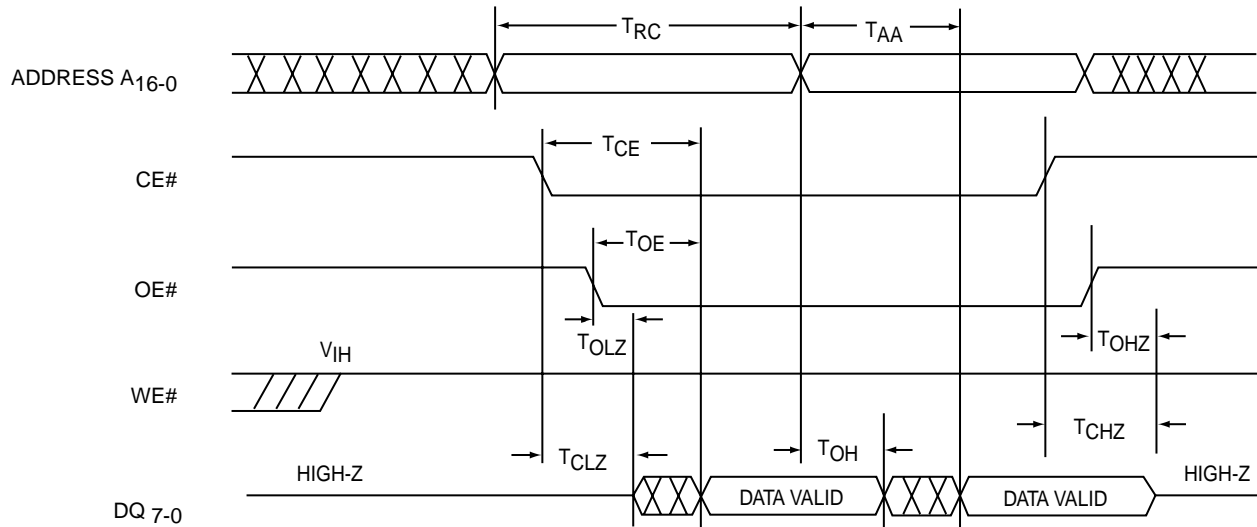
T13.5 304

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



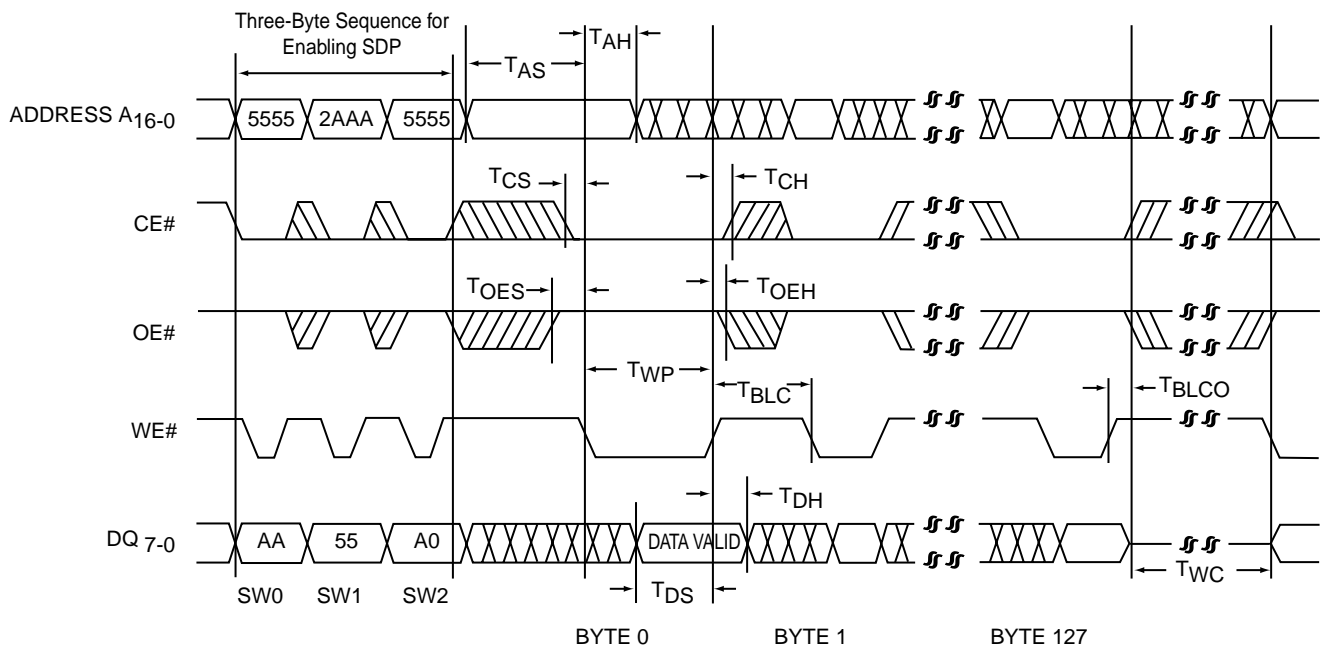
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304 ILL F03.0

FIGURE 4: READ CYCLE TIMING DIAGRAM



304 ILL F04.1

FIGURE 5: WE# CONTROLLED PAGE-WRITE CYCLE TIMING DIAGRAM



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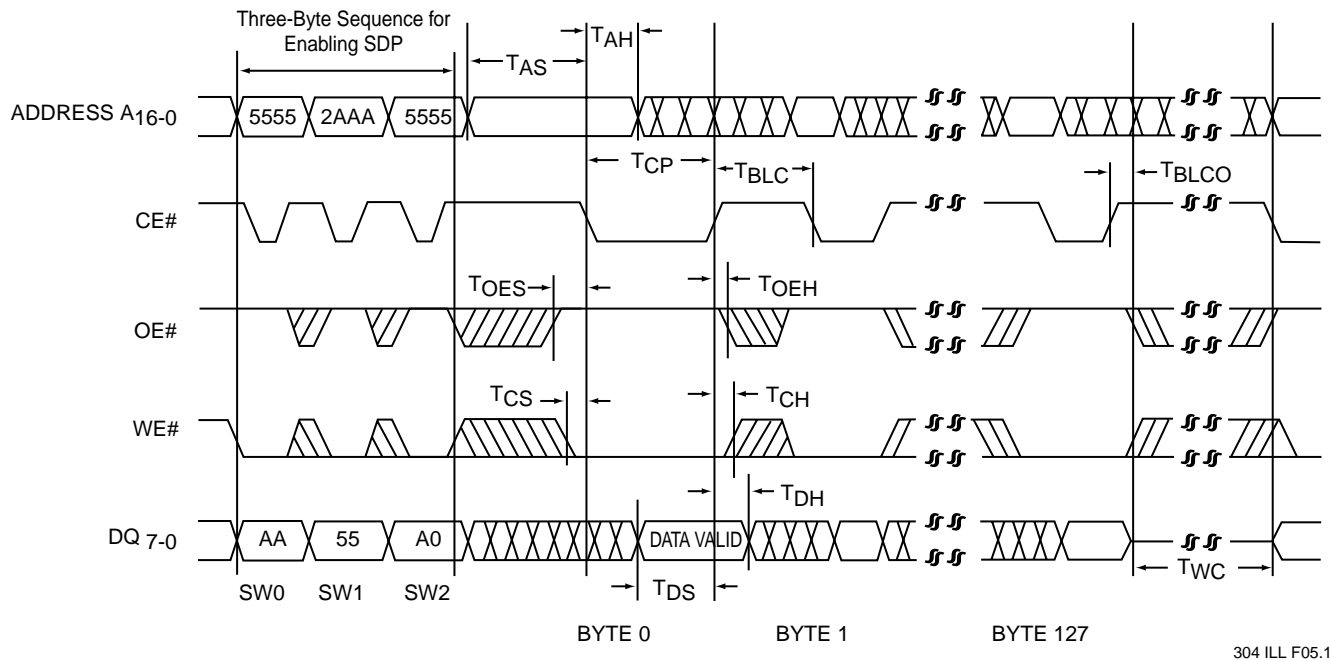


FIGURE 6: CE# CONTROLLED PAGE-WRITE CYCLE TIMING DIAGRAM

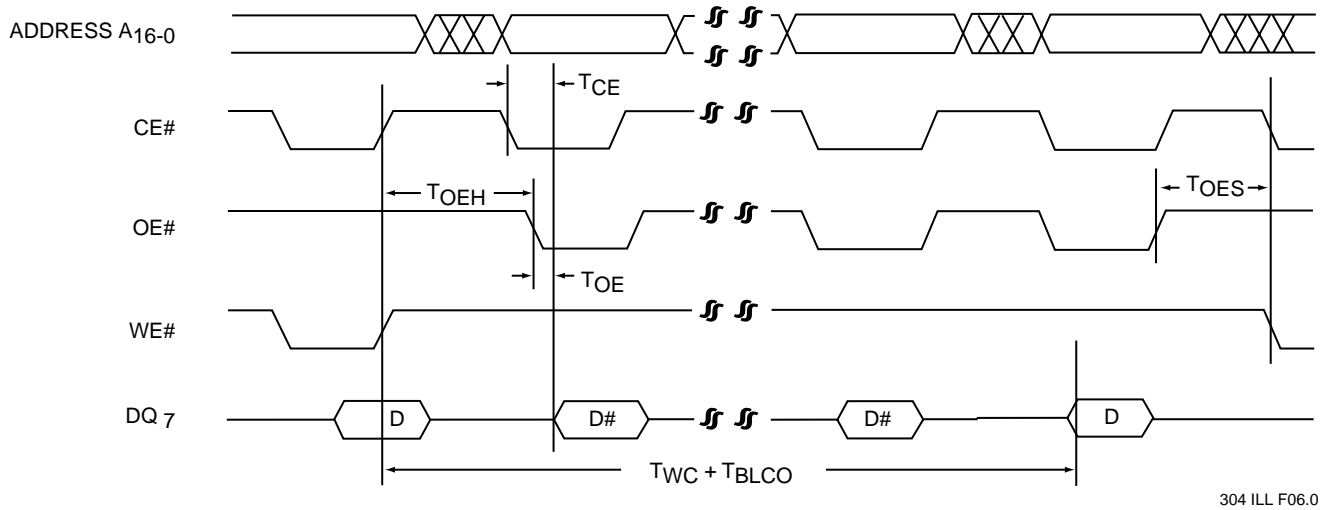


FIGURE 7: DATA# POLLING TIMING DIAGRAM



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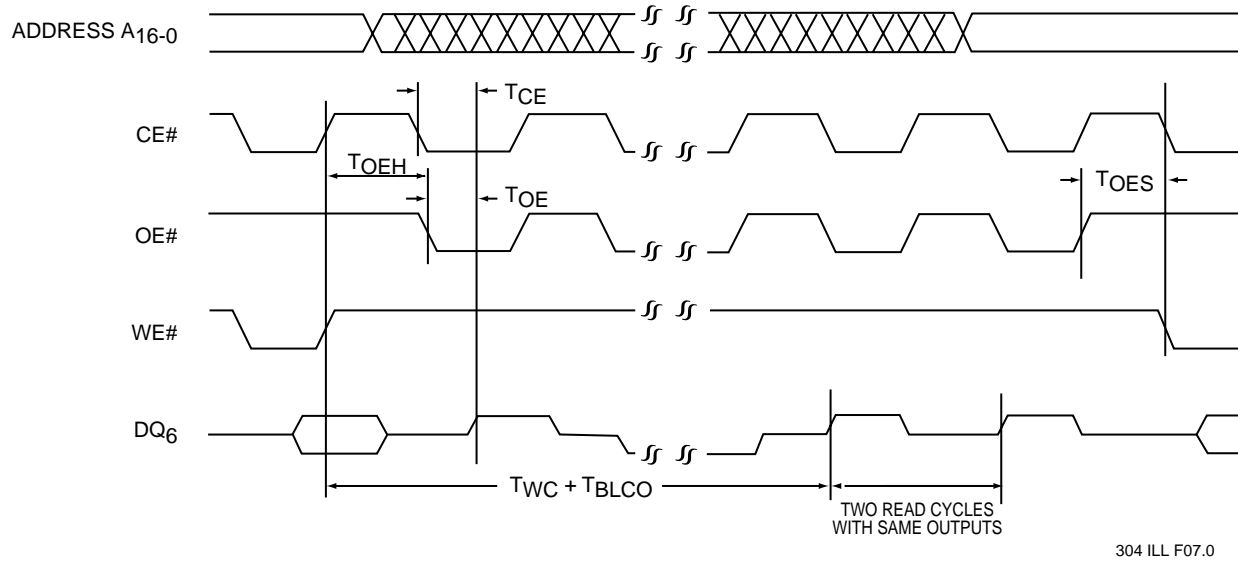


FIGURE 8: TOGGLE BIT TIMING DIAGRAM

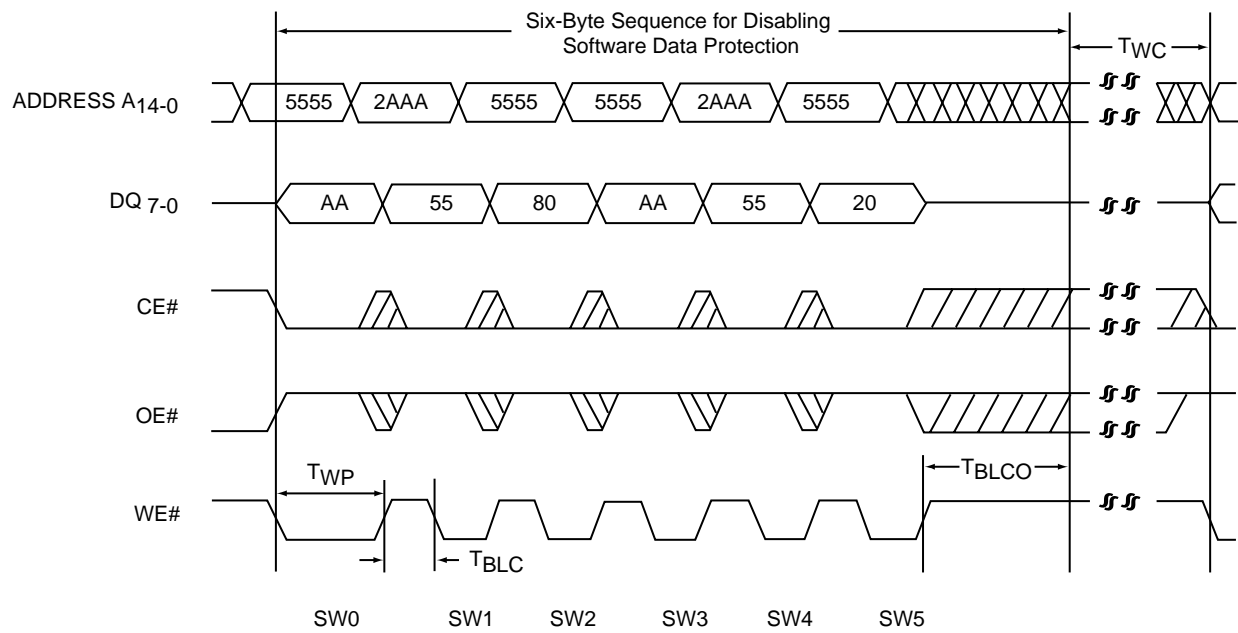
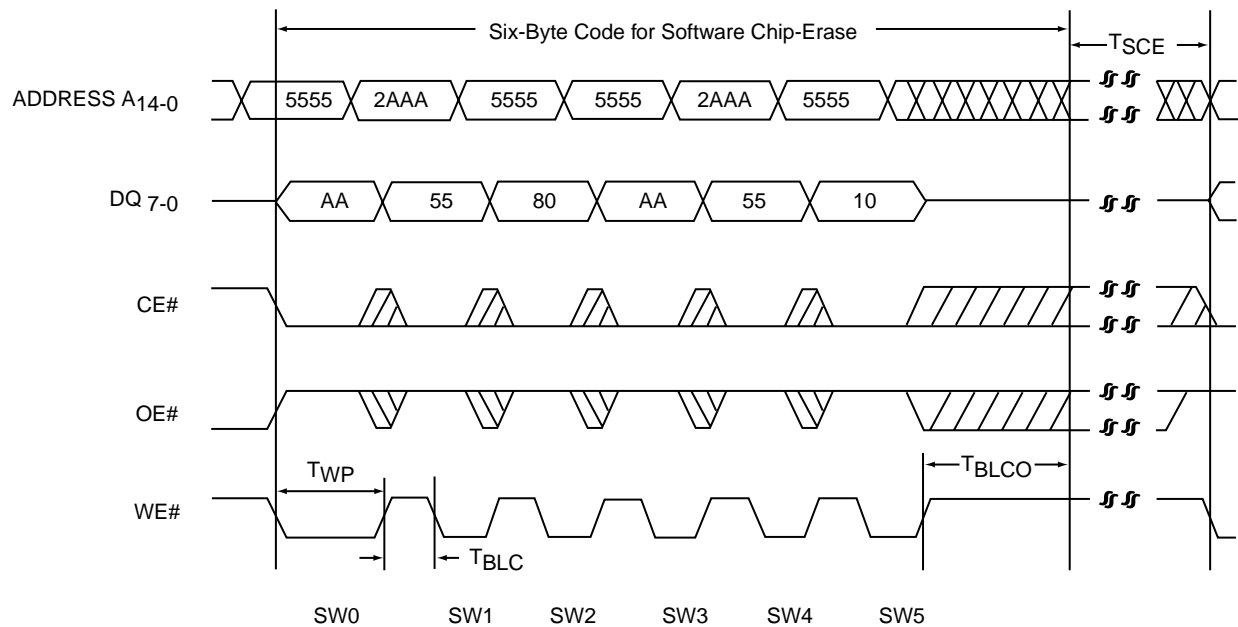


FIGURE 9: SOFTWARE DATA PROTECT DISABLE TIMING DIAGRAM



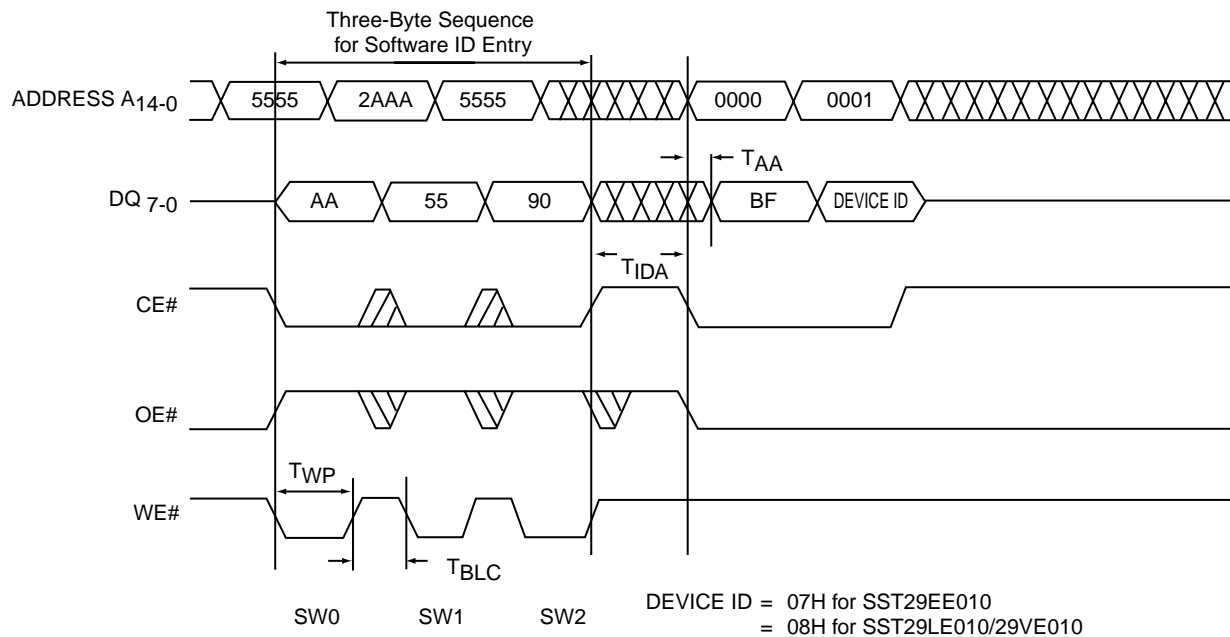
1 Mbit Page-Mode EEPROM SST29EE010 / SST29LE010 / SST29VE010

Data Sheet



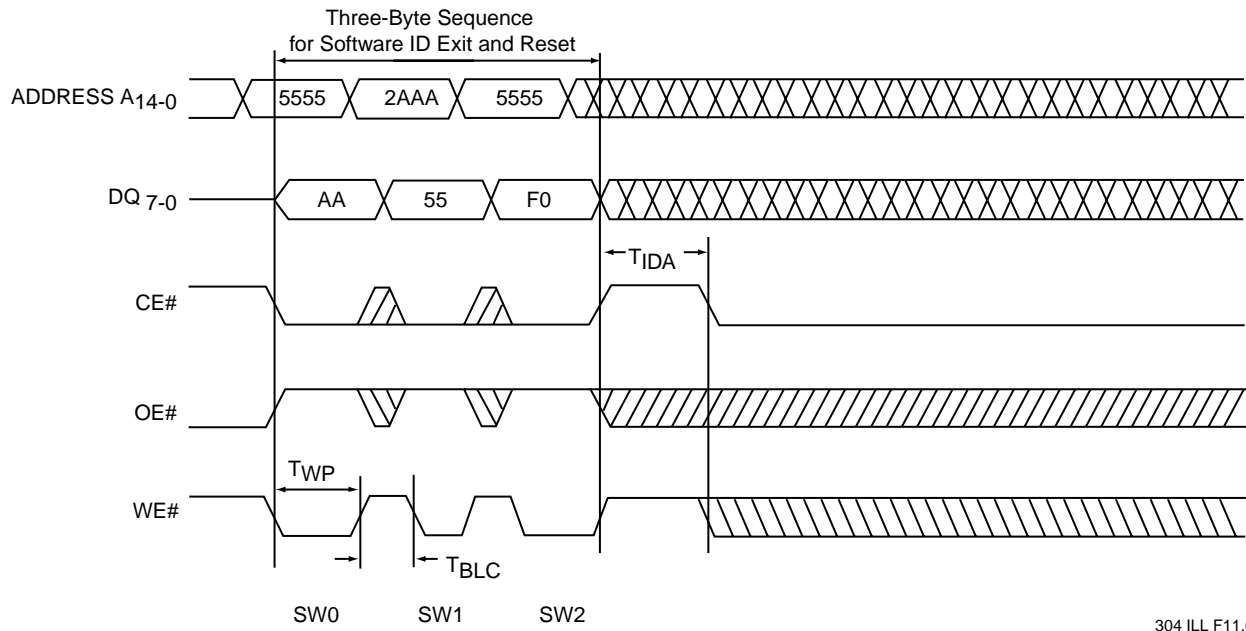
304 ILL F09.1

FIGURE 10: SOFTWARE CHIP-ERASE TIMING DIAGRAM



304 ILL F10.2

FIGURE 11: SOFTWARE ID ENTRY AND READ



304 ILL F11.0

FIGURE 12: SOFTWARE ID EXIT AND RESET



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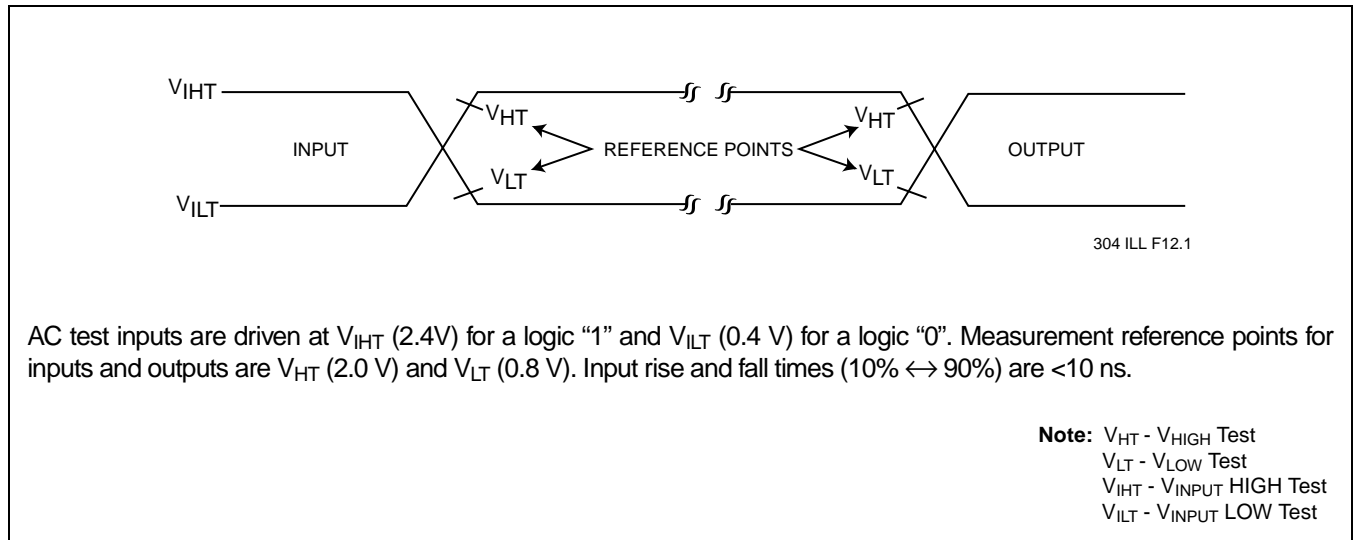


FIGURE 13: AC INPUT/OUTPUT REFERENCE WAVEFORMS

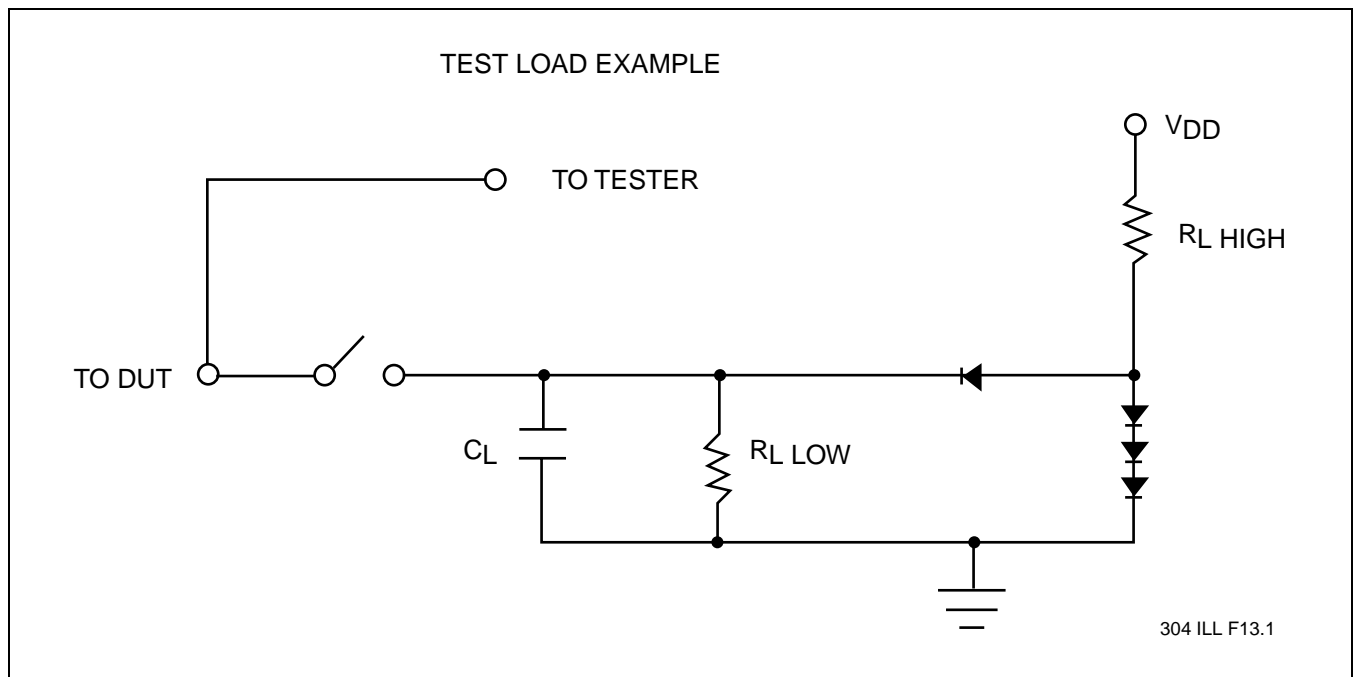


FIGURE 14: A TEST LOAD EXAMPLE

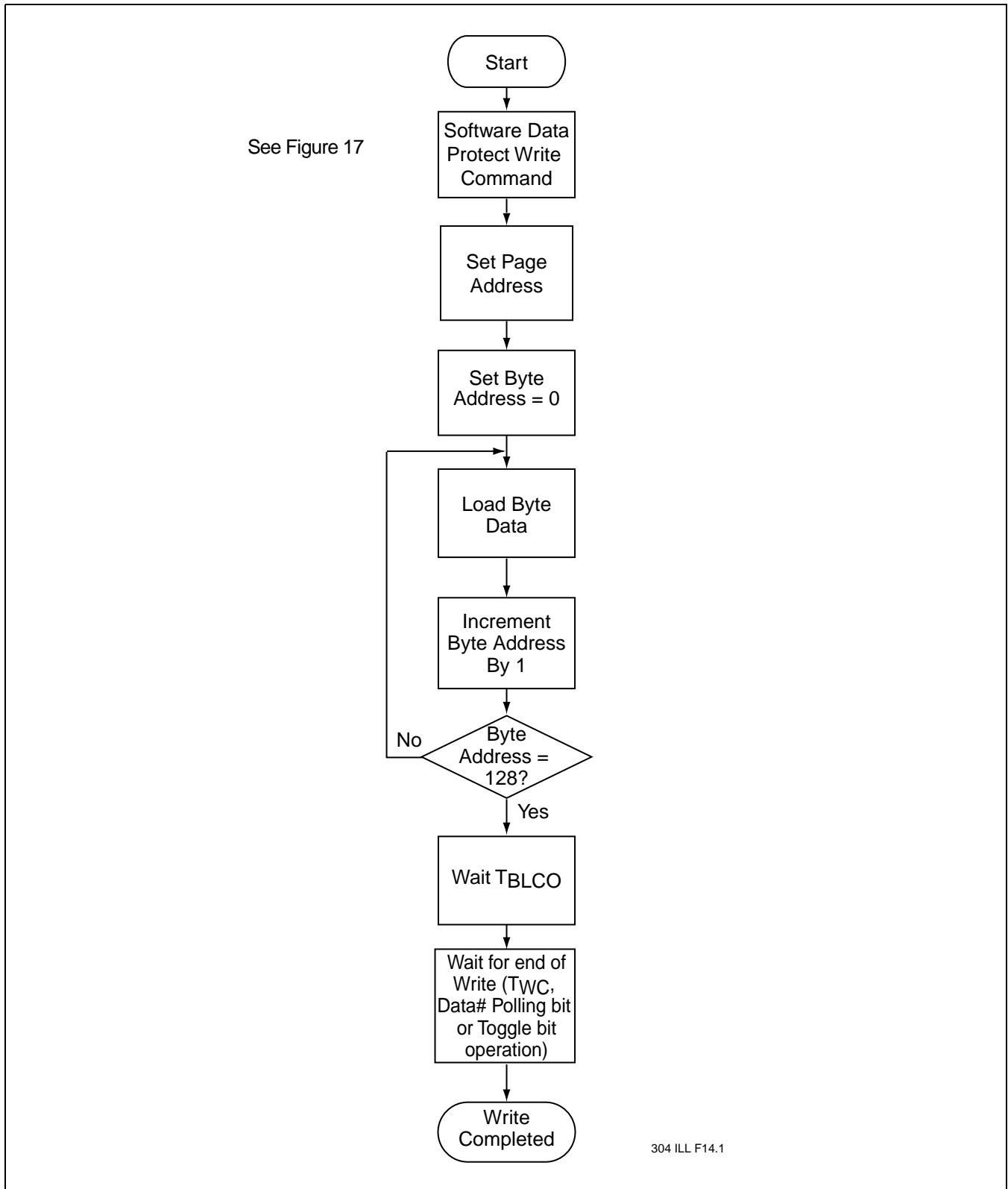


FIGURE 15: WRITE ALGORITHM



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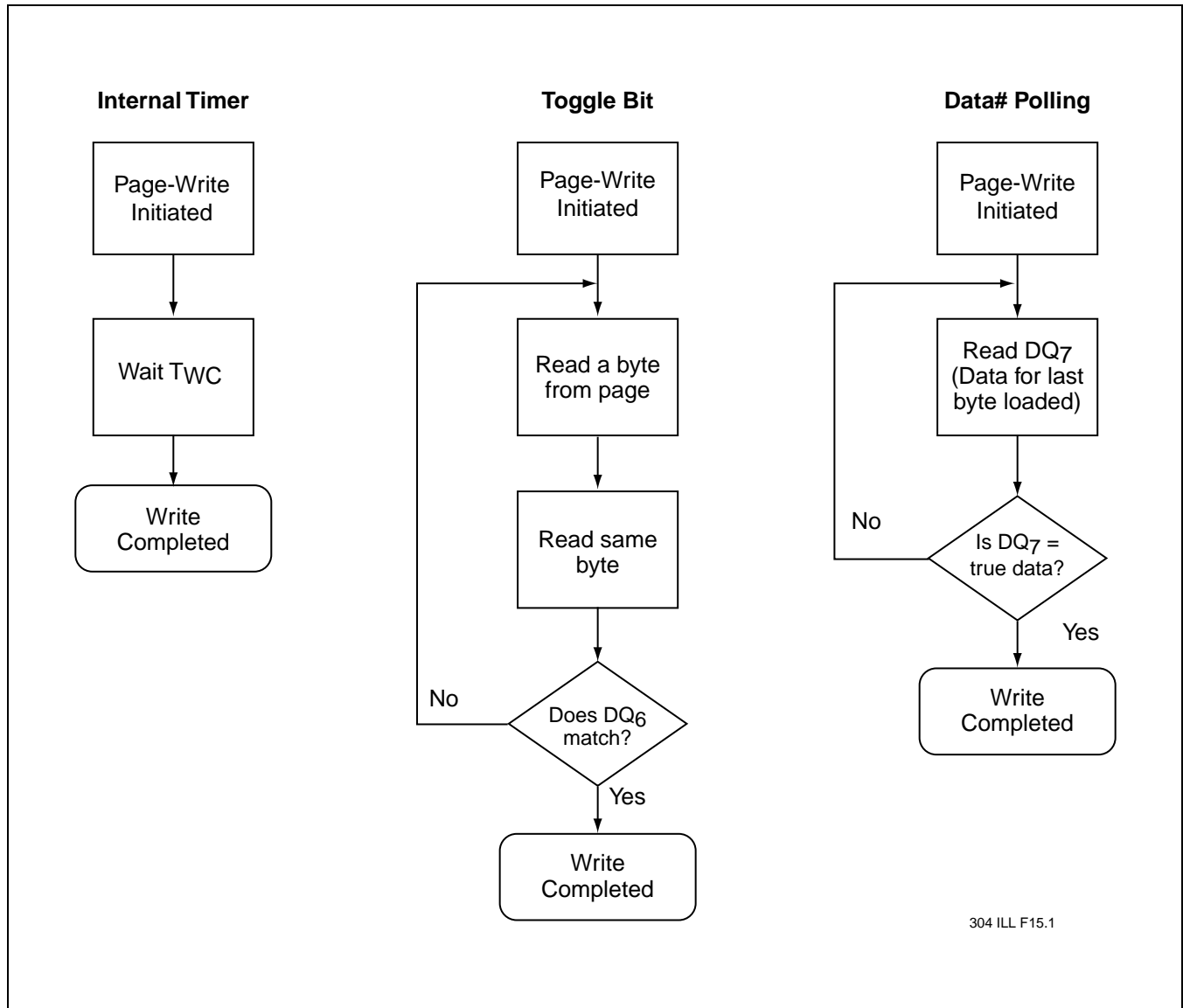


FIGURE 16: WAIT OPTIONS

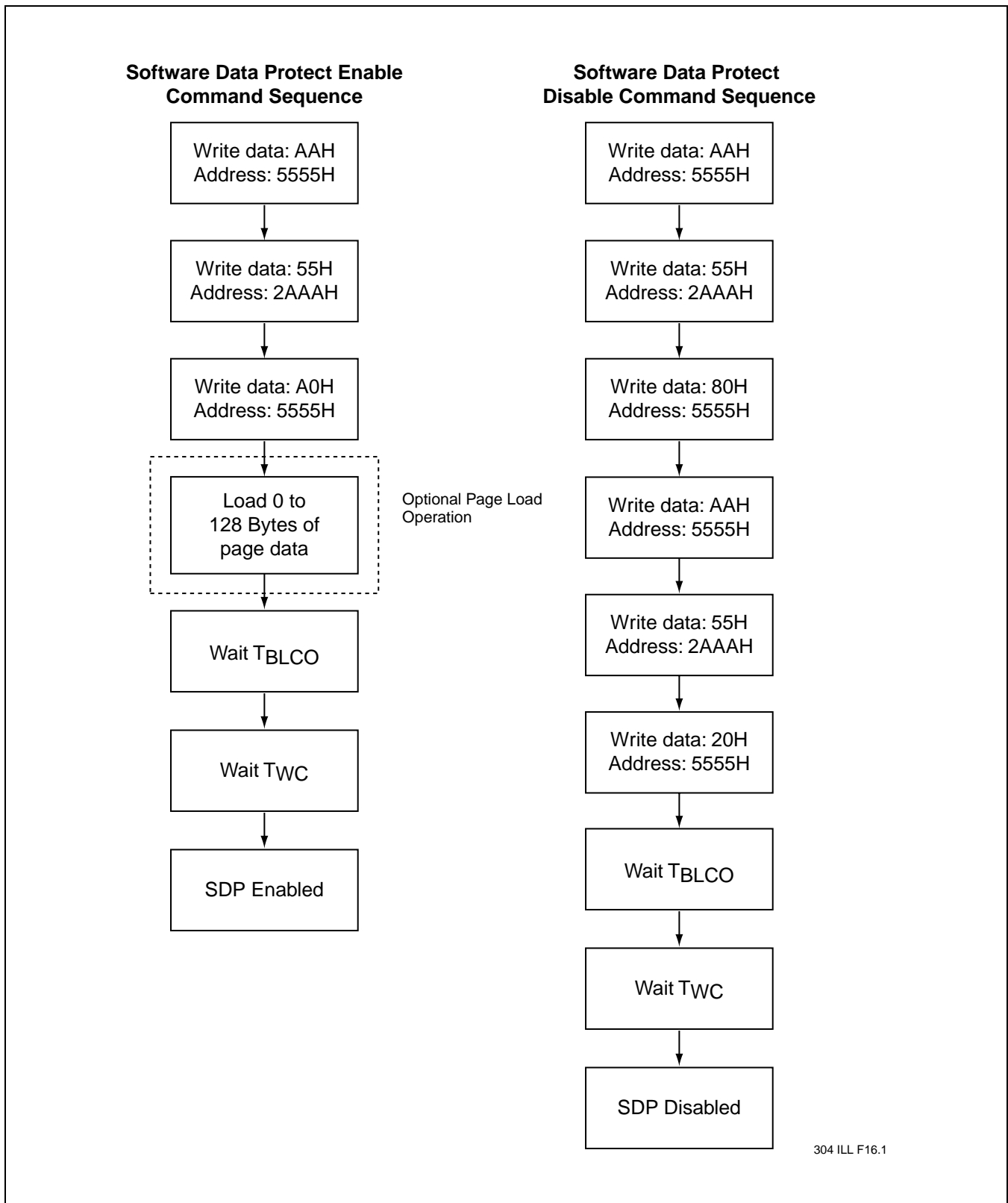


FIGURE 17: SOFTWARE DATA PROTECTION FLOWCHARTS



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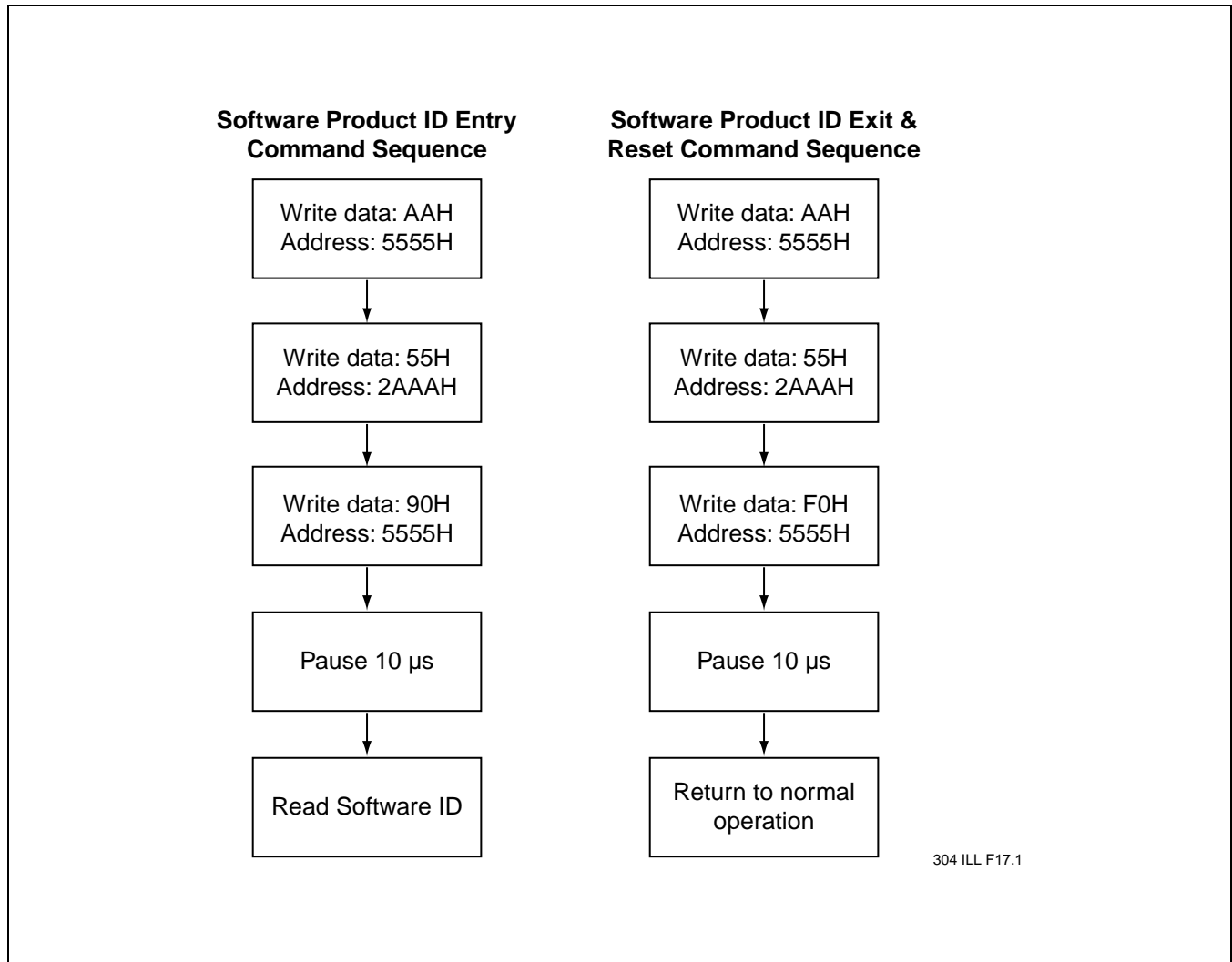


FIGURE 18: SOFTWARE PRODUCT COMMAND FLOWCHARTS

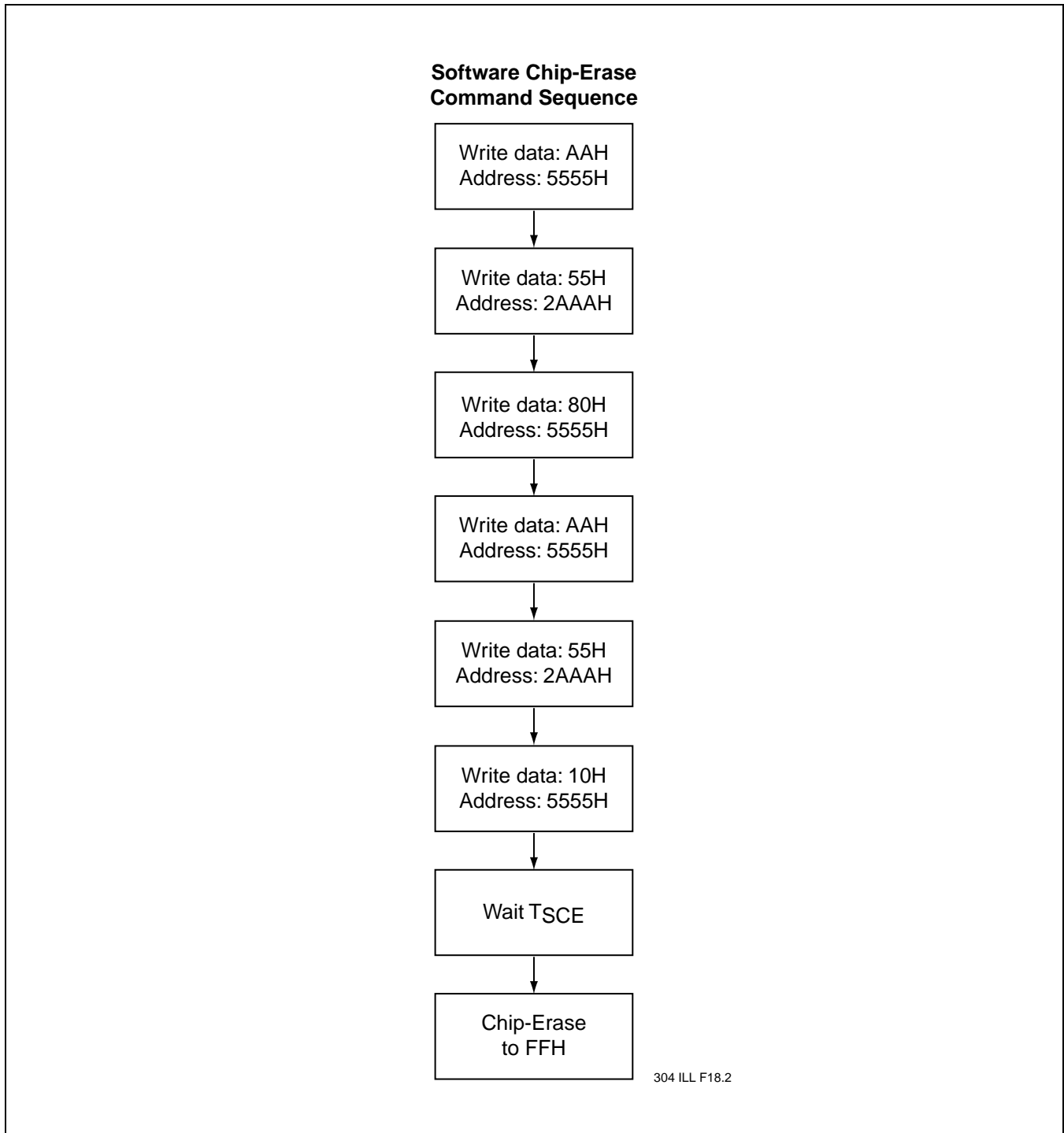


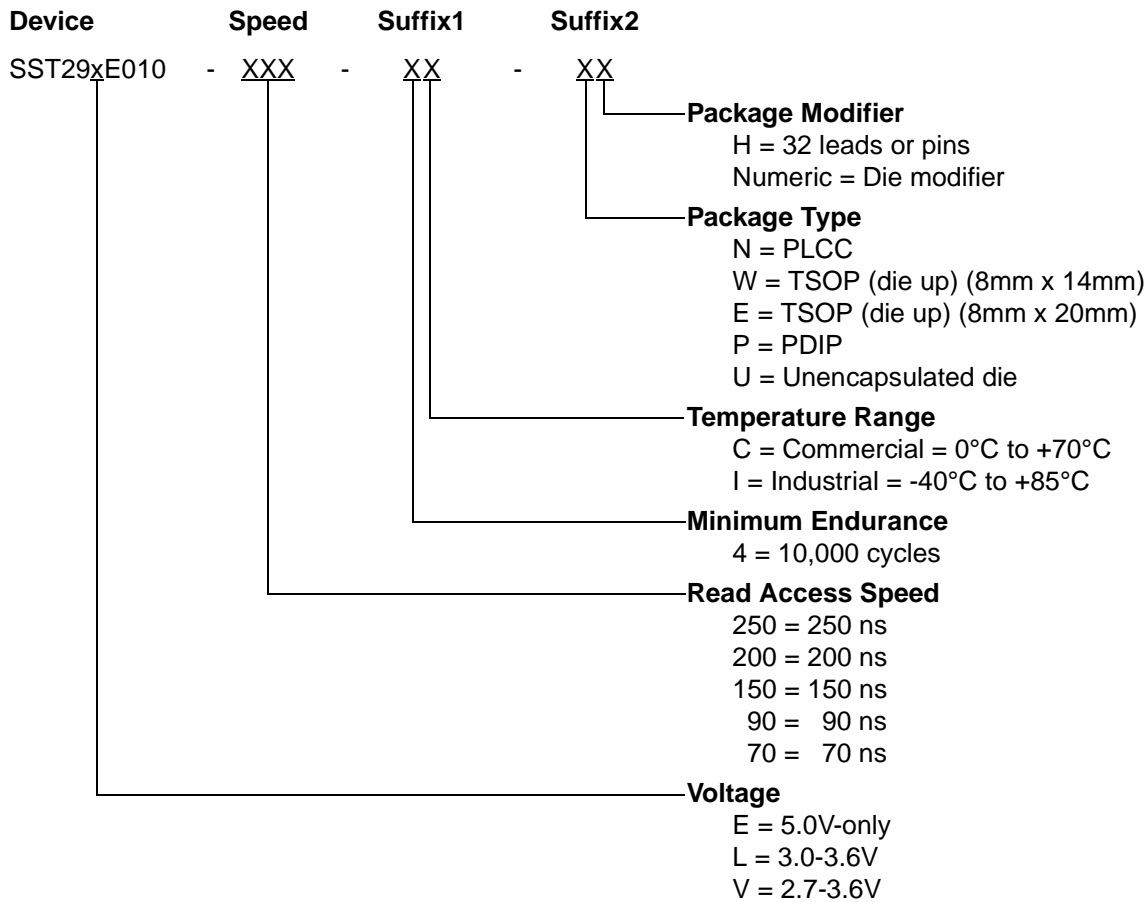
FIGURE 19: SOFTWARE CHIP-ERASE COMMAND CODES



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PRODUCT ORDERING INFORMATION





1 Mbit Page-Mode EEPROM SST29EE010 / SST29LE010 / SST29VE010

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Valid combinations for SST29EE010

| | | | |
|---------------------|---------------------|---------------------|---------------------|
| SST29EE010-70-4C-NH | SST29EE010-70-4C-WH | SST29EE010-70-4C-EH | SST29EE010-70-4C-PH |
| SST29EE010-90-4C-NH | SST29EE010-90-4C-WH | SST29EE010-90-4C-EH | SST29EE010-90-4C-PH |
| SST29EE010-70-4I-NH | SST29EE010-70-4I-WH | SST29EE010-70-4I-EH | |
| SST29EE010-90-4C-U2 | | | |

Valid combinations for SST29LE010

| | | |
|----------------------|----------------------|----------------------|
| SST29LE010-150-4C-NH | SST29LE010-150-4C-WH | SST29LE010-150-4C-EH |
| SST29LE010-150-4I-NH | SST29LE010-150-4I-WH | SST29LE010-150-4I-EH |
| SST29LE010-200-4C-U2 | | |

Valid combinations for SST29VE010

| | | |
|----------------------|----------------------|----------------------|
| SST29VE010-200-4C-NH | SST29VE010-200-4C-WH | SST29VE010-200-4C-EH |
| SST29VE010-200-4I-NH | SST29VE010-200-4I-WH | SST29VE010-200-4I-EH |
| SST29VE010-250-4C-U2 | | |

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

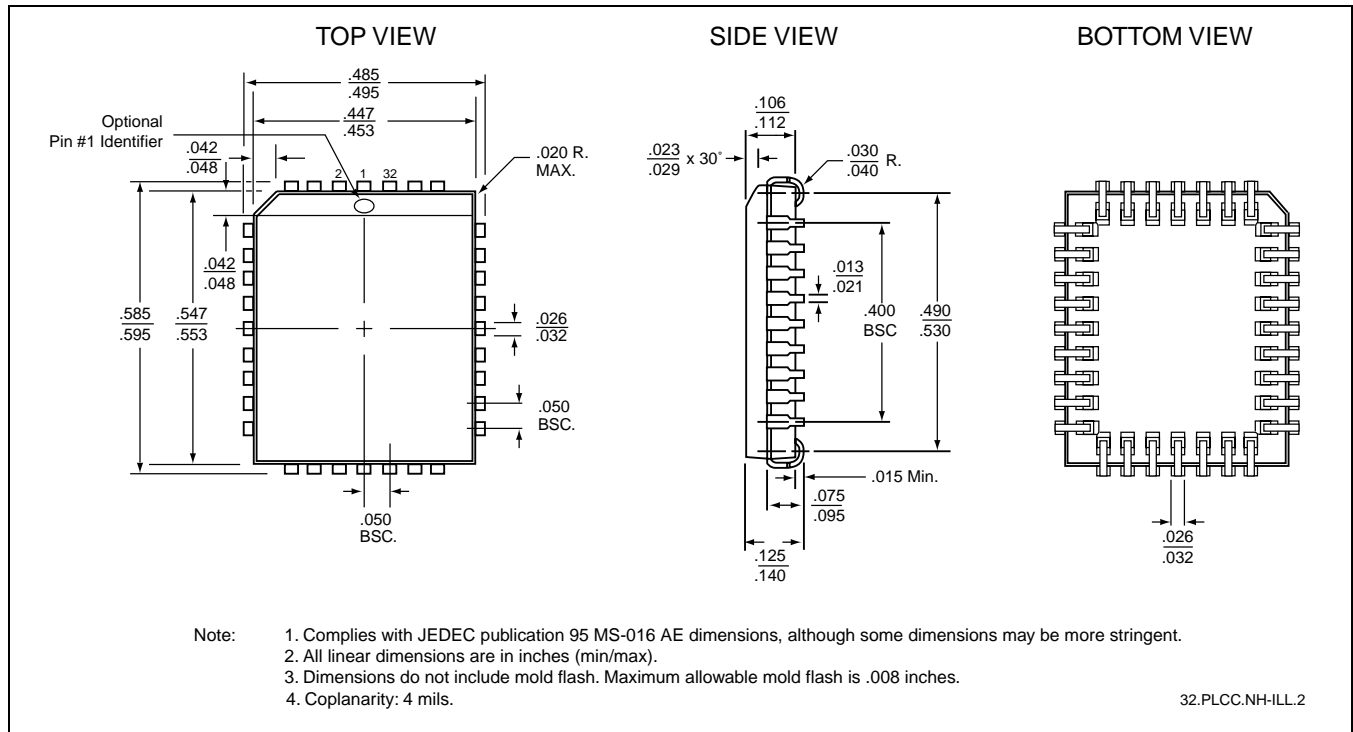
Note: The software Chip-Erase function is not supported by the industrial temperature part.
Please contact SST, if you require this function for an industrial temperature part.



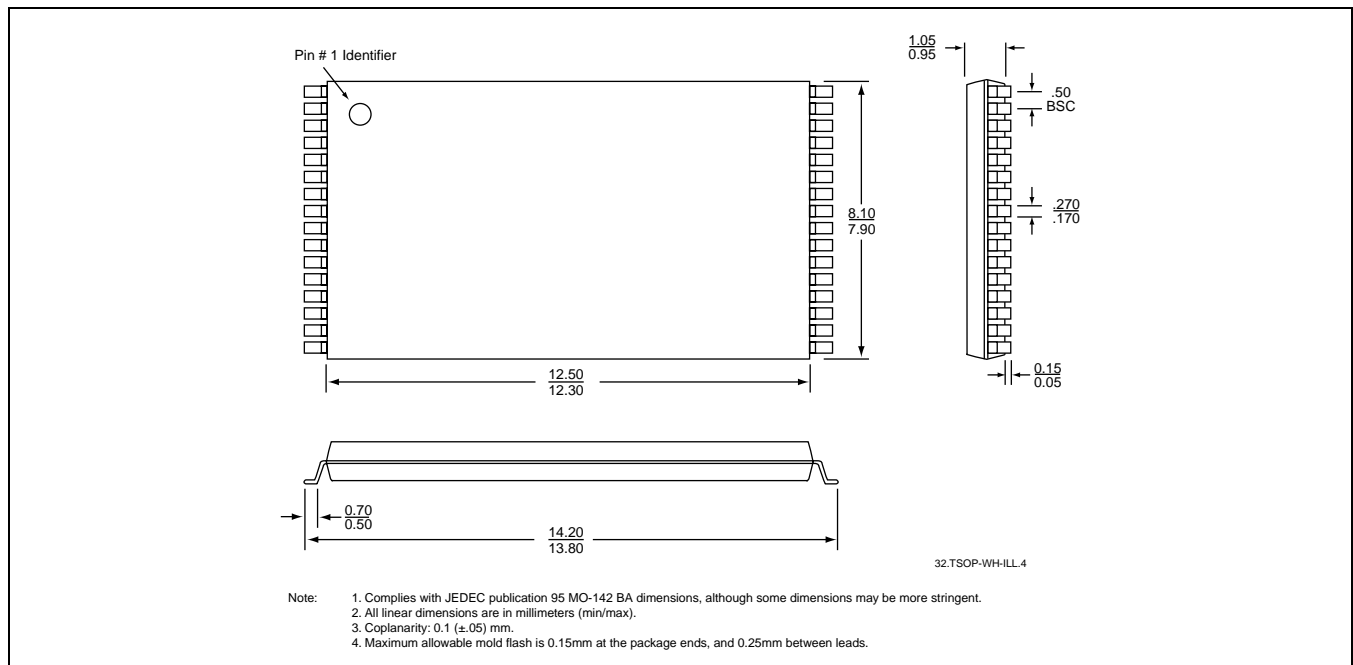
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PACKAGING DIAGRAMS



32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC) SST PACKAGE CODE: NH

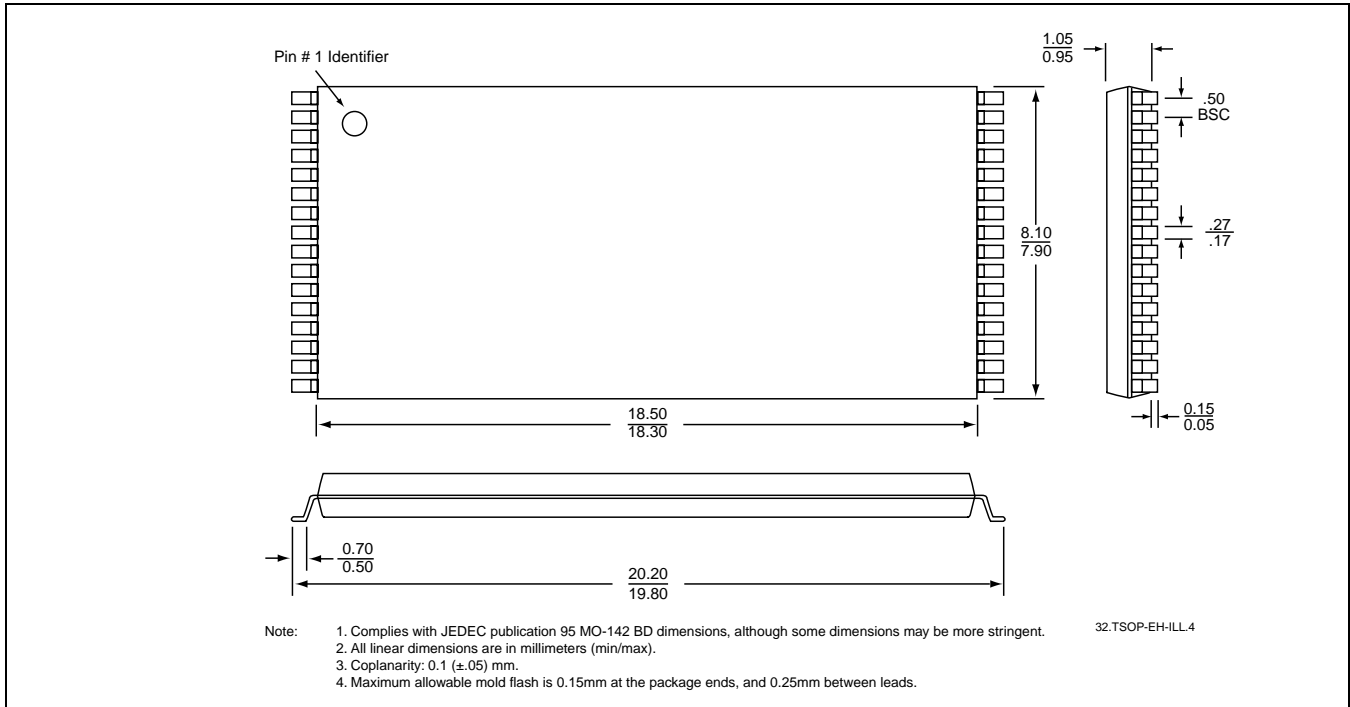


32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM SST PACKAGE CODE: WH

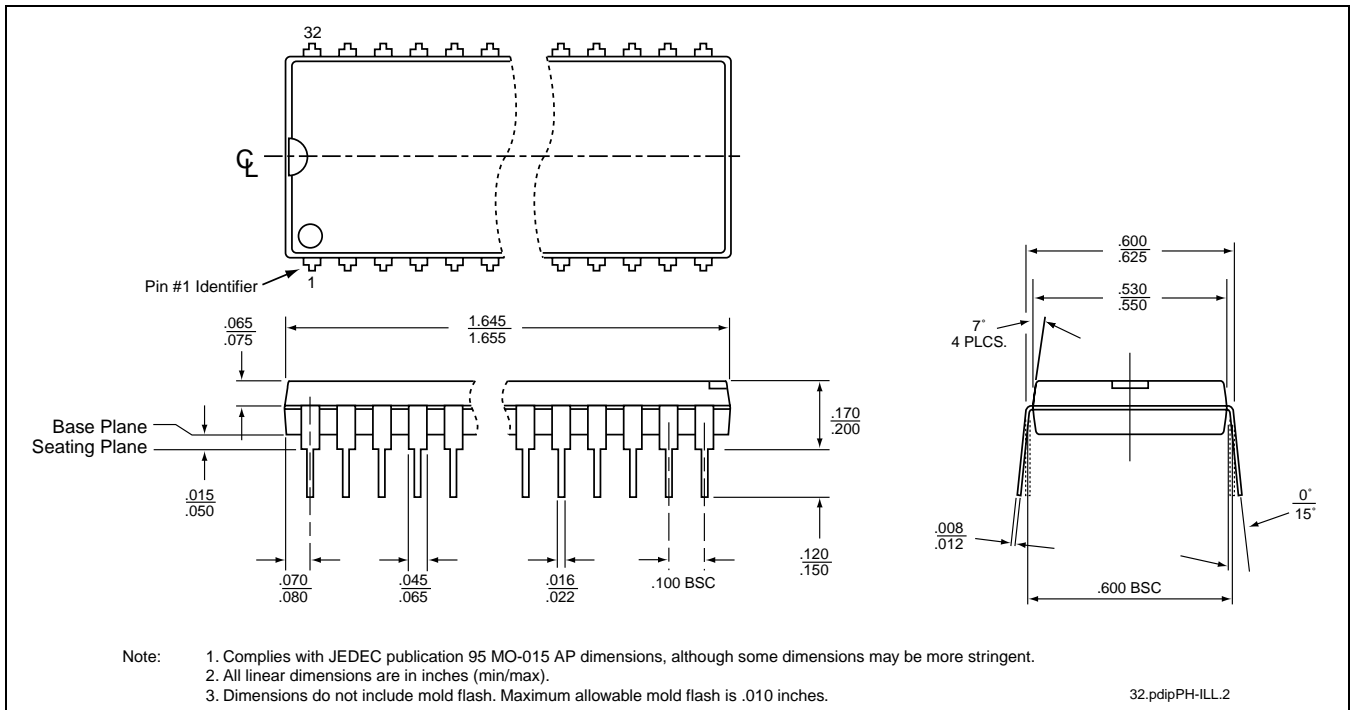


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32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 20MM
SST PACKAGE CODE: EH



32-PIN PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PH