

Product Summary

Part Number	V _{(BR)DS} Min (V)	V _{GS(th)} Max (V)	r _{DS(on)} Max (Ω)	C _{rSS} Max (pF)	t _{ON} Max (ns)
SD211DE	30	1.5	45 @ V _{GS} = 10 V	0.5	2
SD213DE	10	1.5	45 @ V _{GS} = 10 V	0.5	2
SD215DE	20	1.5	45 @ V _{GS} = 10 V	0.5	2
SST211	30	1.5	50 @ V _{GS} = 10 V	0.5	2
SST213	10	1.5	50 @ V _{GS} = 10 V	0.5	2
SST215	20	1.5	50 @ V _{GS} = 10 V	0.5	2

Features

- Ultra-High Speed Switching—t_{ON}: 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @ 5 V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

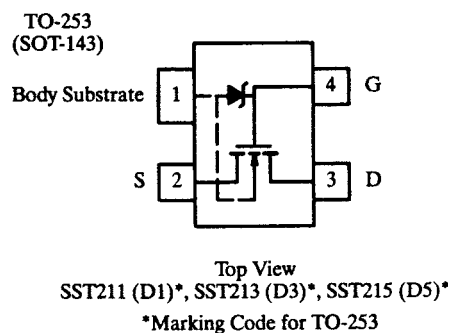
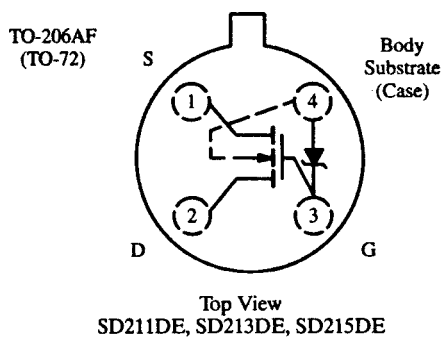
- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

Description

The SD211DE/SST211 series consists of enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video, and high-frequency applications. The SD211 may be used for ±5-V analog switching or as a high speed driver of the SD214. The SD214 is normally used for ±10-V analog switching. These MOSFETs utilize lateral construction to achieve low capacitance

and ultra-fast switching speeds. An integrated Zener diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, and non-Zener protection—SD210DE/214DE.



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage (SD211DE/SST211)	-30/25 V	Drain-Substrate Voltage (SD211DE/SST211)	30 V
(SD213DE/SST213)	-15/25 V	(SD213DE/SST213)	15 V
(SD215DE/SST215)	-25/30 V	(SD215DE/SST215)	25 V
Gate-Substrate Voltage ^a (SD211DE/SST211)	-0.3/25 V	Source-Substrate Voltage (SD211DE/SST211)	15 V
(SD213DE/SST213)	-0.3/25 V	(SD213DE/SST213)	15 V
(SD215DE/SST215)	-0.3/30 V	(SD215DE/SST215)	25 V
Drain-Source Voltage (SD211DE/SST211)	30 V	Drain Current	50 mA
(SD213DE/SST213)	10 V	Lead Temperature (1/16" from case for 10 seconds)	300°C
(SD215DE/SST215)	20 V	Storage Temperature	-65 to 150°C
Source-Drain Voltage (SD211DE/SST21)	10 V	Operating Junction Temperature	-55 to 125°C
(SD213DE/SST213)	10 V	Power Dissipation ^a	300 mW
(SD215DE/SST215)	20 V		

Notes:
a. Derate 3 mW/°C above 25°C

Specifications^a

Parameter	Symbol ^b	Test Conditions ^b	Typ ^c	Limits						Unit	
				211 Series		213 Series		215 Series			
				Min	Max	Min	Max	Min	Max		
Static											
Drain-Source Breakdown Voltage	V _{(BR)DS}	V _{GS} = V _{BS} = 0 V, I _D = 10 μA	35	30							V
		V _{GS} = V _{BS} = -5 V, I _D = 10 nA	30	10		10		20			
Source-Drain Breakdown Voltage	V _{(BR)SD}	V _{GD} = V _{BD} = -5 V, I _S = 10 nA	22	10		10		20			
Drain-Substrate Breakdown Voltage	V _{(BR)DBO}	V _{GB} = 0 V, I _D = 10 nA, Source Open	35	15		15		25			
Source-Substrate Breakdown Voltage	V _{(BR)SBO}	V _{GB} = 0 V, I _S = 10 μA, Drain Open	35	15		15		25			
Drain-Source Leakage	I _{DS(off)}	V _{GS} = V _{BS} = -5 V	V _{DS} = 10 V	0.4		10		10			nA
			V _{DS} = 20 V	0.9					10		
Source-Drain Leakage	I _{SD(off)}	V _{GD} = V _{BD} = -5 V	V _{SD} = 10 V	0.5		10		10			
			V _{SD} = 20 V	1					10		
Gate Leakage	I _{GBS}	V _{DB} = V _{SB} = 0 V, V _{GB} = 30V	0.01		100		100		100		
Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 μA V _{SB} = 0 V	0.8	0.5	1.5	0.1	1.5	0.1	1.5	V	
Drain-Source On-Resistance	r _{DS(on)}	V _{SB} = 0 V I _D = 1 mA	V _{GS} = 5 V (SD Series)	58		70		70		70	Ω
			V _{GS} = 5 V (SST Series)	60		75		75		75	
			V _{GS} = 10 V (SD Series)	38		45		45		45	
			V _{GS} = 10 V (SST Series)	40		50		50		50	
			V _{GS} = 15 V	30							
			V _{GS} = 20 V	26							
			V _{GS} = 25 V	24							

Specifications^a

Parameter	Symbol ^b	Test Conditions ^b	Typ ^c	Limits						Unit	
				211 Series		213 Series		215 Series			
				Min	Max	Min	Max	Min	Max		
Dynamic											
Forward Transconductance	g_{fs}	$V_{DS} = 10\text{ V}$ $V_{SB} = 0\text{ V}$ $I_D = 20\text{ mA}, f = 1\text{ kHz}$	SD Series	11	10		10		10		mS
			SST Series	10.5	9		9		9		
			All	0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = V_{BS} = -15\text{ V}$	SD Series	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$		3.7		5.5		5.5		5.5		
Reverse Transfer Capacitance	C_{rss}		SST Series	4.2							
			SD Series	0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	$t_{d(on)}$	SD Series Only $V_{SB} = 0\text{ V}, V_{IN} 0\text{ to }5\text{ V}, R_G = 25\ \Omega$ $V_{DD} = 5\text{ V}, R_L = 680\ \Omega$		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-Off Time	$t_{d(off)}$			2							
	t_f			6							

Notes:

a. $T_A = 25^\circ\text{C}$ unless otherwise noted.

b. B is the body (substrate) and $V_{(BR)}$ is breakdown.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.