

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

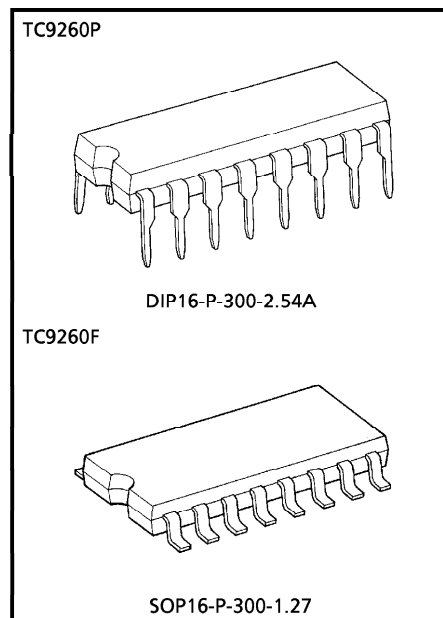
TC9260P, TC9260F

ELECTRONIC VOLUME

The TC9260P and TC9260F are an optimum CMOS which has been designed for electronization of volume control of audio equipment, etc.

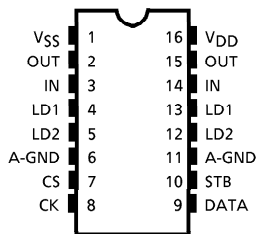
FEATURES

- Attenuation can be controlled from 0dB to -78dB by 2dB / step.
- This ICs feature a built-in loudness circuit. (20dB tap)
- The volume, balance and loudness circuits can be controlled by serial data.
- Chip select input allows control of up to 2 of these chip on the same bus.
- Polysilicon resistors enables low-distortion, high-performance volume system.
- Package is DIP16 and SOP16.

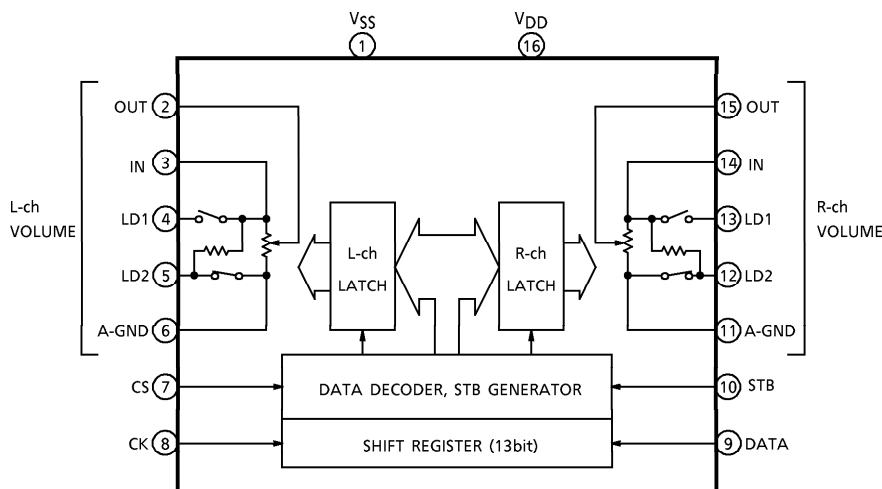


Weight
 DIP16-P-300-2.54A : 1.0g (Typ.)
 SOP16-P-300-1.27 : 0.16g (Typ.)

PIN CONNECTION



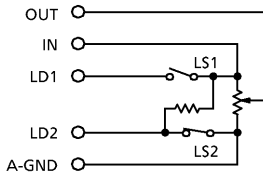
BLOCK DIAGRAM



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PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	NOTE
1	V _{SS}	Digital ground pin	—	—
16	V _{DD}	Power supply pin		
2	L-OUT	Volume output pin	<ul style="list-style-type: none"> ● Volume circuit 	—
15	R-OUT			
3	L-IN	Volume input pin	<ul style="list-style-type: none"> ● Loudness ON : LS1 = ON, LS2 = OFF 	—
14	R-IN			
4	L-LD1	Tap output pins for loudness (1)	<ul style="list-style-type: none"> ● Input pin for designating chip select code. This pin correspond to bit "C1" which is chip select bit in serial data. When CS = "1" and C1 = "1", Data is valid. When CS = "0" and C1 = "0", Data is valid. 	—
13	R-LD1	Tap output pins for loudness (1)		
5	L-LD2	Tap output pins for loudness (2)		
12	R-LD2	Tap output pins for loudness (2)		
6	L-GND	Analog ground pins	<ul style="list-style-type: none"> ● Loudness ON : LS1 = ON, LS2 = OFF 	—
11	R-GND			
7	CS	Chip select input pin	<ul style="list-style-type: none"> ● Input pin for designating chip select code. This pin correspond to bit "C1" which is chip select bit in serial data. When CS = "1" and C1 = "1", Data is valid. When CS = "0" and C1 = "0", Data is valid. 	—
8	CK	Clock input pin	Clock input for data transfer.	Low threshold value input pins
9	DATA	Data input pin	Attenuation channel selection data input terminal. Data consists of 13 bits and input by CK signal.	
10	STB	Strobe input pin	Attenuation setting signal take from DATA and CK terminals are latched when this terminal is placed at "H" level.	

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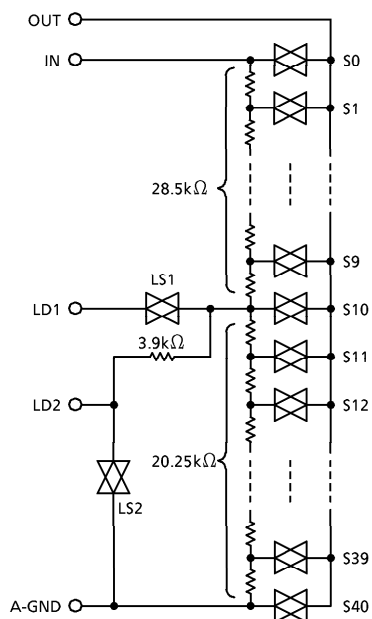
OPERATION

1. Volume circuit

Volume circuit consist of ladder resistor and analog switch.

Tap for loudness is connected to step 10 (20dB). Loudness operation is controlled by LS1 / LS2 switches.

• Equipment circuit



• Volume step and attenuation

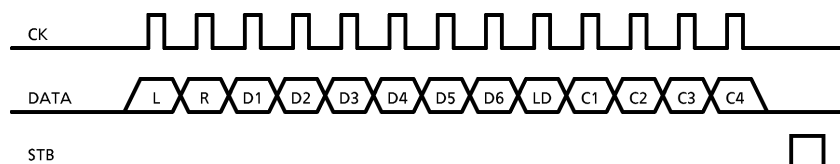
STEP	ATTEN- UATION	STEP	ATTEN- UATION
S0	0 (dB)	S21	42
S1	2	S22	44
S2	4	S23	46
S3	6	S24	48
S4	8	S25	50
S5	10	S26	52
S6	12	S27	54
S7	14	S28	56
S8	16	S29	58
S9	18	S30	60
S10	20	S31	62
S11	22	S32	64
S12	24	S33	66
S13	26	S34	68
S14	28	S35	70
S15	30	S36	72
S16	32	S37	74
S17	34	S38	76
S18	36	S39	78
S19	38	S40	∞
S20	40		

- Loudness ON : LS1 = ON, LS2 = OFF
- Loudness OFF : LS1 = OFF, LS2 = ON

2. Setting volume values

Optional attenuation data is input through the DATA, CK and STB terminals.
Data consists of 18 bits as follows.

(1) Serial data format



(2) Chip select code (C1~C4)

Chip select code is set to use serial bus line in common with other ICs.
Data C2, C3, C4 is fixed 0, 1, 1 in TC9260P, TC9260F.

When level of CS input pin (7pin) correspond to C1 bit, data is valid.

CS	C1	C2	C3	C4
"1"	1	0	1	1
"0"	0	0	1	1

Fixed

(3) L is left-channel select data ; R is right-channel select data. (L/R)

When L = 1, left-channel volume is set ; when R = 1, right-channel volume is set.
(When R = L = 1, both channel volume are set simultaneously).

(4) LD is loudness setting data

When LD = "0", loudness is OFF (LS1 = OFF, LS2 = ON)

When LD = "1", loudness is ON (LS1 = ON, LS2 = OFF)

(5) Volume setting data (D1~D6)

List of volume data and step

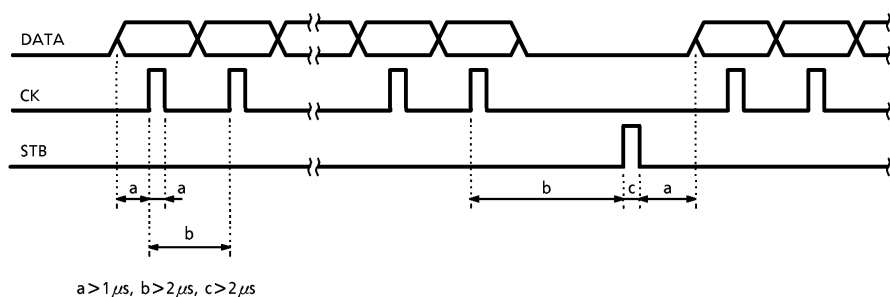
VOLUME VALUE	D1	D2	D3	D4	D5	D6
0dB	0	0	0	0	0	0
2	1	0	0	0	0	0
4	0	1	0	0	0	0
6	1	1	0	0	0	0
8	0	0	1	0	0	0
10	1	0	1	0	0	0
12	0	1	1	0	0	0
14	1	1	1	0	0	0
16	0	0	0	1	0	0
18	1	0	0	1	0	0
20	0	1	0	1	0	0
22	1	1	0	1	0	0
24	0	0	1	1	0	0
26	1	0	1	1	0	0
28	0	1	1	1	0	0
30	1	1	1	1	0	0
32	0	0	0	0	1	0
34	1	0	0	0	1	0
36	0	1	0	0	1	0
38	1	1	0	0	1	0

VOLUME VALUE	D1	D2	D3	D4	D5	D6
40dB	0	0	1	0	1	0
42	1	0	1	0	1	0
44	0	1	1	0	1	0
46	1	1	1	0	1	0
48	0	0	0	1	1	0
50	1	0	0	1	1	0
52	0	1	0	1	1	0
54	1	1	0	1	1	0
56	0	0	1	1	1	0
58	1	0	1	1	1	0
60	0	1	1	1	1	0
62	1	1	1	1	1	0
64	0	0	0	0	0	1
66	1	0	0	0	0	1
68	0	1	0	0	0	1
70	1	1	0	0	0	1
72	0	0	1	0	0	1
74	1	0	1	0	0	1
76	0	1	1	0	0	1
78	1	1	1	0	0	1
∞	0	0	0	1	0	1

(Note) Note that if data other than those listed above are input, volume values are undefined.

(6) Serial data timing

Input CK, DATA and STB according to the following timing.



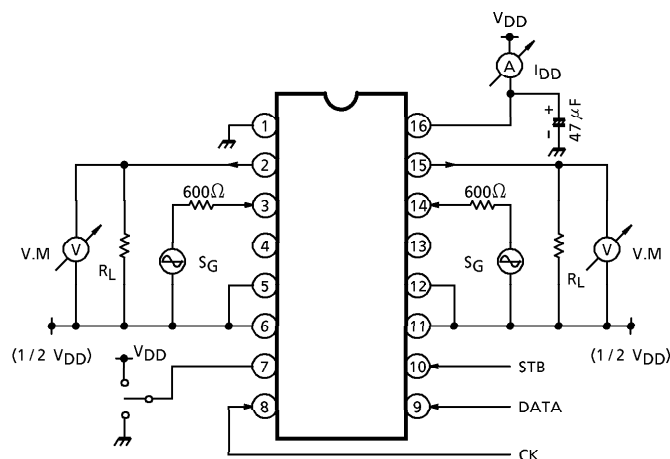
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~15	V
Input Voltage	V _{IN}	-0.3~V _{DD} +0.3	V
Power Dissipation	P _D	300	mW
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

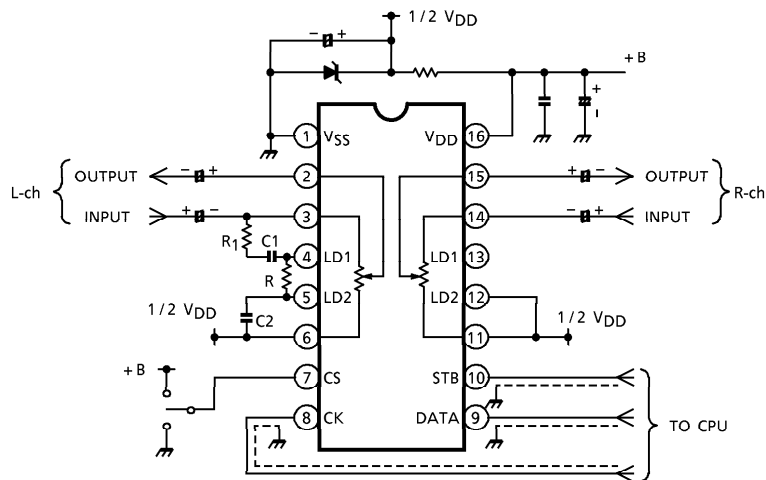
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{DD} = 9V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V _{DD}	—	Ta = -40~85°C	4.5	9.0	12	V
Operating Supply Current	I _{DD}	1	No load	—	0.3	1.0	mA
Input Voltage	"H" Level	V _{IH} (1)	CK, DATA, STB input pin V _{DD} = 4.5~12V	4.0	~	V _{DD}	V
	"L" Level	V _{IL} (1)		0	~	1.0	
Input Voltage	"H" Level	V _{IH} (2)	CS input pin	V _{DD} × 0.7	~	V _{DD}	V
	"L" Level	V _{IL} (2)		0	~	V _{DD} × 0.3	
Input Current	"H" Level	I _{IH}	All input pin	V _{IH} = V _{DD}	-1	—	1
	"L" Level	I _{IL}		V _{IL} = 0V	-1	—	1
Volume Resistance Value	R _V	—	Loudness "OFF"	20	28	37	kΩ
Analog Switch ON Resistance	R _{ON}	—	—	—	250	600	Ω
Attenuation Error	ΔATT	—	—	—	0	±2	dB
Volume Balance Between Left And Right	ΔR _V	—	Volume error between left and right	—	0	±3	%
Total Harmonic Distortion	THD	1	f _{IN} = 1kHz	0dB	—	0.01	—
Maximum Attenuation	ATTM	1	V _{IN} = 1V _{rms}	∞ dB	—	100	—
Cross Talk	CT	1	R _L = 100kΩ	0dB	—	100	—
Output Noise Voltage	V _N	1	R _g = 600Ω	—	2.0	—	μV _{rms}
Operation Frequency	f _{op}	—	CK, DATA, STB	—	—	500	kHz
Minimum Pulse Width	T _{CK}	—	CK input	—	0.5	1.0	μs
	T _{STB}	—	STB input	—	1.0	2.0	

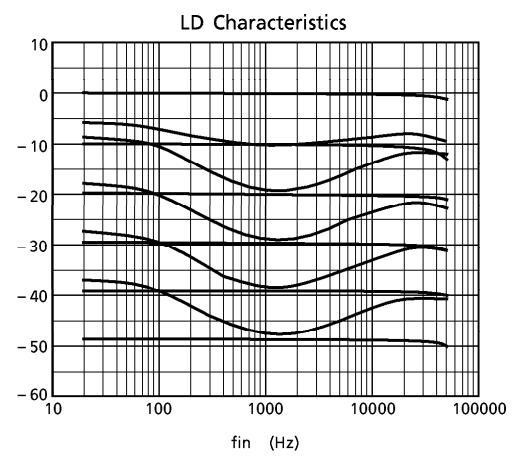
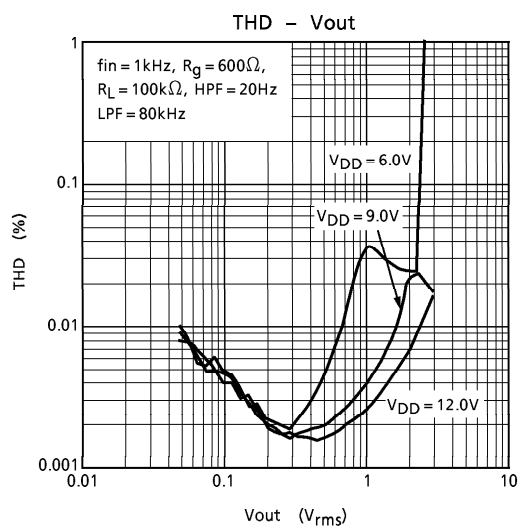
TEST CIRCUIT 1



APPLICATION CIRCUIT

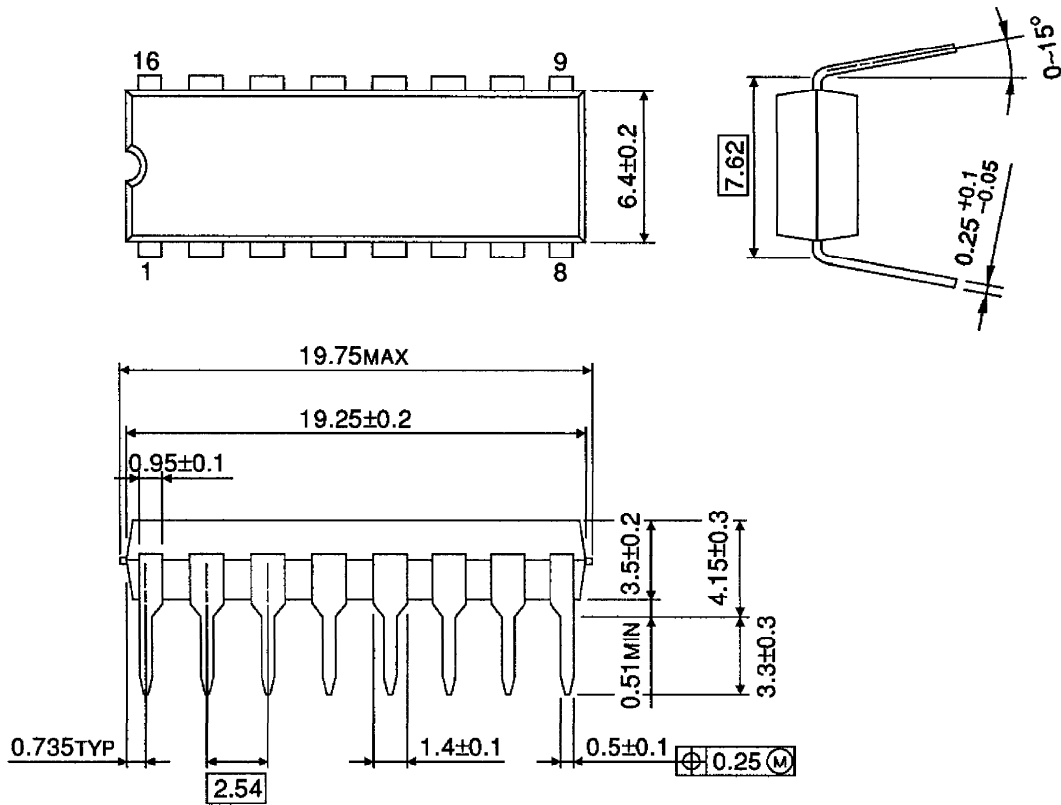


- (Note)
- L-ch circuit is loudness operation, R-ch circuit is without loudness.
 $R_1 = 8.2k\Omega$, $C_1 = 1500pF$, $C_2 = 0.1\mu F$
 - For preventing noise when loudness is turned on or off. $R = 220k\Omega \sim 470k\Omega$
 - High-frequency digital signals are input to pins CK, DATA and STB. Since these signals may cause noise in analog circuits, either use shield wire for CK, DATA, and STB signal lines, or design the pattern so that these signal lines are protected by the ground line.



OUTLINE DRAWING
DIP16-P-300-2.54A

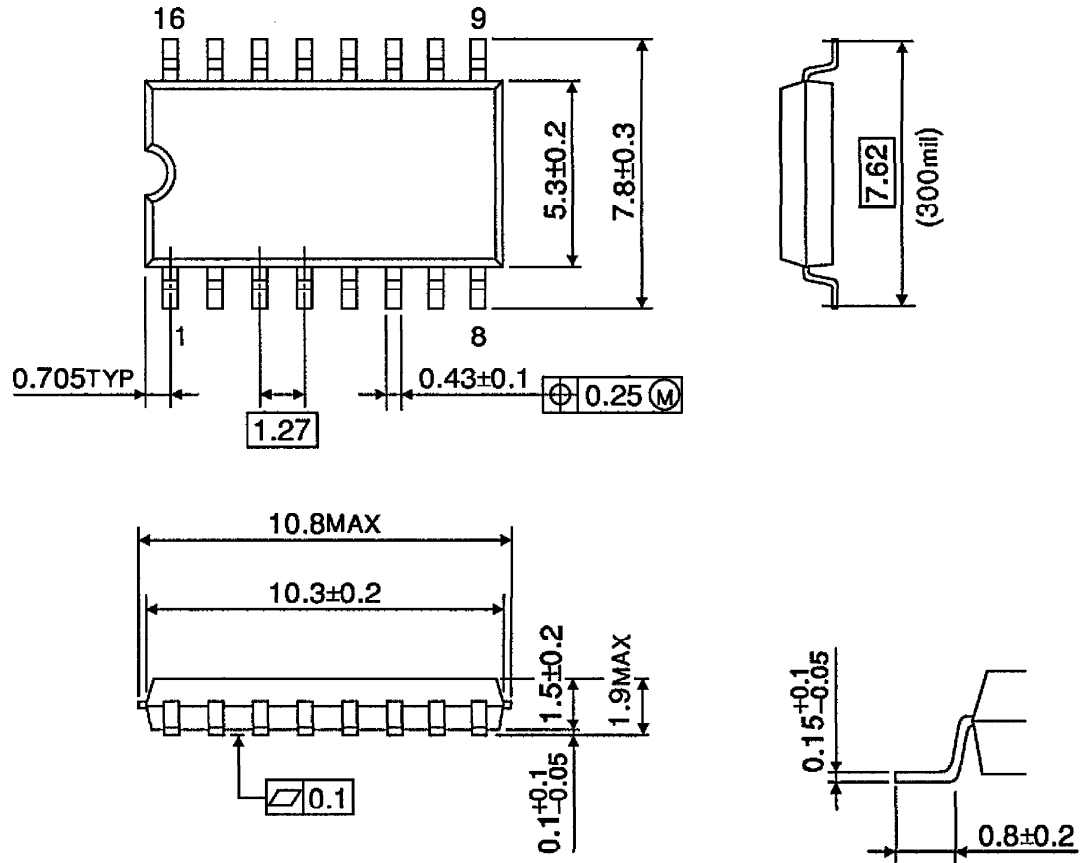
Unit : mm



Weight : 1.0g (Typ.)

OUTLINE DRAWING
SOP16-P-300-1.27

Unit : mm



Weight : 0.16g (Typ.)