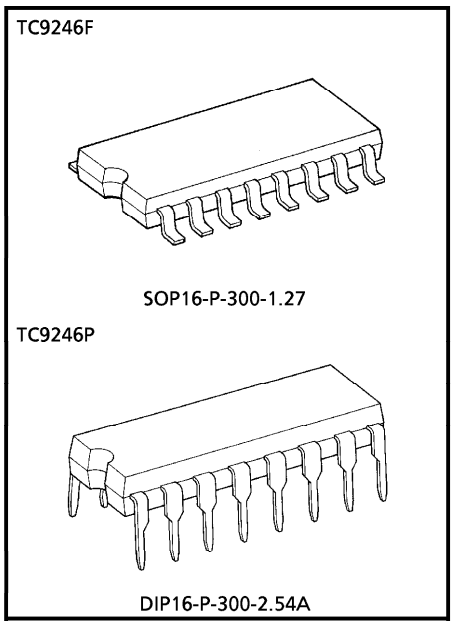
CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC9246F, TC9246P

## PLL IC FOR DIGITAL AUDIO

TC9246F, TC9246P are a clock generating IC to generate master clock required for a system.

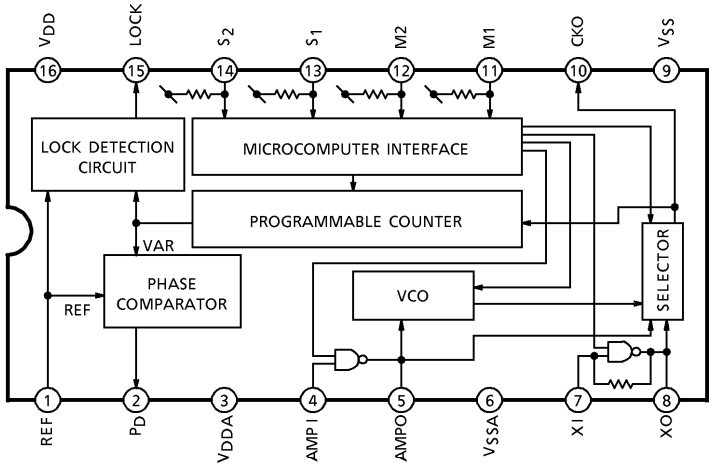



Weight
SOP16-P-300-1.27 : 0.17g (Typ.)
DIP16-P-300-2.54A : 1.11g (Typ.)

### FEATURES

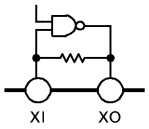
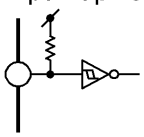
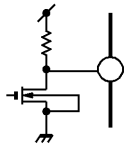
- When reference clock is input, master clock required for a system is generated.
- PLL circuit can be easily constructed by built-in VCO.
- The built-in amplifier for external oscillator makes it possible to select the master clock generation in an external transmitter or that in the built-in VCO by the operation of the microcomputer.
- Detects PLL lock.
- By serially connecting to the TC9245F, TC9245N (Digital In), this IC is usable as a second PLL.
- CMOS silicon gate construction with low power dissipation.
- 2 kinds of package, 16pin MFP and 16pin DIP package.

### BLOCK DIAGRAM




980508EBA2

**PIN FUNCTION**

| PIN No. | SYMBOL | I/O | FUNCTIONAL DESCRIPTION | REMARKS |
|---|---|---|---|---|
| 1 | REF | I | Reference signal input terminal. | — |
| 2 | $P_D$ | O | Phase error signal output terminal. | 3-state output. |
| 3 | $V_{DDA}$ | — | Analog supply voltage terminal. | — |
| 4 | AMPI | I | LPF or oscillator 1 operational amplifier input terminal. | — |
| 5 | AMPO | O | LPF or oscillator 1 operational amplifier output terminal. | — |
| 6 | $V_{SSA}$ | — | Analog ground terminal. | — |
| 7 | XI | I | Oscillator 3 operational amplifier input terminal. | With feedback resistor.   |
| 8 | XO | O | Oscillator 3 operational amplifier output terminal. | |
| 9 | $V_{SS}$ | — | Digital ground terminal. | — |
| 10 | CKO | O | Oscillated clock signal output terminal. | — |
| 11 | M1 | I | Mode selection terminal. | Schmitt input. With pull-up resistor.  |
| 12 | M2 | I | Mode selection terminal. | |
| 13 | $S_1$ | I | Parallel mode : division ratio selection terminal.<br>Serial mode : microcomputer data input terminal. | |
| 14 | $S_2$ | I | Parallel mode : division ratio selection terminal.<br>Serial mode : shift clock signal input terminal. | |
| 15 | LOCK | O | Lock detection signal output terminal. | Open drain. With pull-up resistor.  |
| 16 | $V_{DD}$ | — | Digital supply voltage terminal. | — |

## DESCRIPTION OF OUTLINE

TC9246F, TC9246P are an IC developed for simple and second PLLs and for radiation suppression, and to generate system clock signals for audio DSP.
In particular, the IC is well adapted to audio digital signal processing.
Described below is the concrete operation of the IC.

1. Set operation modes and basic circuit configuration.

Table.1 Set inner operation modes

| M2 | M1 | INNER OPERATION MODE |
|---|---|---|
| L | L | PLL mode where LC oscillator is used |
| L | H | PLL mode where program counter is used |
| H | L | Mode for crystal oscillation (Except that $S_1 = S_2 = L$) |
| | | Mode for simple phase comparison ($S_1 = S_2 = L$) |
| H | H | PLL mode with built-in VCO used |

Table.2 Relation between CKO and REF

| $S_2$ | $S_1$ | CKO OUTPUT | REF INPUT | INNER fs |
|---|---|---|---|---|
| L | L | 768fs | fs | fs |
| L | H | 512fs | | |
| H | L | 256fs | fs | fs |
| H | H | 384fs | | |

(1) PLL mode where LC oscillator is used ;

A varicap diode is connected to pin 4 (AMPI) and pin 5 (AMPO) of inverter amplifier 1 to form an LC oscillator. This allows a very accurate PLL circuit to be built.

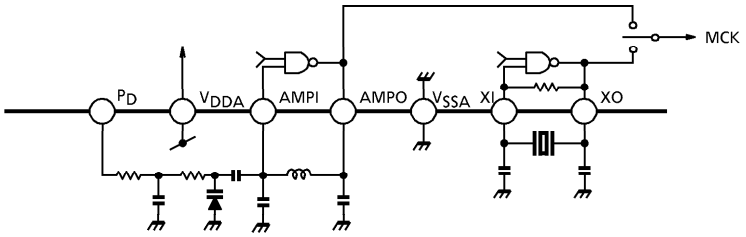



Fig.1 Sample basic PLL circuit-1

(2) PLL mode where program counter is used ;

Using a microcomputer allows the division ratio of the program counter to be set at your disposal.
In this mode, the following four types of data can be set. Up to 15bits are needed for this setting.
Data is caught at the trailing edge of the 16th DCK clock signal. In order that counting may be started when the level at M1 terminal goes "H" from "L", make the terminal "L" first in this mode, as shown in Fig.2.

- $D_9$~$D_0$ ; These bits set a division ratio of the program counter.
  10 binary bits cover the MSB first. (Division ratio : 1 / N = 1 / 5 to 1 / 1023)
- M1D, M2D ; These bits an inner operation mode in accordance with set operation modes covered in Table.1.
  With M1D and M2D being "H" and "L", respectively, all oscillators stop oscillation.
- PS ; This bit sets the polarity of phase error output.
  H represents positive logic and L negative logic.
- $T_1$, $T_2$ ; These are testing bits. Both of $T_1$ and $T_2$ are fixed at H.

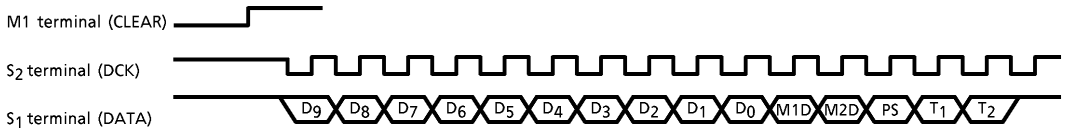



Fig.2 Microcomputer data setting timing chart

(3) Crystal oscillation mode

A crystal oscillator is connected to inverter amplifier 2 incorporating the feedback resistor which inverter exists across pin 7 (XI) and pin 8 (XO) in order to form a crystal oscillator circuit.

(4) PLL mode where incorporated VCO is used

PLL mode where an incorporated VCO oscillator is used. This mode is such that the polarity of phase error output is inverted. Inverter amplifier 1 is used as the active filter.

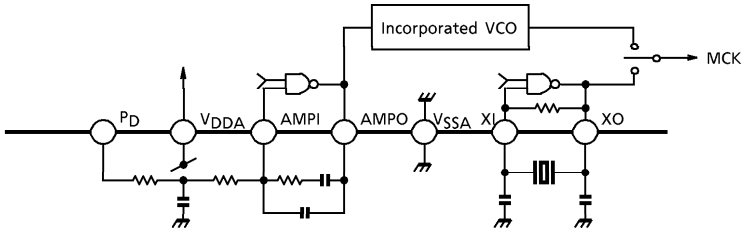



Fig.3 Sample basic PLL circuit-2

(5) Simple phase comparison mode

With $S_1$ and $S_2$ set at L in the crystal oscillation mode, a VAR signal can be entered through pin 7 (XI), a signal of phase errors from the REF signal is issued through PD terminal.

2. Lock detection

When VAR input signals enter the inner window (±3 clocks of CKO/2) successively for a certain period with respect to the REF input signal in the PLL mode, the PLL is considered to be locked. LOCK output is varied from L to H. PLL lock detection period LD is determined by (1/fs) *512. Table.3 shows PLL lock detection periods for typical 3fs for your reference.

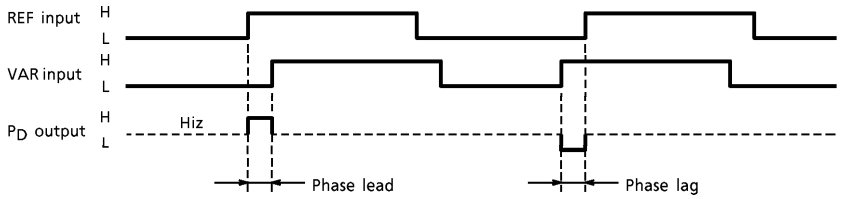
Table.3 Sample PLL lock detection

| Inner fs | 32kHz | 44.1kHz | 48kHz |
|---|---|---|---|
| Lock detection period (LD) | 16ms | 11.6ms | 10.7ms |

A window is made by inner VCO clocks. This makes it impossible to detect errors of the VAR input signal with respect to the REF input signal under 1/32 of divisions.

3. Phase error output

Responding to REF and VAR input shown in the block diagram, a phase error signal is output through the PD terminal. Shown below is the relation between signals.




Sample phase error output timing chart (PS bit = H ; $P_D$ output is based on positive logic.)

(Note) In the PLL mode where built-in VCO is used, the active filter is utilized. This means that output is based on negative logic.

**MAXIMUM RATINGS** (Ta = 25°C)

| CHARACTERISTIC | | SYMBOL | RATING | UNIT |
|---|---|---|---|---|
| Power Supply Voltage | | $V_{DD}$ | −0.3~6.0 | V |
| Input Voltage | | $V_{IN}$ | −0.3~$V_{DD}$ + 0.3 | V |
| Power Dissipation | TC9246F | $P_D$ | 180 | mW |
| | TC9246P | | 300 | |
| Operating Temperature | | $T_{opr}$ | −35~85 | °C |
| Storage Temperature | | $T_{stg}$ | −55~150 | °C |

**ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, Ta = 25°C, $V_{DD}$ = 5V)

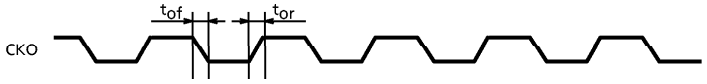
DC characteristics

| CHARACTERISTIC | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| Operating Power Supply Voltage | | $V_{DD}$ | — | Ta = −35~85°C | | 4.5 | 5.0 | 5.5 | V |
| Current Consumption | | $I_{DD}$ | — | — | | — | — | 25.0 | mA |
| Input Voltage | | $V_{IH}$ | — | REF, AMPI, XI, M1, M2, $S_1$, $S_2$ | | 4.0 | — | $V_{DD}$ | V |
| | | $V_{IL}$ | | | | 0.0 | — | 1.0 | |
| Input Amplitude | | $V_{IN}$ | — | XI | | 0.4 | — | 5.0 | $V_{p-p}$ |
| Input Current (1) | "H" Level | $I_{IH}$ (1) | — | REF, AMPI | $V_{IH}$ = 5.0V | — | — | 1.0 | μA |
| | "L" Level | $I_{IL}$ (1) | | | $V_{IL}$ = 0.0V | −1.0 | — | — | |
| Input Current (2) | "H" Level | $I_{IH}$ (2) | — | XI | $V_{IH}$ = 5.0V | — | — | 10 | |
| | "L" Level | $I_{IL}$ (2) | | | $V_{IL}$ = 0.0V | −10 | — | — | |
| Trystate Leak Current | "H" Level | $I_{TLH}$ | — | $P_D$ | $V_{IH}$ = 5.0V | — | — | 1.0 | |
| | "L" Level | $I_{TLL}$ | | | $V_{IL}$ = 0.0V | −1.0 | — | — | |
| Output Current | | $I_{OH}$ | — | $P_D$, CKO, LOCK ($I_{OL}$ only) | $V_{OH}$ = 4.5V | — | — | −3.0 | mA |
| | | $I_{OL}$ | | | $V_{OL}$ = 0.5V | 4.0 | — | — | |
| Pull-up Resistance (1) | | $R_{UP}$ (1) | — | M1, M2, $S_1$, $S_2$ | | — | 20 | — | kΩ |
| Pull-up Resistance (2) | | $R_{UP}$ (2) | — | LOCK | | — | 50 | — | |

AC characteristics

(1) Clock and data output timing

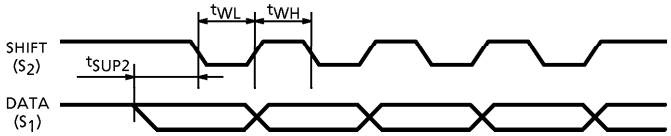
| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| Output Rising Time | $t_{or}$ | — | CKO | — | — | 10 | ns |
| Output Falling Time | $t_{of}$ | — | CKO | — | — | 10 | |



(2) Microcontroller interface timing

| CHARACTERISTIC | | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| Clock Pulse Width | "H" Level | $t_{WH}$ | — | SHIFT | 1 | — | — | μs |
| | "L" Level | $t_{WL}$ | | | 1 | — | — | |
| Set Up Time | | $t_{SUP1}$ | — | SHIFT→DATA | 0.2 | — | — | μs |
| | | $t_{SUP2}$ | | DATA→SHIFT | 0.5 | — | — | |

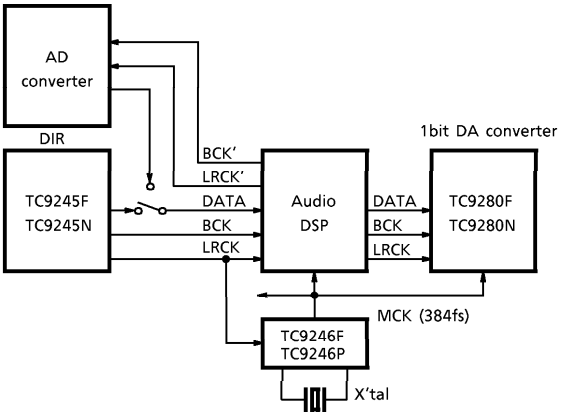
- Data input mode ((M1, M2) = (H, L))




**EXAMPLES OF APPLICABLE CIRCUITS**

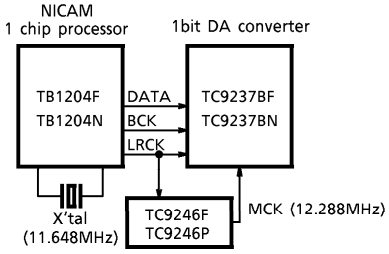
1. System clock generation by AV amplifier (DIR = Digital Audio Interface Receiver IC)

   This example is such that, in order to adopt digital data from audio DSP, clocks are supplied by the crystal oscillator and, with the DIR used, PLL clocks are supplied.



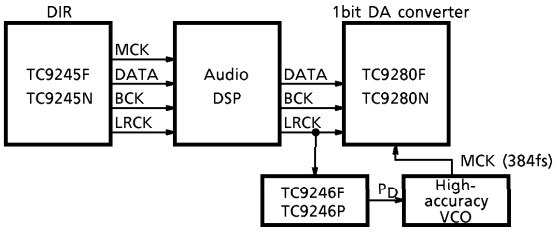

2. Generation of multiple system clocks

   One system may call for system clocks of 256fs and 384fs.



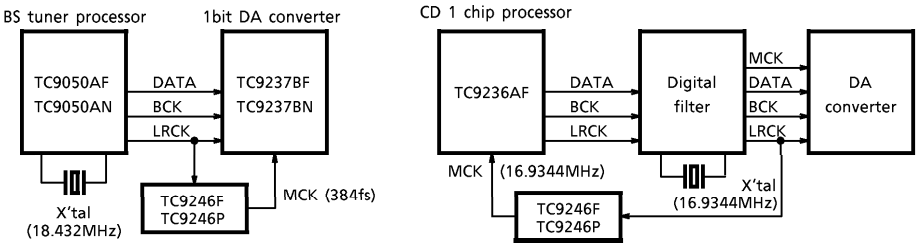
3. Generation of high-accuracy master clock

The appropriate case is that hihg-accureacy master clocks are supplied to a 1bit DA converter with the DIR used. (For example, high-accuracy master clocks are supplied for LC oscillation, VCXO, varimega modules, etc.)



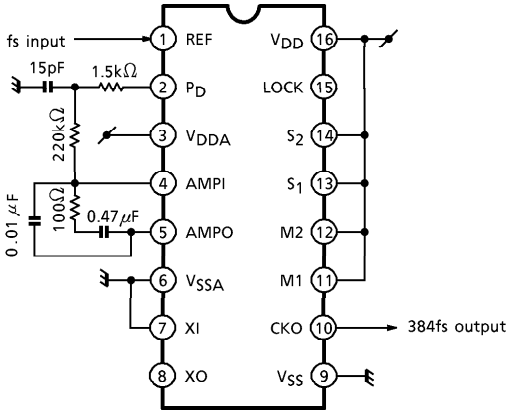

4. Actions against radiation not needed

In some cases, a DA converter is connected at an interval from such signal processors as a BS tuner and a CD player system. In these cases, master clocks should be sent without using complicated wiring and actions taken against radiation not needed.




**APPLICATION CIRCUIT**

384fs clocks are generated in the parallel mode (using built-in VCO).



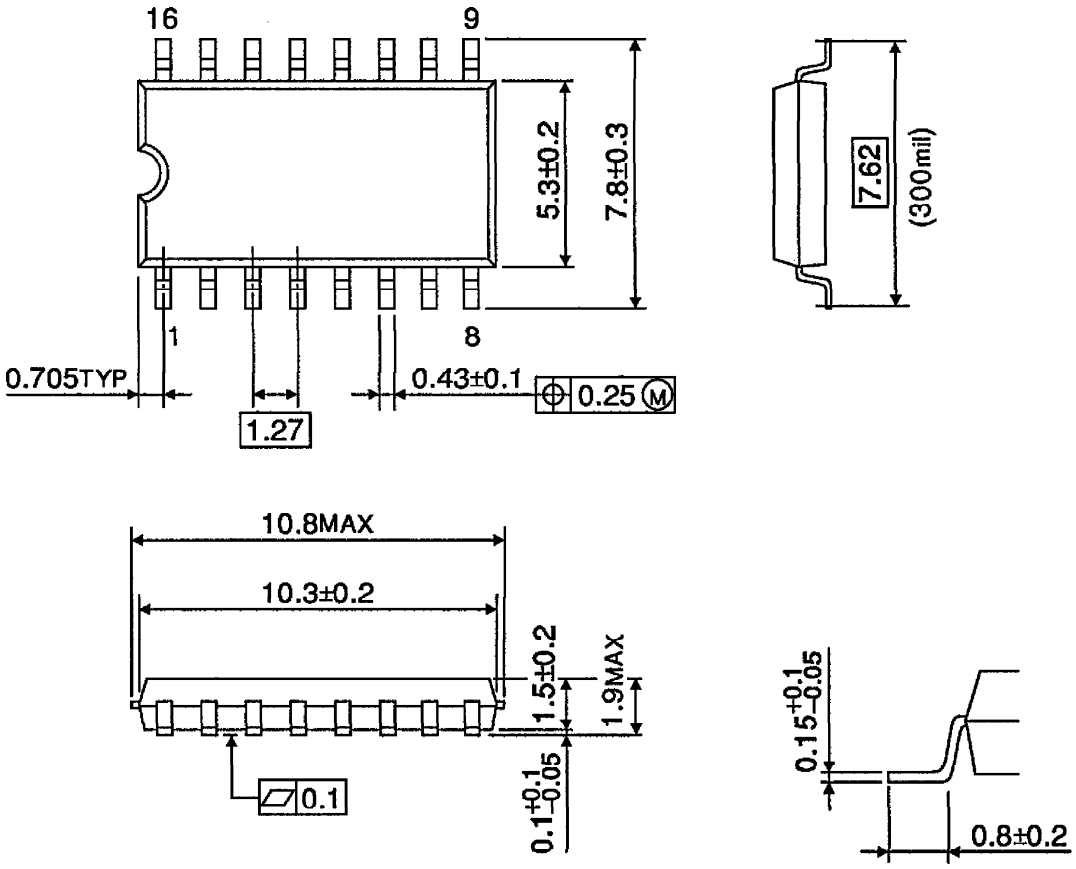

TC9246F, TC9246P

(Note) The PLL configuration and constants are tentative.

**OUTLINE DRAWING**

SOP16-P-300-1.27

Unit : mm

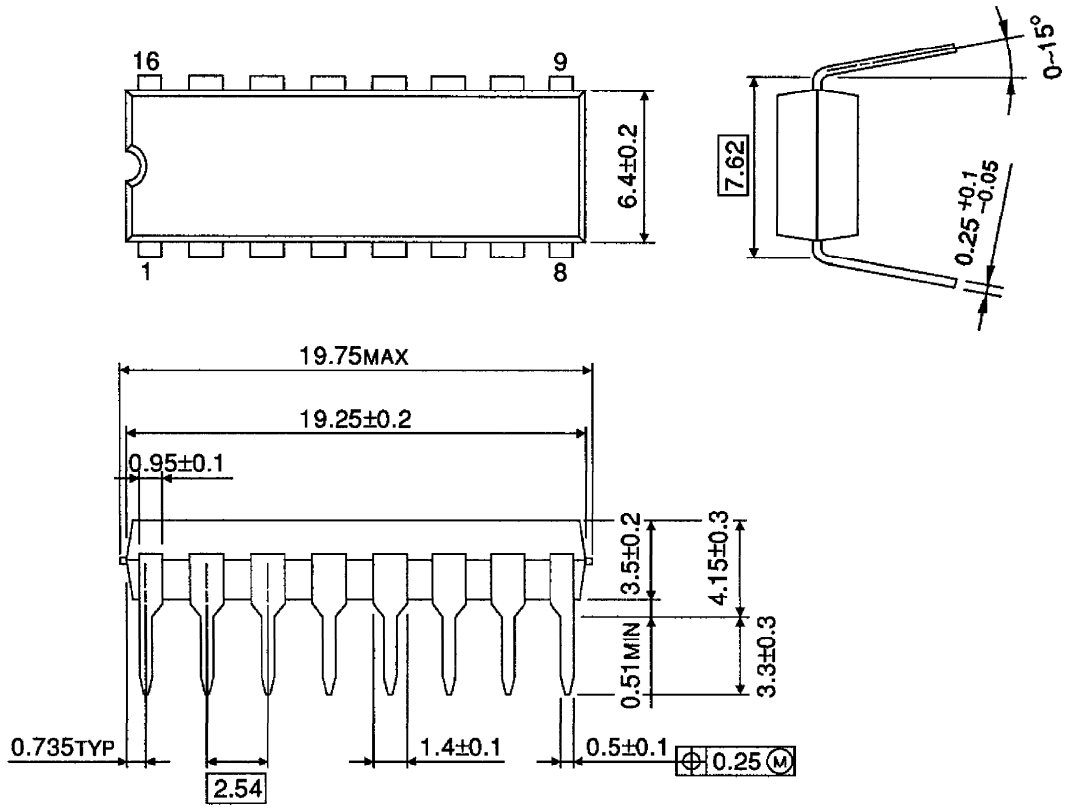



Weight : 0.17g (Typ.)

**OUTLINE DRAWING**

DIP16-P-300-2.54A

Unit : mm




Weight : 1.11g (Typ.)